Programmer’s Guide

Linux Driver Programmer's Guide

ABSTRACT

This programming guide lists the device registers of the DS90UB9702.

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Trademarks

1 Register Maps

The deserializer implements the following register blocks, accessible via I2C as well as the bi-directional control channel:

- Main Registers
- PATGEN and CSI-2 Registers
- FPD-Link RX Port Registers (separate register block for each of the RX ports)
- CSI-2 Registers (separate register block for each of the CSI-2 ports)

Table 1-1. Main Register Map Descriptions

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP			
0x00-0x31	Digital Shared Registers	Shared			
0x33-0x3A	Digital CSI-2 Registers (paged, broadcast write allowed)	CSI-2 TX Port 0 *R: 0x32[4]=0* *W: 0x32[0]=1*		CSI-2 TX Port 1 *R: 0x32[4]=1* *W: 0x32[1]=1*	
0x3B-0x3F	Digital Shared Registers	Reserved			
0x40-0x45	Sensor Registers	Shared			
0x46-0x8F	Digital RX Port Registers (paged, broadcast write allowed)	FPD RX Port 0 *R: 0x4C[5:4]=00* *W: 0x4C[0]=1*	FPD RX Port 1 *R: 0x4C[5:4]=01* *W: 0x4C[1]=1*	FPD RX Port 2 *R: 0x4C[5:4]=10* *W: 0x4C[2]=1*	FPD RX Port 3 *R: 0x4C[5:4]=11* *W: 0x4C[3]=1*
0x90-0x9F	Digital CSI-2 Debug Registers	Shared			
0xA0-0xA7	VC-ID Mapping	FPD RX Port 0	FPD RX Port 1	FPD RX Port 2	FPD RX Port 3
0xA8-0xAF	Reserved	Shared			
0xB0-0xB2	Indirect Access Registers	Shared			
0xB3-0xBF	Digital Share Debug Registers	Shared			
0xC0-0xCF	Digital Shared Registers	Shared			
0xD0-0xDF	Digital RX Port Debug/Interrupt Registers	FPD RX Port 0	FPD RX Port 1	FPD RX Port 2	FPD RX Port 3
0xE0-0xE6	Reserved	Reserved			
0xE7-0xEF	Digital Shared Registers	Shared			
0xF0-0xF7	FPD RX ID	Shared			
0xF8-0xFF	Port I2C Addressing	Shared			

LEGEND:

- RW = Read Write
- RW/SC = RW/SC = Read Write access/Self Clearing bit
- R = Read Only, Permanent value
- R/COR = Read Only, Clear On Read

1.1 Main Registers

Table 1-2 lists the memory-mapped registers for the Main registers. All register offset addresses not listed in Table 1-2 should be considered as reserved locations and the register contents should not be modified.

Table 1-2. MAIN Registers

Address	Acronym	Register Name	Section
0x0	I2C_DEVICE_ID	I2C_DEVICE_ID	Go
0x1	RESET_CTL	RESET_CTL	Go
0x2	GENERAL_CFG	GENERAL_CFG	Go
0x3	REV_MASK_ID	REV_MASK_ID	Go
0x4	DEVICE_STS	DEVICE_STS	Go
0x5	PAR_ERR_THOLD1	PAR_ERR_THOLD1	Go
0x6	PAR_ERR_THOLD0	PAR_ERR_THOLD0	Go
0x7	BCC_Watchdog_Control	BCC_Watchdog_Control	Go
0x8	I2C_Control_1	I2C_Control_1	Go

Table 1-2. MAIN Registers (continued)

Address	Acronym	Register Name	Section
0x9	I2C_Control_2	I2C_Control_2	Go
0xA	SCL_High_Time	SCL_High_Time	Go
0xB	SCL_Low_Time	SCL_Low_Time	Go
0xC	RX_PORT_CTL	RX_PORT_CTL	Go
0xD	IO_CTL	IO_CTL	Go
0xE	GPIO_PIN_STS	GPIO_PIN_STS	Go
0xF	GPIO_INPUT_CTL	GPIO_INPUT_CTL	Go
0x10	GPIO0_PIN_CTL	GPIO0_PIN_CTL	Go
0x11	GPIO1_PIN_CTL	GPIO1_PIN_CTL	Go
0x12	GPIO2_PIN_CTL	GPIO2_PIN_CTL	Go
0x13	GPIO3_PIN_CTL	GPIO3_PIN_CTL	Go
0x14	GPIO4_PIN_CTL	GPIO4_PIN_CTL	Go
0x15	GPIO5_PIN_CTL	GPIO5_PIN_CTL	Go
0x16	GPIO6_PIN_CTL	GPIO6_PIN_CTL	Go
0x17	GPIO7_PIN_CTL	GPIO7_PIN_CTL	Go
0x18	FS_CTL	FS_CTL	Go
0x19	FS_HIGH_TIME_1	FS_HIGH_TIME_1	Go
0x1A	FS_HIGH_TIME_0	FS_HIGH_TIME_0	Go
0x1B	FS_LOW_TIME_1	FS_LOW_TIME_1	Go
0x1C	FS_LOW_TIME_0	FS_LOW_TIME_0	Go
0x1D	MAX_FRM_HI	MAX_FRM_HI	Go
0x1E	MAX_FRM_LO	MAX_FRM_LO	Go
0x1F	CSI_PLL_CTL	CSI_PLL_CTL	Go
0x20	FWD_CTL1	FWD_CTL1	Go
0x21	FWD_CTL2	FWD_CTL2	Go
0x22	FWD_STS	FWD_STS	Go
0x23	INTERRUPT_CTL	INTERRUPT_CTL	Go
0x24	INTERRUPT_STS	INTERRUPT_STS	Go
0x25	TS_CONFIG	TS_CONFIG	Go
0x26	TS_CONTROL	TS_CONTROL	Go
0x27	TS_LINE_HI	TS_LINE_HI	Go
0x28	TS_LINE_LO	TS_LINE_LO	Go
0x29	TS_STATUS	TS_STATUS	Go
0x2A	TIMESTAMP_P0_HI	TIMESTAMP_P0_HI	Go
0x2B	TIMESTAMP_P0_LO	TIMESTAMP_P0_LO	Go
0x2C	TIMESTAMP_P1_HI	TIMESTAMP_P1_HI	Go
0x2D	TIMESTAMP_P1_LO	TIMESTAMP_P1_LO	Go
0x2E	TIMESTAMP_P2_HI	TIMESTAMP_P2_HI	Go
0x2F	TIMESTAMP_P2_LO	TIMESTAMP_P2_LO	Go
0x30	TIMESTAMP_P3_HI	TIMESTAMP_P3_HI	Go
0x31	TIMESTAMP_P3_LO	TIMESTAMP_P3_LO	Go
0x32	CSI_PORT_SEL	CSI_PORT_SEL	Go
0x33	CSI_CTL	CSI_CTL	Go
0x34	CSI_CTL2	CSI_CTL2	Go
0x35	CSI_STS	CSI_STS	Go
0x36	CSI_TX_ICR	CSI_TX_ICR	Go
0x37	CSI_TX_ISR	CSI_TX_ISR	Go

Table 1-2. MAIN Registers (continued)

Address	Acronym	Register Name	Section
0x3D	REFCLK_FREQ	REFCLK_FREQ	Go
0x46	BCC_ERR_CTL	BCC_ERR_CTL	Go
0x47	BCC_STATUS	BCC_STATUS	Go
0x4B	RAW_EMBED_DTYPE	RAW_EMBED_DTYPE	Go
0x4C	FPD3_PORT_SEL	FPD3_PORT_SEL	Go
0x4D	RX_PORT_STS1	RX_PORT_STS1	Go
0x4E	RX_PORT_STS2	RX_PORT_STS2	Go
0x4F	RX_FREQ_HIGH	RX_FREQ_HIGH	Go
0x50	RX_FREQ_LOW	RX_FREQ_LOW	Go
0x51	SENSOR_STS_0	SENSOR_STS_0	Go
0x52	SENSOR_STS_1	SENSOR_STS_1	Go
0x53	SENSOR_STS_2	SENSOR_STS_2	Go
0x54	SENSOR_STS_3	SENSOR_STS_3	Go
0x55	RX_PAR_ERR_HI	RX_PAR_ERR_HI	Go
0x56	RX_PAR_ERR_LO	RX_PAR_ERR_LO	Go
0x57	BIST_ERR_COUNT	BIST_ERR_COUNT	Go
0x58	BCC_CONFIG	BCC_CONFIG	Go
0x59	DATAPATH_CTL1	DATAPATH_CTL1	Go
0x5B	SER_ID	SER_ID	Go
0x5C	SER_ALIAS_ID	SER_ALIAS_ID	Go
0x5D	TARGET_ID_0	TARGET_ID_0	Go
0x5E	TARGET_ID_1	TARGET_ID_1	Go
0x5F	TARGET_ID_2	TARGET_ID_2	Go
0x60	TARGET_ID_3	TARGET_ID_3	Go
0x61	TARGET_ID_4	TARGET_ID_4	Go
0x62	TARGET_ID_5	TARGET_ID_5	Go
0x63	TARGET_ID_6	TARGET_ID_6	Go
0x64	TARGET_ID_7	TARGET_ID_7	Go
0x65	TARGET_ALIAS_0	TARGET_ALIAS_0	Go
0x66	TARGET_ALIAS_1	TARGET_ALIAS_1	Go
0x67	TARGET_ALIAS_2	TARGET_ALIAS_2	Go
0x68	TARGET_ALIAS_3	TARGET_ALIAS_3	Go
0x69	TARGET_ALIAS_4	TARGET_ALIAS_4	Go
0x6A	TARGET_ALIAS_5	TARGET_ALIAS_5	Go
0x6B	TARGET_ALIAS_6	TARGET_ALIAS_6	Go
0x6C	TARGET_ALIAS_7	TARGET_ALIAS_7	Go
0x6D	PORT_CONFIG	PORT_CONFIG	Go
0x6E	BC_GPIO_CTL0	BC_GPIO_CTL0	Go
0x6F	BC_GPIO_CTL1	BC_GPIO_CTL1	Go
0x70	RAW10_ID	RAW10_ID	Go
0x71	RAW12_ID	RAW12_ID	Go
0x73	LINE_COUNT_1	LINE_COUNT_1	Go
0x74	LINE_COUNT_0	LINE_COUNT_0	Go
0x75	LINE_LEN_1	LINE_LEN_1	Go
0x76	LINE_LEN_0	LINE_LEN_0	Go
0x77	FPD3_FREQ_DET_CTL	FPD3_FREQ_DET_CTL	Go
0x78	MAILBOX_1	MAILBOX_1	Go

Table 1-2. MAIN Registers (continued)

Address	Acronym	Register Name	Section
0x79	MAILBOX_2	MAILBOX_2	Go
0x7A	CSI_RX_STS	CSI_RX_STS	Go
0x7B	CSI_ERR_COUNTER	CSI_ERR_COUNTER	Go
0x7C	PORT_CONFIG2	PORT_CONFIG2	Go
0x7D	PORT_PASS_CTL	PORT_PASS_CTL	Go
0x7E	SEN_INT_RISE_CTL	SEN_INT_RISE_CTL	Go
0x7F	SEN_INT_FALL_CTL	SEN_INT_FALL_CTL	Go
0x80	RX_CTL_1	RX_CTL_1	Go
0x89	GPIO9_PIN_CTL	GPIO9_PIN_CTL	Go
0x8A	GPIO10_PIN_CTL	GPIO10_PIN_CTL	Go
0x8B	GPIO_INPUT_CTL_2	GPIO_INPUT_CTL_2	Go
0x8C	REFCLK_DET_INT_CTL	REFCLK_DET_INT_CTL	Go
0x90	CSI0_FRAME_COUNT_HI	CSI0_FRAME_COUNT_HI	Go
0x91	CSI0_FRAME_COUNT_LO	CSI0_FRAME_COUNT_LO	Go
0x92	CSI0_FRAME_ERR_COUNT_HI	CSI0_FRAME_ERR_COUNT_HI	Go
0x93	CSI0_FRAME_ERR_COUNT_LO	CSI0_FRAME_ERR_COUNT_LO	Go
0x94	CSI0_LINE_COUNT_HI	CSI0_LINE_COUNT_HI	Go
0x95	CSI0_LINE_COUNT_LO	CSI0_LINE_COUNT_LO	Go
0x96	CSI0_LINE_ERR_COUNT_HI	CSI0_LINE_ERR_COUNT_HI	Go
0x97	CSI0_LINE_ERR_COUNT_LO	CSI0_LINE_ERR_COUNT_LO	Go
0x98	CSI1_FRAME_COUNT_HI	CSI1_FRAME_COUNT_HI	Go
0x99	CSI1_FRAME_COUNT_LO	CSI1_FRAME_COUNT_LO	Go
0x9A	CSI1_FRAME_ERR_COUNT_HI	CSI1_FRAME_ERR_COUNT_HI	Go
0x9B	CSI1_FRAME_ERR_COUNT_LO	CSI1_FRAME_ERR_COUNT_LO	Go
0x9C	CSI1_LINE_COUNT_HI	CSI1_LINE_COUNT_HI	Go
0x9D	CSI1_LINE_COUNT_LO	CSI1_LINE_COUNT_LO	Go
0x9E	CSI1_LINE_ERR_COUNT_HI	CSI1_LINE_ERR_COUNT_HI	Go
0x9F	CSI1_LINE_ERR_COUNT_LO	CSI1_LINE_ERR_COUNT_LO	Go
0xA0	VC_ID_MAP_0	VC_ID_MAP_0	Go
0xA1	VC_ID_MAP_1	VC_ID_MAP_1	Go
0xA2	VC_ID_MAP_2	VC_ID_MAP_2	Go
0xA3	VC_ID_MAP_3	VC_ID_MAP_3	Go
0xA4	VC_ID_MAP_4	VC_ID_MAP_4	Go
0xA5	VC_ID_MAP_5	VC_ID_MAP_5	Go
0xA6	VC_ID_MAP_6	VC_ID_MAP_6	Go
0xA7	VC_ID_MAP_7	VC_ID_MAP_7	Go
0xB0	IND_ACC_CTL	IND_ACC_CTL	Go
0xB1	IND_ACC_ADDR	IND_ACC_ADDR	Go
0xB2	IND_ACC_DATA	IND_ACC_DATA	Go
0xB3	BIST_CTL	BIST_CTL	Go
0xB8	MODE_IDX_STS	MODE_IDX_STS	Go
0xB9	LINK_ERROR_COUNT	LINK_ERROR_COUNT	Go
0xBC	FV_MIN_TIME	FV_MIN_TIME	Go
0xBE	GPIO_PD_CTL	GPIO_PD_CTL	Go
0xC2	FPD_RATE_CFG	FPD_RATE_CFG	Go
0xC7	CSI_PORT2_FIFO_CTRL	CSI_PORT2_FIFO_CTRL	Go
0xC9	CSI_PLL_DIV	CSI_PLL_DIV	Go

Table 1-2. MAIN Registers (continued)

Address	Acronym	Register Name	Section
0xCA	LOCAL_DEV_ICR	LOCAL_DEV_ICR	Go
0xCB	LOCAL_DEV_ISR	LOCAL_DEV_ISR	Go
0xD0	PORT_DEBUG	PORT_DEBUG	Go
0xD8	PORT_ICR_HI	PORT_ICR_HI	Go
0xD9	PORT_ICR_LO	PORT_ICR_LO	Go
0xDA	PORT_ISR_HI	PORT_ISR_HI	Go
0xDB	PORT_ISR_LO	PORT_ISR_LO	Go
0xDC	FC_GPIO_STS	FC_GPIO_STS	Go
0xDD	FC_GPIO_ICR	FC_GPIO_ICR	Go
0xDE	SEN_INT_RISE_STS	SEN_INT_RISE_STS	Go
0xDF	SEN_INT_FALL_STS	SEN_INT_FALL_STS	Go
0xE4	CHANNEL_MODE	CHANNEL_MODE	Go
0xF0	FPD_RX_ID0	FPD_RX_ID0	Go
0xF1	FPD_RX_ID1	FPD_RX_ID1	Go
0xF2	FPD_RX_ID2	FPD_RX_ID2	Go
0xF3	FPD_RX_ID3	FPD_RX_ID3	Go
0xF4	FPD_RX_ID4	FPD_RX_ID4	Go
0xF5	FPD_RX_ID5	FPD_RX_ID5	Go
0xF6	FPD_RX_ID6	FPD_RX_ID6	Go
0xF8	I2C_RX0_ID	I2C_RX0_ID	Go
0xF9	I2C_RX1_ID	I2C_RX1_ID	Go
0xFA	I2C_RX2_ID	I2C_RX2_ID	Go
0xFB	I2C_RX3_ID	I2C_RX3_ID	Go

Complex bit access types are encoded to fit into small table cells. Table 1-3 shows the codes that are used for access types in this section.

Table 1-3. Main Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WR	W	Write
Reset or Default Value		
-n		Value after reset or the default value

1.1.1 I2C_DEVICE_ID Register (Address = 0x0) [Default = 0x00]

I2C_DEVICE_ID is shown in Table 1-4.

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Table 1-4. I2C_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	DEVICE_ID	R/W	0x0	7-bit I2C ID of Deserializer. Strap This field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and show the strapped ID. When bit 1 of this register is 1, this field is read/write and can be used to assign any valid I2C ID. At power-up, this field is set based on the IDX pin strap value.
0	DES_ID	R/W	0x0	0: Device ID is from strap 1: Register I2C Device ID overrides strapped value

1.1.2 RESET_CTL Register (Address = 0x1) [Default = 0x00]

RESET_CTL is shown in Table 1-5.

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Table 1-5. RESET_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	GPIO_HOLD_B	R/W	0x0	GPIO hold control 0: GPIO hold active 1: GPIO hold released
4:3	RESERVED	R	0x0	Reserved
2	RESTART_AUTOLOAD	RH/W1S	0x0	Restart ROM Auto-load Setting this bit to 1 causes a re-load of the ROM. This bit is self-clearing. Software may check for Auto-load complete by checking the CFG_INIT_DONE bit in the DEVICE_STS register.
1	DIGITAL_RESET1	RH/W1S	0x0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
0	DIGITAL_RESET0	RH/W1S	0x0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation

1.1.3 GENERAL_CFG Register (Address = 0x2) [Default = 0x1E]

GENERAL_CFG is shown in Table 1-6.

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Table 1-6. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	RESERVED
5	I2C_CONTROLLER_EN	R/W	0x0	I2C Controller Enable When this bit is 0, the local I2C controller is disabled, when it is 1, the controller is enabled

Table 1-6. GENERAL_CFG Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	OUTPUT_EN_MODE	R/W	0x1	Output Enable Mode If set to 0, the CSI TX output port will be forced to the high-impedance state if no assigned RX ports have an active Receiver lock. If set to 1, the CSI TX output port will continue in normal operation if no assigned RX ports have an active Receiver lock. CSI TX operation will remain under register control via the CSI_CTL register for each port. If no assigned RX ports have an active Receiver lock, this will result in the CSI Transmitter entering the LP-11 state.
3	OUTPUT_ENABLE	R/W	0x1	Output Enable Control (in conjunction with Output Sleep State Select) If OUTPUT_SLEEP_STATE_SEL is set to 1 and this bit is set to 0, the CSI TX outputs will be forced into a high impedance state.
2	OUTPUT_SLEEP_STATE_SEL	R/W	0x1	OSS Select to control output state when LOCK is low (used in conjunction with Output Enable) When this bit is set to 0, the CSI TX outputs will be forced into a HS-0 state.
1	RX_PARITY_CHECK_EN	R/W	0x1	FPD3 Receiver Parity Checker Enable When enabled, the parity check function is enabled for the FPD3 receiver. This allows detection of errors on the FPD3 receiver data bits. 0: Disable 1: Enable
0	FORCE_REFCLK_DET	R/W	0x0	Force indication of external reference clock 0: Normal operation, reference clock detect circuit indicates the presence of an external reference clock 1: Force reference clock to be indicated present

1.1.4 REV_MASK_ID Register (Address = 0x3) [Default = 0x40]

REV_MASK_ID is shown in Table 1-7.

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Table 1-7. REV_MASK_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	REVISION_ID	R	0x4	Revision ID 0100: DS90UB9702-Q1
3:0	RESERVED	R	0x0	Reserved

1.1.5 DEVICE_STS Register (Address = 0x4) [Default = 0xD0]

DEVICE_STS is shown in Table 1-8.

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Table 1-8. DEVICE_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	CFG_CKSUM_STS	R	0x1	Config Checksum Passed This bit will be set following initialization if the Configuration data in the eFuse ROM had a valid checksum
6	CFG_INIT_DONE	R	0x1	Power-up initialization complete This bit will be set after Initialization is complete. Configuration from eFuse ROM has completed.
5	RX_PLL_LOCK	R	0x0	Reserved
4	REFCLK_VALID	R	0x1	REFCLK valid frequency This bit indicates when a valid frequency has been detected on the REFCLK pin. 0: invalid frequency detected 1: REFCLK frequency between 12MHz and 64MHz

Table 1-8. DEVICE_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

1.1.6 PAR_ERR_THOLD1 Register (Address = 0x5) [Default = 0x01]

PAR_ERR_THOLD1 is shown in Table 1-9.

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Table 1-9. PAR_ERR_THOLD1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PAR_ERR_THOLD_HI	R/W	0x1	FPD Parity Error Threshold High byte This register provides the 8 most significant bits of the Parity Error Threshold value. For each port, if the FPD-Link receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag will be set in the RX_PORT_STS1 register.

1.1.7 PAR_ERR_THOLD0 Register (Address = 0x6) [Default = 0x00]

PAR_ERR_THOLD0 is shown in Table 1-10.

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Table 1-10. PAR_ERR_THOLD0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PAR_ERR_THOLD_LO	R/W	0x0	FPD Parity Error Threshold Low byte This register provides the 8 least significant bits of the Parity Error Threshold value. For each port, if the FPD-Link receiver detects a number of parity errors greater than or equal to this value, the PARITY_ERROR flag will be set in the RX_PORT_STS1 register.

1.1.8 BCC_Watchdog_Control Register (Address = 0x7) [Default = 0xFE]

BCC_Watchdog_Control is shown in Table 1-11.

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Table 1-11. BCC_Watchdog_Control Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	BCC_WATCHDOG_TIMER	R/W	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field must not be set to 0.
0	BCC_WATCHDOG_TIMER_DISABLE	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

1.1.9 I2C_Control_1 Register (Address = 0x8) [Default = 0x1C]

I2C_Control_1 is shown in Table 1-12.

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Table 1-12. I2C_Control_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LOCAL_WRITE_DISABLE	R/W	0x0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C controller attached to the Serializer. Setting this bit does not affect remote access to I2C targets at the Deserializer.
6:4	I2C_SDA_HOLD	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
3:0	I2C_FILTER_DEPTH	R/W	0xC	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

1.1.10 I2C_Control_2 Register (Address = 0x9) [Default = 0x12]

I2C_Control_2 is shown in Table 1-13.

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Table 1-13. I2C_Control_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	SDA_Output_Setup	R/W	0x1	Remote Ack SDA Output Setup When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value will increase setup time in units of 640ns. The nominal output setup time value for SDA to SCL when this field is 0 is 80ns.
3:2	SDA_Output_Delay	R/W	0x0	SDA Output Delay This field configures additional delay on the SDA output relative to the falling edge of SCL. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns 01: 280ns 10: 320ns 11: 360ns
1	I2C_BUS_TIMER_SPEED UP	R/W	0x1	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
0	I2C_BUS_TIMER_DISAB LE	R/W	0x0	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL

1.1.11 SCL_High_Time Register (Address = 0xA) [Default = 0x7A]

SCL_High_Time is shown in Table 1-14.

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Table 1-14. SCL_High_Time Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SCL_HIGH_TIME	R/W	0x7A	I2C Controller SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the reference clock at 25 MHz + 100ppm. The delay includes 5 additional oscillator clock periods. Min_delay= 39.996ns * (SCL_HIGH_TIME + 5)

1.1.12 SCL_Low_Time Register (Address = 0xB) [Default = 0x7A]

SCL_Low_Time is shown in Table 1-15.

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Table 1-15. SCL_Low_Time Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SCL_LOW_TIME	R/W	0x7A	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Controller on the local I2C bus. This value is also used as the SDA setup time by the I2C Target for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the reference clock at 25 MHz + 100ppm. The delay includes 5 additional clock periods. Min_delay= 39.996ns * (SCL_LOW_TIME+ 5)

1.1.13 RX_PORT_CTL Register (Address = 0xC) [Default = 0x00]

RX_PORT_CTL is shown in Table 1-16.

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Table 1-16. RX_PORT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	BCC3_MAP	R/W	0x0	Map Control Channel 3 to I2C Target Port 0: I2C Target Port 0 1: I2C Target Port 1
6	BCC2_MAP	R/W	0x0	Map Control Channel 2 to I2C Target Port 0: I2C Target Port 0 1: I2C Target Port 1
5	BCC1_MAP	R/W	0x0	Map Control Channel 1 to I2C Target Port 0: I2C Target Port 0 1: I2C Target Port 1
4	BCC0_MAP	R/W	0x0	Map Control Channel 0 to I2C Target Port 0: I2C Target Port 0 1: I2C Target Port 1
3	PORT3_EN	R/W	0x0	Port 3 Receiver Enable 0: Disable Port 3 Receiver 1: Enable Port 3 Receiver
2	PORT2_EN	R/W	0x0	Port 2 Receiver Enable 0: Disable Port 2 Receiver 1: Enable Port 2 Receiver
1	PORT1_EN	R/W	0x0	Port 1 Receiver Enable 0: Disable Port 1 Receiver 1: Enable Port 1 Receiver

Table 1-16. RX_PORT_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	PORT0_EN	R/W	0x0	Port 0 Receiver Enable 0: Disable Port 0 Receiver 1: Enable Port 0 Receiver

1.1.14 IO_CTL Register (Address = 0xD) [Default = 0x09]

IO_CTL is shown in Table 1-17.

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Table 1-17. IO_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	SEL3P3V	R/W	0x0	3.3V I/O Select on pins PDB, INTB,I2C 0: 1.8V I/O Supply 1: 3.3V I/O Supply If IO_SUPPLY_MODE_OV is 0, a read of this register will return the detected I/O voltage level.
6	IO_SUPPLY_MODE_OV	R/W	0x0	Override I/O Supply Mode bit If set to 0, the detected voltage level will be used for both SEL3P3V and IO_SUPPLY_MODE controls. If set to 1, the values written to the SEL3P3V and IO_SUPPLY_MODE fields will be used.
5:4	IO_SUPPLY_MODE	R/W	0x0	I/O Supply Mode 00: 1.8V 01: Reserved 10: Reserved 11: 3.3V If IO_SUPPLY_MODE_OV is 0, a read of this register will return the detected I/O voltage level.
3:0	RESERVED	R/W	0x9	Reserved

1.1.15 GPIO_PIN_STS Register (Address = 0xE) [Default = 0x00]

GPIO_PIN_STS is shown in Table 1-18.

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Table 1-18. GPIO_PIN_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	GPIO_STS	R	0x0	GPIO Pin Status This register reads the current values on each of the 8 GPIO pins. Bit 7 reads GPIO7 and bit 0 reads GPIO0.

1.1.16 GPIO_INPUT_CTL Register (Address = 0xF) [Default = 0xEF]

GPIO_INPUT_CTL is shown in Table 1-19.

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Table 1-19. GPIO_INPUT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO7_INPUT_EN	R/W	0x1	GPIO7 Input Enable 0: Disabled 1: Enabled
6	GPIO6_INPUT_EN	R/W	0x1	GPIO6 Input Enable 0: Disabled 1: Enabled

Table 1-19. GPIO_INPUT_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	GPIO5_INPUT_EN	R/W	0x1	GPIO5 Input Enable 0: Disabled 1: Enabled
4	GPIO4_INPUT_EN	R/W	0x0	GPIO4 Input Enable 0: Disabled 1: Enabled
3	GPIO3_INPUT_EN	R/W	0x1	GPIO3 Input Enable 0: Disabled 1: Enabled
2	GPIO2_INPUT_EN	R/W	0x1	GPIO2 Input Enable 0: Disabled 1: Enabled
1	GPIO1_INPUT_EN	R/W	0x1	GPIO1 Input Enable 0: Disabled 1: Enabled
0	GPIO0_INPUT_EN	R/W	0x1	GPIO0 Input Enable 0: Disabled 1: Enabled

1.1.17 GPIO0_PIN_CTL Register (Address = 0x10) [Default = 0x00]

GPIO0_PIN_CTL is shown in Table 1-20.

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Table 1-20. GPIO0_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO0_OUT_SEL	R/W	0x0	GPIO0 Output Select Determines the output data for the selected source. If GPIO0_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO0_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk If GPIO0_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved

Table 1-20. GPIO0_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	GPIO0_OUT_SRC	R/W	0x0	GPIO0 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO0_OUT_VAL	R/W	0x0	GPIO0 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO0_OUT_EN	R/W	0x0	GPIO0 Output Enable 0: Disabled 1: Enabled

1.1.18 GPIO1_PIN_CTL Register (Address = 0x11) [Default = 0x00]

GPIO1_PIN_CTL is shown in Table 1-21.

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Table 1-21. GPIO1_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO1_OUT_SEL	R/W	0x0	GPIO1 Output Select Determines the output data for the selected source. If GPIO1_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO1_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk If GPIO1_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved

Table 1-21. GPIO1_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	GPIO1_OUT_SRC	R/W	0x0	GPIO1 Output Source Select Selects output source for GPIO1 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO1_OUT_VAL	R/W	0x0	GPIO1 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO1_OUT_EN	R/W	0x0	GPIO1 Output Enable 0: Disabled 1: Enabled

1.1.19 GPIO2_PIN_CTL Register (Address = 0x12) [Default = 0x00]

GPIO2_PIN_CTL is shown in Table 1-22.

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Table 1-22. GPIO2_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO2_OUT_SEL	R/W	0x0	GPIO02 Output Select Determines the output data for the selected source. If GPIO2_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO2_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO2_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk If GPIO2_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved

Table 1-22. GPIO2_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	GPIO2_OUT_SRC	R/W	0x0	GPIO2 Output Source Select Selects output source for GPIO2 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO2_OUT_VAL	R/W	0x0	GPIO2 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO2_OUT_EN	R/W	0x0	GPIO2 Output Enable 0: Disabled 1: Enabled

1.1.20 GPIO3_PIN_CTL Register (Address = 0x13) [Default = 0x00]

GPIO3_PIN_CTL is shown in Table 1-23.

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Table 1-23. GPIO3_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO3_OUT_SEL	R/W	0x0	GPIO3 Output Select Determines the output data for the selected source. If GPIO3_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO3_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk If GPIO3_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved

Table 1-23. GPIO3_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	GPIO3_OUT_SRC	R/W	0x0	GPIO3 Output Source Select Selects output source for GPIO3 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO3_OUT_VAL	R/W	0x0	GPIO3 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO3_OUT_EN	R/W	0x0	GPIO3 Output Enable 0: Disabled 1: Enabled

1.1.21 GPIO4_PIN_CTL Register (Address = 0x14) [Default = 0x31]

GPIO4_PIN_CTL is shown in Table 1-24.

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Table 1-24. GPIO4_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO4_OUT_SEL	R/W	0x1	GPIO4 Output Select Determines the output data for the selected source. If GPIO4_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO4_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO4_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk If GPIO4_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved

Table 1-24. GPIO4_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	GPIO4_OUT_SRC	R/W	0x4	GPIO4 Output Source Select Selects output source for GPIO4 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO4_OUT_VAL	R/W	0x0	GPIO4 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO4_OUT_EN	R/W	0x1	GPIO4 Output Enable 0: Disabled 1: Enabled

1.1.22 GPIO5_PIN_CTL Register (Address = 0x15) [Default = 0x00]

GPIO5_PIN_CTL is shown in Table 1-25.

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Table 1-25. GPIO5_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO5_OUT_SEL	R/W	0x0	GPIO5 Output Select Determines the output data for the selected source. If GPIO5_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO5_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO0_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk If GPIO5_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved

Table 1-25. GPIO5_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	GPIO5_OUT_SRC	R/W	0x0	GPIO5 Output Source Select Selects output source for GPIO5 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO5_OUT_VAL	R/W	0x0	GPIO5 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO5_OUT_EN	R/W	0x0	GPIO5 Output Enable 0: Disabled 1: Enabled

1.1.23 GPIO6_PIN_CTL Register (Address = 0x16) [Default = 0x00]

GPIO6_PIN_CTL is shown in Table 1-26.

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Table 1-26. GPIO6_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO6_OUT_SEL	R/W	0x0	GPIO6 Output Select Determines the output data for the selected source. If GPIO6_OUT_SRC is set to 00x (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO6_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO6_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: Reserved If GPIO6_OUT_SRC is set to 110 (the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Ports Synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved

Table 1-26. GPIO6_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	GPIO6_OUT_SRC	R/W	0x0	GPIO6 Output Source Select Selects output source for GPIO6 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO6_OUT_VAL	R/W	0x0	GPIO6 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO6_OUT_EN	R/W	0x0	GPIO6 Output Enable 0: Disabled 1: Enabled

1.1.24 GPIO7_PIN_CTL Register (Address = 0x17) [Default = 0x00]

GPIO7_PIN_CTL is shown in Table 1-27.

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Table 1-27. GPIO7_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO7_OUT_SEL	R/W	0x0	GPIO7 Output Select Determines the output data for the selected source. If GPIO7_OUT_SRC is set to 00x (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO7_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO7_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: Reserved If GPIO7_OUT_SRC is set to 110 (the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Ports Synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved

Table 1-27. GPIO7_PIN_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4:2	GPIO7_OUT_SRC	R/W	0x0	GPIO7 Output Source Select Selects output source for GPIO7 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO7_OUT_VAL	R/W	0x0	GPIO7 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO7_OUT_EN	R/W	0x0	GPIO7 Output Enable 0: Disabled 1: Enabled

1.1.25 FS_CTL Register (Address = 0x18) [Default = 0x00]

FS_CTL is shown in Table 1-28.

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Table 1-28. FS_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	FS_MODE	R/W	0x0	FrameSync Mode 0000: Internal Generated FrameSync, use Back-channel frame clock from port 0 0001: Internal Generated FrameSync, use Back-channel frame clock from port 1 0010: Internal Generated FrameSync, use Back-channel frame clock from port 2 0011: Internal Generated FrameSync, use Back-channel frame clock from port 3 01xx: Internal Generated FrameSync, use 25MHz clock 1000: External FrameSync from GPIO0 1001: External FrameSync from GPIO1 1010: External FrameSync from GPIO2 1011: External FrameSync from GPIO3 1100: External FrameSync from GPIO4 1101: External FrameSync from GPIO5 1110: External FrameSync from GPIO6 1111: External FrameSync from GPIO7
3	FS_SINGLE	RH/W1S	0x0	Generate Single FrameSync pulse When this bit is set, a single FrameSync pulse will be generated. The system will wait for the full duration of the desired pulse before generating another pulse. When using this feature, the FS_GEN_ENABLE bit must remain set to 0. This bit is self-clearing and will always return 0.
2	FS_INIT_STATE	R/W	0x0	FrameSync Initial State This register controls the initial state of the FrameSync signal. 0: FrameSync initial state is 0 1: FrameSync initial state is 1

Table 1-28. FS_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	FS_GEN_MODE	R/W	0x0	FrameSync Generation Mode This control selects between Hi/Lo and 50/50 modes. In Hi/Lo mode, the FrameSync generator will use the FS_HIGH_TIME and FS_LOW_TIME register values to separately control the High and Low periods for the generated FrameSync signal. FrameSync times are based on the settings of the FS_MODE field. In 50/50 mode, the FrameSync generator will use the values in the FS_HIGH_TIME_0, FS_LOW_TIME_1 and FS_LOW_TIME_0 registers as a 24-bit value for both the High and Low periods of the generated FrameSync signal. 0: Hi/Lo 1: 50/50
0	FS_GEN_ENABLE	R/W	0x0	FrameSync Generation Enable 0: Disabled 1: Enabled

1.1.26 FS_HIGH_TIME_1 Register (Address = 0x19) [Default = 0x00]

FS_HIGH_TIME_1 is shown in Table 1-29.

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Table 1-29. FS_HIGH_TIME_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAMESYNC_HIGH_TIME_1	R/W	0x0	FrameSync High Time bits 15:8 The value programmed to the FS_HIGH_TIME register must be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

1.1.27 FS_HIGH_TIME_0 Register (Address = 0x1A) [Default = 0x00]

FS_HIGH_TIME_0 is shown in Table 1-30.

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Table 1-30. FS_HIGH_TIME_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAMESYNC_HIGH_TIME_0	R/W	0x0	FrameSync High Time bits 7:0 The value programmed to the FS_HIGH_TIME register must be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

1.1.28 FS_LOW_TIME_1 Register (Address = 0x1B) [Default = 0x00]

FS_LOW_TIME_1 is shown in Table 1-31.

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Table 1-31. FS_LOW_TIME_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAMESYNC_LOW_TIME_1	R/W	0x0	FrameSync Low Time bits 15:8 The value programmed to the FS_HIGH_TIME register must be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

1.1.29 FS_LOW_TIME_0 Register (Address = 0x1C) [Default = 0x00]

FS_LOW_TIME_0 is shown in Table 1-32.

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Table 1-32. FS_LOW_TIME_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAMESYNC_LOW_TIME_0	R/W	0x0	FrameSync Low Time bits 7:0 The value programmed to the FS_HIGH_TIME register must be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

1.1.30 MAX_FRM_HI Register (Address = 0x1D) [Default = 0x00]

MAX_FRM_HI is shown in Table 1-33.

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Table 1-33. MAX_FRM_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MAX_FRAME_HI	R/W	0x0	CSI-2 Maximum Frame Count bits 15:8 In RAW mode operation, the FPD3 Receiver will create CSI2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field will be generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and will always be 0. If Maximum Frame Count value is non-zero, the frame number will increment for each from 1 up to the Maximum Frame Count value before resetting to 1.

1.1.31 MAX_FRM_LO Register (Address = 0x1E) [Default = 0x04]

MAX_FRM_LO is shown in Table 1-34.

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Table 1-34. MAX_FRM_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MAX_FRAME_LO	R/W	0x4	CSI-2 Maximum Frame Count bits 7:0 In RAW mode operation, the FPD3 Receiver will create CSI2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field will be generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and will always be 0. If Maximum Frame Count value is non-zero, the frame number will increment for each from 1 up to the Maximum Frame Count value before resetting to 1.

1.1.32 CSI_PLL_CTL Register (Address = 0x1F) [Default = 0x10]

CSI_PLL_CTL is shown in Table 1-35.

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Table 1-35. CSI_PLL_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	CSI_TX_SPEED[2]	R/W	0x1	CSI timing register select MSB 'Strap 2.5G: 1'b1 800M: '1'b0 See CSI_TX_SPEED[1:0] description At power-up, this field is set based on the MODE pin strap value.

Table 1-35. CSI_PLL_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	RESERVED	R/W	0x0	Reserved
2	REF_CLK_MODE	R/W	0x0	Reference Clock mode The digital logic requires a 200 MHz reference clock generated from the CSI PLL. If this bit is set to 1, the reference clock will be 100 MHz. 0: clock is 200 MHz 1: clock is 100 MHz
1:0	CSI_TX_SPEED[1:0]	R/W	0x0	CSI timing register select: 'Strap 2.5G: 2'h0 800M: '2'h2 This register selects the operating rate and CSI timing parameters for the CSI Transmitter. In addition to setting this field, the CSI_PLL_DIV register must also be programmed for the correct divider selection. 0_00: 1.6 Gbps serial rate 0_01: 1.2 Gbps serial rate 0_10: 800 Mbps serial rate 0_11: 400 Mbps serial rate 1_xx: 2.5 Gbps serial rate At power-up, this field is set based on the MODE pin strap value.

1.1.33 FWD_CTL1 Register (Address = 0x20) [Default = 0xF0]

FWD_CTL1 is shown in Table 1-36.

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Table 1-36. FWD_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	FWD_PORT3_DIS	R/W	0x1	Disable forwarding of RX Port 3 0: Forwarding enabled 1: Forwarding disabled
6	FWD_PORT2_DIS	R/W	0x1	Disable forwarding of RX Port 2 0: Forwarding enabled 1: Forwarding disabled
5	FWD_PORT1_DIS	R/W	0x1	Disable forwarding of RX Port 1 0: Forwarding enabled 1: Forwarding disabled
4	FWD_PORT0_DIS	R/W	0x1	Disable forwarding of RX Port 0 0: Forwarding enabled 1: Forwarding disabled
3	RX3_MAP	R/W	0x0	Map RX Port 3 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.
2	RX2_MAP	R/W	0x0	Map RX Port 2 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.
1	RX1_MAP	R/W	0x0	Map RX Port 1 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.

Table 1-36. FWD_CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	RX0_MAP	R/W	0x0	Map RX Port 0 to CSI-2 Port 0: CSI-2 Port 0 1: CSI-2 Port 1 It is recommended to disable forwarding for a port before changing the port mapping.

1.1.34 FWD_CTL2 Register (Address = 0x21) [Default = 0x03]

FWD_CTL2 is shown in Table 1-37.

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Table 1-37. FWD_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	FWD_SYNC_AS_AVAIL	R/W	0x0	Synchronized Forwarding As Available During Synchronized Forwarding, each forwarding engine will wait for video data to be available from each enabled port, prior to sending the video line. Setting this bit to a 1 will allow sending the next video line as it becomes available. For example if RX Ports 0 and 1 are being forwarded, port 0 video line will be forwarded when it becomes available, rather than waiting until both ports 0 and ports 1 have video data available. This operation may reduce the likelihood of buffer overflow errors in some conditions. This bit will have no affect in video line concatenation mode and only affects video lines (long packets) rather than synchronization packets. This bit applies to both CSI output ports
5:4	CSI1_SYNC_FWD	R/W	0x0	Enable synchronized forwarding for CSI output port 1 00: Synchronized forwarding disabled 01: Basic Synchronized forwarding enabled 10: Synchronous forwarding with line interleaving 11: Synchronous forwarding with line concatenation Only one of CSI1_RR_FWD and CSI1_SYNC_FWD must be enabled at a time.
3:2	CSI0_SYNC_FWD	R/W	0x0	Enable synchronized forwarding for CSI output port 0 00: Synchronized forwarding disabled 01: Basic Synchronized forwarding enabled 10: Synchronous forwarding with line interleaving 11: Synchronous forwarding with line concatenation Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be enabled at a time.
1	CSI1_RR_FWD	R/W	0x1	Enable best-effort forwarding for CSI output port 1. When this mode is enabled, no attempt is made to synchronize the video traffic. When multiple sources have data available to forward, the data will tend to be forwarded in a round-robin fashion. 0: Round robin forwarding disabled 1: Round robin forwarding enabled Only one of CSI1_RR_FWD and CSI1_SYNC_FWD must be enabled at a time.
0	CSI0_RR_FWD	R/W	0x1	Enable best-effort forwarding for CSI output port 0. When this mode is enabled, no attempt is made to synchronize the video traffic. When multiple sources have data available to forward, the data will tend to be forwarded in a round-robin fashion. 0: Round robin forwarding disabled 1: Round robin forwarding enabled Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be enabled at a time.

1.1.35 FWD_STS Register (Address = 0x22) [Default = 0x00]

FWD_STS is shown in Table 1-38.

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Table 1-38. FWD_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	CSI_REPLICATE_CSI1	R/W	0x0	CSI Replicate Mode for CSI PORT 1 Setting this bit enables 2-lane Replication mode for CSI Port 1. When enabled, data on lanes 0/1 will be replicated to lanes 2/3 for CSI Port 1. In D-PHY mode, the 2nd clock pin will also be enabled the port.
4	RESERVED	R/W	0x0	RESERVED
3	FWD_SYNC_FAIL1	RC	0x0	Forwarding synchronization failed for CSI output port 1 During Synchronized forwarding, this flag indicates a failure of synchronized video has been detected. For this bit to be set, the forwarding process must have previously been successful at sending at least one synchronized video frame. 0: No failure 1: Synchronization failure This bit is cleared on read.
2	FWD_SYNC_FAIL0	RC	0x0	Forwarding synchronization failed for CSI output port 0 During Synchronized forwarding, this flag indicates a failure of synchronized video has been detected. For this bit to be set, the forwarding process must have previously been successful at sending at least one synchronized video frame. 0: No failure 1: Synchronization failure This bit is cleared on read.
1	FWD_SYNC1	R	0x0	Forwarding synchronized for CSI output port 1 During Synchronized forwarding, this bit indicates that the forwarding engine is currently able to provide synchronized video from enabled Receive ports. This bit will always be 0 if Synchronized forwarding is disabled. 0: Video is not synchronized 1: Video is synchronized
0	FWD_SYNC0	R	0x0	Forwarding synchronized for CSI output port 0 During Synchronized forwarding, this bit indicates that the forwarding engine is currently able to provide synchronized video from enabled Receive ports. This bit will always be 0 if Synchronized forwarding is disabled. 0: Video is not synchronized 1: Video is synchronized

1.1.36 INTERRUPT_CTL Register (Address = 0x23) [Default = 0x00]

INTERRUPT_CTL is shown in Table 1-39.

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Table 1-39. INTERRUPT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	INT_EN	R/W	0x0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.
6	IE_DEV	R/W	0x0	Local Device Interrupt. Enable interrupts for general device functions. See the LOCAL_DEV_ICR register for the functions that can generate the local device interrupts.
5	IE_CSI_TX1	R/W	0x0	CSI Transmit Port 1 Interrupt: Enable interrupt from CSI Transmitter Port 1.
4	IE_CSI_TX0	R/W	0x0	CSI Transmit Port 0 Interrupt: Enable interrupt from CSI Transmitter Port 0.
3	IE_RX3	R/W	0x0	RX Port 3 Interrupt: Enable interrupt from Receiver Port 3.

Table 1-39. INTERRUPT_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	IE_RX2	R/W	0x0	RX Port 2 Interrupt: Enable interrupt from Receiver Port 2.
1	IE_RX1	R/W	0x0	RX Port 1 Interrupt: Enable interrupt from Receiver Port 1.
0	IE_RX0	R/W	0x0	RX Port 0 Interrupt: Enable interrupt from Receiver Port 0.

1.1.37 INTERRUPT_STS Register (Address = 0x24) [Default = 0x00]

INTERRUPT_STS is shown in Table 1-40.

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Table 1-40. INTERRUPT_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	INT	R	0x0	Global Interrupt: Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INT_EN bit in the INTERRUPT_CTL register but does depend on the IE_xxx bits. For example, if IE_RX0 and IS_RX0 are both asserted, the INT bit will be set to 1.
6	IS_DEV	R	0x0	Local Device Interrupt: A general device interrupt has been generated. If this bit is set, the LOCAL_DEV_ISR register must be read to determine the source of the interrupt. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt.
5	IS_CSI_TX1	R	0x0	CSI Transmit Port 1 Interrupt: An interrupt has occurred for CSI Transmitter Port 1. This interrupt will be cleared upon reading the CSI_TX_ISR register for CSI Transmit Port 1.
4	IS_CSI_TX0	R	0x0	CSI Transmit Port 0 Interrupt: An interrupt has occurred for CSI Transmitter Port 0. This interrupt will be cleared upon reading the CSI_TX_ISR register for CSI Transmit Port 0.
3	IS_RX3	R	0x0	RX Port 3 Interrupt: An interrupt has occurred for Receive Port 3. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
2	IS_RX2	R	0x0	RX Port 2 Interrupt: An interrupt has occurred for Receive Port 2. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
1	IS_RX1	R	0x0	RX Port 1 Interrupt: An interrupt has occurred for Receive Port 1. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
0	IS_RX0	R	0x0	RX Port 0 Interrupt: An interrupt has occurred for Receive Port 0. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.

1.1.38 TS_CONFIG Register (Address = 0x25) [Default = 0x00]

TS_CONFIG is shown in Table 1-41.

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Table 1-41. TS_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	FS_POLARITY	R/W	0x0	Framesync Polarity Indicates active edge of FrameSync signal 0: Rising edge 1: Falling edge
5:4	TS_RES_CTL	R/W	0x0	Timestamp Resolution Control 00: 40 ns 01: 80 ns 10: 160 ns 11: 1.0 us
3	TS_AS_AVAIL	R/W	0x0	Timestamp Ready Control 0: Normal operation 1: Indicate timestamps ready as soon as all port timestamps are available
2	RESERVED	R	0x0	Reserved
1	TS_FREERUN	R/W	0x0	FreeRun Mode 0: FrameSync mode 1: FreeRun mode
0	TS_MODE	R/W	0x0	Timestamp Mode 0: Line start 1: Frame start

1.1.39 TS_CONTROL Register (Address = 0x26) [Default = 0x00]

TS_CONTROL is shown in Table 1-42.

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Table 1-42. TS_CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	TS_FREEZE	R/W	0x0	Freeze Timestamps 0: Normal operation 1: Freeze timestamps Setting this bit will freeze timestamps and clear the TS_READY flag. The TS_FREEZE bit must be cleared after reading timestamps to resume operation.
3	TS_ENABLE3	R/W	0x0	Timestamp Enable RX Port 3 0: Disabled 1: Enabled
2	TS_ENABLE2	R/W	0x0	Timestamp Enable RX Port 2 0: Disabled 1: Enabled
1	TS_ENABLE1	R/W	0x0	Timestamp Enable RX Port 1 0: Disabled 1: Enabled
0	TS_ENABLE0	R/W	0x0	Timestamp Enable RX Port 0 0: Disabled 1: Enabled

1.1.40 TS_LINE_HI Register (Address = 0x27) [Default = 0x00]

TS_LINE_HI is shown in Table 1-43.

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Table 1-43. TS_LINE_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TS_LINE_HI	R/W	0x0	Timestamp Line, upper 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number must be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start

1.1.41 TS_LINE_LO Register (Address = 0x28) [Default = 0x00]

TS_LINE_LO is shown in Table 1-44.

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Table 1-44. TS_LINE_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TS_LINE_LO	R/W	0x0	Timestamp Line, lower 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number must be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start

1.1.42 TS_STATUS Register (Address = 0x29) [Default = 0x00]

TS_STATUS is shown in Table 1-45.

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Table 1-45. TS_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	TS_READY	R	0x0	Timestamp Ready This flag indicates when timestamps are ready to be read. This flag will be cleared when the TS_FREEZE bit is set.
3	TS_VALID3	R	0x0	Timestamp Valid, RX Port 3
2	TS_VALID2	R	0x0	Timestamp Valid, RX Port 2
1	TS_VALID1	R	0x0	Timestamp Valid, RX Port 1
0	TS_VALID0	R	0x0	Timestamp Valid, RX Port 0

1.1.43 TIMESTAMP_P0_HI Register (Address = 0x2A) [Default = 0x00]

TIMESTAMP_P0_HI is shown in Table 1-46.

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Table 1-46. TIMESTAMP_P0_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P0_HI	R	0x0	Timestamp, upper 8 bits, RX Port 0

1.1.44 TIMESTAMP_P0_LO Register (Address = 0x2B) [Default = 0x00]

TIMESTAMP_P0_LO is shown in Table 1-47.

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Table 1-47. TIMESTAMP_P0_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P0_LO	R	0x0	Timestamp, lower 8 bits, RX Port 0

1.1.45 TIMESTAMP_P1_HI Register (Address = 0x2C) [Default = 0x00]

TIMESTAMP_P1_HI is shown in Table 1-48.

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Table 1-48. TIMESTAMP_P1_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P1_HI	R	0x0	Timestamp, upper 8 bits, RX Port 1

1.1.46 TIMESTAMP_P1_LO Register (Address = 0x2D) [Default = 0x00]

TIMESTAMP_P1_LO is shown in Table 1-49.

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Table 1-49. TIMESTAMP_P1_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P1_LO	R	0x0	Timestamp, lower 8 bits, RX Port 1

1.1.47 TIMESTAMP_P2_HI Register (Address = 0x2E) [Default = 0x00]

TIMESTAMP_P2_HI is shown in Table 1-50.

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Table 1-50. TIMESTAMP_P2_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P2_HI	R	0x0	Timestamp, upper 8 bits, RX Port 2

1.1.48 TIMESTAMP_P2_LO Register (Address = 0x2F) [Default = 0x00]

TIMESTAMP_P2_LO is shown in Table 1-51.

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Table 1-51. TIMESTAMP_P2_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P2_LO	R	0x0	Timestamp, lower 8 bits, RX Port 2

1.1.49 TIMESTAMP_P3_HI Register (Address = 0x30) [Default = 0x00]

TIMESTAMP_P3_HI is shown in Table 1-52.

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Table 1-52. TIMESTAMP_P3_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P3_HI	R	0x0	Timestamp, upper 8 bits, RX Port 3

1.1.50 TIMESTAMP_P3_LO Register (Address = 0x31) [Default = 0x00]

TIMESTAMP_P3_LO is shown in Table 1-53.

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Table 1-53. TIMESTAMP_P3_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	TIMESTAMP_P3_LO	R	0x0	Timestamp, lower 8 bits, RX Port 3

1.1.51 CSI_PORT_SEL Register (Address = 0x32) [Default = 0x00]

CSI_PORT_SEL is shown in Table 1-54.

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Table 1-54. CSI_PORT_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	TX_READ_PORT	R/W	0x0	Select TX port for register read This field selects one of the two TX port register blocks for readback. This applies to the subsequent registers prefixed CSI. 0: Port 0 registers 1: Port 1 registers
3:2	RESERVED	R	0x0	Reserved
1	TX_WRITE_PORT_1	R/W	0x0	Write Enable for TX port 1 registers This bit enables writes to TX port 1 registers. Any combination of TX port registers can be written simultaneously. This applies to the subsequent registers prefixed CSI. 0: Writes disabled 1: Writes enabled
0	TX_WRITE_PORT_0	R/W	0x0	Write Enable for TX port 0 registers This bit enables writes to TX port 0 registers. Any combination of TX port registers can be written simultaneously. This applies to the subsequent registers prefixed CSI. 0: Writes disabled 1: Writes enabled

1.1.52 CSI_CTL Register (Address = 0x33) [Default = 0x00]

CSI_CTL is shown in Table 1-55.

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Table 1-55. CSI_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	CSI_CAL_EN	R/W	0x0	Enable initial CSI Skew-Calibration sequence When the initial skew-calibration sequence is enabled, the CSI Transmitter will send the sequence at initialization, prior to sending any HS data. This bit must be set when operating at 1.6 Gbps CSI speed (as configured in the CSI_PLL register). 0: Disabled 1: Enabled
5:4	CSI_LANE_COUNT	R/W	0x0	CSI lane count 00: 4 lanes 01: 3 lanes 10: 2 lanes 11: 1 lane
3:2	CSI_ULP	R/W	0x0	Force LP00 state on data/clock lanes 00: Normal operation 01: LP00 state forced only on data lanes 10: Reserved 11: LP00 state forced on data and clock lanes

Table 1-55. CSI_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	CSI_CONTS_CLOCK	R/W	0x0	Enable CSI continuous clock mode When enabled, the CSI Transmitter will enter continuous clock mode upon transmission of the first packet. 0: Disabled 1: Enabled
0	CSI_ENABLE	R/W	0x0	Enable CSI output 0: Disabled 1: Enabled Forwarding must be disabled (via the FWD_CTL1 register) prior to enabling or disabling the CSI output.

1.1.53 CSI_CTL2 Register (Address = 0x34) [Default = 0x00]

CSI_CTL2 is shown in Table 1-56.

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Table 1-56. CSI_CTL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5:4	CSI_CAL_LEN	R	0x0	These bits control the length of the periodic calibration sequence 00: 2^{10} bits 01: 2^{12} bits 10: 2^{14} bits 11: 2^{15} bits
3	CSI_PASS_MODE	R/W	0x0	CSI PASS indication mode Determines whether the CSI Pass indication is for a single port or all enabled ports. 0: Assert PASS if at least one enabled Receive port is providing valid video data 1: Assert PASS only if ALL enabled Receive ports are providing valid video data
2	CSI_CAL_INV	R/W	0x0	CSI Calibration Inverted Data pattern During the CSI skew-calibration pattern, the CSI Transmitter will send a sequence of 01010101 data (first bit 0). Setting this bit to a 1 will invert the sequence to 10101010 data.
1	CSI_CAL_SINGLE	RH/W1S	0x0	Enable single periodic CSI Skew-Calibration sequence Setting this bit will send a single skew-calibration sequence from the CSI Transmitter. The skew-calibration sequence will be the 1010 bit sequence required for periodic calibration. The calibration sequence will be sent at the next idle period on the CSI interface. This bit is self-clearing and will reset to 0 after the calibration sequence is sent. Note: Adjust skew cal settings from CSI_CAL_LEN and CSI_CAL_INV with a separate register write prior to setting this bit
0	CSI_CAL_PERIODIC	R/W	0x0	Enable periodic CSI Skew-Calibration sequence When the periodic skew-calibration sequence is enabled, the CSI Transmitter will send the periodic skew-calibration sequence following the sending of Frame End packets. Note: Adjust skew cal settings from CSI_CAL_LEN and CSI_CAL_INV with a separate register write prior to setting this bit 0: Disabled 1: Enabled

1.1.54 CSI_STS Register (Address = 0x35) [Default = 0x00]

CSI_STS is shown in Table 1-57.

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Table 1-57. CSI_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	TX_PORT_NUM	R	0x0	TX Port Number This read-only field indicates the number of the currently selected TX read port.
3:2	RESERVED	R	0x0	Reserved
1	TX_PORT_SYNC	R	0x0	TX Port Synchronized Thist bit indicates the CSI Transmit Port is able to properly synchronize input data streams from multiple sources. This bit will be 0 if synchronization is disabled via the FWD_CTL2 register. 0: Input streams are not synchronized 1: Input streams are synchronized
0	PASS	R	0x0	TX Port Pass Indicates valid data is available on at least one port, or on all ports if configured for all port status via the CSI_PASS_MODE bit in the CSI_CTL2 register. The function differs based on mode of operation. In asynchronous operation, the TX_PORT_PASS indicates the CSI port is actively delivering valid video data. The status will be cleared based on detection of an error condition that interrupts transmission. During Synchronized forwarding, the TX_PORT_PASS indicates valid data is available for delivery on the CSI TX output. Data may not be delivered if ports are not synchronized. The TX_PORT_SYNC status is a better indicator that valid data is being delivered to the CSI transmit port.

1.1.55 CSI_TX_ICR Register (Address = 0x36) [Default = 0x00]

CSI_TX_ICR is shown in Table 1-58.

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Table 1-58. CSI_TX_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	IE_RX_PORT_INT	R/W	0x0	RX Port Interrupt Enable Enable interrupt based on receiver port interrupt for the RX Ports being forwarded to the CSI Transmit Port.
3	IE_CSI_SYNC_ERROR	R/W	0x0	CSI Sync Error interrupt Enable Enable interrupt on CSI Synchronization enable.
2	IE_CSI_SYNC	R/W	0x0	CSI Synchronized interrupt Enable Enable interrupts on CSI Transmit Port assertion of CSI Synchronized Status.
1	IE_CSI_PASS_ERROR	R/W	0x0	CSI RX Pass Error interrupt Enable Enable interrupt on CSI Pass Error
0	IE_CSI_PASS	R/W	0x0	CSI Pass interrupt Enable Enable interrupt on CSI Transmit Port assertion of CSI Pass.

1.1.56 CSI_TX_ISR Register (Address = 0x37) [Default = 0x00]

CSI_TX_ISR is shown in Table 1-59.

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Table 1-59. CSI_TX_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-59. CSI_TX_ISR Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	IS_RX_PORT_INT	R	0x0	RX Port Interrupt A Receiver port interrupt has been generated for one of the RX Ports being forwarded to the CSI Transmit Port. A read of the associated port receive status registers will clear this interrupt. See the PORT_ISR_HI and PORT_ISR_LO registers for details.
3	IS_CSI_SYNC_ERROR	RC	0x0	CSI Sync Error interrupt A synchronization error has been detected for multiple video stream inputs to the CSI Transmitter.
2	IS_CSI_SYNC	RC	0x0	CSI Synchronized interrupt CSI Transmit Port assertion of CSI Synchronized Status. Current status for CSI Sync can be read from the TX_PORT_SYNC flag in the CSI_STS register.
1	IS_CSI_PASS_ERROR	RC	0x0	CSI RX Pass Error interrupt A deassertion of CSI Pass has been detected on one of the RX Ports being forwarded to the CSI Transmit Port
0	IS_CSI_PASS	RC	0x0	CSI Pass interrupt CSI Transmit Port assertion of CSI Pass detected. Current status for the CSI Pass indication can be read from the TX_PORT_PASS flag in the CSI_STS register

1.1.57 REFCLK_FREQ Register (Address = 0x3D) [Default = 0x19]

REFCLK_FREQ is shown in Table 1-60.

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Table 1-60. REFCLK_FREQ Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	REFCLK_FREQ	R	0x19	REFCLK frequency measurement in MHz.

1.1.58 BCC_ERR_CTL Register (Address = 0x46) [Default = 0x00]

BCC_ERR_CTL is shown in Table 1-61.

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Table 1-61. BCC_ERR_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	BCC_ACK_REMOTE_READ	R/W	0x0	Enable Control Channel to acknowledge start of remote read. When operating with a link partner that supports Enhanced Error Checking for the Bidirectional Control Channel, setting this bit allows the Deserializer to generate an internal acknowledge to the beginning of a remote I2C target read. This allows additional error detection at the Seserializer. This bit must not be set when operating with Serializers that do not support Enhanced Error Checking. 0: Disable 1: Enable
6	BCC_EN_DATA_CHK	R/W	0x0	Enable checking of returned data Enhanced Error checking can check for errors on returned data during an acknowledge cycle for data sent to remote devices over the Bidirectional Control Channel. In addition, If an error is detected, this register control will allow changing a remote Ack to a Nack to indicate the data error on the local I2C interface. This bit must not be set when operating with Serializers that do not support Enhanced Error checking as they will not always return the correct data during an Ack. 0: Disable returned data error detection 1: Enable returned data error detection

Table 1-61. BCC_ERR_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	BCC_EN_ENH_ERROR	R/W	0x0	Enable Enhanced Error checking in Bidirectional Control Channel The Bidirectional Control Channel can detect certain error conditions and terminate transactions if an error is detected. This capability can be disabled by setting this bit to 0. 0: Disable Enhanced Error checking 1: Enable Enhanced Error checking
4:3	FORCE_BCC_ERROR	R/W	0x0	BCC Force Error The BCC Force Error control causes an error to be forced on the BCC over the back channel. 00: No error 01: Force CRC Error on BCC frame= BCC_FRAME_SEL 10: Force CRC Error on normal frame following BCC frame= BCC_FRAME_SEL 11: FORCE Data Error on BCC frame= BCC_FRAME_SEL Setting this control generates a single error on the back channel signaling.
2:0	BCC_FRAME_SEL	R/W	0x0	BCC Frame Select The BCC Frame Select allows selection of the forward channel BCC frame which will include the error condition selected in the force control bits of this register. BCC transfers are sent in bytes for each block transferred. This value may be set in range of 0 to 7 to force an error on any of the first 8 bytes sent on the BCC forward channel.

1.1.59 BCC_STATUS Register (Address = 0x47) [Default = 0x00]

BCC_STATUS is shown in Table 1-62.

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Table 1-62. BCC_STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	
5	BCC_SEQ_ERROR	RC	0x0	Bidirectional Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. If BCC_EN_ENH_ERR is 0 (disabled), this register is read-only copy of the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. If BCC_EN_ENH_ERR is 1 (enabled), this register is cleared on read of this register.
4	BCC_CONTROLLER_ERR	RC	0x0	BCC Controller Error This flag indicates a Forward Channel BCC Sequence, BCC CRC, or Lock error occurred while waiting for a response from the Serializer while the BCC I2C Controller is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.
3	BCC_CONTROLLER_TO	RC	0x0	BCC Target Timeout Error This bit will be set if the BCC Watchdog Timer expires will waiting for a response from the Serializer while the BCC I2C Controller is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.
2	BCC_TARGET_ERR	RC	0x0	BCC Target Error This flag indicates a Forward Channel BCC Sequence, BCC CRC, or Lock error occurred while waiting for a response from the Serializer while the BCC I2C Target is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.
1	BCC_TARGET_TO	RC	0x0	BCC Target Timeout Error This bit will be set if the BCC Watchdog Timer expires will waiting for a response from the Serializer while the BCC I2C Target is active. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.

Table 1-62. BCC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	BCC_RESP_ERR	RC	0x0	BCC Response Error This flag indicates an error has been detected in response to a command on the Bidirectional Control Channel. When the I2C Target is active, the Serializer will return data written (I2C address, offset, or data). When the I2C Target is active, the Serializer will return data read. The BCC function checks the returned data for errors, and will set this flag if an error is detected. This flag is cleared on read of this register. This indication is available only if BCC_EN_ENH_ERR is set to 1.

1.1.60 RAW_EMBED_DTYPE Register (Address = 0x4B) [Default = 0x12]

RAW_EMBED_DTYPE is shown in Table 1-63.

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Table 1-63. RAW_EMBED_DTYPE Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	EMBED_DTYPE_EN	R/W	0x0	Embeded Data Type Enable When the receiver is programmed for Raw mode data, this register field allows setting the Data Type field for the first N lines to indicated embedded non-image data. 0: All long packets will be forwarded as RAW10 or RAW12 video data 1-3: Send first N long packets (1, 2, or 3) as Embedded data using the data type in the EMBED_DTYPE_ID field of this register. This control has no effect if the Receiver is programmed to receive CSI formatted data.
5:0	EMBED_DTYPE_ID	R/W	0x12	Embedded Data Type If sending embedded data is enabled via the EMBED_DTYPE_EN control in this register, the Data Type field for the first N lines of each frame will use this value rather than the value programmed in the RAW12_ID or RAW10_ID registers. The default setting matches the CSI-2 specification for Embedded 8-bit non Image Data.

1.1.61 FPD3_PORT_SEL Register (Address = 0x4C) [Default = 0x00]

FPD3_PORT_SEL is shown in Table 1-64.

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Table 1-64. FPD3_PORT_SEL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PHYS_PORT_NUM	R	0x0	Physical port number This field provides the physical port connection when reading from a remote device via the Bidirectional Control Channel. When accessed via local I2C interfaces, the value returned is always 0. When accessed via Bidirectional Control Channel, the value returned is the port number of the Receive port connection.
5:4	RX_READ_PORT	R/W	0x0	Select RX port for register read This field selects one of the four RX port register blocks for readback. This applies to all paged FPD Receiver port registers. 00: Port 0 registers 01: Port 1 registers 10: Port 2 registers 11: Port 3 registers When accessed via local I2C interfaces, the default setting is 0. When accessed via Bidirectional Control Channel, the default value is the port number of the Receive port connection.

Table 1-64. FPD3_PORT_SEL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	RX_WRITE_PORT_3	R/W	0x0	Write Enable for RX port 3 registers This bit enables writes to RX port 3 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 3. 1 for RX Port 3
2	RX_WRITE_PORT_2	R/W	0x0	Write Enable for RX port 2 registers This bit enables writes to RX port 2 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 2. 1 for RX Port 2
1	RX_WRITE_PORT_1	R/W	0x0	Write Enable for RX port 1 registers This bit enables writes to RX port 1 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 1. 1 for RX Port 1
0	RX_WRITE_PORT_0	R/W	0x0	Write Enable for RX port 0 registers This bit enables writes to RX port 0 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bidirectional Control Channel, the default value is 1 if accessed over RX port 0. 1 for Rx Port 0

1.1.62 RX_PORT_STS1 Register (Address = 0x4D) [Default = 0x00]

RX_PORT_STS1 is shown in Table 1-65.

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Table 1-65. RX_PORT_STS1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RX_PORT_NUM	R	0x0	RX Port Number This read-only field indicates the number of the currently selected RX read port.
5	BCC_CRC_ERROR	RC	0x0	Bidirectional Control Channel CRC Error Detected This bit indicates a CRC error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.
4	LOCK_STS_CHG	RC	0x0	Lock Status Changed This bit is set if a change in receiver lock status has been detected since the last read of this register. Current lock status is available in the LOCK_STS bit of this register This bit is cleared on read.

Table 1-65. RX_PORT_STS1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	BCC_SEQ_ERROR/ BCC_ERROR	RC	0x0	The function of this bit depends on the setting of the BCC_EN_ENH_ERR control in the BCC_ERR_CTL register. If BCC_EN_ENH_ERR is 0 (disabled), this register is defined as follows: Bidirectional Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read. If BCC_EN_ENH_ERR is 1 (enabled), this register is defined as follows: Bidirectional Control Channel Error Flag This flag indicates one or more errors have been detected during Bidirectional Control Channel communication with the Deserializer. The BCC_STATUS register contains further information on the type of error detected. This bit will be cleared upon read of the BCC_STATUS register.
2	PARITY_ERROR	R	0x0	FPD parity errors detected This flag is set when the number of parity errors detected is greater than the threshold programmed in the PAR_ERR_THOLD registers. 1: Number of FPD parity errors detected is greater than the threshold 0: Number of FPD parity errors is below the threshold This bit is cleared when the RX_PAR_ERR_HI/LO registers are cleared.
1	PORT_PASS	R	0x0	Receiver PASS indication This bit indicates the current status of the Receiver PASS indication. The requirements for setting the Receiver PASS indication are controlled by the PORT_PASS_CTL register. 1: Receive input has met PASS criteria 0: Receive input does not meet PASS criteria
0	LOCK_STS	R	0x0	FPD-Link receiver is locked to incoming data 1: Receiver is locked to incoming data 0: Receiver is not locked

1.1.63 RX_PORT_STS2 Register (Address = 0x4E) [Default = 0x00]

RX_PORT_STS2 is shown in Table 1-66.

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Table 1-66. RX_PORT_STS2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	LINE_LEN_UNSTABLE	RC	0x0	Line Length Unstable If set, this bit indicates the line length was detected as unstable during a previous video frame. The line length is considered to be stable if all the lines in the video frame have the same length. This flag will remain set until read.
6	LINE_LEN_CHG	RC	0x0	Line Length Changed 1: Change of line length detected 0: Change of line length not detected This bit is cleared on read.
5	FPD_ENCODE_ERROR	RC	0x0	FPD Encoder error detected If set, this flag indicates an error in the FPD-Link encoding has been detected by the FPD-Link receiver. This bit is cleared on read. Note, to detect FPD Encoder errors, the LINK_ERROR_COUNT must be enabled with a LINK_ERR_THRESH value greater than 1. Otherwise, the loss of Receiver Lock will prevent detection of the Encoder error.

Table 1-66. RX_PORT_STS2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	BUFFER_ERROR	RC	0x0	Packet buffer error detected. If this bit is set, an overflow condition has occurred on the packet buffer FIFO. 1: Packet Buffer error detected 0: No Packet Buffer errors detected This bit is cleared on read.
3	CSI_ERROR	R	0x0	CSI Receive error detected See the CSI_RX_STS register for details.
2	FPD_FREQ_STABLE	R	0x0	FPD Frequency measurement stable Indicates the FPD input clock frequency is stable. Setting of this flag is dependent on the stability control settings in the FREQ_DET_CTL register. This field is not applicable for rates >4.16 Gbps
1	NO_FPD_CLK	R	0x0	No FPD-Link input clock detected When set, this bit indicates that no FPD Clock has been detected. This bit will be set if the input frequency is below the setting programmed in the FREQ_LO_THR setting in the FREQ_DET_CTL register. This field is not applicable for rates >4.16 Gbps
0	LINE_CNT_CHG	RC	0x0	Line Count Changed 1: Change of line count detected 0: Change of line count not detected This bit is cleared on read.

1.1.64 RX_FREQ_HIGH Register (Address = 0x4F) [Default = 0x00]

RX_FREQ_HIGH is shown in Table 1-67.

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Table 1-67. RX_FREQ_HIGH Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FREQ_CNT_HIGH	R	0x0	Frequency Counter High Byte (MHz) The Frequency counter reports the measured frequency for the FPD Receiver. This portion of the field is the integer value in MHz. Frequency measurements will scale with reference clock frequency. This field is not applicable for rates >4.16 Gbps

1.1.65 RX_FREQ_LOW Register (Address = 0x50) [Default = 0x00]

RX_FREQ_LOW is shown in Table 1-68.

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Table 1-68. RX_FREQ_LOW Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FREQ_CNT_LOW	R	0x0	Frequency Counter Low Byte (1/256 MHz) The Frequency counter reports the measured frequency for the FPD Receiver. This portion of the field is the fractional value in 1/256 MHz. Frequency measurements will scale with reference clock frequency. This field is not applicable for rates >4.16 Gbps

1.1.66 SENSOR_STS_0 Register (Address = 0x51) [Default = 0x00]

SENSOR_STS_0 is shown in Table 1-69.

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Table 1-69. SENSOR_STS_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SENSOR_STS_0	R	0x0	Sensor Status Register 0 This field provides status from the Serializer. It is automatically loaded from the forward channel. Refer to the Serializer Datasheet

1.1.67 SENSOR_STS_1 Register (Address = 0x52) [Default = 0x00]

SENSOR_STS_1 is shown in Table 1-70.

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Table 1-70. SENSOR_STS_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SENSOR_STS_1	R	0x0	Sensor Status Register 1 This field provides status from the Serializer. It is automatically loaded from the forward channel. Refer to the Serializer Datasheet

1.1.68 SENSOR_STS_2 Register (Address = 0x53) [Default = 0x00]

SENSOR_STS_2 is shown in Table 1-71.

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Table 1-71. SENSOR_STS_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SENSOR_STS_2	R	0x0	Sensor Status Register 2 This field provides status from the Serializer. It is automatically loaded from the forward channel. Refer to the Serializer Datasheet

1.1.69 SENSOR_STS_3 Register (Address = 0x54) [Default = 0x00]

SENSOR_STS_3 is shown in Table 1-72.

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Table 1-72. SENSOR_STS_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SENSOR_STS_3	R	0x0	Sensor Status Register 3 This field provides status from the Serializer. It is automatically loaded from the forward channel. Refer to the Serializer Datasheet

1.1.70 RX_PAR_ERR_HI Register (Address = 0x55) [Default = 0x00]

RX_PAR_ERR_HI is shown in Table 1-73.

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Table 1-73. RX_PAR_ERR_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PAR_ERROR_BYTE_1	R	0x0	Number of FPD3 parity errors – 8 most significant bits The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register will be cleared upon reading the RX_PAR_ERR_LO register.

1.1.71 RX_PAR_ERR_LO Register (Address = 0x56) [Default = 0x00]

RX_PAR_ERR_LO is shown in Table 1-74.

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Table 1-74. RX_PAR_ERR_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PAR_ERROR_BYTE_0	RC	0x0	Number of FPD3 parity errors – 8 least significant bits The parity error counter registers return the number of data parity errors that have been detected on the FPD3 Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX PARITY CHECKER ENABLE bit in register 0x2 prior to reading the parity error count registers. This register will be cleared on read.

1.1.72 BIST_ERR_COUNT Register (Address = 0x57) [Default = 0x00]

BIST_ERR_COUNT is shown in Table 1-75.

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Table 1-75. BIST_ERR_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	BIST_ERROR_COUNT	R	0x0	Bist Error Count Returns BIST error count

1.1.73 BCC_CONFIG Register (Address = 0x58) [Default = 0x1E]

BCC_CONFIG is shown in Table 1-76.

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Table 1-76. BCC_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7	I2C_PASS_THROUGH_ALL	R/W	0x0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
6	I2C_PASS_THROUGH	R/W	0x0	I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled
5	AUTO_ACK_ALL	R/W	0x0	Automatically Acknowledge all I2C writes independent of the forward channel lock state or status of the remote Acknowledge 1: Enable 0: Disable
4	BC_ALWAYS_ON	R/W	0x1	Back channel enable Strap 1: Back channel is always enabled independent of I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL 0: Back channel enable requires setting of either I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL This bit may only be written via a local I2C controller. At power-up, this field is set based on the MODE pin strap value.
3	BC_CRC_GEN_ENABLE	R/W	0x1	Back Channel CRC Generator Enable 0: Disable 1: Enable

Table 1-76. BCC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2:0	BC_FREQ_SELECT	R/W	0x6	Back Channel Frequency Select Strap 000: 2.5 Mbps (default for DS90UB913 compatibility) 001: Reserved 010: 10 Mbps 011: Reserved 100: Reserved 101: 25 Mbps 110: 50 Mbps (default for DS90UB953 compatibility) 111: Reserved Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Deserializer must first be programmed to Auto-Ack operation to avoid a control channel timeout due to lack of response from the Serializer.

1.1.74 DATAPATH_CTL1 Register (Address = 0x59) [Default = 0x00]

DATAPATH_CTL1 is shown in Table 1-77.

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Table 1-77. DATAPATH_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OVERRIDE_FC_CONFIG	R/W	0x0	1: Disable loading of the DATAPATH_CTL registers from the forward channel, keeping locally written values intact 0: Allow forward channel loading of DATAPATH_CTL registers
6:2	RESERVED	R/W	0x0	Reserved
1:0	FC_GPIO_EN	R/W	0x0	Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs 00: GPIOs disabled 01: One GPIO 10: Two GPIOs 11: Four GPIOs This field is normally loaded from the remote serializer. It can be overwritten if the OVERRIDE_FC_CONFIG bit in this register is 1.

1.1.75 SER_ID Register (Address = 0x5B) [Default = 0x00]

SER_ID is shown in Table 1-78.

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Table 1-78. SER_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SER_ID	R/W	0x0	Remote Serializer ID This field is normally loaded automatically from the remote Serializer.
0	FREEZE_DEVICE_ID	R/W	0x0	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written.

1.1.76 SER_ALIAS_ID Register (Address = 0x5C) [Default = 0x00]

SER_ALIAS_ID is shown in Table 1-79.

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Table 1-79. SER_ALIAS_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	SER_ALIAS_ID	R/W	0x0	7-bit Remote Serializer Alias ID Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Target ID register. A value of 0 in this field disables access to the remote I2C Target.
0	SER_AUTO_ACK	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Serializer independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

1.1.77 TARGET_ID_0 Register (Address = 0x5D) [Default = 0x00]

TARGET_ID_0 is shown in Table 1-80.

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Table 1-80. TARGET_ID_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID0	R/W	0x0	7-bit Remote Target Device ID 0 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

1.1.78 TARGET_ID_1 Register (Address = 0x5E) [Default = 0x00]

TARGET_ID_1 is shown in Table 1-81.

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Table 1-81. TARGET_ID_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID1	R/W	0x0	7-bit Remote Target Device ID 1 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

1.1.79 TARGET_ID_2 Register (Address = 0x5F) [Default = 0x00]

TARGET_ID_2 is shown in Table 1-82.

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Table 1-82. TARGET_ID_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID2	R/W	0x0	7-bit Remote Target Device ID 2 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.

Table 1-82. TARGET_ID_2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	RESERVED	R	0x0	Reserved.

1.1.80 TARGET_ID_3 Register (Address = 0x60) [Default = 0x00]

TARGET_ID_3 is shown in Table 1-83.

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Table 1-83. TARGET_ID_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID3	R/W	0x0	7-bit Remote Target Device ID 3 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

1.1.81 TARGET_ID_4 Register (Address = 0x61) [Default = 0x00]

TARGET_ID_4 is shown in Table 1-84.

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Table 1-84. TARGET_ID_4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID4	R/W	0x0	7-bit Remote Target Device ID 4 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

1.1.82 TARGET_ID_5 Register (Address = 0x62) [Default = 0x00]

TARGET_ID_5 is shown in Table 1-85.

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Table 1-85. TARGET_ID_5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID5	R/W	0x0	7-bit Remote Target Device ID 5 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

1.1.83 TARGET_ID_6 Register (Address = 0x63) [Default = 0x00]

TARGET_ID_6 is shown in Table 1-86.

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Table 1-86. TARGET_ID_6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID6	R/W	0x0	7-bit Remote Target Device ID 6 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

1.1.84 TARGET_ID_7 Register (Address = 0x64) [Default = 0x00]

TARGET_ID_7 is shown in Table 1-87.

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Table 1-87. TARGET_ID_7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ID7	R/W	0x0	7-bit Remote Target Device ID 7 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

1.1.85 TARGET_ALIAS_0 Register (Address = 0x65) [Default = 0x00]

TARGET_ALIAS_0 is shown in Table 1-88.

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Table 1-88. TARGET_ALIAS_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID0	R/W	0x0	7-bit Remote Target Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID0 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_0	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 0 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

1.1.86 TARGET_ALIAS_1 Register (Address = 0x66) [Default = 0x00]

TARGET_ALIAS_1 is shown in Table 1-89.

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Table 1-89. TARGET_ALIAS_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID1	R/W	0x0	7-bit Remote Target Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID1 register. A value of 0 in this field disables access to the remote I2C Target.

Table 1-89. TARGET_ALIAS_1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	TARGET_AUTO_ACK_1	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 1 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

1.1.87 TARGET_ALIAS_2 Register (Address = 0x67) [Default = 0x00]

TARGET_ALIAS_2 is shown in Table 1-90.

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Table 1-90. TARGET_ALIAS_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID2	R/W	0x0	7-bit Remote Target Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID2 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_2	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 2 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

1.1.88 TARGET_ALIAS_3 Register (Address = 0x68) [Default = 0x00]

TARGET_ALIAS_3 is shown in Table 1-91.

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Table 1-91. TARGET_ALIAS_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID3	R/W	0x0	7-bit Remote Target Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID3 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_3	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 3 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

1.1.89 TARGET_ALIAS_4 Register (Address = 0x69) [Default = 0x00]

TARGET_ALIAS_4 is shown in Table 1-92.

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Table 1-92. TARGET_ALIAS_4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID4	R/W	0x0	7-bit Remote Target Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID4 register. A value of 0 in this field disables access to the remote I2C Target.

Table 1-92. TARGET_ALIAS_4 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	TARGET_AUTO_ACK_4	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 4 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

1.1.90 TARGET_ALIAS_5 Register (Address = 0x6A) [Default = 0x00]

TARGET_ALIAS_5 is shown in Table 1-93.

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Table 1-93. TARGET_ALIAS_5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID5	R/W	0x0	7-bit Remote Target Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID5 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_5	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 5 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

1.1.91 TARGET_ALIAS_6 Register (Address = 0x6B) [Default = 0x00]

TARGET_ALIAS_6 is shown in Table 1-94.

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Table 1-94. TARGET_ALIAS_6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID6	R/W	0x0	7-bit Remote Target Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID6 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_6	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 6 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

1.1.92 TARGET_ALIAS_7 Register (Address = 0x6C) [Default = 0x00]

TARGET_ALIAS_7 is shown in Table 1-95.

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Table 1-95. TARGET_ALIAS_7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	TARGET_ALIAS_ID7	R/W	0x0	7-bit Remote Target Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction will be remapped to the address specified in the Target ID7 register. A value of 0 in this field disables access to the remote I2C Target.

Table 1-95. TARGET_ALIAS_7 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	TARGET_AUTO_ACK_7	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 7 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

1.1.93 PORT_CONFIG Register (Address = 0x6D) [Default = 0x78]

PORT_CONFIG is shown in Table 1-96.

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Table 1-96. PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Default	Description
7	CSI_WAIT_FS1	R/W	0x0	CSI Wait for FrameStart packet with count 1 The CSI Receiver will wait for a Frame Start packet with count of 1 before accepting other packets This bit has no effect in RAW FPD3 input modes.
6	CSI_WAIT_FS	R/W	0x1	CSI Wait for FrameStart packet CSI2 Receiver will wait for a Frame Start packet before accepting other packets This bit has no effect in RAW FPD3 input modes.
5	CSI_FWD_CKSUM	R/W	0x1	Forward CSI packets with checksum errors 0: Do not forward errored packets 1: Forward errored packets This bit has no effect in RAW FPD3 input modes.
4	CSI_FWD_ECC	R/W	0x1	Forward CSI packets with ECC errors 0: Do not forward errored packets 1: Forward errored packets
3	CSI_FWD_LEN	R/W	0x1	In FPD3 RAW Mode, Discard first video line if FV to LV setup time is not met. 0: Forward truncated 1st video line 1: Discard truncated 1st video line In FPD3 CSI Mode, Forward CSI packets with length errors 0: Do not forward errored packets 1: Forward errored packets
2:0	RESERVED	R	0x0	Reserved

1.1.94 BC_GPIO_CTL0 Register (Address = 0x6E) [Default = 0x88]

BC_GPIO_CTL0 is shown in Table 1-97.

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Table 1-97. BC_GPIO_CTL0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	BC_GPIO1_SEL	R/W	0x8	Back channel GPIO1 Select: Determines the data sent on GPIO1 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO1_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved
3:0	BC_GPIO0_SEL	R/W	0x8	Back channel GPIO0 Select: Determines the data sent on GPIO0 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO0_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved

1.1.95 BC_GPIO_CTL1 Register (Address = 0x6F) [Default = 0x88]

BC_GPIO_CTL1 is shown in Table 1-98.

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Table 1-98. BC_GPIO_CTL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	BC_GPIO3_SEL	R/W	0x8	Back channel GPIO3 Select: Determines the data sent on GPIO3 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO3_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved
3:0	BC_GPIO2_SEL	R/W	0x8	Back channel GPIO2 Select: Determines the data sent on GPIO2 for the port back channel. 0xxx: Pin GPIOx where x is BC_GPIO2_SEL[2:0] 1000: Constant value of 0 1001: Constant value of 1 1010: FrameSync signal 1011 - 1111: Reserved

1.1.96 RAW10_ID Register (Address = 0x70) [Default = 0x2B]

RAW10_ID is shown in Table 1-99.

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Table 1-99. RAW10_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RAW10_VC	R/W	0x0	RAW10 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW10 data in DVP mode. The field value defaults to the FPD-Link receive port number
5:0	RAW10_ID	R/W	0x2B	RAW10 ID This field configures the CSI data type used in RAW10 DVP mode. The default of 0x2B matches the CSI specification.

1.1.97 RAW12_ID Register (Address = 0x71) [Default = 0x2C]

RAW12_ID is shown in Table 1-100.

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Table 1-100. RAW12_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RAW12_VC	R/W	0x0	RAW12 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW12 data in DVP mode. The field value defaults to the FPD-Link receive port number
5:0	RAW12_ID	R/W	0x2C	RAW12 ID This field configures the CSI data type used in RAW12 DVP mode. The default of 0x2C matches the CSI specification.

1.1.98 LINE_COUNT_1 Register (Address = 0x73) [Default = 0x00]

LINE_COUNT_1 is shown in Table 1-101.

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Table 1-101. LINE_COUNT_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_COUNT_HI	R	0x0	High byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value will be frozen until read.

1.1.99 LINE_COUNT_0 Register (Address = 0x74) [Default = 0x00]

LINE_COUNT_0 is shown in Table 1-102.

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Table 1-102. LINE_COUNT_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_COUNT_LO	R	0x0	Low byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value will be frozen until read. In addition, when reading the LINE_COUNT registers, the LINE_COUNT_LO will be latched upon reading LINE_COUNT_HI to ensure consistency between the two portions of the Line Count.

1.1.100 LINE_LEN_1 Register (Address = 0x75) [Default = 0x00]

LINE_LEN_1 is shown in Table 1-103.

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Table 1-103. LINE_LEN_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_LEN_HI	R	0x0	High byte of Line Length The Line Length reports the line length recorded during the most recent video frame. If line length is not stable during the frame, this register will report the length of the last line in the video frame. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value will be frozen until read.

1.1.101 LINE_LEN_0 Register (Address = 0x76) [Default = 0x00]

LINE_LEN_0 is shown in Table 1-104.

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Table 1-104. LINE_LEN_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	LINE_LEN_LO	R	0x0	Low byte of Line Length The Line Length reports the length of the most recent video line. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value will be frozen until read. In addition, when reading the LINE_LEN registers, the LINE_LEN_LO will be latched upon reading LINE_LEN_HI to ensure consistency between the two portions of the Line Length.

1.1.102 FPD3_FREQ_DET_CTL Register (Address = 0x77) [Default = 0xC5]

FPD3_FREQ_DET_CTL is shown in Table 1-105.

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Table 1-105. FPD3_FREQ_DET_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	FREQ_HYST	R/W	0x3	FPD3 Frequency Detect Hysteresis: The Frequency detect hysteresis controls reporting of the FPD3 Clock frequency stability via the FREQ_STABLE status in the RX_PORT_STS2 register. The frequency is considered stable when the frequency remains within a range of +/- the FREQ_HYST value from the previous measurement. The FREQ_HYST setting is in MHz. This field is not applicable for rates >4.16 Gbps
5:4	FREQ_STABLE_THR	R/W	0x0	FPD3 Frequency Stability Threshold: The Frequency detect circuit can be used to detect a stable clock frequency. The Stability Threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00: 40us 01: 80us 10: 320us 11: 1.28ms This field is not applicable for rates >4.16 Gbps
3:0	FREQ_LO_THR	R/W	0x5	FPD3 Frequency Low Threshold: Sets the low threshold for the Clock frequency detect circuit in MHz. If the input clock is below this threshold, the NO_FPD3_CLK status will be set to 1. This field is not applicable for rates >4.16 Gbps

1.1.103 MAILBOX_1 Register (Address = 0x78) [Default = 0x00]

MAILBOX_1 is shown in Table 1-106.

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Table 1-106. MAILBOX_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MAILBOX_0	R/W	0x0	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C controllers on opposite ends of the link.

1.1.104 MAILBOX_2 Register (Address = 0x79) [Default = 0x01]

MAILBOX_2 is shown in Table 1-107.

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Table 1-107. MAILBOX_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	MAILBOX_1	R/W	0x1	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C controllers on opposite ends of the link.

1.1.105 CSI_RX_STS Register (Address = 0x7A) [Default = 0x00]

CSI_RX_STS is shown in Table 1-108.

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Table 1-108. CSI_RX_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	RESERVED	R	0x0	Reserved

Table 1-108. CSI_RX_STS Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	LENGTH_ERR	RC	0x0	Packet Length Error detected for received CSI packet If set, this bit indicates a packet length error was detected on at least one CSI packet received from the camera. Packet length errors occur if the data length field in the packet header does not match the actual data length for the packet. 1: One or more Packet Length errors have been detected 0: No Packet Length errors have been detected This bit is cleared on read.
2	CKSUM_ERR	RC	0x0	Data Checksum Error detected for received CSI packet If set, this bit indicates a data checksum error was detected on at least one CSI packet received from the camera. Data checksum errors indicate an error was detected in the packet data portion of the CSI packet. 1: One or more Data Checksum errors have been detected 0: No Data Checksum errors have been detected This bit is cleared on read.
1	ECC2_ERR	RC	0x0	2-bit ECC Error detected for received CSI packet If set, this bit indicates a multi-bit ECC error was detected on at least one CSI packet received from the camera. Multi-bit errors are not corrected by the device. 1: One or more multi-bit ECC errors have been detected 0: No multi-bit ECC errors have been detected This bit is cleared on read.
0	ECC1_ERR	RC	0x0	1-bit ECC Error detected for received CSI packet If set, this bit indicates a single-bit ECC error was detected on at least one CSI packet received from the camera. Single-bit errors are corrected by the device. 1: One or more 1-bit ECC errors have been detected 0: No 1-bit ECC errors have been detected This bit is cleared on read.

1.1.106 CSI_ERR_COUNTER Register (Address = 0x7B) [Default = 0x00]

CSI_ERR_COUNTER is shown in Table 1-109.

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Table 1-109. CSI_ERR_COUNTER Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI_ERR_CNT	RC	0x0	CSI Error Counter Register This register counts the number of CSI packets received with errors since the last read of the counter.

1.1.107 PORT_CONFIG2 Register (Address = 0x7C) [Default = 0x20]

PORT_CONFIG2 is shown in Table 1-110.

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Table 1-110. PORT_CONFIG2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RAW10_8BIT_CTL	R/W	0x0	Raw10 8-bit mode When Raw10 Mode is enabled for the port, the input data will be processed as 8-bit data and packed accordingly for transmission over CSI. 00: Normal Raw10 Mode 01: Reserved 10: 8-bit processing using upper 8 bits 11: 8-bit processing using lower 8 bits

Table 1-110. PORT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	DISCARD_ON_PAR_ERR	R/W	0x1	Discard frames on Parity Error 0: Forward packets with parity errors 1: Truncate Frames if a parity error is detected
4	DISCARD_ON_LINE_SIZE	R/W	0x0	Discard frames on Line Size 0: Allow changes in Line Size within packets 1: Truncate Frames if a change in line size is detected
3	DISCARD_ON_FRAME_SIZE	R/W	0x0	Discard frames on change in Frame Size When enabled, a change in the number of lines in a frame will result in truncation of the packet. The device will resume forwarding video frames based on the PASS_THRESHOLD setting in the PORT_PASS_CTL register. 0: Allow changes in Frame Size 1: Truncate Frames if a change in frame size is detected
2	RESERVED	R	0x0	Reserved
1	LV_POLARITY	R/W	0x0	LineValid Polarity This register indicates the expected polarity for the LineValid indication received in Raw mode. 1: LineValid is low for the duration of the video line 0: LIneValid is high for the duration of the video line This bit is ignored if AUTO_POLARITY is set.
0	FV_POLARITY	R/W	0x0	FrameValid Polarity This register indicates the expected polarity for the FrameValid indication received in Raw mode. 1: FrameValid is low for the duration of the video frame 0: FrameValid is high for the duration of the video frame This bit is ignored if AUTO_POLARITY is set.

1.1.108 PORT_PASS_CTL Register (Address = 0x7D) [Default = 0x00]

PORT_PASS_CTL is shown in Table 1-111.

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Table 1-111. PORT_PASS_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	PASS_DISCARD_EN	R/W	0x0	Pass Discard Enable Discard packets if PASS is not indicated. 0: Ignore PASS for forwarding packets 1: Discard packets when PASS is not true
6	PASS_CLEAR_CNT	R/W	0x0	This bit controls the values read back from the LINE_COUNT_1, LINE_COUNT_0, LINE_LEN_1, and LINE_LEN_0 registers. 0: Registers read back the counter values regardless of the state of the PASS flag 1: Registers read back zero when the PASS flag is de-asserted and the count values when PASS is asserted
5	PASS_LINE_CNT	R/W	0x0	Pass Line Count Control This register controls whether the device will include line count in qualification of the Pass indication: 0: Don't check line count 1: Check line count When checking line count, Pass will be deasserted upon detection of a change in the number of video lines per frame. Pass will not be reasserted until the PASS_THRESHOLD setting is met.
4	PASS_LINE_SIZE	R/W	0x0	Pass Line Size Control This register controls whether the device will include line size in qualification of the Pass indication: 0: Don't check line size 1: Check line size When checking line size, Pass will be deasserted upon detection of a change in video line size. Pass will not be reasserted until the PASS_THRESHOLD setting is met.

Table 1-111. PORT_PASS_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	PASS_PARITY_ERR	R/W	0x0	Parity Error Mode If this bit is set to 0, the port Pass indication will be deasserted for every parity error detected on the FPD3 Receive interface. If this bit is set to a 1, the port Pass indication will be cleared on a parity error and remain clear until the PASS_THRESHOLD is met.
2	PASS_WDOG_DIS	R/W	0x0	RX Port Pass Watchdog disable When enabled, if the FPD Receiver does not detect a valid frame end condition within two video frame periods, the Pass indication will be deasserted. The watchdog timer will not have any effect if the PASS_THRESHOLD is set to 0. 0: Enable watchdog timer for RX Pass 1: Disable watchdog timer for RX Pass
1:0	PASS_THRESHOLD	R/W	0x0	Pass Threshold Register This register controls the number of valid frames before asserting the port Pass indication. If set to 0, PASS will be asserted after Receiver Lock detect. If non-zero, PASS will be asserted following reception of the programmed number of valid frames.

1.1.109 SEN_INT_RISE_CTL Register (Address = 0x7E) [Default = 0x00]

SEN_INT_RISE_CTL is shown in Table 1-112.

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Table 1-112. SEN_INT_RISE_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SEN_INT_RISE_MASK	R/W	0x0	Sensor Interrupt Rise Mask This register provides the interrupt mask for detecting rising edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in this register, a rising edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in the SEN_INT_RISE_STS register.

1.1.110 SEN_INT_FALL_CTL Register (Address = 0x7F) [Default = 0x00]

SEN_INT_FALL_CTL is shown in Table 1-113.

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Table 1-113. SEN_INT_FALL_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SEN_INT_FALL_MASK	R/W	0x0	Sensor Interrupt Fall Mask This register provides the interrupt mask for detecting falling edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in this register, a falling edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in the SEN_INT_FALL_STS register.

1.1.111 RX_CTL_1 Register (Address = 0x80) [Default = 0x00]

RX_CTL_1 is shown in Table 1-114.

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Table 1-114. RX_CTL_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RX_CLK_RST	R/W	0x0	RX clock reset

Table 1-114. RX_CTL_1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	RESERVED	R/W	0x0	Reserved
2	RX_CLK_1_OV	R/W	0x0	RX clock 1 override
1	RESERVED	R/W	0x0	Reserved
0	RX_CLK_2_OV	R/W	0x0	RX clock 2 override

1.1.112 GPIO9_PIN_CTL Register (Address = 0x89) [Default = 0x00]

GPIO9_PIN_CTL is shown in Table 1-115.

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Table 1-115. GPIO9_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO9_OUT_SEL	R/W	0x0	GPIO9 Output Select Determines the output data for the selected source. If GPIO9_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO9_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO9_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk If GPIO9_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved
4:2	GPIO9_OUT_SRC	R/W	0x0	GPIO9 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO9_OUT_VAL	R/W	0x0	GPIO9 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO9_OUT_EN	R/W	0x0	GPIO9 Output Enable 0: Disabled 1: Enabled

1.1.113 GPIO10_PIN_CTL Register (Address = 0x8A) [Default = 0x00]

GPIO10_PIN_CTL is shown in Table 1-116.

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Table 1-116. GPIO10_PIN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	GPIO10_OUT_SEL	R/W	0x0	GPIO10 Output Select Determines the output data for the selected source. If GPIO10_OUT_SRC is set to 0xx (one of the RX Ports), the following selections apply: 000: Received GPIO0 001: Received GPIO1 010: Received GPIO2 011: Received GPIO3 100: RX Port Lock indication 101: RX Port Pass indication 110: Frame Valid signal 111: Line Valid signal If GPIO10_OUT_SRC is set to 100 (Device Status), the following selections apply: 000: Value in GPIO10_OUT_VAL 001: Logical OR of Lock indication from enabled RX ports 010: Logical AND of Lock indication from enabled RX ports 011: Logical AND of Pass indication from enabled RX ports 100: FrameSync signal 101: FPD Interrupt (Active High) 110: FPD Interrupt (Active Low) 111: External Refclk If GPIO10_OUT_SRC is set to 11x (one of the CSI Transmit ports), the following selections apply: 000: Pass (AND of selected RX port status) 001: Pass (OR of selected RX port status) 010: Frame Valid (sending video frame) 011: Line Valid (sending video line) 100: Synchronized - multi-port data is synchronized 101: CSI TX Port Interrupt (Active High) 110: CSI TX Port Interrupt (Active Low) 111: Reserved
4:2	GPIO10_OUT_SRC	R/W	0x0	GPIO10 Output Source Select Selects output source for GPIO0 data: 000: RX Port 0 001: RX Port 1 010: RX Port 2 011: RX Port 3 100: Device Status 101: Reserved 110: CSI TX Port 0 111: CSI TX Port 1
1	GPIO10_OUT_VAL	R/W	0x0	GPIO10 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value.
0	GPIO10_OUT_EN	R/W	0x0	GPIO10 Output Enable 0: Disabled 1: Enabled

1.1.114 GPIO_INPUT_CTL_2 Register (Address = 0x8B) [Default = 0x04]

GPIO_INPUT_CTL_2 is shown in Table 1-117.

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Table 1-117. GPIO_INPUT_CTL_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-117. GPIO_INPUT_CTL_2 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	INTB_PAD_EN	R/W	0x1	1: Enables INTB in Open Drain for GPIO3 pin 0: GPIO3 pin is controlled by GPIO3_PIN_CTL
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

1.1.115 REFCLK_DET_INT_CTL Register (Address = 0x8C) [Default = 0x00]

REFCLK_DET_INT_CTL is shown in Table 1-118.

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Table 1-118. REFCLK_DET_INT_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:3	RESERVED	R	0x0	
2	REFCLK_NOT_IMMEDIATE	R/W	0x0	REFCLK not detected immediate interrupt When this bit is set to a 1, an interrupt may be generated when a valid REFCLK is NOT detected as indicated by the REFCLK_VALID register status equal to 0. This control allows constant interrupt generation as long as the event is true. As long as the REFCLK_VALID=0, this will cause an interrupt. While REFCLK_VALID=0, the only way to clear this interrupt condition is to clear this bit. To generate REFCLK interrupts, the IE_REFCLK_DET register control must be set in the LOCAL_DEV_ICR register
1	REFCLK_LOST_INT	R/W	0x0	REFCLK lost interrupt When this bit is set to a 1, an interrupt may be generated when a valid REFCLK is NOT detected as indicated by the REFCLK_VALID register status changing from 1 to 0. This enable allows detecting the loss of REFCLK_VALID rather than the steady-state condition. To generate REFCLK interrupts, the IE_REFCLK_DET register control must be set in the LOCAL_DEV_ICR register
0	REFCLK_DET_INT	R/W	0x0	REFCLK detect interrupt When this bit is set to a 1, an interrupt may be generated when a valid REFCLK is detected as indicated by the REFCLK_VALID register status. To generate REFCLK interrupts, the IE_REFCLK_DET register control must be set in the LOCAL_DEV_ICR register

1.1.116 CSI0_FRAME_COUNT_HI Register (Address = 0x90) [Default = 0x00]

CSI0_FRAME_COUNT_HI is shown in Table 1-119.

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Table 1-119. CSI0_FRAME_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI0_FRAME_COUNT_HI	RC	0x0	CSI Port 0, Frame Counter MSBs This register reads the number of CSI video frames transmitted from the mapped FPD ports to CSI0. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI0_FRAME_COUNT. The LSBs of the counter are sampled into the CSI0_FRAME_COUNT_LO register and the counter is cleared.

1.1.117 CSI0_FRAME_COUNT_LO Register (Address = 0x91) [Default = 0x00]

CSI0_FRAME_COUNT_LO is shown in Table 1-120.

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Table 1-120. CSI0_FRAME_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI0_FRAME_COUNT_LO	R	0x0	CSI Port 0, Frame Counter LSBs This register reads the number of CSI video frames transmitted from the mapped FPD ports to CSI0. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI0_FRAME_COUNT. The CSI0_FRAME_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

1.1.118 CSI0_FRAME_ERR_COUNT_HI Register (Address = 0x92) [Default = 0x00]

CSI0_FRAME_ERR_COUNT_HI is shown in Table 1-121.

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Table 1-121. CSI0_FRAME_ERR_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI0_FRAME_ERR_COUNT_HI	RC	0x0	CSI Port 0, Frame Counter with Errors MSBs This register counts the number of CSI video frames transmitted from the mapped FPD ports to CSI0 with errors. When read, this register returns the value of bits [15:8] of the 16-bit counterCSI0_FRAME_ERR_COUNT. The LSBs of the counter are sampled into the CSI0_FRAME_ERR_COUNT_LO register and the counter is cleared.

1.1.119 CSI0_FRAME_ERR_COUNT_LO Register (Address = 0x93) [Default = 0x00]

CSI0_FRAME_ERR_COUNT_LO is shown in Table 1-122.

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Table 1-122. CSI0_FRAME_ERR_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI0_FRAME_ERR_COUNT_LO	R	0x0	CSI Port 0, Frame Counter with Errors LSBs This register counts the number of CSI video frames transmitted from the mapped FPD ports to CSI0 with errors. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI0_FRAME_ERR_COUNT. The CSI0_FRAME_ERR_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

1.1.120 CSI0_LINE_COUNT_HI Register (Address = 0x94) [Default = 0x00]

CSI0_LINE_COUNT_HI is shown in Table 1-123.

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Table 1-123. CSI0_LINE_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI0_LINE_COUNT_HI	RC	0x0	CSI Port 0, Line Counter MSBs This register reads the number of CSI video lines transmitted from the mapped FPD ports to CSI0. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI0_LINE_COUNT. The LSBs of the counter are sampled into the CSI0_LINE_COUNT_LO register and the counter is cleared.

1.1.121 CSI0_LINE_COUNT_LO Register (Address = 0x95) [Default = 0x00]

CSI0_LINE_COUNT_LO is shown in Table 1-124.

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Table 1-124. CSI0_LINE_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI0_LINE_COUNT_LO	R	0x0	CSI Port 0, Line Counter LSBs This register reads the number of CSI video lines transmitted from the mapped FPD ports to CSI0. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI0_LINE_COUNT. The CSI0_LINE_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

1.1.122 CSI0_LINE_ERR_COUNT_HI Register (Address = 0x96) [Default = 0x00]

CSI0_LINE_ERR_COUNT_HI is shown in Table 1-125.

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Table 1-125. CSI0_LINE_ERR_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI0_LINE_ERR_COUNT_HI	RC	0x0	CSI Port 0, Line Counter with Errors MSBs This register counts the number of CSI video lines transmitted from the mapped FPD ports to CSI0 with errors. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI0_LINE_ERR_COUNT. The LSBs of the counter are sampled into the CSI0_LINE_ERR_COUNT_LO register and the counter is cleared.

1.1.123 CSI0_LINE_ERR_COUNT_LO Register (Address = 0x97) [Default = 0x00]

CSI0_LINE_ERR_COUNT_LO is shown in Table 1-126.

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Table 1-126. CSI0_LINE_ERR_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI0_LINE_ERR_COUNT_LO	R	0x0	CSI Port 0, Line Counter with Errors LSBs This register counts the number of CSI video lines transmitted from the mapped FPD ports to CSI0 with errors. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI0_LINE_ERR_COUNT. The CSI0_LINE_ERR_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

1.1.124 CSI1_FRAME_COUNT_HI Register (Address = 0x98) [Default = 0x00]

CSI1_FRAME_COUNT_HI is shown in Table 1-127.

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Table 1-127. CSI1_FRAME_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI1_FRAME_COUNT_HI	RC	0x0	CSI Port 1, Frame Counter MSBs This register reads the number of CSI video frames transmitted from the mapped FPD ports to CSI1. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI1_FRAME_COUNT. The LSBs of the counter are sampled into the CSI1_FRAME_COUNT_LO register and the counter is cleared.

1.1.125 CSI1_FRAME_COUNT_LO Register (Address = 0x99) [Default = 0x00]

CSI1_FRAME_COUNT_LO is shown in Table 1-128.

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Table 1-128. CSI1_FRAME_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI1_FRAME_COUNT_LO	R	0x0	CSI Port 1, Frame Counter LSBs This register reads the number of CSI video frames transmitted from the mapped FPD ports to CSI1. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI1_FRAME_COUNT. The CSI1_FRAME_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

1.1.126 CSI1_FRAME_ERR_COUNT_HI Register (Address = 0x9A) [Default = 0x00]

CSI1_FRAME_ERR_COUNT_HI is shown in Table 1-129.

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Table 1-129. CSI1_FRAME_ERR_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI1_FRAME_ERR_COUNT_HI	RC	0x0	CSI Port 1, Frame Counter with Errors MSBs This register counts the number of CSI video frames transmitted from the mapped FPD ports to CSI1 with errors. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI1_FRAME_ERR_COUNT. The LSBs of the counter are sampled into the CSI1_FRAME_ERR_COUNT_LO register and the counter is cleared.

1.1.127 CSI1_FRAME_ERR_COUNT_LO Register (Address = 0x9B) [Default = 0x00]

CSI1_FRAME_ERR_COUNT_LO is shown in Table 1-130.

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Table 1-130. CSI1_FRAME_ERR_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI1_FRAME_ERR_COUNT_LO	R	0x0	CSI Port 1, Frame Counter with Errors LSBs This register counts the number of CSI video frames transmitted from the mapped FPD ports to CSI1 with errors. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI1_FRAME_ERR_COUNT. The CSI1_FRAME_ERR_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

1.1.128 CSI1_LINE_COUNT_HI Register (Address = 0x9C) [Default = 0x00]

CSI1_LINE_COUNT_HI is shown in Table 1-131.

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Table 1-131. CSI1_LINE_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI1_LINE_COUNT_HI	RC	0x0	CSI Port 1, Line Counter MSBs This register reads the number of CSI video lines transmitted from the mapped FPD ports to CSI1. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI1_LINE_COUNT. The LSBs of the counter are sampled into the CSI1_LINE_COUNT_LO register and the counter is cleared.

1.1.129 CSI1_LINE_COUNT_LO Register (Address = 0x9D) [Default = 0x00]

CSI1_LINE_COUNT_LO is shown in Table 1-132.

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Table 1-132. CSI1_LINE_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI1_LINE_COUNT_LO	R	0x0	CSI Port 1, Line Counter LSBs This register reads the number of CSI video lines transmitted from the mapped FPD ports to CSI1. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI1_LINE_COUNT. The CSI1_LINE_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

1.1.130 CSI1_LINE_ERR_COUNT_HI Register (Address = 0x9E) [Default = 0x00]

CSI1_LINE_ERR_COUNT_HI is shown in Table 1-133.

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Table 1-133. CSI1_LINE_ERR_COUNT_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI1_LINE_ERR_COUNT_HI	RC	0x0	CSI Port 1, Line Counter with Errors MSBs This register counts the number of CSI video lines transmitted from the mapped FPD ports to CSI1 with errors. When read, this register returns the value of bits [15:8] of the 16-bit counter CSI1_LINE_ERR_COUNT. The LSBs of the counter are sampled into the CSI1_LINE_ERR_COUNT_LO register and the counter is cleared.

1.1.131 CSI1_LINE_ERR_COUNT_LO Register (Address = 0x9F) [Default = 0x00]

CSI1_LINE_ERR_COUNT_LO is shown in Table 1-134.

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Table 1-134. CSI1_LINE_ERR_COUNT_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI1_LINE_ERR_COUNT_LO	R	0x0	CSI Port 1, Line Counter with Errors LSBs This register counts the number of CSI video lines transmitted from the mapped FPD ports to CSI1 with errors. When read, this register returns the value of bits [7:0] of the 16-bit counter CSI1_LINE_ERR_COUNT. The CSI1_LINE_ERR_COUNT_HI register must be read first to snapshot the LSBs of the counter into this register.

1.1.132 VC_ID_MAP_0 Register (Address = 0xA0) [Default = 0x10]

VC_ID_MAP_0 is shown in Table 1-135.

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Table 1-135. VC_ID_MAP_0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI_VC_MAP_0	R/W	0x10	If, the input VC_ID (from 971 and 953/935/951) is 0, it can be remapped to CSI_VC_MAP_0[3:0] If, the input VC_ID (from 971) is 1, it can be remapped to CSI_VC_MAP_0[7:4] Used for CSI-2 mode only. For DVP mode (933/913A) see registers 0x70-0x71

1.1.133 VC_ID_MAP_1 Register (Address = 0xA1) [Default = 0x32]

VC_ID_MAP_1 is shown in Table 1-136.

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Table 1-136. VC_ID_MAP_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI_VC_MAP_1	R/W	0x32	If, the input VC_ID (from 971) is 2, it can be remapped to CSI_VC_MAP_1[3:0] If, the input VC_ID (from 971) is 3, it can be remapped to CSI_VC_MAP_1[7:4] Used for CSI-2 mode only. For DVP mode (933/913A) see registers 0x70-0x71

1.1.134 VC_ID_MAP_2 Register (Address = 0xA2) [Default = 0x54]

VC_ID_MAP_2 is shown in Table 1-137.

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Table 1-137. VC_ID_MAP_2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI_VC_MAP_2	R/W	0x54	If, the input VC_ID (from 971) is 4, it can be remapped to CSI_VC_MAP_2[3:0] If, the input VC_ID from 971 is 5 (or from 953/935/951 is 1), it can be remapped to CSI_VC_MAP_2[7:4] Used for CSI-2 mode only. For DVP mode (933/913A) see registers 0x70-0x71

1.1.135 VC_ID_MAP_3 Register (Address = 0xA3) [Default = 0x76]

VC_ID_MAP_3 is shown in Table 1-138.

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Table 1-138. VC_ID_MAP_3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI_VC_MAP_3	R/W	0x76	If, the input VC_ID (from 971) is 6, it can be remapped to CSI_VC_MAP_3[3:0] If, the input VC_ID (from 971) is 7, it can be remapped to CSI_VC_MAP_3[7:4] Used for CSI-2 mode only. For DVP mode (933/913A) see registers 0x70-0x71

1.1.136 VC_ID_MAP_4 Register (Address = 0xA4) [Default = 0x98]

VC_ID_MAP_4 is shown in Table 1-139.

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Table 1-139. VC_ID_MAP_4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI_VC_MAP_4	R/W	0x98	If, the input VC_ID (from 971) is 8, it can be remapped to CSI_VC_MAP_4[3:0] If, the input VC_ID (from 971) is 9, it can be remapped to CSI_VC_MAP_4[7:4] Used for CSI-2 mode only. For DVP mode (933/913A) see registers 0x70-0x71

1.1.137 VC_ID_MAP_5 Register (Address = 0xA5) [Default = 0xBA]

VC_ID_MAP_5 is shown in Table 1-140.

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Table 1-140. VC_ID_MAP_5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI_VC_MAP_5	R/W	0xBA	If, the input VC_ID from 971 is 10 (or from 953/935/951 is 2), it can be remapped to CSI_VC_MAP_5[3:0] If, the input VC_ID (from 971) is 11, it can be remapped to CSI_VC_MAP_5[7:4] Used for CSI-2 mode only. For DVP mode (933/913A) see registers 0x70-0x71

1.1.138 VC_ID_MAP_6 Register (Address = 0xA6) [Default = 0xDC]

VC_ID_MAP_6 is shown in Table 1-141.

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Table 1-141. VC_ID_MAP_6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI_VC_MAP_6	WR	0xDC	If, the input VC_ID (from 971) is 12, it can be remapped to CSI_VC_MAP_6[3:0] If, the input VC_ID (from 971) is 13, it can be remapped to CSI_VC_MAP_6[7:4] Used for CSI-2 mode only. For DVP mode (933/913A) see registers 0x70-0x71

1.1.139 VC_ID_MAP_7 Register (Address = 0xA7) [Default = 0xFE]

VC_ID_MAP_7 is shown in Table 1-142.

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Table 1-142. VC_ID_MAP_7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	CSI_VC_MAP_7	R/W	0xFE	If, the input VC_ID (from 971) is 14, it can be remapped to CSI_VC_MAP_7[3:0] If, the input VC_ID from 971 is 15 (or from 953/935/951 is 3), it can be remapped to CSI_VC_MAP_7[7:4] Used for CSI-2 mode only. For DVP mode (933/913A) see registers 0x70-0x71

1.1.140 IND_ACC_CTL Register (Address = 0xB0) [Default = 0x00]

IND_ACC_CTL is shown in Table 1-143.

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Table 1-143. IND_ACC_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:2	IA_SEL	R/W	0x0	Indirect Access Register Select: Selects target for register access 0000: Pattern Generator Registers 0001: FPD RX Port 0 Registers 0010: FPD RX Port 1 Registers 0011: FPD RX Port 2 Registers 0100: FPD RX Port 3 Registers 0110: Simultaneous write to FPD RX Port 0-3 registers 0111: CSI-2 Registers
1	IA_AUTO_INC	R/W	0x0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1
0	IA_READ	R/W	0x0	Indirect Access Read: Setting this allows generation of a read strobe to the selected register block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the IND_ACC_DATA register. This function is only required for blocks that need to pre-fetch register data. Note that this bit needs to be set (to 1) if we need to do COR on an indirect page

1.1.141 IND_ACC_ADDR Register (Address = 0xB1) [Default = 0x00]

IND_ACC_ADDR is shown in Table 1-144.

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Table 1-144. IND_ACC_ADDR Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IA_ADDR	R/W	0x0	Indirect Access Register Offset: This register contains the 8-bit register offset for the indirect access.

1.1.142 IND_ACC_DATA Register (Address = 0xB2) [Default = 0x00]

IND_ACC_DATA is shown in Table 1-145.

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Table 1-145. IND_ACC_DATA Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	IA_DATA	R/W	0x0	Indirect Access Data: Writing this register will cause an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register will return the value of the selected block register

1.1.143 BIST_CTL Register (Address = 0xB3) [Default = 0x08]

BIST_CTL is shown in Table 1-146.

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Table 1-146. BIST_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	BIST_OUT_MODE	R/W	0x0	BIST Output Mode 00: No toggling 01: Alternating 1/0 toggling 1x: Toggle based on BIST data
5:4	RESERVED	R/W	0x0	Reserved
3	BIST_PIN_CONFIG	R/W	0x1	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through bits 2:0 in this register
2:1	BIST_CLOCK_SOURCE	R/W	0x0	BIST Clock Source This register field selects the BIST Clock Source at the Serializer. These register bits are automatically written to the CLOCK SOURCE bits (register offset 0x14) in the Serializer after BIST is enabled. See the appropriate Serializer register descriptions for details. Note: When connected to a DS90UB913A, a setting of 0x3 may result in a clock frequency that is too slow for proper recovery.
0	BIST_EN	R/W	0x0	BIST Control 1: Enabled 0: Disabled

1.1.144 MODE_IDX_STS Register (Address = 0xB8) [Default = 0xF8]

MODE_IDX_STS is shown in Table 1-147.

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Table 1-147. MODE_IDX_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	IDX_DONE	R	0x1	IDX Done: If set, indicates the IDX decode has completed and latched into the IDX status bits.
6:4	IDX	R	0x7	IDX Decode 3-bit decode from IDX pin
3	MODE_DONE	R	0x1	MODE Done: If set, indicates the MODE decode has completed and latched into the MODE status bits.
2:0	MODE	R	0x0	MODE Decode 3-bit decode from MODE pin

1.1.145 LINK_ERROR_COUNT Register (Address = 0xB9) [Default = 0x13]

LINK_ERROR_COUNT is shown in Table 1-148.

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Table 1-148. LINK_ERROR_COUNT Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	LINK_ERR_COUNT_EN	R/W	0x1	Enable serial link data integrity error count 1: Enable error count 0: DISABLE

Table 1-148. LINK_ERROR_COUNT Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3:0	LINK_ERR_THRESH	R/W	0x3	Link error count threshold. The Link Error Counter monitors the forward channel link and determines when link will be dropped. The link error counter is pixel clock based. Parity errors and FPD-Link encoding errors are monitored. If the error counter is enabled, the deserializer will lose lock once the error counter reaches the LINK_ERR_THRESH value. If the link error counter is disabled, the deserilizer will lose lock after one error. The control bits in DIGITAL_DEBUG_2 register can be used to disable error conditions individually.

1.1.146 FV_MIN_TIME Register (Address = 0xBC) [Default = 0x80]

FV_MIN_TIME is shown in Table 1-149.

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Table 1-149. FV_MIN_TIME Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FRAME_VALID_MIN	R/W	0x80	Frame Valid Minimum Time This register controls the minimum time the FrameValid (FV) must be active before the Raw mode FPD3 receiver generates a FrameStart packet. Duration is in FPD3 clock periods.

1.1.147 GPIO_PD_CTL Register (Address = 0xBE) [Default = 0x00]

GPIO_PD_CTL is shown in Table 1-150.

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Table 1-150. GPIO_PD_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO7_PD_DIS	R/W	0x0	GPI7 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
6	GPIO6_PD_DIS	R/W	0x0	GPIO6 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
5	GPIO5_PD_DIS	R/W	0x0	GPIO5 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
4	GPIO4_PD_DIS	R/W	0x0	GPIO4 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
3	RESERVED	R/W	0x0	

Table 1-150. GPIO_PD_CTL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2	GPIO2_PD_DIS	R/W	0x0	GPIO2 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
1	GPIO1_PD_DIS	R/W	0x0	GPIO1 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor
0	GPIO0_PD_DIS	R/W	0x0	GPIO0 Pull-down Resistor Disable: The GPIO pins by default include a pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1: Disable GPIO pull-down resistor 0: Enable GPIO pull-down resistor

1.1.148 FPD_RATE_CFG Register (Address = 0xC2) [Default = 0x00]

FPD_RATE_CFG is shown in Table 1-151.

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Table 1-151. FPD_RATE_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	FPD_RATE_CFG_CH3	R/W	0x0	FPD Rate Configuration Channel3: 00: 7.55G mode 01: 3.775G mode 10: 1.8875G mode 11: RESERVED
5:4	FPD_RATE_CFG_CH2	R/W	0x0	FPD Rate Configuration Channel2: 00: 7.55G mode 01: 3.775G mode 10: 1.8875G mode 11: RESERVED
3:2	FPD_RATE_CFG_CH1	R/W	0x0	FPD Rate Configuration Channel1: 00: 7.55G mode 01: 3.775G mode 10: 1.8875G mode 11: RESERVED
1:0	FPD_RATE_CFG_CH0	R/W	0x0	FPD Rate Configuration Channel0: 00: 7.55G mode 01: 3.775G mode 10: 1.8875G mode 11: RESERVED

1.1.149 CSI_PORT2_FIFO_CTRL Register (Address = 0xC7) [Default = 0x00]

CSI_PORT2_FIFO_CTRL is shown in Table 1-152.

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Table 1-152. CSI_PORT2_FIFO_CTRL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-152. CSI_PORT2_FIFO_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	RESERVED	R/W	0x0	Reserved
4	CSI_PORT2_EN	R/W	0x0	CSI Transmit Port2 Enable Setting this bit enables the CSI-2 Transmit Port 2 for replication of either CSI Transmit Port 0 or 1 data. Selection of which CSI Transmit port is replicated is determined by the REPLICATE_CSI2_SEL register control. This bit must be set prior to enabling the selected CSI Transmit Port.
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	CSI_FIFO_UNDERRUN		0x0	CSI Port 2 FIFO Underrun Flag If this bit is set, an underrun has been detected on the CSI Port 2 FIFO. This register will be cleared on read.
0	CSI_FIFO_OVERFLOW		0x0	CSI Port 2 FIFO Overflow Flag If this bit is set, an overflow has been detected on the CSI Port 2 FIFO. This register will be cleared on read.

1.1.150 CSI_PLL_DIV Register (Address = 0xC9) [Default = 0x32]

CSI_PLL_DIV is shown in Table 1-153.

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Table 1-153. CSI_PLL_DIV Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R	0x0	
5:0	CSI_TX_SPEED2	R/W	0x32	CSI_TX_SPEED2 Strap 2.5G: 6'h32 800M: 6'h20 This register selects the operating rate and CSI timing parameters for the CSI Transmitter. In addition to setting this field, the CSIPLL_REG_1 indirect register (0x92) on the CSI-2 Page7 must also be programmed for the correct selection. 2.5G: 6'h32 1.6G: 6'h20 1.5G: 6'h1E 1.2G: 6'h30 800M: 6'h20 400M: 6'h20 At power-up, this field is set based on the MODE pin strap value.

1.1.151 LOCAL_DEV_ICR Register (Address = 0xCA) [Default = 0x00]

LOCAL_DEV_ICR is shown in Table 1-154.

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Table 1-154. LOCAL_DEV_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	IE_CSI_PORT2_FIFO	R/W	0x0	Interrupt on CSI Port2 FIFO Status When enabled, an interrupt will be generated on detection of an error on the CSI Port2 FIFO. CSI2 FIFO status is reported in the CSI_PORT2_FIFO_CTRL register.
4	RESERVED	R/W	0x0	RESERVED

Table 1-154. LOCAL_DEV_ICR Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	IE_REFCLK_DET	R/W	0x0	Interrupt on change in REFCLK Detect status When enabled, an interrupt will be generated on detection of a change in sensor the Reference clock status based on configuration in the REFCLK_DET_INT_CTL register. Reference clock status is reported in the REFCLK_VALID bit in the DEVICE_STS Register
2	RESERVED	R/W	0x0	RESERVED
1	RESERVED	R/W	0x0	RESERVED
0	RESERVED	R/W	0x0	RESERVED

1.1.152 LOCAL_DEV_ISR Register (Address = 0xCB) [Default = 0x00]

LOCAL_DEV_ISR is shown in Table 1-155.

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Table 1-155. LOCAL_DEV_ISR Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5	IS_CSI_PORT2_FIFO		0x0	Interrupt on CSI PORT2 FIFO Status An error on the CSI Port2 FIFO has been detected. This interrupt indicates there might be errors on the datapath when replicating data to the CSI Port2 interface. CSI2 FIFO status is reported in the CSI_PORT2_FIFO_CTRL register. This interrupt condition will be cleared by reading the CSI_PORT2_FIFO_CTRL register.
4	RESERVED	R	0x0	RESERVED
3	IS_REFCLK_DET		0x0	Interrupt on change in REFCLK Detect status A change in sensor the Reference clock status has been detected. Reference clock status is reported in the REFCLK_VALID bit in the DEVICE_STS Register. This interrupt condition will be cleared by reading this register.
2	RESERVED	R	0x0	RESERVED
1	RESERVED	R	0x0	RESERVED
0	RESERVED	R	0x0	RESERVED

1.1.153 PORT_DEBUG Register (Address = 0xD0) [Default = 0x00]

PORT_DEBUG is shown in Table 1-156.

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Table 1-156. PORT_DEBUG Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	RESERVED
5	SER_BIST_ACT	R	0x0	Serializer BIST active This register indicates the Serializer is in BIST mode. If the Deserializer is not in BIST mode, this could indicate an error condition.
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	FORCE_BC_ERRORS	R/W	0x0	This bit introduces continuous errors into Back channel frame.
0	FORCE_1_BC_ERROR	RH/W1S	0x0	This bit introduces one error into Back channel frame. Self clearing bit.

1.1.154 PORT_ICR_HI Register (Address = 0xD8) [Default = 0x00]

PORT_ICR_HI is shown in Table 1-157.

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Table 1-157. PORT_ICR_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	IE_FC_GPIO	R/W	0x0	Interrupt on FC GPIO signals When enabled, an interrupt will be generated on detection of a change in one of the Forward Channel GPIO signals. Forward Channel GPIO status is reported in the FC_GPIO_STS register.
3	IE_FC_SEN_STS	R/W	0x0	Interrupt on change in Sensor Status When enabled, an interrupt will be generated on detection of a change in sensor status as reported in the SEN_INT_RISE_STS and SEN_INT_FALL_STS registers.
2	IE_FPD_ENC_ERR	R/W	0x0	Interrupt on FPD-Link Receiver Encoding Error When enabled, an interrupt will be generated on detection of an encoding error on the FPD-Link interface for the receive port as reported in the FPD_ENC_ERROR bit in the RX_PORT_STS2 register
1	IE_BCC_SEQ_ERR/ IE_BCC_ERROR	R/W	0x0	The function of this bit depends on the setting of the BCC_EN_ENH_ERR control in the BCC_ERR_CTL register. If BCC_EN_ENH_ERR is 0 (disabled), this register is defined as follows: Interrupt on BCC SEQ Sequence Error When enabled, an interrupt will be generated if a Sequence Error is detected for the Bidirectional Control Channel forward channel receiver as reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. If BCC_EN_ENH_ERR is 1 (enabled), this register is defined as follows: Interrupt on BCC Error When enabled, an interrupt will be generated if a BCC Error is detected for the Bidirectional Control Channel receiver as reported in the BCC_ERROR bit in the RX_PORT_STS1 register.
0	IE_BCC_CRC_ERR	R/W	0x0	Interrupt on BCC CRC error detect When enabled, an interrupt will be generated if a CRC error is detected on a Bidirectional Control Channel frame received over the FPD-Link forward channel as reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register.

1.1.155 PORT_ICR_LO Register (Address = 0xD9) [Default = 0x00]

PORT_ICR_LO is shown in Table 1-158.

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Table 1-158. PORT_ICR_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	RESERVED
6	IE_LINE_LEN_CHG	R/W	0x0	Interrupt on Video Line length When enabled, an interrupt will be generated if the length of the video line changes. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register.
5	IE_LINE_CNT_CHG	R/W	0x0	Interrupt on Video Line count When enabled, an interrupt will be generated if the number of video lines per frame changes. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register.
4	IE_BUFFER_ERR	R/W	0x0	Interrupt on Receiver Buffer Error When enabled, an interrupt will be generated if the Receive Buffer overflow is detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register.

Table 1-158. PORT_ICR_LO Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3	IE_CSI_RX_ERR	R/W	0x0	Interrupt on CSI Receiver Error When enabled, an interrupt will be generated on detection of an error by the CSI Receiver. CSI Receiver errors are reported in the CSI_RX_STS register (address 0x7A).
2	IE_FPD_PAR_ERR	R/W	0x0	Interrupt on FPD-Link Receiver Parity Error When enabled, an interrupt will be generated on detection of parity errors on the FPD-Link interface for the receive port. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register.
1	IE_PORT_PASS	R/W	0x0	Interrupt on change in Port PASS status When enabled, an interrupt will be generated on a change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register.
0	IE_LOCK_STS	R/W	0x0	Interrupt on change in Lock Status When enabled, an interrupt will be generated on a change in lock status. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register.

1.1.156 PORT_ISR_HI Register (Address = 0xDA) [Default = 0x00]

PORT_ISR_HI is shown in Table 1-159.

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Table 1-159. PORT_ISR_HI Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4	IS_FC_GPIO	R	0x0	FC GPIO Interrupt Status A change in forward channel GPIO signal has been detected. Forward Channel GPIO status is reported in the FC_GPIO_STS register. This interrupt condition will be cleared by reading the FC_GPIO_STS register.
3	IS_FC_SEN_STS	R	0x0	Interrupt on change in Sensor Status A change in Sensor Status has been detected. Sensor Status is reported in the SENSOR_STS_X registers. This interrupt condition will be cleared by reading the SEN_INT_RISE_STS and SEN_INT_FALL_STS registers.
2	IS_FPD_ENC_ERR	R	0x0	FPD-Link Receiver Encode Error Interrupt Status An encoding error on the FPD-Link interface for the receive port has been detected. Status is reported in the FPD_ENC_ERROR bit in the RX_PORT_STS2 register. This interrupt condition will be cleared by reading the RX_PORT_STS2 register.

Table 1-159. PORT_ISR_HI Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	IS_BCC_SEQ_ERR/ IS_BCC_ERROR	R	0x0	The function of this bit depends on the setting of the BCC_EN_ENH_ERR control in the BCC_ERR_CTL register. If BCC_EN_ENH_ERR is 0 (disabled), this register is defined as follows: BCC CRC Sequence Error Interrupt Status A Sequence Error has been detected for the Bidirectional Control Channel forward channel receiver. Status is reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. This interrupt condition will be cleared by reading the RX_PORT_STS1 register. If BCC_EN_ENH_ERR is 1 (enabled), this register is defined as follows: BCC Error Interrupt Status An error has been detected for the Bidirectional Control Channel forward channel receiver. Status is reported in the BCC_ERROR bit in the RX_PORT_STS1 register with detailed reporting in the BCC_STATUS register. This interrupt condition will be cleared by reading the BCC_STATUS register.
0	IS_BCC_CRC_ERR	R	0x0	BCC CRC error detect Interrupt Status A CRC error has been detected on a Bidirectional Control Channel frame received over the FPD-Link forward channel. Status is reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register. This interrupt condition will be cleared by reading the RX_PORT_STS1 register.

1.1.157 PORT_ISR_LO Register (Address = 0xDB) [Default = 0x00]

PORT_ISR_LO is shown in Table 1-160.

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Table 1-160. PORT_ISR_LO Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	RESERVED
6	IS_LINE_LEN_CHG	R	0x0	Video Line Length Interrupt Status A change in video line length has been detected. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register. This interrupt condition will be cleared by reading the RX_PORT_STS2 register.
5	IS_LINE_CNT_CHG	R	0x0	Video Line Count Interrupt Status A change in number of video lines per frame has been detected. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register. This interrupt condition will be cleared by reading the RX_PORT_STS2 register.
4	IS_BUFFER_ERR	R	0x0	Receiver Buffer Error Interrupt Status A Receive Buffer overflow has been detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register. This interrupt condition will be cleared by reading the RX_PORT_STS2 register.
3	IS_CSI_RX_ERR	R	0x0	CSI Receiver Error Interrupt Status The CSI Receiver has detected an error. CSI Receiver errors are reported in the CSI_RX_STS register (address 0x7A). This interrupt condition will be cleared by reading the CSI_RX_STS register.
2	IS_FPD_PAR_ERR	R	0x0	FPD-Link Receiver Parity Error Interrupt Status A parity error on the FPD-Link interface for the receive port has been detected. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register. This interrupt condition will be cleared by reading the RX_PORT_STS1 register.

Table 1-160. PORT_ISR_LO Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
1	IS_PORT_PASS	R	0x0	Port Valid Interrupt Status A change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register. This interrupt condition will be cleared by reading the RX_PORT_STS1 register.
0	IS_LOCK_STS	R	0x0	Lock Interrupt Status A change in lock status has been detected. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register. This interrupt condition will be cleared by reading the RX_PORT_STS1 register.

1.1.158 FC_GPIO_STS Register (Address = 0xDC) [Default = 0x00]

FC_GPIO_STS is shown in Table 1-161.

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Table 1-161. FC_GPIO_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO3_INT_STS	RC	0x0	GPIO3 Interrupt Status This bit indicates an interrupt condition has been met for GPIO3. This bit is cleared on read.
6	GPIO2_INT_STS	RC	0x0	GPIO2 Interrupt Status This bit indicates an interrupt condition has been met for GPIO2. This bit is cleared on read.
5	GPIO1_INT_STS	RC	0x0	GPIO1 Interrupt Status This bit indicates an interrupt condition has been met for GPIO1. This bit is cleared on read.
4	GPIO0_INT_STS	RC	0x0	GPIO0 Interrupt Status This bit indicates an interrupt condition has been met for GPIO0. This bit is cleared on read.
3	FC_GPIO3_STS	R	0x0	Forward Channel GPIO3 Status This bit indicates the current value for forward channel GPIO3.
2	FC_GPIO2_STS	R	0x0	Forward Channel GPIO2 Status This bit indicates the current value for forward channel GPIO2.
1	FC_GPIO1_STS	R	0x0	Forward Channel GPIO1 Status This bit indicates the current value for forward channel GPIO1.
0	FC_GPIO0_STS	R	0x0	Forward Channel GPIO0 Status This bit indicates the current value for forward channel GPIO0.

1.1.159 FC_GPIO_ICR Register (Address = 0xDD) [Default = 0x00]

FC_GPIO_ICR is shown in Table 1-162.

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Table 1-162. FC_GPIO_ICR Register Field Descriptions

Bit	Field	Type	Default	Description
7	GPIO3_FALL_IE	R/W	0x0	GPIO3 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO3.
6	GPIO3_RISE_IE	R/W	0x0	GPIO3 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO3.
5	GPIO2_FALL_IE	R/W	0x0	GPIO2 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO2.

Table 1-162. FC_GPIO_ICR Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	GPIO2_RISE_IE	R/W	0x0	GPIO2 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO2.
3	GPIO1_FALL_IE	R/W	0x0	GPIO1 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO1.
2	GPIO1_RISE_IE	R/W	0x0	GPIO1 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO1.
1	GPIO0_FALL_IE	R/W	0x0	GPIO0 Fall Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO0.
0	GPIO0_RISE_IE	R/W	0x0	GPIO0 Rise Interrupt Enable If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO0.

1.1.160 SEN_INT_RISE_STS Register (Address = 0xDE) [Default = 0x00]

SEN_INT_RISE_STS is shown in Table 1-163.

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Table 1-163. SEN_INT_RISE_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SEN_INT_RISE	RC	0x0	Sensor Interrupt Rise Status This register provides the interrupt status for rising edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in the SEN_INT_RISE_MASK register, a rising edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in this register.

1.1.161 SEN_INT_FALL_STS Register (Address = 0xDF) [Default = 0x00]

SEN_INT_FALL_STS is shown in Table 1-164.

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Table 1-164. SEN_INT_FALL_STS Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SEN_INT_FALL	RC	0x0	Sensor Interrupt Fall Status This register provides the interrupt status for falling edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in the SEN_INT_FALL_MASK register, a falling edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in this register.

1.1.162 CHANNEL_MODE Register (Address = 0xE4) [Default = 0x00]

CHANNEL_MODE is shown in Table 1-165.

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Table 1-165. CHANNEL_MODE Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R/W	0x0	Reserved

Table 1-165. CHANNEL_MODE Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2:0	REG_FPD_FUNC_MODE	R/W	0x0	FPD interface Mode Selection: Strap 0,1,2,4 000: 7.55 Gbps Sync Mode 001: 7.55 Gbps Non-sync Mode 010: FPD3 CSI Sync/Non-sync Mode 011: Reserved 100: FPD3 DVP RAW12 HF 101: FPD3 DVP RAW10 110: FPD3 DVP RAW12 LF 111: Reserved At power-up, this field is set based on the MODE pin strap value.

1.1.163 FPD_RX_ID0 Register (Address = 0xF0) [Default = 0x5F]

FPD_RX_ID0 is shown in Table 1-166.

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Table 1-166. FPD_RX_ID0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_RX_ID0	R	0x5F	FPD_RX_ID0: First byte ID code: '_ '

1.1.164 FPD_RX_ID1 Register (Address = 0xF1) [Default = 0x55]

FPD_RX_ID1 is shown in Table 1-167.

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Table 1-167. FPD_RX_ID1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_RX_ID1	R	0x55	FPD_RX_ID1: 2nd byte of ID code: 'U '

1.1.165 FPD_RX_ID2 Register (Address = 0xF2) [Default = 0x42]

FPD_RX_ID2 is shown in Table 1-168.

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Table 1-168. FPD_RX_ID2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_RX_ID2	R	0x42	FPD_RX_ID2: 3rd byte of ID code: 'B '

1.1.166 FPD_RX_ID3 Register (Address = 0xF3) [Default = 0x39]

FPD_RX_ID3 is shown in Table 1-169.

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Table 1-169. FPD_RX_ID3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_RX_ID3	R	0x39	FPD_RX_ID3: 4th byte of ID code: '9 '

1.1.167 FPD_RX_ID4 Register (Address = 0xF4) [Default = 0x37]

FPD_RX_ID4 is shown in Table 1-170.

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Table 1-170. FPD_RX_ID4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_RX_ID4	R	0x37	FPD_RX_ID4: 4th byte of ID code: '7'

1.1.168 FPD_RX_ID5 Register (Address = 0xF5) [Default = 0x30]

FPD_RX_ID5 is shown in Table 1-171.

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Table 1-171. FPD_RX_ID5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_RX_ID5	R	0x30	FPD_RX_ID5: 5th byte of ID code: '0'

1.1.169 FPD_RX_ID6 Register (Address = 0xF6) [Default = 0x32]

FPD_RX_ID6 is shown in Table 1-172.

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Table 1-172. FPD_RX_ID6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	FPD_RX_ID6	R	0x32	FPD_RX_ID5: 5th byte of ID code: '2'

1.1.170 I2C_RX0_ID Register (Address = 0xF8) [Default = 0x00]

I2C_RX0_ID is shown in Table 1-173.

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Table 1-173. I2C_RX0_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RX_PORT0_ID	R/W	0x0	7-bit Receive Port 0 I2C ID Configures the decoder for detecting transactions designated for Receiver port 0 registers. This provides a simpler method of accessing device registers specifically for port 0 without having to use the paging function to select the register page. A value of 0 in this field disables the Port0 decoder.
0	RESERVED	R	0x0	Reserved

1.1.171 I2C_RX1_ID Register (Address = 0xF9) [Default = 0x00]

I2C_RX1_ID is shown in Table 1-174.

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Table 1-174. I2C_RX1_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RX_PORT1_ID	R/W	0x0	7-bit Receive Port 1 I2C ID Configures the decoder for detecting transactions designated for Receiver port 1 registers. This provides a simpler method of accessing device registers specifically for port 1 without having to use the paging function to select the register page. A value of 0 in this field disables the Port1 decoder.
0	RESERVED	R	0x0	Reserved

1.1.172 I2C_RX2_ID Register (Address = 0xFA) [Default = 0x00]

I2C_RX2_ID is shown in Table 1-175.

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Table 1-175. I2C_RX2_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RX_PORT2_ID	R/W	0x0	7-bit Receive Port 2 I2C ID Configures the decoder for detecting transactions designated for Receiver port 2 registers. This provides a simpler method of accessing device registers specifically for port 2 without having to use the paging function to select the register page. A value of 0 in this field disables the Port2 decoder.
0	RESERVED	R	0x0	Reserved

1.1.173 I2C_RX3_ID Register (Address = 0xFB) [Default = 0x00]

I2C_RX3_ID is shown in Table 1-176.

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Table 1-176. I2C_RX3_ID Register Field Descriptions

Bit	Field	Type	Default	Description
7:1	RX_PORT3_ID	R/W	0x0	7-bit Receive Port 3 I2C ID Configures the decoder for detecting transactions designated for Receiver port 3 registers. This provides a simpler method of accessing device registers specifically for port 3 without having to use the paging function to select the register page. A value of 0 in this field disables the Port3 decoder.
0	RESERVED	R	0x0	Reserved

1.2 PATGEN_and_CSI-2_Trim Registers

Table 1-177 lists the memory-mapped registers for the PATGEN_and_CSI-2_Trim registers. All register offset addresses not listed in Table 1-177 should be considered as reserved locations and the register contents should not be modified.

Table 1-177. PATGEN_AND_CSI-2_TRIM Registers

Address	Acronym	Register Name	Section
0x1	PGEN_CTL	PGEN_CTL	Go
0x2	PGEN_CFG	PGEN_CFG	Go
0x3	PGEN_CSI_DI	PGEN_CSI_DI	Go
0x4	PGEN_LINE_SIZE1	PGEN_LINE_SIZE1	Go
0x5	PGEN_LINE_SIZE0	PGEN_LINE_SIZE0	Go
0x6	PGEN_BAR_SIZE1	PGEN_BAR_SIZE1	Go
0x7	PGEN_BAR_SIZE0	PGEN_BAR_SIZE0	Go
0x8	PGEN_ACT_LPF1	PGEN_ACT_LPF1	Go
0x9	PGEN_ACT_LPF0	PGEN_ACT_LPF0	Go
0xA	PGEN_TOT_LPF1	PGEN_TOT_LPF1	Go
0xB	PGEN_TOT_LPF0	PGEN_TOT_LPF0	Go
0xC	PGEN_LINE_PD1	PGEN_LINE_PD1	Go
0xD	PGEN_LINE_PD0	PGEN_LINE_PD0	Go
0xE	PGEN_VBP	PGEN_VBP	Go
0xF	PGEN_VFP	PGEN_VFP	Go
0x10	PGEN_COLOR0	PGEN_COLOR0	Go
0x11	PGEN_COLOR1	PGEN_COLOR1	Go

Table 1-177. PATGEN_AND_CSI-2_TRIM Registers (continued)

Address	Acronym	Register Name	Section
0x12	PGEN_COLOR2	PGEN_COLOR2	Go
0x13	PGEN_COLOR3	PGEN_COLOR3	Go
0x14	PGEN_COLOR4	PGEN_COLOR4	Go
0x15	PGEN_COLOR5	PGEN_COLOR5	Go
0x16	PGEN_COLOR6	PGEN_COLOR6	Go
0x17	PGEN_COLOR7	PGEN_COLOR7	Go
0x18	PGEN_COLOR8	PGEN_COLOR8	Go
0x19	PGEN_COLOR9	PGEN_COLOR9	Go
0x1A	PGEN_COLOR10	PGEN_COLOR10	Go
0x1B	PGEN_COLOR11	PGEN_COLOR11	Go
0x1C	PGEN_COLOR12	PGEN_COLOR12	Go
0x1D	PGEN_COLOR13	PGEN_COLOR13	Go
0x1E	PGEN_COLOR14	PGEN_COLOR14	Go
0x1F	PGEN_COLOR15	PGEN_COLOR15	Go
0x21	CSI1_PGEN_CTL	CSI1_PGEN_CTL	Go
0x22	CSI1_PGEN_CFG	CSI1_PGEN_CFG	Go
0x23	CSI1_PGEN_CSI_DI	CSI1_PGEN_CSI_DI	Go
0x24	CSI1_PGEN_LINE_SIZE1	CSI1_PGEN_LINE_SIZE1	Go
0x25	CSI1_PGEN_LINE_SIZE0	CSI1_PGEN_LINE_SIZE0	Go
0x26	CSI1_PGEN_BAR_SIZE1	CSI1_PGEN_BAR_SIZE1	Go
0x27	CSI1_PGEN_BAR_SIZE0	CSI1_PGEN_BAR_SIZE0	Go
0x28	CSI1_PGEN_ACT_LPF1	CSI1_PGEN_ACT_LPF1	Go
0x29	CSI1_PGEN_ACT_LPF0	CSI1_PGEN_ACT_LPF0	Go
0x2A	CSI1_PGEN_TOT_LPF1	CSI1_PGEN_TOT_LPF1	Go
0x2B	CSI1_PGEN_TOT_LPF0	CSI1_PGEN_TOT_LPF0	Go
0x2C	CSI1_PGEN_LINE_PD1	CSI1_PGEN_LINE_PD1	Go
0x2D	CSI1_PGEN_LINE_PD0	CSI1_PGEN_LINE_PD0	Go
0x2E	CSI1_PGEN_VBP	CSI1_PGEN_VBP	Go
0x2F	CSI1_PGEN_VFP	CSI1_PGEN_VFP	Go
0x30	CSI1_PGEN_COLOR0	CSI1_PGEN_COLOR0	Go
0x31	CSI1_PGEN_COLOR1	CSI1_PGEN_COLOR1	Go
0x32	CSI1_PGEN_COLOR2	CSI1_PGEN_COLOR2	Go
0x33	CSI1_PGEN_COLOR3	CSI1_PGEN_COLOR3	Go
0x34	CSI1_PGEN_COLOR4	CSI1_PGEN_COLOR4	Go
0x35	CSI1_PGEN_COLOR5	CSI1_PGEN_COLOR5	Go
0x36	CSI1_PGEN_COLOR6	CSI1_PGEN_COLOR6	Go
0x37	CSI1_PGEN_COLOR7	CSI1_PGEN_COLOR7	Go
0x38	CSI1_PGEN_COLOR8	CSI1_PGEN_COLOR8	Go
0x39	CSI1_PGEN_COLOR9	CSI1_PGEN_COLOR9	Go
0x3A	CSI1_PGEN_COLOR10	CSI1_PGEN_COLOR10	Go
0x3B	CSI1_PGEN_COLOR11	CSI1_PGEN_COLOR11	Go
0x3C	CSI1_PGEN_COLOR12	CSI1_PGEN_COLOR12	Go
0x3D	CSI1_PGEN_COLOR13	CSI1_PGEN_COLOR13	Go
0x3E	CSI1_PGEN_COLOR14	CSI1_PGEN_COLOR14	Go
0x3F	CSI1_PGEN_COLOR15	CSI1_PGEN_COLOR15	Go
0x40	CSI0_TCK_PREP	CSI0_TCK_PREP	Go
0x41	CSI0_TCK_ZERO	CSI0_TCK_ZERO	Go

Table 1-177. PATGEN_AND_CSI-2_TRIM Registers (continued)

Address	Acronym	Register Name	Section
0x42	CSI0_TCK_TRAIL	CSI0_TCK_TRAIL	Go
0x43	CSI0_TCK_POST	CSI0_TCK_POST	Go
0x44	CSI0_THS_PREP	CSI0_THS_PREP	Go
0x45	CSI0_THS_ZERO	CSI0_THS_ZERO	Go
0x46	CSI0_THS_TRAIL	CSI0_THS_TRAIL	Go
0x47	CSI0_THS_EXIT	CSI0_THS_EXIT	Go
0x48	CSI0_TPLX	CSI0_TPLX	Go
0x66	CSI1_TCK_PREP	CSI1_TCK_PREP	Go
0x67	CSI1_TCK_ZERO	CSI1_TCK_ZERO	Go
0x68	CSI1_TCK_TRAIL	CSI1_TCK_TRAIL	Go
0x69	CSI1_TCK_POST	CSI1_TCK_POST	Go
0x6A	CSI1_THS_PREP	CSI1_THS_PREP	Go
0x6B	CSI1_THS_ZERO	CSI1_THS_ZERO	Go
0x6C	CSI1_THS_TRAIL	CSI1_THS_TRAIL	Go
0x6D	CSI1_THS_EXIT	CSI1_THS_EXIT	Go
0x6E	CSI1_TPLX	CSI1_TPLX	Go

Complex bit access types are encoded to fit into small table cells. Table 1-178 shows the codes that are used for access types in this section.

Table 1-178. PATGEN_and_CSI-2_Trim Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

1.2.1 PGEN_CTL Register (Address = 0x1) [Default = 0x00]

PGEN_CTL is shown in Table 1-179.

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Table 1-179. PGEN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PGEN_CSI_VC_MSB	R/W	0x0	CSI Virtual Channel Identifier MSBs This field controls the Most Significant two bits of the Virtual Channel Identifier field in the CSI packet header.
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3:1	RESERVED	R/W	0x0	Reserved
0	PGEN_ENABLE	R/W	0x0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

1.2.2 PGEN_CFG Register (Address = 0x2) [Default = 0x33]

PGEN_CFG is shown in Table 1-180.

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Table 1-180. PGEN_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	PGEN_FIXED_EN	R/W	0x0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0: Send Color Bar Pattern 1: Send Fixed Color Pattern
6	RESERVED	R/W	0x0	Reserved
5:4	NUM_CBARS	R/W	0x3	Number of Color Bars 00: 1 Color Bar 01: 2 Color Bars 10: 4 Color Bars 11: 8 Color Bars
3:0	BLOCK_SIZE	R/W	0x3	Block Size. For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 15.

1.2.3 PGEN_CSI_DI Register (Address = 0x3) [Default = 0x24]

PGEN_CSI_DI is shown in Table 1-181.

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Table 1-181. PGEN_CSI_DI Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PGEN_CSI_VC	R/W	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier
5:0	PGEN_CSI_DT	R/W	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.

1.2.4 PGEN_LINE_SIZE1 Register (Address = 0x4) [Default = 0x07]

PGEN_LINE_SIZE1 is shown in Table 1-182.

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Table 1-182. PGEN_LINE_SIZE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[15:8]	R/W	0x7	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

1.2.5 PGEN_LINE_SIZE0 Register (Address = 0x5) [Default = 0x80]

PGEN_LINE_SIZE0 is shown in Table 1-183.

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Table 1-183. PGEN_LINE_SIZE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

1.2.6 PGEN_BAR_SIZE1 Register (Address = 0x6) [Default = 0x00]

PGEN_BAR_SIZE1 is shown in Table 1-184.

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Table 1-184. PGEN_BAR_SIZE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

1.2.7 PGEN_BAR_SIZE0 Register (Address = 0x7) [Default = 0xF0]

PGEN_BAR_SIZE0 is shown in Table 1-185.

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Table 1-185. PGEN_BAR_SIZE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

1.2.8 PGEN_ACT_LPF1 Register (Address = 0x8) [Default = 0x01]

PGEN_ACT_LPF1 is shown in Table 1-186.

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Table 1-186. PGEN_ACT_LPF1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[15:8]	R/W	0x1	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

1.2.9 PGEN_ACT_LPF0 Register (Address = 0x9) [Default = 0xE0]

PGEN_ACT_LPF0 is shown in Table 1-187.

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Table 1-187. PGEN_ACT_LPF0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

1.2.10 PGEN_TOT_LPF1 Register (Address = 0xA) [Default = 0x02]

PGEN_TOT_LPF1 is shown in Table 1-188.

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Table 1-188. PGEN_TOT_LPF1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[15:8]	R/W	0x2	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

1.2.11 PGEN_TOT_LPF0 Register (Address = 0xB) [Default = 0x0D]

PGEN_TOT_LPF0 is shown in Table 1-189.

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Table 1-189. PGEN_TOT_LPF0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[7:0]	R/W	0xD	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

1.2.12 PGEN_LINE_PD1 Register (Address = 0xC) [Default = 0x0C]

PGEN_LINE_PD1 is shown in Table 1-190.

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Table 1-190. PGEN_LINE_PD1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[15:8]	R/W	0xC	Line Period Most significant byte of the line period. In 800 Mbps and 1.6 Gbps CSI-2 modes, units are 10ns and the default setting for the line period registers sets a line period of 31.75 microseconds. In 1.2 Gbps CSI-2 mode, units are 13.33ns and the default setting for the line period registers sets a line period of 42.33 microseconds. In 400 Mbps CSI-2 mode, units are 20ns and the default setting for the line period registers sets a line period of 63.5 microseconds.

1.2.13 PGEN_LINE_PD0 Register (Address = 0xD) [Default = 0x67]

PGEN_LINE_PD0 is shown in Table 1-191.

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Table 1-191. PGEN_LINE_PD0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period Least significant byte of the line period. In 800 Mbps and 1.6 Gbps CSI-2 modes, units are 10ns and the default setting for the line period registers sets a line period of 31.75 microseconds. In 1.2 Gbps CSI-2 mode, units are 13.33ns and the default setting for the line period registers sets a line period of 42.33 microseconds. In 400 Mbps CSI-2 mode, units are 20ns and the default setting for the line period registers sets a line period of 63.5 microseconds.

1.2.14 PGEN_VBP Register (Address = 0xE) [Default = 0x21]

PGEN_VBP is shown in Table 1-192.

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Table 1-192. PGEN_VBP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_VBP	R/W	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

1.2.15 PGEN_VFP Register (Address = 0xF) [Default = 0x0A]

PGEN_VFP is shown in Table 1-193.

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Table 1-193. PGEN_VFP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_VFP	R/W	0xA	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

1.2.16 PGEN_COLOR0 Register (Address = 0x10) [Default = 0xAA]

PGEN_COLOR0 is shown in Table 1-194.

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Table 1-194. PGEN_COLOR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0. For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

1.2.17 PGEN_COLOR1 Register (Address = 0x11) [Default = 0x33]

PGEN_COLOR1 is shown in Table 1-195.

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Table 1-195. PGEN_COLOR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

1.2.18 PGEN_COLOR2 Register (Address = 0x12) [Default = 0xF0]

PGEN_COLOR2 is shown in Table 1-196.

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Table 1-196. PGEN_COLOR2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

1.2.19 PGEN_COLOR3 Register (Address = 0x13) [Default = 0x7F]

PGEN_COLOR3 is shown in Table 1-197.

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Table 1-197. PGEN_COLOR3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

1.2.20 PGEN_COLOR4 Register (Address = 0x14) [Default = 0x55]

PGEN_COLOR4 is shown in Table 1-198.

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Table 1-198. PGEN_COLOR4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

1.2.21 PGEN_COLOR5 Register (Address = 0x15) [Default = 0xCC]

PGEN_COLOR5 is shown in Table 1-199.

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Table 1-199. PGEN_COLOR5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

1.2.22 PGEN_COLOR6 Register (Address = 0x16) [Default = 0x0F]

PGEN_COLOR6 is shown in Table 1-200.

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Table 1-200. PGEN_COLOR6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR6	R/W	0xF	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

1.2.23 PGEN_COLOR7 Register (Address = 0x17) [Default = 0x80]

PGEN_COLOR7 is shown in Table 1-201.

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Table 1-201. PGEN_COLOR7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

1.2.24 PGEN_COLOR8 Register (Address = 0x18) [Default = 0x00]

PGEN_COLOR8 is shown in Table 1-202.

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Table 1-202. PGEN_COLOR8 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

1.2.25 PGEN_COLOR9 Register (Address = 0x19) [Default = 0x00]

PGEN_COLOR9 is shown in Table 1-203.

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Table 1-203. PGEN_COLOR9 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

1.2.26 PGEN_COLOR10 Register (Address = 0x1A) [Default = 0x00]

PGEN_COLOR10 is shown in Table 1-204.

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Table 1-204. PGEN_COLOR10 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

1.2.27 PGEN_COLOR11 Register (Address = 0x1B) [Default = 0x00]

PGEN_COLOR11 is shown in Table 1-205.

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Table 1-205. PGEN_COLOR11 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

1.2.28 PGEN_COLOR12 Register (Address = 0x1C) [Default = 0x00]

PGEN_COLOR12 is shown in Table 1-206.

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Table 1-206. PGEN_COLOR12 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

1.2.29 PGEN_COLOR13 Register (Address = 0x1D) [Default = 0x00]

PGEN_COLOR13 is shown in Table 1-207.

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Table 1-207. PGEN_COLOR13 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

1.2.30 PGEN_COLOR14 Register (Address = 0x1E) [Default = 0x00]

PGEN_COLOR14 is shown in Table 1-208.

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Table 1-208. PGEN_COLOR14 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

1.2.31 PGEN_COLOR15 Register (Address = 0x1F) [Default = 0x00]

PGEN_COLOR15 is shown in Table 1-209.

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Table 1-209. PGEN_COLOR15 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR15	R/W	0x0	Pattern Generator Color 15 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

1.2.32 CSI1_PGEN_CTL Register (Address = 0x21) [Default = 0x00]

CSI1_PGEN_CTL is shown in Table 1-210.

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Table 1-210. CSI1_PGEN_CTL Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PGEN_CSI_VC_MSB	R/W	0x0	CSI Virtual Channel Identifier MSBs This field controls the Most Significant two bits of the Virtual Channel Identifier field in the CSI packet header.
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3:2	RESERVED	R/W	0x0	Reserved
1	PGEN_SIMUL_CTL	R/W	0x0	CSI1 Simultaneous control Enable Setting this bit to 1 will enable simultaneous control of both CSI0 and CSI1 pattern generators. Register writes in the range of 0x00 to 0x1F will write to the equivalent registers in CSI1 (i.e. 0x20 to 0x3F). 1: Enable Simultaneous control 0: Disable Simultaneous control
0	PGEN_ENABLE	R/W	0x0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

1.2.33 CSI1_PGEN_CFG Register (Address = 0x22) [Default = 0x33]

CSI1_PGEN_CFG is shown in Table 1-211.

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Table 1-211. CSI1_PGEN_CFG Register Field Descriptions

Bit	Field	Type	Default	Description
7	PGEN_FIXED_EN	R/W	0x0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0: Send Color Bar Pattern 1: Send Fixed Color Pattern
6	RESERVED	R/W	0x0	Reserved
5:4	NUM_CBARS	R/W	0x3	Number of Color Bars 00: 1 Color Bar 01: 2 Color Bars 10: 4 Color Bars 11: 8 Color Bars
3:0	BLOCK_SIZE	R/W	0x3	Block Size. For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 15.

1.2.34 CSI1_PGEN_CSI_DI Register (Address = 0x23) [Default = 0x24]

CSI1_PGEN_CSI_DI is shown in Table 1-212.

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Table 1-212. CSI1_PGEN_CSI_DI Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	PGEN_CSI_VC	R/W	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier
5:0	PGEN_CSI_DT	R/W	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.

1.2.35 CSI1_PGEN_LINE_SIZE1 Register (Address = 0x24) [Default = 0x07]

CSI1_PGEN_LINE_SIZE1 is shown in Table 1-213.

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Table 1-213. CSI1_PGEN_LINE_SIZE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[15:8]	R/W	0x7	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

1.2.36 CSI1_PGEN_LINE_SIZE0 Register (Address = 0x25) [Default = 0x80]

CSI1_PGEN_LINE_SIZE0 is shown in Table 1-214.

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Table 1-214. CSI1_PGEN_LINE_SIZE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

1.2.37 CSI1_PGEN_BAR_SIZE1 Register (Address = 0x26) [Default = 0x00]

CSI1_PGEN_BAR_SIZE1 is shown in Table 1-215.

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Table 1-215. CSI1_PGEN_BAR_SIZE1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

1.2.38 CSI1_PGEN_BAR_SIZE0 Register (Address = 0x27) [Default = 0xF0]

CSI1_PGEN_BAR_SIZE0 is shown in Table 1-216.

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Table 1-216. CSI1_PGEN_BAR_SIZE0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

1.2.39 CSI1_PGEN_ACT_LPF1 Register (Address = 0x28) [Default = 0x01]

CSI1_PGEN_ACT_LPF1 is shown in Table 1-217.

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Table 1-217. CSI1_PGEN_ACT_LPF1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[15:8]	R/W	0x1	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

1.2.40 CSI1_PGEN_ACT_LPF0 Register (Address = 0x29) [Default = 0xE0]

CSI1_PGEN_ACT_LPF0 is shown in Table 1-218.

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Table 1-218. CSI1_PGEN_ACT_LPF0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

1.2.41 CSI1_PGEN_TOT_LPF1 Register (Address = 0x2A) [Default = 0x02]

CSI1_PGEN_TOT_LPF1 is shown in Table 1-219.

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Table 1-219. CSI1_PGEN_TOT_LPF1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[15:8]	R/W	0x2	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

1.2.42 CSI1_PGEN_TOT_LPF0 Register (Address = 0x2B) [Default = 0x0D]

CSI1_PGEN_TOT_LPF0 is shown in Table 1-220.

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Table 1-220. CSI1_PGEN_TOT_LPF0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_TOT_LPF[7:0]	R/W	0xD	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

1.2.43 CSI1_PGEN_LINE_PD1 Register (Address = 0x2C) [Default = 0x0C]

CSI1_PGEN_LINE_PD1 is shown in Table 1-221.

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Table 1-221. CSI1_PGEN_LINE_PD1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[15:8]	R/W	0xC	Line Period Most significant byte of the line period. In 800 Mbps and 1.6 Gbps CSI-2 modes, units are 10ns and the default setting for the line period registers sets a line period of 31.75 microseconds. In 1.2 Gbps CSI-2 mode, units are 13.33ns and the default setting for the line period registers sets a line period of 42.33 microseconds. In 400 Mbps CSI-2 mode, units are 20ns and the default setting for the line period registers sets a line period of 63.5 microseconds.

1.2.44 CSI1_PGEN_LINE_PD0 Register (Address = 0x2D) [Default = 0x67]

CSI1_PGEN_LINE_PD0 is shown in Table 1-222.

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Table 1-222. CSI1_PGEN_LINE_PD0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period Least significant byte of the line period. In 800 Mbps and 1.6 Gbps CSI-2 modes, units are 10ns and the default setting for the line period registers sets a line period of 31.75 microseconds. In 1.2 Gbps CSI-2 mode, units are 13.33ns and the default setting for the line period registers sets a line period of 42.33 microseconds. In 400 Mbps CSI-2 mode, units are 20ns and the default setting for the line period registers sets a line period of 63.5 microseconds.

1.2.45 CSI1_PGEN_VBP Register (Address = 0x2E) [Default = 0x21]

CSI1_PGEN_VBP is shown in Table 1-223.

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Table 1-223. CSI1_PGEN_VBP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_VBP	R/W	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

1.2.46 CSI1_PGEN_VFP Register (Address = 0x2F) [Default = 0x0A]

CSI1_PGEN_VFP is shown in Table 1-224.

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Table 1-224. CSI1_PGEN_VFP Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_VFP	R/W	0xA	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

1.2.47 CSI1_PGEN_COLOR0 Register (Address = 0x30) [Default = 0xAA]

CSI1_PGEN_COLOR0 is shown in Table 1-225.

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Table 1-225. CSI1_PGEN_COLOR0 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0. For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

1.2.48 CSI1_PGEN_COLOR1 Register (Address = 0x31) [Default = 0x33]

CSI1_PGEN_COLOR1 is shown in Table 1-226.

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Table 1-226. CSI1_PGEN_COLOR1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

1.2.49 CSI1_PGEN_COLOR2 Register (Address = 0x32) [Default = 0xF0]

CSI1_PGEN_COLOR2 is shown in Table 1-227.

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Table 1-227. CSI1_PGEN_COLOR2 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

1.2.50 CSI1_PGEN_COLOR3 Register (Address = 0x33) [Default = 0x7F]

CSI1_PGEN_COLOR3 is shown in Table 1-228.

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Table 1-228. CSI1_PGEN_COLOR3 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

1.2.51 CSI1_PGEN_COLOR4 Register (Address = 0x34) [Default = 0x55]

CSI1_PGEN_COLOR4 is shown in Table 1-229.

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Table 1-229. CSI1_PGEN_COLOR4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

1.2.52 CSI1_PGEN_COLOR5 Register (Address = 0x35) [Default = 0xCC]

CSI1_PGEN_COLOR5 is shown in Table 1-230.

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Table 1-230. CSI1_PGEN_COLOR5 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

1.2.53 CSI1_PGEN_COLOR6 Register (Address = 0x36) [Default = 0x0F]

CSI1_PGEN_COLOR6 is shown in Table 1-231.

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Table 1-231. CSI1_PGEN_COLOR6 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR6	R/W	0xF	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

1.2.54 CSI1_PGEN_COLOR7 Register (Address = 0x37) [Default = 0x80]

CSI1_PGEN_COLOR7 is shown in Table 1-232.

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Table 1-232. CSI1_PGEN_COLOR7 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

1.2.55 CSI1_PGEN_COLOR8 Register (Address = 0x38) [Default = 0x00]

CSI1_PGEN_COLOR8 is shown in Table 1-233.

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Table 1-233. CSI1_PGEN_COLOR8 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

1.2.56 CSI1_PGEN_COLOR9 Register (Address = 0x39) [Default = 0x00]

CSI1_PGEN_COLOR9 is shown in Table 1-234.

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Table 1-234. CSI1_PGEN_COLOR9 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

1.2.57 CSI1_PGEN_COLOR10 Register (Address = 0x3A) [Default = 0x00]

CSI1_PGEN_COLOR10 is shown in Table 1-235.

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Table 1-235. CSI1_PGEN_COLOR10 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

1.2.58 CSI1_PGEN_COLOR11 Register (Address = 0x3B) [Default = 0x00]

CSI1_PGEN_COLOR11 is shown in Table 1-236.

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Table 1-236. CSI1_PGEN_COLOR11 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

1.2.59 CSI1_PGEN_COLOR12 Register (Address = 0x3C) [Default = 0x00]

CSI1_PGEN_COLOR12 is shown in Table 1-237.

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Table 1-237. CSI1_PGEN_COLOR12 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

1.2.60 CSI1_PGEN_COLOR13 Register (Address = 0x3D) [Default = 0x00]

CSI1_PGEN_COLOR13 is shown in Table 1-238.

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Table 1-238. CSI1_PGEN_COLOR13 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

1.2.61 CSI1_PGEN_COLOR14 Register (Address = 0x3E) [Default = 0x00]

CSI1_PGEN_COLOR14 is shown in Table 1-239.

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Table 1-239. CSI1_PGEN_COLOR14 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

1.2.62 CSI1_PGEN_COLOR15 Register (Address = 0x3F) [Default = 0x00]

CSI1_PGEN_COLOR15 is shown in Table 1-240.

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Table 1-240. CSI1_PGEN_COLOR15 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	PGEN_COLOR15	R/W	0x0	Pattern Generator Color 15 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

1.2.63 CSI0_TCK_PREP Register (Address = 0x40) [Default = 0x00]

CSI0_TCK_PREP is shown in Table 1-241.

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Table 1-241. CSI0_TCK_PREP Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_PREP_OV	R/W	0x0	Override CSI Tck-prep parameter 0: Tck-prep is automatically determined 1: Override Tck-prep with value in bits 6:0 of this register
6:0	MR_TCK_PREP	R/W	0x0	Tck-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.64 CSI0_TCK_ZERO Register (Address = 0x41) [Default = 0x00]

CSI0_TCK_ZERO is shown in Table 1-242.

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Table 1-242. CSI0_TCK_ZERO Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_ZERO_OV	R/W	0x0	Override CSI Tck-zero parameter 0: Tck-zero is automatically determined 1: Override Tck-zero with value in bits 6:0 of this register
6:0	MR_TCK_ZERO	R/W	0x0	Tck-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.65 CSI0_TCK_TRAIL Register (Address = 0x42) [Default = 0x00]

CSI0_TCK_TRAIL is shown in Table 1-243.

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Table 1-243. CSI0_TCK_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_TRAIL_OV	R/W	0x0	Override CSI Tck-trail parameter 0: Tck-trail is automatically determined 1: Override Tck-trail with value in bits 6:0 of this register
6:0	MR_TCK_TRAIL	R/W	0x0	Tck-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.66 CSI0_TCK_POST Register (Address = 0x43) [Default = 0x00]

CSI0_TCK_POST is shown in Table 1-244.

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Table 1-244. CSI0_TCK_POST Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_POST_OV	R/W	0x0	Override CSI Tck-post parameter 0: Tck-post is automatically determined 1: Override Tck-post with value in bits 6:0 of this register
6:0	MR_TCK_POST	R/W	0x0	Tck-post value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.67 CSI0_THS_PREP Register (Address = 0x44) [Default = 0x00]

CSI0_THS_PREP is shown in Table 1-245.

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Table 1-245. CSI0_THS_PREP Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_PREP_OV	R/W	0x0	Override CSI Ths-prep parameter 0: Ths-prep is automatically determined 1: Override Ths-prep with value in bits 6:0 of this register
6:0	MR_THS_PREP	R/W	0x0	Ths-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.68 CSI0_THS_ZERO Register (Address = 0x45) [Default = 0x00]

CSI0_THS_ZERO is shown in Table 1-246.

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Table 1-246. CSI0_THS_ZERO Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_ZERO_OV	R/W	0x0	Override CSI Ths-zero parameter 0: Ths-zero is automatically determined 1: Override Ths-zero with value in bits 6:0 of this register
6:0	MR_THS_ZERO	R/W	0x0	Ths-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.69 CSI0_THS_TRAIL Register (Address = 0x46) [Default = 0x00]

CSI0_THS_TRAIL is shown in Table 1-247.

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Table 1-247. CSI0_THS_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_TRAIL_OV	R/W	0x0	Override CSI Ths-trail parameter 0: Ths-trail is automatically determined 1: Override Ths-trail with value in bits 6:0 of this register

Table 1-247. CSI0_THS_TRAIL Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:0	MR_THS_TRAIL	R/W	0x0	Ths-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.70 CSI0_THS_EXIT Register (Address = 0x47) [Default = 0x00]

CSI0_THS_EXIT is shown in Table 1-248.

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Table 1-248. CSI0_THS_EXIT Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_EXIT_OV	R/W	0x0	Override CSI Ths-exit parameter 0: Ths-exit is automatically determined 1: Override Ths-exit with value in bits 6:0 of this register
6:0	MR_THS_EXIT	R/W	0x0	Ths-exit value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.71 CSI0_TPLX Register (Address = 0x48) [Default = 0x00]

CSI0_TPLX is shown in Table 1-249.

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Table 1-249. CSI0_TPLX Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TPLX_OV	R/W	0x0	Override CSI Tplx parameter 0: Tplx is automatically determined 1: Override Tplx with value in bits 6:0 of this register
6:0	MR_TPLX	R/W	0x0	Tplx value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.72 CSI1_TCK_PREP Register (Address = 0x66) [Default = 0x00]

CSI1_TCK_PREP is shown in Table 1-250.

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Table 1-250. CSI1_TCK_PREP Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_PREP_OV	R/W	0x0	Override CSI Tck-prep parameter 0: Tck-prep is automatically determined 1: Override Tck-prep with value in bits 6:0 of this register
6:0	MR_TCK_PREP	R/W	0x0	Tck-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.73 CSI1_TCK_ZERO Register (Address = 0x67) [Default = 0x00]

CSI1_TCK_ZERO is shown in Table 1-251.

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Table 1-251. CSI1_TCK_ZERO Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_ZERO_OV	R/W	0x0	Override CSI Tck-zero parameter 0: Tck-zero is automatically determined 1: Override Tck-zero with value in bits 6:0 of this register
6:0	MR_TCK_ZERO	R/W	0x0	Tck-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.74 CSI1_TCK_TRAIL Register (Address = 0x68) [Default = 0x00]

CSI1_TCK_TRAIL is shown in Table 1-252.

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Table 1-252. CSI1_TCK_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_TRAIL_OV	R/W	0x0	Override CSI Tck-trail parameter 0: Tck-trail is automatically determined 1: Override Tck-trail with value in bits 6:0 of this register
6:0	MR_TCK_TRAIL	R/W	0x0	Tck-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.75 CSI1_TCK_POST Register (Address = 0x69) [Default = 0x00]

CSI1_TCK_POST is shown in Table 1-253.

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Table 1-253. CSI1_TCK_POST Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TCK_POST_OV	R/W	0x0	Override CSI Tck-post parameter 0: Tck-post is automatically determined 1: Override Tck-post with value in bits 6:0 of this register
6:0	MR_TCK_POST	R/W	0x0	Tck-post value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.76 CSI1_THS_PREP Register (Address = 0x6A) [Default = 0x00]

CSI1_THS_PREP is shown in Table 1-254.

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Table 1-254. CSI1_THS_PREP Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_PREP_OV	R/W	0x0	Override CSI Ths-prep parameter 0: Ths-prep is automatically determined 1: Override Ths-prep with value in bits 6:0 of this register
6:0	MR_THS_PREP	R/W	0x0	Ths-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.77 CSI1_THS_ZERO Register (Address = 0x6B) [Default = 0x00]

CSI1_THS_ZERO is shown in Table 1-255.

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Table 1-255. CSI1_THS_ZERO Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_ZERO_OV	R/W	0x0	Override CSI Ths-zero parameter 0: Ths-zero is automatically determined 1: Override Ths-zero with value in bits 6:0 of this register
6:0	MR_THS_ZERO	R/W	0x0	Ths-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.78 CSI1_THS_TRAIL Register (Address = 0x6C) [Default = 0x00]

CSI1_THS_TRAIL is shown in Table 1-256.

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Table 1-256. CSI1_THS_TRAIL Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_TRAIL_OV	R/W	0x0	Override CSI Ths-trail parameter 0: Ths-trail is automatically determined 1: Override Ths-trail with value in bits 6:0 of this register
6:0	MR_THS_TRAIL	R/W	0x0	Ths-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.79 CSI1_THS_EXIT Register (Address = 0x6D) [Default = 0x00]

CSI1_THS_EXIT is shown in Table 1-257.

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Table 1-257. CSI1_THS_EXIT Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_THS_EXIT_OV	R/W	0x0	Override CSI Ths-exit parameter 0: Ths-exit is automatically determined 1: Override Ths-exit with value in bits 6:0 of this register
6:0	MR_THS_EXIT	R/W	0x0	Ths-exit value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.2.80 CSI1_TPLX Register (Address = 0x6E) [Default = 0x00]

CSI1_TPLX is shown in Table 1-258.

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Table 1-258. CSI1_TPLX Register Field Descriptions

Bit	Field	Type	Default	Description
7	MR_TPLX_OV	R/W	0x0	Override CSI Tplx parameter 0: Tplx is automatically determined 1: Override Tplx with value in bits 6:0 of this register

Table 1-258. CSI1_TPLX Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6:0	MR_TPLX	R/W	0x0	Tplx value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

1.3 FPD_RX_Port_Analog Registers

Table 1-259 lists the memory-mapped registers for the FPD_RX_Port_Analog registers. All register offset addresses not listed in Table 1-259 should be considered as reserved locations and the register contents should not be modified.

Table 1-259. FPD_RX_PORT_ANALOG Registers

Address	Acronym	Register Name	Section
0x4	REG_RX_4	REG_RX_4	Go
0xD	REG_RX_D	REG_RX_D	Go
0x1B	REG_RX_1B	REG_RX_1B	Go
0x21	REG_RX_21	REG_RX_21	Go
0x25	REG_RX_25	REG_RX_25	Go
0x27	REG_RX_27	REG_RX_27	Go
0x28	REG_RX_28	REG_RX_28	Go
0x2B	REG_RX_2B	REG_RX_2B	Go
0x2C	REG_RX_2C	REG_RX_2C	Go
0x2E	REG_RX_2E	REG_RX_2E	Go
0x71	REG_RX_71	REG_RX_71	Go
0x90	REG_RX_90	REG_RX_90	Go
0x9E	REG_RX_9E	REG_RX_9E	Go
0xA8	REG_RX_A8	REG_RX_A8	Go
0xA9	REG_RX_A9	REG_RX_A9	Go
0xAA	REG_RX_AA	REG_RX_AA	Go
0xF0	REG_RX_F0	REG_RX_F0	Go

Complex bit access types are encoded to fit into small table cells. Table 1-260 shows the codes that are used for access types in this section.

Table 1-260. FPD_RX_Port_Analog Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

1.3.1 REG_RX_4 Register (Address = 0x4) [Default = 0x00]

REG_RX_4 is shown in Table 1-261.

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Table 1-261. REG_RX_4 Register Field Descriptions

Bit	Field	Type	Default	Description
7:5	SERDES_DRIVER_MODE	R/W	0x0	write 0 when interacting with DS90UB971-Q1 Do not change value otherwise
4	RESERVED	R/W	0x0	Reserved
3:0	RESERVED	R/W	0x0	Reserved

1.3.2 REG_RX_D Register (Address = 0xD) [Default = 0x3F]

REG_RX_D is shown in Table 1-262.

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Table 1-262. REG_RX_D Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:0	SERDES_DRIVER_EN	R/W	0x3F	Enable driver

1.3.3 REG_RX_1B Register (Address = 0x1B) [Default = 0x00]

REG_RX_1B is shown in Table 1-263.

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Table 1-263. REG_RX_1B Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6:4	SERDES_DRIVER_CTL1	R/W	0x0	write 0 when interacting with DS90UB971-Q1 Do not change value otherwise
3	SERDES_DRIVER_CTL2	R/W	0x0	0: when interacting with DS90UB971-Q1 1: when interacting with DS90UB953-Q1/DS90UB933-Q1/ DS90UB913A-Q1
2:1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

1.3.4 REG_RX_21 Register (Address = 0x21) [Default = 0x2D]

REG_RX_21 is shown in Table 1-264.

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Table 1-264. REG_RX_21 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SERDES_SYSTEM_INIT	R/W	0x2D	Write 0x2F

1.3.5 REG_RX_25 Register (Address = 0x25) [Default = 0x41]

REG_RX_25 is shown in Table 1-265.

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Table 1-265. REG_RX_25 Register Field Descriptions

Bit	Field	Type	Default	Description
7:0	SERDES_SYSTEM_RST	RH/W1S	0x41	SERDES apply reset mode: write 0xC1 SERDES remove reset mode: write 0x41

1.3.6 REG_RX_27 Register (Address = 0x27) [Default = 0x00]

REG_RX_27 is shown in Table 1-266.

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Table 1-266. REG_RX_27 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SERDES_START_EQ	R/W	0x0	Write 0x0

1.3.7 REG_RX_28 Register (Address = 0x28) [Default = 0x23]

REG_RX_28 is shown in Table 1-267.

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Table 1-267. REG_RX_28 Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SERDES_END_EQ	R/W	0x23	Write 0x23

1.3.8 REG_RX_2B Register (Address = 0x2B) [Default = 0x04]

REG_RX_2B is shown in Table 1-268.

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Table 1-268. REG_RX_2B Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SERDES_EQ_OFFSET	R/W	0x4	Write 0x04

1.3.9 REG_RX_2C Register (Address = 0x2C) [Default = 0x00]

REG_RX_2C is shown in Table 1-269.

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Table 1-269. REG_RX_2C Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SERDES_EQ_STATUS	R	0x0	Reads back the current EQ settting

1.3.10 REG_RX_2E Register (Address = 0x2E) [Default = 0x00]

REG_RX_2E is shown in Table 1-270.

Return to the Summary Table.

Table 1-270. REG_RX_2E Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	SERDES_EQ_EN	R/W	0x0	0 - SERDES EQ is disabled 1 - SERDES EQ is enabled
5:0	RESERVED	R	0x0	Reserved

1.3.11 REG_RX_71 Register (Address = 0x71) [Default = 0x40]

REG_RX_71 is shown in Table 1-271.

Return to the Summary Table.

Table 1-271. REG_RX_71 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	SERDES_GAIN_OVERRIDE	R/W	0x1	Write 0x0
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

1.3.12 REG_RX_90 Register (Address = 0x90) [Default = 0x00]

REG_RX_90 is shown in Table 1-272.

Return to the Summary Table.

Table 1-272. REG_RX_90 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	SERDES_EQ_CTL1	R/W	0x0	0: Disable 1: Enable
5:0	RESERVED	R	0x0	Reserved

1.3.13 REG_RX_9E Register (Address = 0x9E) [Default = 0x20]

REG_RX_9E is shown in Table 1-273.

Return to the Summary Table.

Table 1-273. REG_RX_9E Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	SERDES_EQ_CTL2	R/W	0x1	1: Disable 0: Enable
4	RESERVED	R/W	0x0	Reserved
3:0	RESERVED	R/W	0x0	Reserved

1.3.14 REG_RX_A8 Register (Address = 0xA8) [Default = 0x00]

REG_RX_A8 is shown in Table 1-274.

Return to the Summary Table.

Table 1-274. REG_RX_A8 Register Field Descriptions

Bit	Field	Type	Default	Description
7	SERDES_EQ_MODE	R/W	0x0	Write 1
6	RESERVED	R/W	0x0	Reserved

Table 1-274. REG_RX_A8 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5:0	RESERVED	R	0x0	Reserved

1.3.15 REG_RX_A9 Register (Address = 0xA9) [Default = 0x23]

REG_RX_A9 is shown in Table 1-275.

Return to the Summary Table.

Table 1-275. REG_RX_A9 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5:0	SERDES_EQ_MAX	R/W	0x23	Write 0x23

1.3.16 REG_RX_AA Register (Address = 0xAA) [Default = 0x00]

REG_RX_AA is shown in Table 1-276.

Return to the Summary Table.

Table 1-276. REG_RX_AA Register Field Descriptions

Bit	Field	Type	Default	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SERDES_EQ_MIN	R/W	0x0	Write 0x0

1.3.17 REG_RX_F0 Register (Address = 0xF0) [Default = 0x40]

REG_RX_F0 is shown in Table 1-277.

Return to the Summary Table.

Table 1-277. REG_RX_F0 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0x0	Reserved
6	SERDES_EQ_OVERRIDE	R/W	0x1	Write 0
5	RESERVED	R/W	0x0	Reserved
4:0	RESERVED	R/W	0x0	Reserved

1.4 CSI2 Registers

Table 1-278 lists the memory-mapped registers for the CSI2 registers. All register offset addresses not listed in Table 1-278 should be considered as reserved locations and the register contents should not be modified.

Table 1-278. CSI2 Registers

Address	Acronym	Register Name	Section
0x92	CSIPLL_REG_1	CSIPLL_REG_1	Go

Complex bit access types are encoded to fit into small table cells. Table 1-279 shows the codes that are used for access types in this section.

Table 1-279. CSI2 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

Table 1-279. CSI2 Access Type Codes (continued)

Access Type	Code	Description
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

1.4.1 CSIPLL_REG_1 Register (Address = 0x92) [Default = 0x50]

CSIPLL_REG_1 is shown in Table 1-280.

Return to the Summary Table.

Table 1-280. CSIPLL_REG_1 Register Field Descriptions

Bit	Field	Type	Default	Description
7:4	CSI_TX_SPEED3	R/W	0x5	CSI_TX_SPEED3 This register selects the operating rate and CSI timing parameters for the CSI Transmitter. In addition to setting this field, the CSI_PLL_DIV register (0xC9) on the Main Page must also be programmed for the correct selection. 2.5G: 4'h4 1.6G: 4'h4 1.5G: 4'h4 1.2G: 4'h5 800M: 4'h5 400M: 4'h6
3:0	RESERVED	R/W	0x0	Reserved

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2022	*	Initial Release

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