EVM User's Guide: J722SXH01EVM

J722SXH01 Evaluation Module

Description

The J722SXH01EVM is a fully functional hardware platform built around the J722S/AM67x/TDA4VEN,/TDA4AEN vision and display processor, which includes scalable Arm® Cortex®-A53 performance, image signal processor (ISP) supporting up to 600MP/s, up to 4 tera-operations-per-second (TOPS) AI accelerator, along with embedded features such as triple high-definition display support, high-performance 3D-GPU, 4K video acceleration, and other extensive peripherals. The EVM is designed as a low cost, standalone test and development platform to provide users the basic resources to evaluate performance and develop software for the J722S/AM67x/TDA4VEN/TDA4AEN family of processors.

Get Started

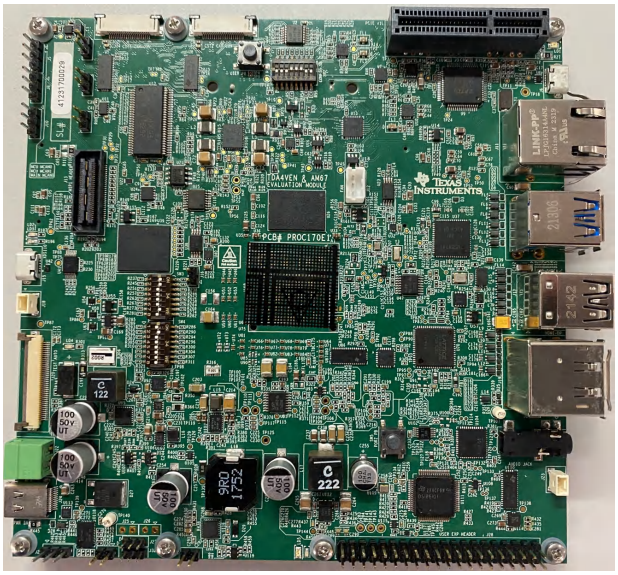
1. Order the EVM at J722SXH01EVM.
2. Download the EVM Design Files.
3. Download the software from J722SXH01EVM.
4. Read this user's guide.

Features

- Processing: Quad 64-bit Arm Cortex-A53 up to 1.4GHz, two ARM Cortex R5F single core up to 800MHz
- Display: dual panel support with up to 3840p x 1080p display resolution, one dual-channel LVDS and one MIPI®-DSI 4L. One HDMI™ connector from DPI/RGB88 and one DisplayPort connector from MIPI-DSI
- High speed interface: PCie card slot for Wi-Fi®, SDD, or other modules; one RJ-45 Ethernet 1000Mbps or 100Mbps with TSN support
- Connectivity: three Type-A USB3.0, one Type-C dual-role device (DRD) supports USB booting, onboard XDS110 Joint Action Group (JTAG) emulator, four universal asynchronous receiver-transmitters (UARTs) via USB2.0-B
- Storage: 8GB LPDDR4, 32GB eMMC; 512MB Octal Flash; bootable interfaces on EVM include removable microSD, eMMC, Octal Serial NOR/NAND flash, Ethernet, UART
- Security capable (Secure boot, Arm® TrustZone®, cryptography)
- Software: TI processor SDK Linux®, RT-Linux, RTOS MCU+ SDK, QNX SDK, out-of-box demos including Android®

Applications

- Automotive and industrial
  - Automotive front camera systems
  - Automotive surround view and park assistance systems
  - Industrial HMI
  - Robot teach pendant



1 Evaluation Module Overview

1.1 Introduction

The J722SXH01EVM contains a variety of both on-board peripherals and external interfaces, giving customers the flexibility to customize the platform tailored to the needs. This design is not a reference design, as the design includes circuity for software development/debug and configuration flexibility. However, some portions of the design are optimized and can be considered as reference. The J722SXH01EVM EVM supports multiple feature-rich software development kits (SDK) not covered in this user's guide. This technical user's guide describes how to use the hardware as well as some of the architecture and design elements of the EVM.

J722SXH01EVM includes multiple display connectors that enable supporting up to three screens, up to four mobile industry processor interface (MIPI) CSI-2 camera connectors, a PCIe card slot connector for Wi-Fi®, Solid State Drive (SSD), or other modules, one Gigabit Ethernet port, four USB 3.0 ports, and UART to USB circuit for debut output.

The J722SXH01EVM supports Linux® and FreeRTOS™ development with a feature-rich software development kit (SDK). On-chip emulation logic allows for emulation and debugging using standard development tools such as the Code Composer Studio™ integrated development environment (IDE) (CCSTUDIO) as well as an intuitive out-of-box user's guide to quickly start design evaluation.

1.2 Kit Contents

The EVM orderable part number is: J722SXH01EVM. This kit includes:

- J722SXH01EVM EVM
- Micro-SD Card (blank)
- USB cable: Type-A to Micro-B (used for emulation/terminal)
- USB cable: Type-A to Type-C
- EVM user's guide pamphlet
- EVM disclaimer and standard terms

The EVM is powered from a Type-C power supply, but the power supply is not included. For more information on the types of supplies recommended with the EVM, see Section 2.3.

1.3 Device Information

Many different devices and technologies are used to create this EVM. The list below details some key Texas Instruments devices included on this design and links to get additional information.

Function	Device Info
Processor, SoC	TDA4VEN-Q1, TDA4AEN-Q1, AM67
Power management, SoC	TPS6522311-Q1
Power regulator, SoC	TPS62875-Q1
Audio Codec	TLV320AIC3106, TLV320AIC3106-Q1
CAN-FD Bus transceiver	TCAN1462V-Q1
DisplayPort Bridge	SN65DSI86, SN65DSI86-Q1
Emulator (XDS110)	TM4C1294NCPDT
Ethernet PHY, Gb	DP83867E
IO expansion	TCA6424A
Power monitor	INA226, INA226-Q1
Power regulator (12V, 3V3)	LM5141, LM5141-Q1
Power regulator (5V)	LM61480, LM61480-Q1
Temperature sensor	TMP100, TMP100-Q1
USB Hub controller	TUSB8041, TUSB8041-Q1
USB Power controller	TPS25750
USB Type-C controller	TUSB321

1.4 Specification

The figure below shows the functional block diagram of the EVM.

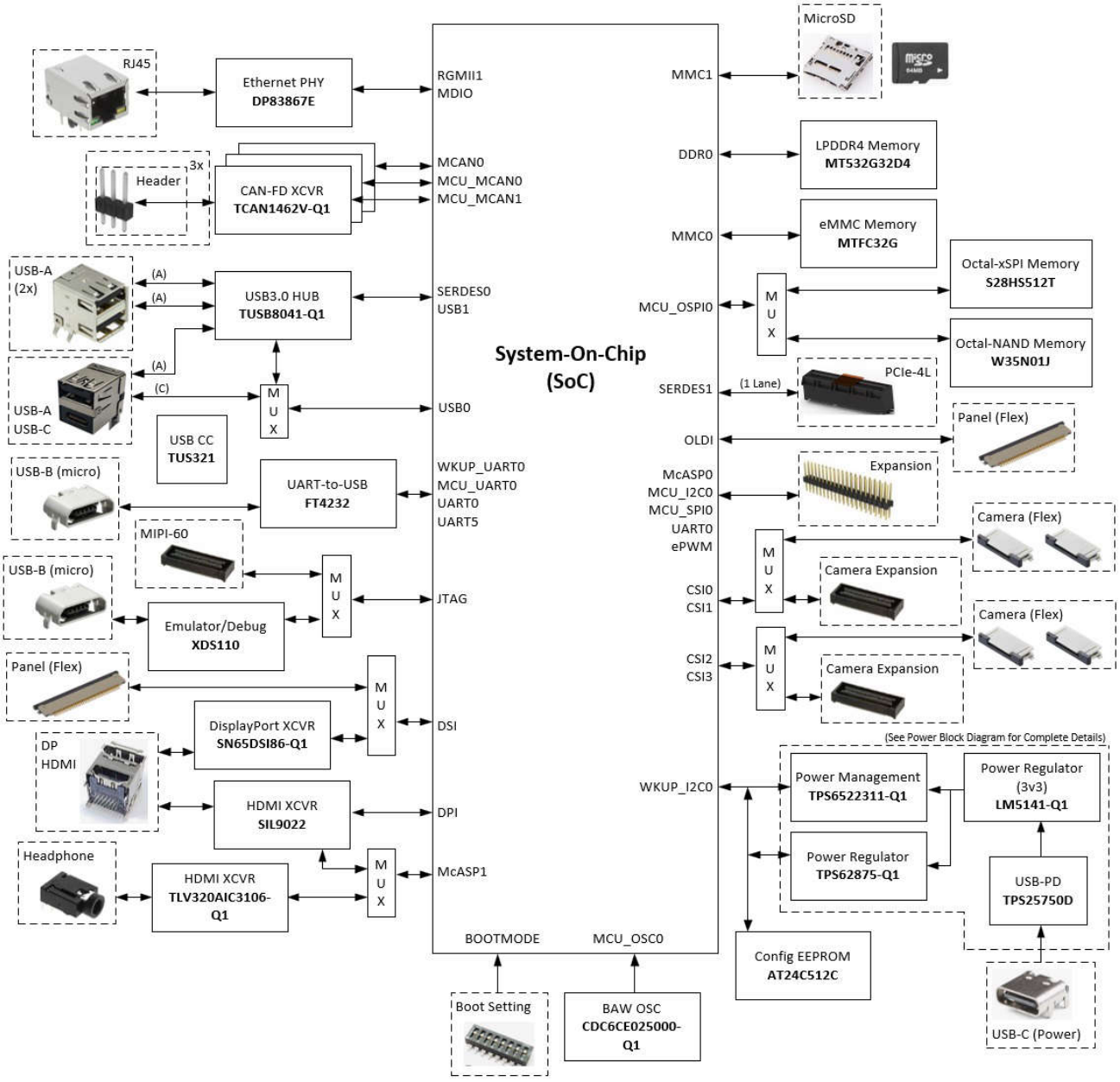


Figure 1-1. J722SXH01EVM Block Diagram

2 Hardware

2.1 Key Features and Interfaces

The J722SXH01EVM is a high performance, standalone development platform that enables users to evaluate and develop automotive and industrial applications using the Texas Instruments' J722S/AM67x/TDA4VEN/TDA4AEN processor. A summary of the EVM features include:

- Processor (also referred to as SoC or System-on-Chip)
  - Texas Instruments' J722S Super-Set device
- Optimized power management design
  - Multiple low power modes (IO retention, DDR retention)
  - Multiple clock and power domains.
- Memory
  - 8GByte LPDD4 DRAM (supports data rate up to 4000Mb/s)
  - 32GByte eMMC, version 5.1 compliant
  - 512Mb serial flash, Octal-NOR
  - 512Mb serial flash, Octal-NAND
  - Micro SD card cage with UHS-1 support
- Development
  - Multiple boot options and configurations
  - Integrated Emulation/Debugger (XDS110) with optional external support
  - Integrated power measurement
  - Multiple serial ports for terminals/logging
  - Multiple user defined input/outputs
- Interfaces
  - Audio headset plus microphone, 3.5mm
  - Up to four camera inputs, MIPI-CSI2, 22pin flex cable
  - HDMI display (supports up to 1080p and UXGA)
  - DisplayPort display (supports up to 1080p)
  - PCIe Gen3 card Slot, 4 Lane (only 1L supported)
  - USB2.0 Type-C interface with support for DFP, UFP, and DRP
  - Up to 4 USB3.0 Type-A/C Host Interfaces
  - Wired Ethernet interface, RJ45 (supports data rates up to 1Gbps)
  - Up to three Wired CAN-Bus Interfaces (supports data rates up to 8Mbps)
- Expansion/user add-on
  - 40 pin header (supports I2C, SPI, UART, I2S, PWM, GPIO)
  - Camera expansion (supports four CSI2-4L, I2C, GPIO)

The EVM images identify the locations of these key features and user interfaces (top and bottom view).

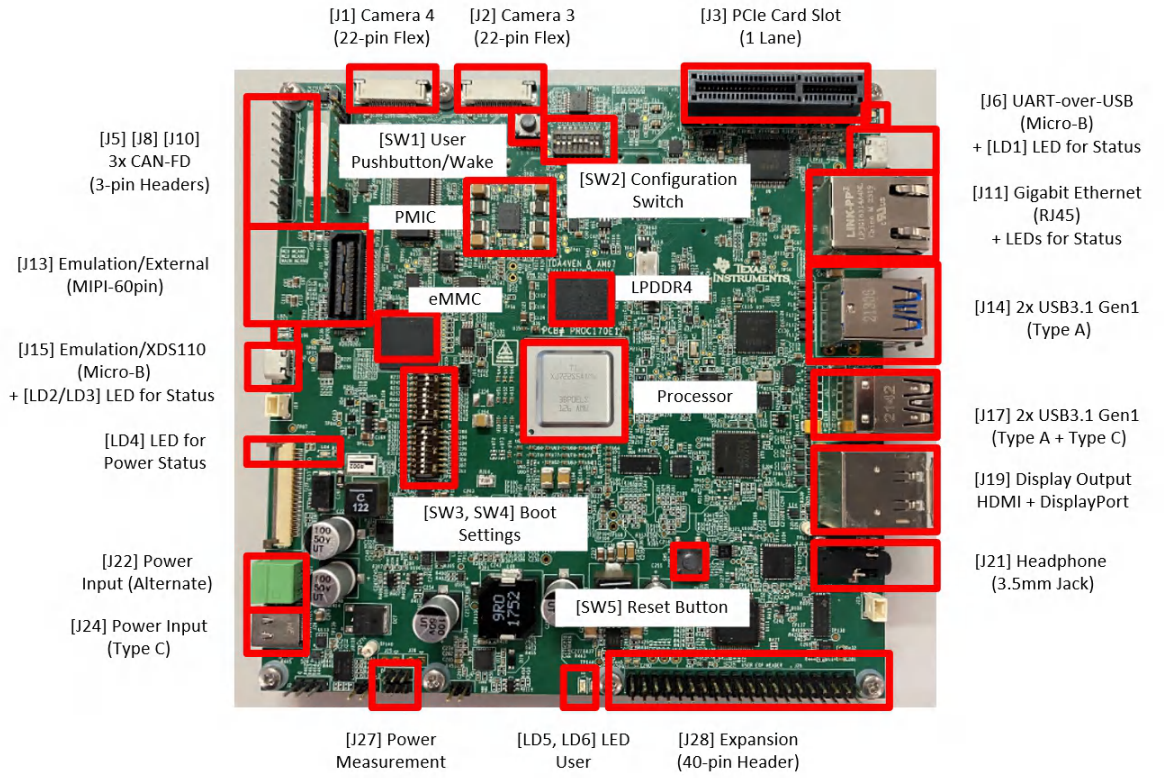


Figure 2-1. Key Features and Interfaces (Top)

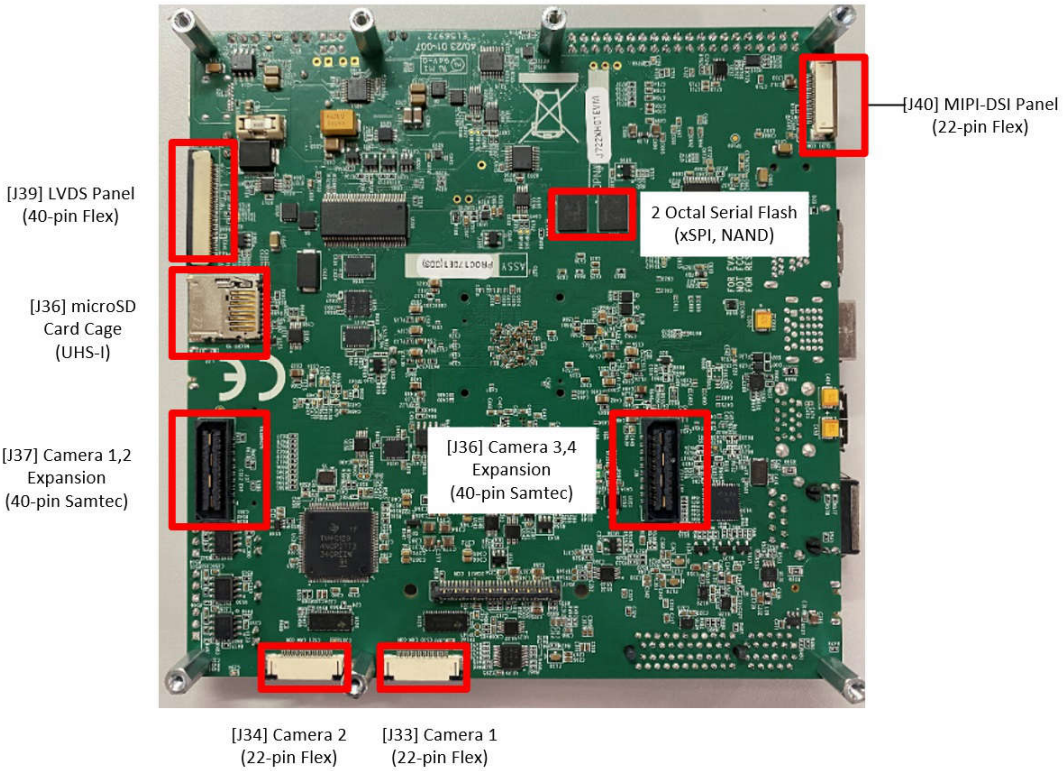


Figure 2-2. Key Features and Interfaces (Bottom)

2.2 Power On/Off Procedure

The below procedure is a brief summary of the steps required to power on and off the EVM. For more in-depth information, please refer to follow-on sections of this guide.

Power ON Procedure

1. Set the boot dip switches of the EVM (SW3, SW4) to the desired boot mode. See Section 2.4.1 for additional information on how to configure the boot mode of the EVM. By default, switches must be set to boot from MicroSD card.
2. Connect the boot media (if applicable).
3. Attach the USB-C® power supply cable to the power input connector (J24) of the EVM. See Section 2.3 for additional information on power supply requirements.
4. Connect the USB-C power supply to power source (AC power outlet or other).
5. Visually inspect the power LED (LD4) is illuminated (color red).

Power OFF Procedure

1. Disconnect your USB-C power supply from power source (AC power outlet or other).
2. Remove the USB-C power supply cable from the EVM (J24).

Power DOWN Procedure

1. With the EVM powered ON, press and hold the *RESET* button (SW5) for approximately 5 seconds.
2. Visually inspect the power LED (LD4) is not illuminated (color red).
3. To wake the EVM (from power down), press and release the *USER* button (SW1). Visually inspect the power LED (LD4) is illuminated (color red).

2.3 Power Input

A power supply is not included with the EVM and must be purchased separately. The requirements for the external power supply/accessory are:

- USB-C with Power Delivery (PD) compliance
- Nominal Output Voltage: 5-20VDC
- Minimum Output Current: 3000mA
- Efficiency Level V

Note

TI recommends using an external power supply or power accessory that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, and so forth.

There are many USB Type C power supply manufactures and models available in the market, but testing the EVM with every combination Is not possible. The table below lists several recommended supplies tested with the EVM.

Table 2-1. Recommended External Power Supply

Manufacturer	Part #/Model #	Description	Ordering Information
GlobTek, Inc.	TR9CZ3000USBCG2R6BF2	AC/DC DESKTOP ADAPTER 5V-20V 60W	1939-1794-ND [Digikey part#]
Qualtek	QADC-65-20-08CB	AC/DC DESKTOP ADAPTER 20V 65W	Q1251-ND [Digikey part#]

2.3.1 Power Input

The dedicated power input connector is a USB Type C connector [J24] with Power Delivery 3.0 support. The input can accept wide range of input voltages (5V to 20V). The exact power required for the EVM is largely dependent on the application and the connected peripherals. The recommended supplies are listed in Section 2.3. These supplies are 20V Type C supplies capable of supplying up to 60W of power (20VDC at 3A). However, a 60W supply can limit available processing with processor or limit some of the available peripherals. USB and PCIe peripherals can require significant power and the reason the higher wattage supply can be required.

A red LED [LD4] is illuminated to indicate an active power supply is connected and on-board regulators are active.

2.3.2 Power Budget Considerations

The exact power required for the EVM is largely dependent on the application, usage of the on-board peripherals, and power needs of add-on devices. The table below shows the power estimates the EVM can support. Again, the input supply must be capable of supplying the power needs for your application and your connected peripherals.

Table 2-2. Power Supply Allocation

Function	Power	Description
Processor core	Up to 15W	Processor, Memory
On-board peripherals	Up to 3W	SD card, Ethernet, Logic
USB ports	Up to 22W	USB Hub Type A Ports (2.8A at 5V) Type C Port (1.5A at 5V)
PCIe port	Up to 25W	PCIe Card Slot (2A at 12V, 3A at 3.3V)
Camera ports	Up to 3W	Cam Ports (1A at 3.3V)
Displays	Up to 3W	DP, HDMI Transceivers HDMI Panel (55mA at 5V) DP Panel (0.5A at 3.3V)
Expansion interfaces	Up to 15W	40p Expansion (2A at 3.3V, 1.5A at 5V)

2.4 User Inputs and Settings

The EVM supports several mechanisms for the user to configure, control, and provide input to the system.

2.4.1 Boot Configuration Settings

The boot mode for the EVM is defined by two banks of dip switches [SW3, SW4]. These switch settings are mapped directly to the BOOTMODE pins of the processor. See the technical reference manual (TRM) of the processor for a complete definition of all supported boot modes.

Note

An OFF setting provides a logic low level ('0') and an ON setting provides a logic high level ('1'). The Test Automation Interfaces provides capability to over-ride these switch settings, but that advanced feature not discussed in this manual.

As shown in the diagram, the BOOTMODE order is reversed from the Dip Switch assignment. For example, BOOTMODE [2:0] selects the PLL configuration. The EVM uses a 25Mhz clock source, thus BOOTMODE [2:0] must be set to '011'. Dip switch SW3[1:3] must be set to ON-ON-OFF or ‘110’ (order reversed).

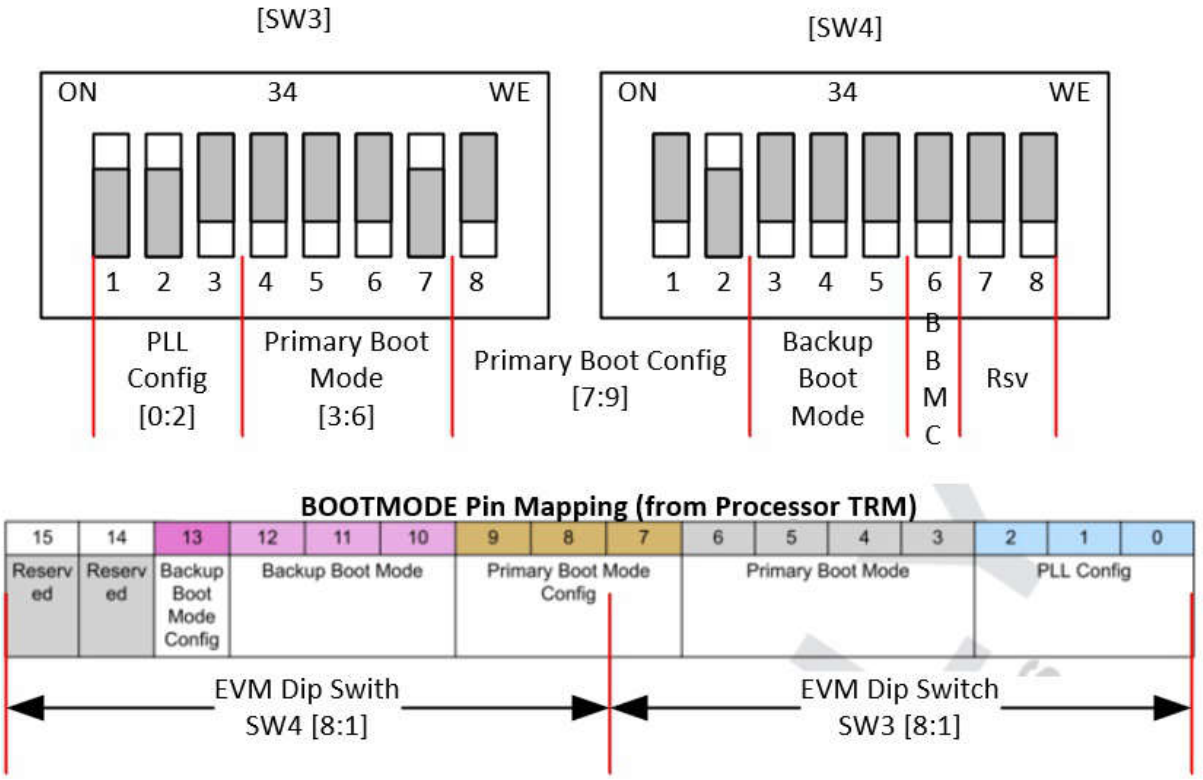


Figure 2-3. Dip Switch [SW3, SW4] Mapping to BOOTMODE

The default setting of the EVM is configured for Micro SD card boot. The boot settings are:

SW3[1:8] = 1100 0010 and SW4[1:8] = 0100 0000

Another common boot configuration is No-Boot. This is used when downloading code using an emulator/ XDS110. That boot settings is:

SW3[1:8] = 1101 1111 and SW4[1:8] = 0000 0000

Other boot modes such as eMMC, Serial Flash, USB, Ethernet, and UART are supported. Please refer to processor's TRM for specific settings and complete list of supported modes.

Table 2-3. Processor Bootmode Settings [SW2 Switch 1-3]

Processor Boot Source	SW2.1	SW2.2	SW2.3
MicroSD Card [J32]	OFF	OFF	OFF
Non-Volatile Flash (xSPI)	OFF	OFF	ON
eMMC	ON	ON	OFF
Reserved	OFF	ON	ON
UART (for Flashing)	ON	OFF	ON
No Boot (JTAG/Emulator)	ON	OFF	OFF
Ethernet[J10]	OFF	ON	OFF

2.4.2 Board Configuration Settings

Dip switch [SW2] is used to configure different options available on the EVM. The table below lists each switch and the assigned function and definition.

Table 2-4. Board Configuration Settings [SW2]

[SW2] Position	Function	Description
SW2.1	Serial flash memory selection	(OFF) = xSPI NOR Memory is selected (default) (ON) = Octal-NAND is selected
SW2.[2:3]	USB Type C mode selection	(OFF, OFF) = DRP / Dual Role Port (default) (OFF, ON) = DFP / Downstream Facing Port (ON, OFF) = UFP / Upstream Facing Port
SW2.4	Camera IO voltage selection	(OFF) = IO Levels are set to 1.8V (ON) = IO Levels are set to 3.3V (default) Voltage levels of CSI2-RX signals is defined by MIPI specification.
SW2.5	Watchdog disable	(OFF) = Watchdog is enabled (ON) = Watchdog is disabled (default)
SW2.6	Configuration EEPROM protection	(OFF) = EEPROM is NOT write-protected (ON) = EEPROM is write-protected (default)
SW2.[7:8]	Reserved and Test mode	(OFF, OFF) = Normal EVM operation (default)

2.4.3 Reset Pushbutton

When pressed [SW5], the EVM is issued a Power-On (Cold) Reset, and is held in reset until the button is released.

If the pushbutton is held longer than 5 seconds, then the system powers down. The system can be restarted by either pressing the User Pushbutton [SW1] or by cycling power to the board.

2.4.4 User Pushbutton And LEDs

The pushbutton [SW1] can be used for several different functions.

Function 1: User Defined Input/Interrupt. The pushbutton [SW1] is connected with the processor (MCU_GPIO0_11), and can be programmed for variety of user input/interrupt needs.

Function 2: System Wake from Powerdown. Power down can be either software-initiated power down (using GPIO1_30) or from pressing/holding reset pushbutton [SW5].

A green LED [LD5] and red LED [LD6] are available as user indicators, and can be programmed for a variety of user output needs. Green LED [LD5] is controlled using IO Expander. Red LED [LD6] is controlled using processor GPIO1_49.

Refer to Section 2.7.3 and Section 2.7.4 tables for IO definitions and programming specifics.

2.5 Standard Interfaces

The EVM provides industry standard interfaces/connectors to provide access to a wide variety of peripherals. As these interfaces are standard, specific pin information is not provided in this document.

2.5.1 Audio Input/Output

The EVM supports stereo headset audio via a 3.5mm audio jack [J21]. Texas Instruments TLV320AIC3106 provides the audio conversions (DAC and ADC). The audio output conversion supports sampling rates of 8KHz to 96KHz. The audio input includes pre-amp and automatic gain control. The audio codec also integrates the headphone driver and microphone bias circuits.

2.5.2 DisplayPort and HDMI

The EVM supports up to three display outputs, two of which are supported on standard display interfaces. The 3rd interface (LVDS) is supported on a expansion interface, and is defined in more detail in Section 2.6.

DisplayPort panels are supported via standard DP cable interface [J19]. The interface supports resolutions to 1080p (1920x1080). HDMI panels are supported via standard HDMI connector [J19], and supports resolutions up to 1080p (1920x1080) and UXGA (1600x1200). Both DisplayPort and HDMI interfaces can be used simultaneously with stacked DP/HDMI connector [J19].

2.5.3 Gigabit Ethernet

A wired Ethernet network is supported via RJ45 cable interface [J11], and is compatible with IEEE 802.3 10BASETe,100BASE-TX, and 1000BASE-T specifications. The connector includes status indicators for link and activity.

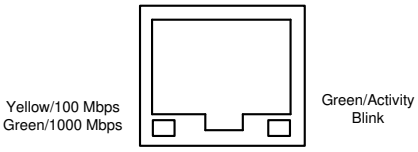


Figure 2-4. RJ45 LED Indicators [J11]

Power-Over-Ethernet (PoE) is not supported. The Ethernet PHY supported on the EVM is Texas Instruments DP83867E.

2.5.4 JTAG and Emulation

The EVM supports an integrated XDS110 emulator for loading and debugging software. The USB micro-B connector [J15] of the EVM is connected to a Host-PC using supplied USB cable (Type-A to Micro-B).
The computer can use Texas Instruments' Code Composer Studio (CCS) to establish a connection with the processor and download and debug software on the various processor cores. The emulator circuit is powered via USB VBUS power. LEDs [LD2] [LD3] are used to indicate an active connection with Host-PC/processor. The green LED [LD3] indicates USB connection with Host-PC and the red LED [LD2] indicates processor connection with CCS.

Optionally, an external JTAG emulation/debugger can connect using a dedicated emulation connector [J13]. The connector is aligned with the MIPI 60-pin Emulator standard and expands the debug capability to include TRACE support. Several different Texas Instruments' emulators can be used, including XDS560v2, XDS110, and XDS200. Note that some can require 3rd party adapters for interfacing with the MIPI-60 connector.

Selection between the on-board and external emulator is done automatically, while switching to external emulator is only when connection is made to the MIPI-60 connector [J13].

2.5.5 MicroSD Card Cage

The EVM supports a micro-SD card cage [J36]. The EVM supports UHS-1 class memory cards, including SDHC and SXDC. The connector is a PUSH-PUSH connector, meaning you push to insert the card and push again to remove the card.

A MicroSD Card (blank) is included with the EVM.

2.5.6 PCIe Card Module

The EVM supports a PCIe Gen3 card slot [J3] for supporting full size PCIe cards. The slot accepts up to 4-Lane cards, but only 1-Lane of communication is supported. This expansion interface is used for a wide variety of peripherals, and supports the following interfaces: PCIe (1L) and I2C.

The EVM can supply up to 25W to the PCIe card [J3], which complies with the PCIe specification.

2.5.7 UARTs for Terminal and Logging

Four UARTs ports are provided for terminal and logging functions using a UART-over-USB transceiver. When the USB micro-B connector (J6) of the EVM is connected to a Host-PC using supplied USB cable (Type-A to Micro-B), the computer can establish Virtual Com Ports which can be used with any terminal emulation application. Virtual Com Port drivers for the transceiver (FT4232HL) can be obtained from FTDI Chip.

Depending on the other Host-PC resources available, the Virtual COM Ports are not located at COM1-4. However, the ports remain in the same numerical order.

Table 2-5. UART to COM Port Mapping

Processor UART	Host-PC COM Port
WKUP_UART0	COM 1
MCU_UART0	COM 2
UART0	COM 3
UART5	COM 4

The circuit is powered through BUS power, therefore the COM connection is not lost when the EVM power is removed. An LED [LD1] is used to indicate an active COM connection with Host-PC.

2.5.8 USB Interfaces

The EVM supports up to four USB3.0 Gen1 interfaces, three Type A ports [J14][J17] plus one USB3.0 Gen1 port on the Type C port [J17]. The USB3.0 ports are connected to on-board USB hub (TUSB8041) and support only DFP mode. The Type C port [J17] has option (and defaults) to support USB2.0 multiple roles (DFP/UFP/DRP). This provides support for the USB boot modes of the processor. Refer to Section 2.7.4 tables for programming specifics on configuration and selection of the Type C connector.

The combined VBUS output for the Type A ports is limited to 2.8A. The VBUS output for the Type C port is limited to 1.5A. The EVM cannot be powered from these ports.

2.6 Expansion Interfaces

The EVM supports expansion interfaces that have non-standard/custom pinouts. Each of those interfaces are introduced and specific pin information is provided.

2.6.1 Camera Interface, 22-Pin Flex

The EVM supports four 22-pin flex (0.5mm pitch) connectors [J1][J2] [J33] [J34] for interfacing with camera modules. Each camera interface provides MIPI CSI-2 interface (4 lanes), clock or control signals, and power (3.3V) to the camera. The camera interfaces are shared/multiplexed between the 22-pin flex connectors and the 40-pin high speed expansion. See Section 2.7.4 for details on selection control.

To enable identical camera modules to be used simultaneously, I2C mux is used to select each camera (TCA9543). The voltage level for Clock/Control signals is selectable between 1.8V and 3.3V. See Section 2.7.4 for details.

Table 2-6. Camera Flex Pin Definition [J1]

Pin #	Pin Name	Description	Dir
1	GND	Ground	Output
2	CSI3_D0_N	CSIPort 3 Data Lane 0	Input
3	CSI3_D0_P	CSIPort 3 Data Lane 0	Input
4	GND	Ground	
5	CSI3_D1_N	CSIPort 3 Data Lane 1	Input
6	CSI3_D1_P	CSIPort 3 Data Lane 1	Input
7	GND	Ground	
8	CSI3_CLK_N	CSIPort 3 CLK	Input
9	CSI3_CLK_P	CSIPort 3 CLK	Input
10	GND	Ground	

Table 2-6. Camera Flex Pin Definition [J1] (continued)

Pin #	Pin Name	Description	Dir
11	CSI3_D2_N	CSIPort 3 Data Lane 2	Input
12	CSI3_D2_P	CSIPort 3 Data Lane 2	Input
13	GND	Ground	
14	CSI3_D3_N	CSIPort 3 Data Lane 3	Input
15	CSI3_D3_P	CSIPort 3 Data Lane 3	Input
16	GND	Ground	
17	CAM_PWDN	GPIO, typically used for Pwr-Dwn (See GPIO Table)	Bi-Dir
18	CAM_AUX	GPIO, typically used for AUX (See GPIO Table)	Bi-Dir
19	GND	Ground	
20	I2C_SCL	I2C Clock, TCA9543 Port 1 (See I2C Table)	Output
21	I2C_SDA	I2C Data, TCA9543 Port 1 (See I2C Table)	Bi-Dir
22	Power	Power, 3.3V	Output

Table 2-7. Camera Flex Pin Definition [J2]

Pin #	Pin Name	Description	Dir
1	GND	Ground	Output
2	CSI2_D0_N	CSIPort 2 Data Lane 0	Input
3	CSI2_D0_P	CSIPort 2 Data Lane 0	Input
4	GND	Ground	
5	CSI2_D1_N	CSIPort 2 Data Lane 1	Input
6	CSI2_D1_P	CSIPort 2 Data Lane 1	Input
7	GND	Ground	
8	CSI2_CLK_N	CSIPort 2 CLK	Input
9	CSI2_CLK_P	CSIPort 2 CLK	Input
10	GND	Ground	
11	CSI2_D2_N	CSIPort 2 Data Lane 2	Input
12	CSI2_D2_P	CSIPort 2 Data Lane 2	Input
13	GND	Ground	
14	CSI2_D3_N	CSIPort 2 Data Lane 3	Input
15	CSI2_D3_P	CSIPort 2 Data Lane 3	Input
16	GND	Ground	
17	CAM_PWDN	GPIO, typically used for Pwr-Dwn (See GPIO Table)	Bi-Dir
18	CAM_AUX	GPIO, typically used for AUX (See GPIO Table)	Bi-Dir
19	GND	Ground	
20	I2C_SCL	I2C Clock, TCA9543 Port 0 (See I2C Table)	Output
21	I2C_SDA	I2C Data, TCA9543 Port 0 (See I2C Table)	Bi-Dir
22	Power	Power, 3.3V	Output

Table 2-8. Camera Flex Pin Definition [J33]

Pin #	Pin Name	Description	Dir
1	GND	Ground	Output
2	CSI0_D0_N	CSIPort 0 Data Lane 0	Input
3	CSI0_D0_P	CSIPort 0 Data Lane 0	Input
4	GND	Ground	
5	CSI0_D1_N	CSIPort 0 Data Lane 1	Input
6	CSI0_D1_P	CSIPort 0 Data Lane 1	Input
7	GND	Ground	
8	CSI0_CLK_N	CSIPort 0 CLK	Input
9	CSI0_CLK_P	CSIPort 0 CLK	Input
10	GND	Ground	
11	CSI0_D2_N	CSIPort 0 Data Lane 2	Input
12	CSI0_D2_P	CSIPort 0 Data Lane 2	Input
13	GND	Ground	
14	CSI0_D3_N	CSIPort 0 Data Lane 3	Input
15	CSI0_D3_P	CSIPort 0 Data Lane 3	Input
16	GND	Ground	
17	CAM_PWDN	GPIO, typically used for Pwr-Dwn (See GPIO Table)	Bi-Dir
18	CAM_AUX	GPIO, typically used for AUX (See GPIO Table)	Bi-Dir
19	GND	Ground	
20	I2C_SCL	I2C Clock, TCA9543 Port 0 (See I2C Table)	Output
21	I2C_SDA	I2C Data, TCA9543 Port 0 (See I2C Table)	Bi-Dir
22	Power	Power, 3.3V	Output

Table 2-9. Camera Flex Pin Definition [J34]

Pin #	Pin Name	Description	Dir
1	GND	Ground	Output
2	CSI1_D0_N	CSIPort 1 Data Lane 0	Input
3	CSI1_D0_P	CSIPort 1 Data Lane 0	Input
4	GND	Ground	
5	CSI1_D1_N	CSIPort 1 Data Lane 1	Input
6	CSI1_D1_P	CSIPort 1 Data Lane 1	Input
7	GND	Ground	
8	CSI1_CLK_N	CSIPort 1 CLK	Input
9	CSI1_CLK_P	CSIPort 1 CLK	Input
10	GND	Ground	
11	CSI1_D2_N	CSIPort 1 Data Lane 2	Input
12	CSI1_D2_P	CSIPort 1 Data Lane 2	Input
13	GND	Ground	
14	CSI1_D3_N	CSIPort 1 Data Lane 3	Input
15	CSI1_D3_P	CSIPort 1 Data Lane 3	Input
16	GND	Ground	
17	CAM_PWDN	GPIO, typically used for Pwr-Dwn (See GPIO Table)	Bi-Dir
18	CAM_AUX	GPIO, typically used for AUX (See GPIO Table)	Bi-Dir
19	GND	Ground	
20	I2C_SCL	I2C Clock, TCA9543 Port 1 (See I2C Table)	Output

Table 2-9. Camera Flex Pin Definition [J34] (continued)

Pin #	Pin Name	Description	Dir
21	I2C_SDA	I2C Data, TCA9543 Port 1 (See I2C Table)	Bi-Dir
22	Power	Power, 3.3V	Output

2.6.2 Camera Interface, 40-Pin Expansion

The EVM includes two 40-pin (2x20, 2.54mm pitch) high speed camera interface expansion connectors [J36] [J37]. Each expansion connector supports two MIPI CSI-2 (4 lanes each), power, and control signals (I2C, GPIO, and so forth). The camera expansion interfaces are shared or multiplexed between the 40-pin high speed expansion and the 22-pin flex connectors and. See Section 2.7.4 for details on selection control.

To enable identical camera modules to be used simultaneously, I2C mux is used to select each camera (TCA9543). The voltage level for Clock/Control signals is selectable between 1.8V and 3.3V. See Section 2.7.4 for details.

Table 2-10. 40-Pin High-Speed Camera Expansion Pin Definition [J36]

Pin #	Pin Name	Description (Processor Pin #)	Dir
1	Power	Input Power Dependent (5V-20V)	Output
2	I2C_SCL	I2C Clock, TCA9543 Port 0 (See I2C Table)	Bi-Dir
3	Power	Input Power Dependent (5V-20V)	Output
4	I2C_SDA	I2C Data, TCA9543 Port 0 (See I2C Table)	Bi-Dir
5	CSI2_CLK_P	CSIPort 2 Clock	Input
6	GPIO/PWMA	GPIO, See GPIO Table	Bi-Dir
7	CSI2_CLK_N	CSIPort 2 Clock	Input
8	GPIO/PWMB	GPIO, See GPIO Table	Bi-Dir
9	CSI2_D0_P	CSIPort 2 Data Lane 0	Input
10	REFCLK	25MHz Clock Source	Output
11	CSI2_D0_N	CSI Port 2 Data Lane 0	Input
12	GND	Ground	
13	CSI2_D1_P	CSI Port 2 Data Lane 1	Input
14	RESETz	Reset, See GPIO Table	Output
15	CSI2_D1_N	CSI Port 2 Data Lane 1	Input
16	GND	Ground	
17	CSI2_D2_P	CSI Port 2 Data Lane 2	Input
18	GPIO	GPIO, See GPIO Table	Bi-Dir
19	CSI2_D2_N	CSI Port 2 Data Lane 2	Input
20	GPIO	GPIO, See GPIO Table	Bi-Dir
21	CSI2_D3_P	CSI Port 2 Data Lane 3	Input
22	GPIO	GPIO, See GPIO Table	Bi-Dir
23	CSI2_D3_N	CSI Port 2 Data Lane 3	Input
24	GND	Ground	
25	CSI3_CLK_P	CSI Port 3 Clock	Input
26	CSI3_D3_P	CSI Port 3 Data Lane 3	Input
27	CSI3_CLK_N	CSI Port 3 Clock	Input
28	CSI3_D3_N	CSI Port 3 Data Lane 3	Input

Table 2-10. 40-Pin High-Speed Camera Expansion Pin Definition [J36] (continued)

Pin #	Pin Name	Description (Processor Pin #)	Dir
29	CSI3_D0_P	CSI Port 3 Data Lane 0	Input
30	Power	Power, 3.3V	Output
31	CSI3_D0_N	CSI Port 3 Data Lane 0	Input
32	Power	Power, 3.3V	Output
33	CSI3_D1_P	CSI Port 3 Data Lane 1	Input
34	Power	Power, 3.3V	Output
35	CSI3_D1_N	CSI Port 3 Data Lane 1	Input
36	Power	Power, 3.3V	Output
37	CSI3_D2_P	CSI Port 3 Data Lane 2	Input
38	Power	Power, IO Level (1.8 or 3.3V)	Output
39	CSI3_D2_N	CSI Port 3 Data Lane 2	Input
40	Power	Power, IO Level (1.8 or 3.3V)	Output

Table 2-11. 40-Pin High-Speed Camera Expansion Pin Definition [J37]

Pin #	Pin Name	Description (Processor Pin #)	Dir
1	Power	Input Power Dependent (5V-20V)	Output
2	I2C_SCL	I2C Clock, TCA9543 Port 0 (See I2C Table)	Bi-Dir
3	Power	Input Power Dependent (5V-20V)	Output
4	I2C_SDA	I2C Data, TCA9543 Port 0 (See I2C Table)	Bi-Dir
5	CSI0_CLK_P	CSIPort 0 Clock	Input
6	GPIO/PWMA	GPIO, See GPIO Table	Bi-Dir
7	CSI0_CLK_N	CSIPort 0 Clock	Input
8	GPIO/PWMB	GPIO, See GPIO Table	Bi-Dir
9	CSI0_D0_P	CSIPort 0 Data Lane 0	Input
10	REFCLK	25MHz Clock Source	Output
11	CSI0_D0_N	CSI Port 0 Data Lane 0	Input
12	GND	Ground	
13	CSI0_D1_P	CSI Port 0 Data Lane 1	Input
14	RESETz	Reset, See GPIO Table	Output
15	CSI0_D1_N	CSI Port 0 Data Lane 1	Input
16	GND	Ground	
17	CSI0_D2_P	CSI Port 0 Data Lane 2	Input
18	GPIO	GPIO, See GPIO Table	Bi-Dir
19	CSI0_D2_N	CSI Port 0 Data Lane 2	Input
20	GPIO	GPIO, See GPIO Table	Bi-Dir
21	CSI0_D3_P	CSI Port 0 Data Lane 3	Input
22	GPIO	GPIO, See GPIO Table	Bi-Dir
23	CSI0_D3_N	CSI Port 0 Data Lane 3	Input
24	GND	Ground	
25	CSI1_CLK_P	CSI Port 1 Clock	Input
26	CSI1_D3_P	CSI Port 1 Data Lane 3	Input
27	CSI1_CLK_N	CSI Port 1 Clock	Input

Table 2-11. 40-Pin High-Speed Camera Expansion Pin Definition [J37] (continued)

Pin #	Pin Name	Description (Processor Pin #)	Dir
28	CSI1_D3_N	CSI Port 1 Data Lane 3	Input
29	CSI1_D0_P	CSI Port 1 Data Lane 0	Input
30	Power	Power, 3.3V	Output
31	CSI1_D0_N	CSI Port 1 Data Lane 0	Input
32	Power	Power, 3.3V	Output
33	CSI1_D1_P	CSI Port 1 Data Lane 1	Input
34	Power	Power, 3.3V	Output
35	CSI1_D1_N	CSI Port 1 Data Lane 1	Input
36	Power	Power, 3.3V	Output
37	CSI1_D2_P	CSI Port 1 Data Lane 2	Input
38	Power	Power, IO Level (1.8 or 3.3V)	Output
39	CSI1_D2_N	CSI Port 1 Data Lane 2	Input
40	Power	Power, IO Level (1.8 or 3.3V)	Output

2.6.3 CAN-Bus Interface

The EVM supports three Controller Area Network (CAN) Bus interfaces [J5] [J8] [J10].

Table 2-12. CAN-FD Interface Assignment

Connector Ref	Processor Resource
J5	MCU_CAN0
J8	MCU_CAN1
J10	CAN0

Each CAN-FD interface is supported on a 3-pin, 2.54mm pitch header. The interface meets ISO 11898-2 and ISO 11898-5 physical standards, and supports CAN and optimized CAN-FD performance up to 8Mbps. Each includes CAN Bus end-point termination. If the EVM is included in a network with more than two nodes, then the termination needs to be adjusted.

Table 2-13. CAN-FD Interface Pin Definition [J5] [J8] [J10]

Pin #	Pin Name	Description	Dir
1	CAN_H	High level CAN Bus IO	Bi-Dir
2	GND	Ground	
3	CAN_L	Low level CAN Bus IO	Bi-Dir

2.6.4 DSI Display Interface

The EVM supports a 22-pin flex (0.5mm pitch) connector [J40] for interfacing with external display modules and panels. The interface provides MIPI DSI-2 interface (4 lanes), clock and control signals, and power (3.3V) to the panel. The DSI interface is shared and multiplexed between the 22-pin flex connectors and on-board DisplayPort transceiver. See Section 2.7.4 table for details on selection control.

Table 2-14. DSI Display Pin Definition [J40]

Pin #	Pin Name	Description	Dir
1	Power	Power, 3.3V	Output
2	I2C_SDA	I2C Data (I2C1)	Bi-Dir
3	I2C_SCL	I2C Clock (I2C1)	Output
4	GND	Ground	
5	GPIO1	GPIO, Undefined (See GPIO Table)	Bi-Dir
6	GPIO0	GPIO, Undefined (See GPIO Table)	Bi-Dir
7	GND	Ground	
8	DSI0_D3_P	DSIPort 0 Data Lane 3	Input
9	DSI0_D3_N	DSIPort 0 Data Lane 3	Input
10	GND	Ground	
11	DSI1_D2_P	DSIPort 0 Data Lane 2	Input
12	DSI1_D2_N	DSIPort 0 Data Lane 2	Input
13	GND	Ground	
14	DSI0_CLK_P	DSIPort 0 CLK	Input
15	DSI0_CLK_N	DSIPort 0 CLK	Input
16	GND	Ground	
17	DSI0_D1_P	DSIPort 0 Data Lane 1	Input
18	DSI0_D1_N	DSIPort 0 Data Lane 1	Input
19	GND	Ground	
20	DSI0_D0_P	DSIPort 0 Data Lane 0	Input
21	DSI0_D0_N	DSIPort 0 Data Lane 0	Input
22	GND	Ground	Output

2.6.5 OLDI/LVDS Display Interface

The EVM supports a 40-pin flex (0.5mm pitch) connector [J39] for interfacing with external display modules/ panels. The interface provides OLDI/LVDS capable of supporting a single link panel (up to 1920x720p) or dual link panel (up to 3840x1080p). Clock/Control signals, and power (3.3V) are also supported to the panel.

Table 2-15. OLDI/LVDS Display Pin Definition [J39]

Pin #	Pin Name	Description	Dir
1	GND	Ground	
2	CH2_LVDS_A3P	LVDS Channel #2 Data Lane 3	Output
3	CH2_LVDS_A3N	LVDS Channel #2 Data Lane 3	Output
4	GND	Ground	
5	CH2_LVDS_A2P	LVDS Channel #2 Data Lane 2	Output
6	CH2_LVDS_A2N	LVDS Channel #2 Data Lane 2	Output
7	GND	Ground	

Table 2-15. OLDI/LVDS Display Pin Definition [J39] (continued)

Pin #	Pin Name	Description	Dir
8	CH2_LVDS_CLKP	LVDS Channel #2 Clock Lane	Output
9	CH2_LVDS_CLKN	LVDS Channel #2 Clock Lane	Output
10	GND	Ground	
11	CH2_LVDS_A1P	LVDS Channel #2 Data Lane 1	Output
12	CH2_LVDS_A1N	LVDS Channel #2 Data Lane 1	Output
13	GND	Ground	
14	CH2_LVDS_A0P	LVDS Channel #2 Data Lane 0	Output
15	CH2_LVDS_A0N	LVDS Channel #2 Data Lane 0	Output
16	GND	Ground	
17	CH1_LVDS_A3P	LVDS Channel #1 Data Lane 3	Output
18	CH1_LVDS_A3N	LVDS Channel #1 Data Lane 3	Output
19	GND	Ground	
20	CH1_LVDS_A2P	LVDS Channel #1 Data Lane 2	Output
21	CH1_LVDS_A2N	LVDS Channel #1 Data Lane 2	Output
22	GND	Ground	
23	CH1_LVDS_CLKP	LVDS Channel #1 Clock Lane	Output
24	CH1_LVDS_CLKN	LVDS Channel #1 Clock Lane	Output
25	GND	Ground	
26	CH1_LVDS_A1P	LVDS Channel #1 Data Lane 1	Output
27	CH1_LVDS_A1N	LVDS Channel #1 Data Lane 1	Output
28	GND	Ground	
29	CH1_LVDS_A0P	LVDS Channel #1 Data Lane 0	Output
30	CH1_LVDS_A0N	LVDS Channel #1 Data Lane 0	Output
31	GND	Ground	
32	Interrupt	GPIO, typically used as Interrupt (See GPIO Table)	Bi-Dir
33	Reset	GPIO, typically used as reset (See GPIO Table)	Bi-Dir
34	GND	Ground	
35	GND	Ground	
36		open/not connected	
37		open/not connected	
38	I2C_SDA	I2C Data (I2C1)	Bi-Dir
39	I2C_SCL	I2C Clock (I2C1)	Output
40	Power	Power, 3.3V	Output

2.6.6 User Expansion Header

The EVM includes a 40-pin (2x20, 2.54mm pitch) expansion interface [J28]. The expansion connector supports variety of interfaces including: I2C, serial peripheral interface (SPI), I2S with Audio clock, UART, pulse width modulator (PWM), and GPIO. All signals on the interfaces are 3.3V levels.

To help clarify connectivity between this interface and the processor, the table includes the pin location of the connected processor in parenthesis '( )'.

Table 2-16. Expansion Header Pin Definition [J28]

Pin #	Pin Name	Description (TDA4VM Pin #)	Dir
1	Power	Power,3.3 V	Output
2	Power	Power,5.0 V	Output
3	I2C_SDA	MCU I2CBus #0, Data (E11)	Bi-Dir
4	Power	Power,5.0 V	Output
5	I2C_SCL	MCU I2CBus #0, Clock (B13)	Bi-Dir
6	GND	Ground	
7	GP_CLK/GPIO	REFCLK2/GPIO0 #38 (W26)	Bi-Dir
8	UART_TXD	UART#1 Transmit (F24)	Output
9	GND	Ground	
10	UART_RXD	UART#1 Receive (C27)	Input
11	GPIO	UART#1 RST/GPIO1 #8 (A26)	Bi-Dir
12	I2S_SCLK	McASP #0 ACLKX (D25)	Bi-Dir
13	GPIO	GPIO0 #33 (N22)	Bi-Dir
14	GND	Ground	
15	GPIO	UART#1 CTS/GPIO1 #7 (A25)	Bi-Dir
16	GPIO	GPIO0#3 (B5)	Bi-Dir
17	Power	Power,3.3V	Output
18	GPIO	GPIO0#39 (N24)	Bi-Dir
19	SPI_PICO	MCU SPI#1 Data 0 (B12)	Bi-Dir
20	GND	Ground	
21	SPI_POCI	MCU SPI#1 Data 1 (C11)	Bi-Dir
22	GPIO	GPIO0#42 (P21)	Bi-Dir
23	SPI_SCLK	MCU SPI#1 Clock (A9)	Bi-Dir
24	SPI_CS0	MCU SPI #1 Chip Select 0 C12)	Bi-Dir
25	GND	Ground	
26	SPI_CS1	MCU SPI #1 Chip Select 1 (A10)	Bi-Dir
27	ID_SDA	WKUP I2C #0 Data (D11)	Bi-Dir
28	ID_SCL	WKUP I2C #0 Clock (B9)	Bi-Dir
29	GPIO	EHRPWM0_A/ GPIO1 #15 (B20)	Bi-Dir
30	GND	Ground	
31	GPIO	EHRPWM1_A/ GPIO1 #17 (D20)	Bi-Dir
32	PWM0	EHRPWM0_B/ GPIO1 #16 (C20)	Output
33	PWM1	EHRPWM1_B/ GPIO1 #18 (E19)	Output
34	GND	Ground	
35	I2S_FS	McASP #0 AFSX (C26)	Bi-Dir
36	GPIO	GPIO0#41 (R27)	Bi-Dir
37	GPIO	GPIO0#36 (P26)	Bi-Dir
38	I2S_DIN	McASP #0 AXR0 (F23)	Bi-Dir
39	GND	Ground	

Table 2-16. Expansion Header Pin Definition [J28] (continued)

Pin #	Pin Name	Description (TDA4VM Pin #)	Dir
40	I2S_DOUT	McASP #0 AXR1 (B25)	Bi-Dir

2.7 Circuit Details

This sections provides additional details on the EVM design and processor connections. The top level block diagram shows the overall connectivity of the EVM (Section 1.4).

2.7.1 Interface Mapping

The processor is provided in Table 2-17.

Table 2-17. Interface Mapping Table

Connected Peripheral	Processor Resources	Components / Part Numbers
Memory, LPDDR4 DRAM	DDR0	Micron MT53E2G32D4DE-046 AUT:C
Memory, eMMC Flash	MMC0	Micron MTFC32GAZAQHD-IT
Memory, xSPI NOR Flash	MCU_OSPI0	CypressS28HS512TGABHM010, Winbond W35N01JWTBAG
Micro-SDCard Cage	MMC1	
Audio	McASP1, I2C0	Texas Instruments TLV320AIC3106
CAN (3x)	MCU_MCAN0, MCU_MCAN1, MCAN0	Texas Instruments TCAN1462V
Camera connectors	CSI0,CSI1, CSI2, CSI3, I2C2	
Display port	DSI0, I2C1	Texas Instruments SN65DSI86
EEPROM, board identification	WKUP_I2C0	MicrochipTech AT24C512C
Expansion Header (40-pin)	McASP0, MCU_SPI0, UART1, MCU_I2C0, WKUP_I2C0	
HDMI	DPI0, McASP1, I2C1	Silicon Labs SIL9022ACNU
OLDI	OLDI0, I2C1	
PCIe	PCIe0, I2C0	
Power Measurement	I2C0	Texas Instruments INA226
UART Terminal	WKUP_UART0, MCU_UART0, UART0, UART5	FTDI FT4232HS
USB Type A (3x)	USB1, USB1_SS	Texas Instruments TUSB8041
USB Type C + CC Controller	USB0, USB1	Texas Instruments TUSB321
Wired Ethernet	RGMII1, MDIO	Texas Instruments DP83867E

2.7.2 I2C Address Mapping

The I2C Mapping Table provides the complete I2C address mapping details supported on the EVM.

Table 2-18. I2C Mapping Table

Interface Name	Processor Resources		Components / Part Numbers
	I2C Port	Address	
Buck Regulator	WKUP_I2C0	0x44	Texas Instruments TPS62875-Q1
Power Management IC	WKUP_I2C0	0x48, 0x49, 0x4A & 0x4B	Texas Instruments TPS65221-Q1
EEPROM, Board Id	WKUP_I2C0	0x51	MicrochipTech AT24C512C
Expansion Header (40p)	WKUP_I2C0	Add-on	
Expansion Header (40p)	MCU_I2C0	Add-on	
Audio Codec	I2C0	0x1B	Texas Instruments TLV320AIC3106
Input PD Controller	I2C0	0x20	Texas Instruments TPS25750
IO expander	I2C0	0x23	Texas Instruments TCA6424
Power Monitor/Measurement	I2C0	0x40 - 0x47, 0x4C - 0x4F	Texas Instruments INA226
Temperature Sensor	I2C0	0x48, 0x49	Texas Instruments TMP100NA
Clock Generator	I2C0	0x68	Texas Instruments LMK3H0102
PCIe	I2C0	Add-on	
IO Expander	I2C1	0x20	Texas Instruments TCA6416
DP Transceiver	I2C1	0x2C	Texas Instruments SN65DSI86
HDMI Transceiver	I2C1	0x3B, 0x3F, 0x62	Silicon Labs SIL9022
DSI Expansion	I2C1	Add-on	
OLDI Expansion	I2C1	Add-on	
Camera I2C Switch	I2C2	0x70, 0x71	Texas Instruments TCA9543A
Camera Expansion	I2C2	Add-on	
Test Automation Boot Mode	Reserved	0x22	Texas Instruments TCA6424

2.7.3 GPIO Mapping

The General Purpose IOs of processor are segmented into two major groups as WKUP/MCU and MAIN, but are used interchangeably for this design. Table 2-19 describes the GPIO mapping to the EVM peripherals of the processor and provides the default settings.

Table 2-19. GPIO Mapping

Processor GPIO	Processor Pin Name	Function	Dir/Level	Remarks
GPIO0_12	OSPI0_CSn1	Power Management IC Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Request (default)
GPIO0_13	OSPI0_CSn2	Ethernet PHY Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Request (default)
GPIO0_14	OSPI0_CSn3	Serial Flash Memory Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Request (default)
GPIO0_15	GPMC0_AD0	CSI0 Camera Expansion (J33, J37)	Bi-Dir	Expansion Board Specific (J33.17, J37.8)
GPIO0_16	GPMC0_AD1	CSI0 Camera Expansion (J33, J37)	Bi-Dir	Expansion Board Specific (J33.18, J37.18)
GPIO0_17	GPMC0_AD2	CSI1 Camera Expansion (J34, J37)	Bi-Dir	Expansion Board Specific (J34.17, J37.20)
GPIO0_18	GPMC0_AD3	CSI1 Camera Expansion (J34, J37)	Bi-Dir	Expansion Board Specific (J34.18, J37.22)
GPIO0_19	GPMC0_AD4	CSI2 Camera Expansion (J2, J36)	Bi-Dir	Expansion Board Specific (J2.17, J36.8)
GPIO0_20	GPMC0_AD5	CSI2 Camera Expansion (J2, J36)	Bi-Dir	Expansion Board Specific (J2.18, J36.18)
GPIO0_21	GPMC0_AD6	CSI3 Camera Expansion (J1, J36)	Bi-Dir	Expansion Board Specific (J1.17, J36.20)
GPIO0_22	GPMC0_AD7	CSI3 Camera Expansion (J1, J36)	Bi-Dir	Expansion Board Specific (J1.18, J36.22)
GPIO0_31	GPMC0_CLK	CSI0/CSI1 Camera Expansion (J37)	Bi-Dir	Expansion Board Specific (Pin 6)
GPIO0_33	GPMC0_OEn_Ren	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 13)
GPIO0_36	GPMC0_BE1n	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 37)
GPIO0_38	GPMC0_WAIT1	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 7)
GPIO0_41	GPMC0_CSn0	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 36)
GPIO0_42	GPMC0_CSn1	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 22)
GPIO0_67	MMC2_DAT1	Display Expander Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Request (default)
GPIO0_68	MMC2_DAT0	Reset for Camera Expansion (J36, J37)	Output	'0' - Device Reset (default), '1' - Normal Operation
GPIO0_69	MMC2_CLK	CSI2/CSI3 Camera Expansion (J36)	Bi-Dir	Expansion Board Specific (Pin 6)
GPIO0_70	MMC2_CMD	SD Card IO Voltage Selection	Output	'0' – SD Card IO Voltage is 1.8V'1' – SD Card IO Voltage is3.3 V (default)
GPIO0_71	MMC2_SDCD	Test Point (TP85)	Bi-Dir	Test Point Access (TP85)
GPIO0_72	MMC2_SDWP	Reserved / Ethernet Expansion	Input	Reserved
GPIO1_15	SPI0_CS0	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 29)

Table 2-19. GPIO Mapping (continued)

Processor GPIO	Processor Pin Name	Function	Dir/Level	Remarks
GPIO1_16	SPI0_CS1	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 32)
GPIO1_17	SPI0_CLK	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 31)
GPIO1_18	SPI0_D0	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 33)
GPIO1_19	SPI0_D1	eFUSE Power Supply Enable	Output	'0'– Disabled (default) , '1'– Enabled
GPIO1_30	EXT_REFCLK1	System Power Down	Output	'0'– Normal Operation (default) , '1'– System Power Down/Off
GPIO1_31	EXTINTn	Test Automation Interrupt #1	Input	'0' – Active Interrupt Request '1' – No Interrupt Request (default)
GPIO1_49	MMC1_SDWP	User LED	Output	'0' - LED [LD6] Off (Default), '1' - LED [LD6] On / Red
MCU_GPIO0_7	MCU_UART0_CTSn	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 16)
MCU_GPIO0_8	MCU_UART0_RTSn	40 pin Expansion Header (J28)	Bi-Dir	Expansion Board Specific (Pin 18)
MCU_GPIO0_11	WKUP_UART0_CTSn	SW1 Pushbutton	Input	'0' – SW1 is Pressed'1' – SW1 is NOT Pressed(default)
MCU_GPIO0_12	WKUP_UART0_RTSn	CAN-Bus PHY Stand-by [J5, J8]	Output	'0' - Normal Mode, '1' - Standby Mode (default)
MCU_GPIO0_23	WKUP_CLKOUT0	Watchdog Timer Interrupt	Output	'0' – Active Interrupt Request '1' – No Interrupt Request (default)

2.7.4 I2C GPIO Expander Mapping

The EVM uses I2C-based IO expanders for additional GPIO and peripheral control. Table 2-20 explains the functionality of each IO and the default setting.

Table 2-20. IO Expander Mapping Table

IO Expander Port	Schematic Net Name	Function	Dir/ Level	Remarks
I2C Bus: I2C0, Addr: 0x23 (TCA6424)				
P00	TRC_MUX_SEL	Configures EVM for TRACE (Debug). Impacted functions are primarily Camera, Audio	Output	'0' - Normal Operation ,'1' - TRACE Enabled (default)
P01	OSPI/ ONAND_MUX_SEL	Serial Flash Selection	Bi-Dir	'0' - Octal xSPI, '1' - Octal NAND (default selected with configuration switch [SW2])
P02	MCASP1_FET_SEL	McASP1 Audio Selection	Output	'0' - HDMI (default), '1' - Headset/ Codec
P03	CTRL_PM_I2C_OE#	Enable Processor Access to Integrated Power Measurement	Output	'0' - Disable (default), '1' - Enable
P04	CSI_VIO_SEL	Camera I2C/GPIO Voltage Level Selection (MIPI defines voltage level for CSI2)	Bi-Dir	'0' - 1.8V IO, '1 '- 3.3V IO (default selected with configuration switch [SW2])
P05	USB2.0_MUX_SEL	USB Selection for Type-C Connector	Output	'0'- USB2.0 (DFP/UFP/DRP) (default), '1'- USB3.0 (DFP)
P06	CSI01_MUX_SEL_2	Camera Selection for CSI Ports 0/1	Output	'0'- 40-pin Camera Expansion [J37] (default),'1'-22-pin Flex Camera [J33, J34]
P07	CSI23_MUX_SEL_2	Camera Selection for CSI Ports 2/3	Output	'0'- 40-pin Camera Expansion [J36] (default),'1'-22-pin Flex Camera [J1, J2]
P10	LMK1_OE1	Clock Enable for 100MHz PCIe (Processor) (Not currently supported, PCIe clock source from Processor)	Output	'0' - Clock Disabled (default), '1' - Clock Enabled
P11	LMK1_OE0	Clock Enable for 100MHz PCIe (PCIe Card) (Not currently supported, PCIe clock source from Processor)	Output	'0' - Clock Disabled (default), '1' - Clock Enabled
P12	LMK2_OE0	Clock Enable for Processor SERDES (Not currently supported, SERDES clock sourced internally from Processor)	Output	'0' - Clock Disabled (default), '1' - Clock Enabled
P13	LMK2_OE1	Clock Enable for DisplayPort Transceiver (Not currently supported, DP clock sourced from dedicated oscillator)	Output	'0' - Clock Disabled (default), '1' - Clock Enabled
P14	GPIO_RGMII1_RST#	Ethernet PHY Reset	Output	'0' - Ethernet is Reset, '1' - Ethernet is NOT Reset (default)
P15	GPIO_AUD_RSTn	Audio Headphone (Codec) Reset	Output	'0' - Audio is Reset (default), '1' - Audio is NOT Reset
P16	GPIO_eMMC_RSTn	eMMC Flash Memory Reset	Output	'0' - Memory is Reset, '1' - Memory is NOT Reset (default)

Table 2-20. IO Expander Mapping Table (continued)

IO Expander Port	Schematic Net Name	Function	Dir/ Level	Remarks
P17	GPIO_uSD_PWR_EN	Micro SD Card Power Enable	Output	'0' - Card Power is Disabled, '1' - Card Power is Enabled (default)
P20	USER_LED2	User LED [LD5] / Green	Output	'0' - LED is ON, '1' - LED is OFF (default)
P21	MCAN0_STB	CAN-Bus PHY Stand-by [J10]	Output	'0' - Normal Mode, '1' - Standby Mode (default)
P22	PCIe0_1L_RC_RSTz	PCIe Card Reset	Output	See PCIe Specification (PERST#) for more details. (Default = '0')
P23	PCIe0_1L_PRSNT#	PCIe Hot Plug / Card Detect	Input	See PCIe Specification (PRSNT#) for more details. (Default = '1')
P24	ENET1_EXP_SPARE2	Reserved / Ethernet Expansion	Input	Reserved
P25	ENET1_EXP_PWRDN	Reserved / Ethernet Expansion	Output	Reserved
P26	ENET1_I2CMUX_SEL	Reserved / Ethernet Expansion	Output	Reserved
P27	ENET1_EXP_RESETZ	Reserved / Ethernet Expansion	Output	Reserved
I2C Bus: I2C1, Addr: 0x20 (TCA6416)				
P00	DSI_Mux_SEL_2	Display Selection for Processor's DSI Port	Output	'0'- DisplayPort [J19] (default), '1'- DSI Expansion [J40]
P01	GPIO_eDP_ENABLE	DisplayPort Transceiver Reset	Output	'0' - DisplayPort is Reset (default), '1' - DisplayPort is NOT Reset
P02	DP0_PWR_SW_EN	DisplayPort Monitor Enable	Output	'0' - Monitor is Disabled (default), '1' - Monitor is Enabled
P03	GPIO_OLDI_RSTn	Display Expansion (OLDI) Panel Reset [J39]	Output	'0' - Panel is Reset (default), '1' - Panel is NOT Reset
P04	GPIO_HDMI_RSTn	HDMI Transceiver Reset	Output	'0' - HDMI is Reset (default), '1' - HDMI is NOT Reset
P05	HDMI_LS_OE	HDMI Monitor Enable	Output	'0' - Monitor is Disabled (default), '1' - Monitor is Enabled
P10	DSI_GPIO0	Display Expansion (DSI) General IO [J40]	Bi-Dir	DSI Panel Specific (Pin 6)
P11	DSI_GPIO1	Display Expansion (DSI) General IO [J40]	Bi-Dir	DSI Panel Specific (Pin 5)
P12	DSI_EDID	Display Expansion (DSI) General IO [J23]	Input	DSI Panel Specific (Pin 3)
P13	IO_eDP_IRQ	DisplayPort Monitor Detect	Input	'0' - No Monitor Detected (default), '1' - Monitor Detected
P14	OLDI_INT#	Display Expansion (OLDI) Panel Interrupt [J39]	Input	'0' - Interrupt Pending, '1' - No Interrupt Pending
P15	HDMI_INTn	HDMI Monitor Detect	Input	'0' - No Monitor Detected (default), '1' - Monitor Detected

2.7.5 Power Monitoring

The EVM includes integrated power monitoring/measurement capability for eleven (11) discrete power rails, giving user critical power usage details for optimizing the processor application. The on-board analog-to-digital converters (INA226) are accessed via I2C, and can be read both by the processor and externally via 3-pin header [J27]. Table 2-21 describes the I2C address and the power rail information of the ADC as is assigned. (Note, the Power Monitor I2C bus is a dedicated bus and can be access externally without impact to other I2C activity.)

Table 2-21. Power Monitoring Device

INA I2C Address	Power Rail	Nominal Value (Volts)	Shunt Value (Ohms)
0X40	Processor Core (VDD_CORE)	0.85	0.005 Ohms
0X41	Processor RAM, SERDES (VDDR_CORE, VDDA_CORE, ...)	0.85	0.01 Ohms
0X42	Processor Analog/PHY (VDDA_1P8_CSI, VDDA_1P8_USB, ...)	1.8	0.01 Ohms
0X43	Processor CORE for IO Retention (VDD_CANUART)	0.75	0.01 Ohms
0X44	Processor IO for SD Card (VDDSHV5)	3.3/1.8	0.01 Ohms
0X45	Processor VDD IO at 1.8 (VDD_IO_1V8)	1.8	0.01 Ohms
0X46	System Level Power (Processor + Memory + Peripherals)	3.3	0.002 Ohms
0X47	Processor DRAM IO (VDDS_DDR) + DRAM Memory	1.1	0.01 Ohms
0X4C	Processor IO (VDDSHV_MCU, VDDSHV0, …)	3.3	0.01 Ohms
0X4D	Processor Analog/PLL (VDDA_PLLx, VDDA_MCU, …)	1.8	0.01 Ohms
0X4E	Processor IO for IO Retention (VDDSHV_CANUART)	3.3	0.01 Ohms

2.7.6 Identification EEPROM

The EVM board identified and revision information are stored in an on-board EEPROM. The first 259 bytes of memory are pre-programmed with EVM identification information. The format of that data is provided in the table below. The remaining 32509 bytes are available for data or code storage.

The EEPROM is accessible from WKUP I2C0 port of processor at address 0x51.

Table 2-22. Board ID memory Header Information

Field Name	Offset / Size	Value	Comments
MAGIC	0000/ 4B	0xEE3355AA	Header Identifier
M_TYPE	0004/1B	0x1	Fixed length and variable position board ID header
M_LENGTH	0005/2B	0x37	Size of payload
B_TYPE	0007/1B	0x10	Payload type
B_LENGTH	0008/2B	0x2E	Offset to next header
B_NAME	000A/16B	AM67/TDA4VENX-EVM	Name of the board
DESIGN_REV	001A/2B	E1	Revision number of the design
PROC_NBR	001C/4B	170	Design Reference Number
VARIANT	0020/2B	1	Design variant number
PCB_REV	0022/2B	E1	Revision number of the PCB
SCHBOM_REV	0024/2B	0	Revision number of the schematic
SWR_REV	0026/2B	1	First software release number
VENDORID	0028/2B	1	
BUILD_WK	002A/2B		Week of the year of production
BUILD_YR	002C/2B		Year of production
BOARDID	002E/6B	0	
SERIAL_NBR	0034/4B		Incrementing board number
DDR_INFO	0038/1B	0x11	DDR Info Header Identifier
DDR_LENGTH	0039/2B	0x2	DDR Info Size
DDR_CONTROL	003B/2B	0xC560	DDR Control Word
END_LIST	003D/1B	0xFE	End Marker

2.7.7 Memory and Storage

For volatile memory, the EVM features 8GB of Micron LPDDR4 memory (MT53E2G32D4DE-046). The 32b interface can support transfer rates up to 4000MT/s providing supper fast access to data. While the EVM design is not considered to be reference, the LPDDR4 design portion (both schematic and PCB design) can be considered reference and must be followed when customers are implementing designs.

For fast booting options, the EVM features two different technologies of Serial Flash storage. 512Mb of Octal-xSPI flash is available from Cypress (S28HS512TGABHM010), supporting data rates up to 166MB/s (SDR) and 400MB/s (DDR). 1Gb of Octal-NAND flash is available from Winbond (W35N01JWTBAG), supporting data rates up to 166MB/s (SDR) and 240MB/s (DDR). These storage devices share the same processor interface and cannot be used simultaneously. For details on how to select each device, see Section 2.4.2 and Section 2.7.4.

For mass storage options, the EVM again supports two different memory options. A removable Section 2.5.5 supports external memory cards up to UHS-I data rates (104MB/s). For on-board storage, 32GB is available from Micron (MTFC32GAZAQHD-IT) supporting data rates up to 200MB/s (HS200) and 400MB/s (HS400).

2.7.8 Power Distribution

The EVM utilizes an array of DC-DC converters and linear regulators to power the processor, memories, and peripheral components with the necessary voltage and power required. The figure below shows the high level power architecture used on the EVM.

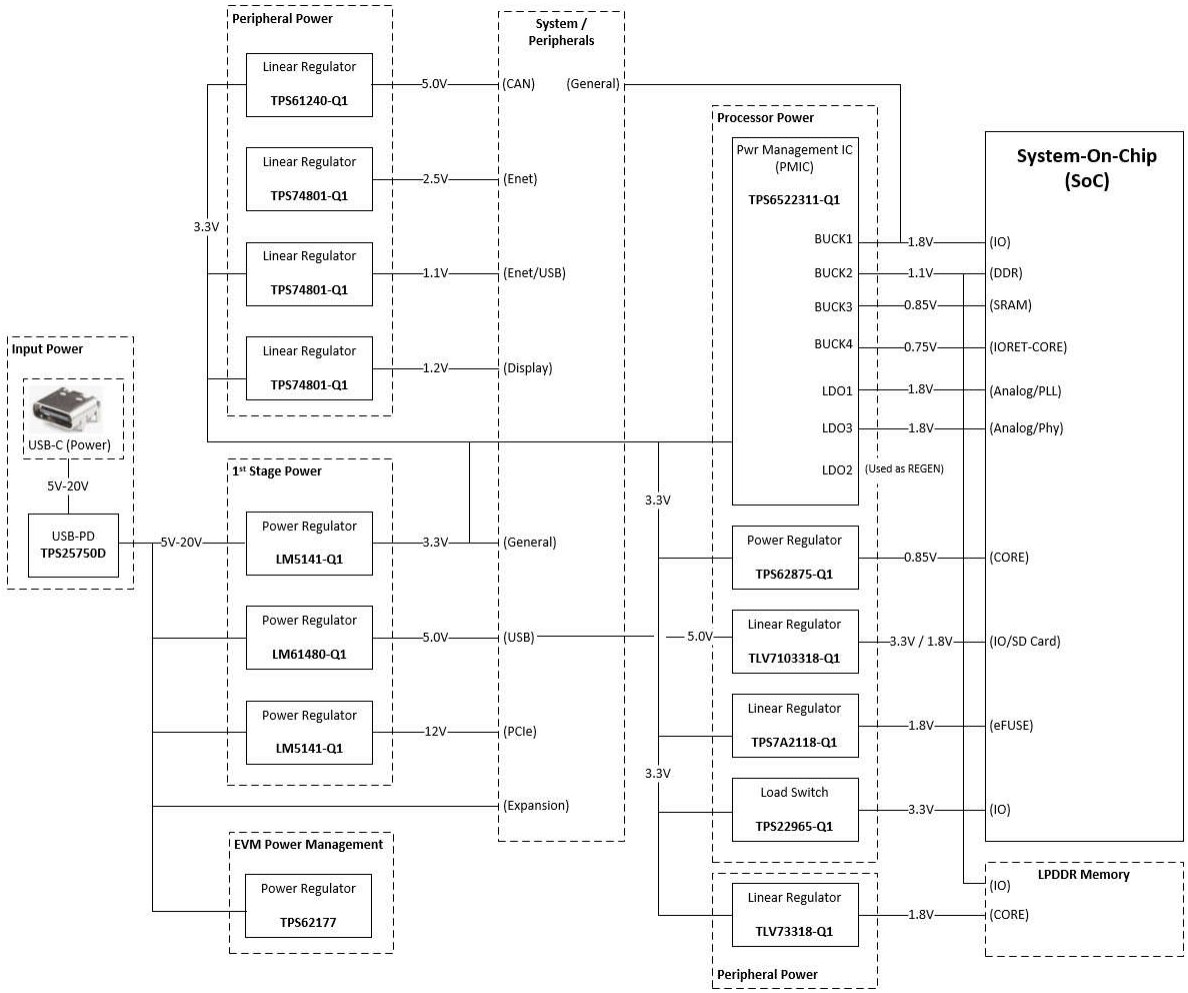


Figure 2-5. Power Architecture

The power flow begins from an external supply connecting to the USB Type-C power connector [J24]. See Section 2.3 for specifics on external power supply requirements. The USB Power Delivery device (TPS25750D) negotiates the input voltage from 5V up to 20V depending upon input supply capability. The 1st Stage Power regulators then generate the EVMs primary power rails of 3.3Volts (LM5141-Q1), 5.0Volts (LM61480-Q1), and 12.0Volts (LM5141-Q1). A small 3.3Volt regulator (TPS62177) is used for management circuitry to control EVM ON/OFF features with push-buttons. Some of the on-board peripherals of the EVM have specific voltage and power requirements and are satisfied with several linear regulators (TPS74801-Q1).

The Power Management IC (TPS6522311-Q1) is specifically designed to meet the voltage, power, and sequencing requirements of the processor. The PMIC includes the capability to manage supplemental regulators and is capable of meeting ASIL-B safety requirements. The low voltage, high current power rail of the processor is sourced from a *stackable* SMSP regulator (TPS62875-Q1) to allow for power design size optimization based on the specific applications power needs. This specific PDN implementation includes additional power resources to support advance low power modes such as IO and DDR Retention. Additional power resources are also included to provide the ability to demonstrate both high performance use-cases (operating at 0.85V) and the lower power or performance use cases (operating at 0.75V).

3 Hardware Design Files

The hardware design files are combined to a single package and available for download at Design Files. The package file can contain multiple EVM board revisions (directories). The naming convention is as follows for PROC*xyz*E*wq*_RP where:

- PROC: Indicates TI's Processor Product.

- *xyz*: Unique ID for this Evaluation Board (example is '170' for this design).

- E: E indicates Pre-Production, blank for Production.

- *wq*: Indicates Revision (w - Major, blank/q - Minor).

- _RP: Release Package Notation.

Example (oldest to latest revision):

PROC170E1A: Pre-Production, version '1A'

PROC170E2: Pre-Production, Version '2'.

PROC170A: Production, Version 'A'.

See schematic history/change log for complete list of changes for each revision.

3.1 Schematics

The schematics are available in both design format (Cadence Allegro, *_SCH.DSN) and searchable PDF (*_SCH.PDF). Both are included as part of the design package and available for download at Design Files.

3.2 PCB Layouts

The PCB design and manufacturing information is available in several different file formats. Below is a list of PCB files included in the design package available for download at Design Files.

Table 3-1. PCB Design and Manufacturing Files

File Type (Extension)	Description
Design file (*_BRD.ZIP)	Allegro PCB design file/zip
Design file (*_ODBGRB.ZIP)	Design file exported to ODB++/Zip
Design file extract (ALG)	For import into other design tools
Fabrication drawing (*_FAB.PDF)	Fabrication info in viewable format
Manufacturing file (_274XGBR.ZIP)	Gerber data, RS-274/ZIP
Manufacturing file (*_STL.ZIP)	Gerber data, STL/Zip
Manufacturing file (*_BRD.IPC)	IPC-D 465 Gerber data supplement
Layers drawing (*_LAYERS.PDF)	Viewable images of each PCB Layer
Stack-up (*_STACKUP.PDF)	PCB Stack-up from PCB manufacturer

3.3 Bill of Materials (BOM)

The Bill Of Materials (BOM) is available in spreadsheet format (Microsoft Excel, *_BOM.XLSX) and is included as part of the design package download at Design Files.

4 Compliance Information

4.1 Thermal Compliance

There is opportunity for elevated heat on and near the processor, use caution particularly at elevated ambient temperatures!

Although the processor and heat sink are not burn hazards, caution must be used when handling the EVM due to increased heat in the processor area.

	**Caution**	Hot surface. Contact can cause burns. Do not touch.

4.2 EMC, EMI, and ESD Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). TI recommends this product be used in an ESD controlled environment. This can include a temperature and/or humidity-controlled environment to limit the buildup of ESD. TI also recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory condition and the applied standard is as per ENC IEC 61326-1:2021.

5 Additional Information

5.1 Known Hardware or Software Issues

There are no known issues with the EVM.

5.2 Trademarks

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