1 Introduction

This chapter introduces the features, subsystems, and architecture of the J784S4 Processor Platform high-performance System-on-Chip (SoC).

Note

This document describes the Superset architecture, processors and peripherals of the J784S4 Family of SoCs, which are part of the K3 Multicore SoC architecture platform. The J742S2 Processor Family is a subset of the J784S4 Processor Family. Not all features are available on each family of devices. The superset J784S4 and J742S2 devices are available for preproduction software development. Software should constrain the features used to match the intended production device. For more information on the specific features, processors and peripherals available on a particular device, refer to the Device Comparison table in the corresponding device-specific Data sheet.

The J784S4 Processor Platforms are hereinafter commonly referred to as J784S4 *platform*, *device*, or *SoC*.

TI limits support for this family of SoCs to features that are supported via Software Development Kits (SDK). The SDK “build sheet” is available for download as part of each SDK and should be referenced to understand the subset of SoC hardware functionality that is available in software:

https://www.ti.com/tool/PROCESSOR-SDK-J784S4

https://www.ti.com/tool/PROCESSOR-SDK-J742S2

https://www.ti.com/tool/PROCESSOR-SDK-AM69A

https://www.ti.com/toll/PROCESSOR-SDK-AM69

This document describes the Superset features of the Modules integrated into this Device. See the Module Integration section of this document for a list of module features not supported by the integration on this Device.

1.1 Device Overview

1.1.1 Device Overview Feature List

The TDA4VH and TDA4AH SoCs are targeted for automotive applications and aim to meet the complex processing needs of modern embedded products. They are designed as a high performance and highly integrated device architecture, providing significant levels of processing power, graphics capability, video and imaging processing, virtualization, and coherent memory support.

Key distinguishing device features:

- 64-bit architecture with virtualization and coherent memory support, which leverages full processing capability of 64-bit Arm® Cortex® -A72
- Integration of vision hardware processing accelerators to facilitate extensive processing requirements in low power budget for automotive ADAS , autonomous mobile robot, and edge AI applications
- Integration of multiple general-purpose microcontroller unit (MCU) clusters with a dual Arm® Cortex®-R5F MCU subsystem available for general purpose use as either two separate cores operating in lockstep, intended to help customers achieve functional safety goals for their end products
- Integration of multiple fixed and floating-point C71x Digital Signal Processors (DSP) that significantly boost power over a broad range of general signal processing tasks for both general applications and

automotive functions which also incorporate advanced techniques to improve control code efficiency and ease of programming such as branch prediction, protected pipeline, precise exception and virtual memory management
- Multiple tightly coupled Matrix Multiplication Accelerators (MMA) that extend the C71x DSP architecture's scalar and vector facilities enabling deep learning and enhance vision, analytics and wide range of general applications. The achieved total TOPS (Tera Operations Per Second) performance significantly differentiates the device for single board computer in machine vision and deep learning applications
- Multi-display support, including flexibility to interface with different panel types (eDP, DSI, DPI) with multi-layer hardware composition
- Integration of hardware features that help applications to achieve functional safety mechanisms
- Robust security architecture with sandboxed Security Controller managing all secure configurations with high performance client-server messaging scheme between secure Security Controller and all cores
- Simplified solution for power supply management, enabling lower cost system solution (on-die bias LDOs and power good comparators for minimal power sequencing requirements consistent with low cost supply design)

Processor cores:

- Up to Four C7x floating point, vector DSP, up to 1.0 GHz, 320 GFLOPS, 1024 GOPS
- Up to Four Deep-learning matrix multiply accelerator (MMA), up to 32 TOPS (8b) at 1.0 GHz
- TwoVision Processing Accelerators (VPAC) with Image Signal Processor (ISP) and multiple vision assist accelerators
- Depth and Motion Processing Accelerators (DMPAC)
- Eight Arm® Cortex®-A72 microprocessor subsystem at up to 2.0 GHz
  - 2MB shared L2 cache per quad-core Cortex®-A72 cluster
  - 32KB L1 DCache and 48KB L1 ICache per Cortex®-A72 core
- Eight Arm® Cortex®-R5F MCUs at up to 1.0 GHz
  - 16K I-Cache, 16K D-Cache, 64K L2 TCM
  - Two Arm® Cortex®-R5F MCUs in isolated MCU subsystem
  - Six Arm® Cortex®-R5F MCUs in general compute partition
- GPU IMG BXS-64-4, 256kB Cache, up to 800 MHz, 50 GFLOPS, 4 GTexels/s
- Custom-designed interconnect fabric supporting near max processing entitlement

Memory subsystem:

- Up to 8MB of on-chip L3 RAM with ECC and coherency
  - ECC error protection
  - Shared coherent cache
  - Supports internal DMA engine
- Up to Four External Memory Interface (EMIF) module with ECC
  - Supports LPDDR4 memory types
  - Supports speeds up to 4266 MT/s
  - Up to 4x32-b bus with inline ECC up to 68 GB/s

Functional Safety:

- Functional Safety-Compliant targeted (on select part numbers)
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 functional safety system design up to ASIL-D/SIL-3 targeted
  - Systematic capability up to ASIL-D/SIL-3 targeted
  - Hardware integrity up to ASIL-D/SIL-3 targeted for MCU Domain
  - Hardware integrity up to ASIL-B/SIL-2 targeted for Main Domain
  - Safety-related certification
    - ISO 26262 planned
- AEC-Q100 qualilfied on part number variants ending in Q1

Device security (on select part numbers):

- Secure boot with secure runtime support
- Customer programmable root key, up to RSA-4K or ECC-512

- Embedded hardware security module
- Crypto hardware accelerators – PKA with ECC, AES, SHA, RNG, DES and 3DES

High speed serial interfaces:

- Integrated ethernet switch supporting up to 8 (TDA4xH) or 4 (TDA4xP) external ports
  - Two ports support 5Gb, 10Gb USXGMII or 5Gb XFI
  - All ports support 1Gb, 2.5Gb SGMII
  - All ports can support QSGMII. A maximum of 2 (TDA4xH) or 1 (TDA4xP) QSGMII can be enabled and uses all 8 or 4 internal lanes
- Up to 4x2-L/2x4L (TDA4xH) or 2x2L/1x4L (TDA4xP) PCI-Express® (PCIe) Gen3 controllers
  - Gen1 (2.5GT/s), Gen2 (5.0GT/s), and Gen3 (8.0GT/s) operation with auto-negotiation
- One USB 3.0 dual-role device (DRD) subsystem
  - Enhanced SuperSpeed Gen1 Port
  - Supports Type-C switching
  - Independently configurable as USB host, USB peripheral, or USB DRD
- Three CSI2.0 4L RX plus Two CSI2.0 4L TX

Ethernet

- Two RGMII/RMII interfaces

Automotive interfaces:

- Twenty Modular Controller Area Network (MCAN) modules with full CAN-FD support

Display subsystem:

- Two DSI 4L TX (up to 2.5k)
- One eDP/DP interface with Multi-Display Support (MST)
- One DPI

Audio interfaces:

- Five Multichannel Audio Serial Port (MCASP) modules

Video acceleration:

- H.264/H.265 Encode/Decode, up to 960MP/s (TDA4xH) or 480MP/s (TDA4xP)

Flash memory interfaces:

- Embedded MultiMediaCard Interface (eMMC™ 5.1)
- One Secure Digital® 3.0/Secure Digital Input Output 3.0 interfaces (SD3.0/SDIO3.0)
- Universal Flash Storage (UFS 2.1) interface with two lanes
- Two simultaneous flash interfaces configured as
  - One OSPI or HyperBus™ or QSPI flash interfaces, and
  - One QSPI flash interface

System-on-Chip (SoC) architecture:

- 16-nm FinFET technology
- 31 mm × 31 mm, 0.8-mm pitch, 1414-pin FCBGA (ALY), enables IPC class 3 PCB routing

TPS6594-Q1 Companion Power Management ICs (PMIC):

- Functional Safety-Compliant support up to ASIL-D
- Flexible mapping to support different use cases

1.1.2 Device Block Diagram

Figure 1-1 shows the SoCs top-level block diagram with domains partitions.

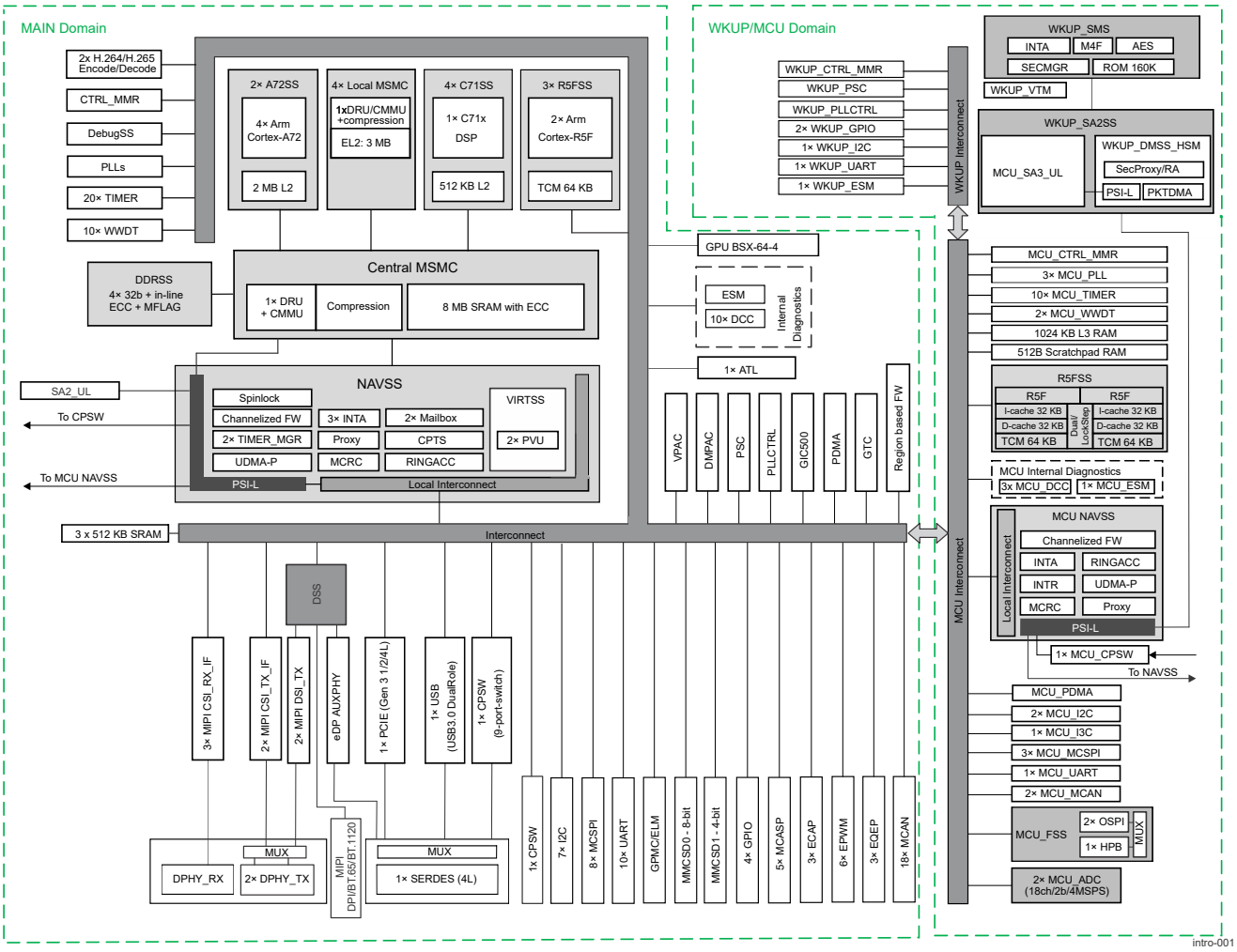

Figure 1-1. Device Top-level Block Diagram

1.1.3 Modules Allocation and Instances within Device Domains

Table 1-1 shows device IPs allocation within device domains.

Table 1-1. Modules Allocation and Instances within Device Domains

Module Full Name	Module Abbreviation	Domain		
		WKUP	MCU	MAIN
Quad-core Arm Cortex-A72 MPU	A72SS	-	-	2
Dual-core Arm Cortex-R5F Subsystem	R5FSS	-	1	3
C71x Digital Signal Processor Subsystem with Matrix Multiplication Accelerator	C71SS	-	-	4

Table 1-1. Modules Allocation and Instances within Device Domains (continued)

Module Full Name	Module Abbreviation	Domain		
		WKUP	MCU	MAIN
Arm Cortex-M4F based Security Management Subsystem	SMS	1	-	-
Graphics Processing Unit (BXS-64-4)	GPU	-	-	1
Video Accelerator	CODEC	-	-	2
Vision Pre-processing Accelerator	VPAC	-	-	2
Depth and Motion Perception Accelerator	DMPAC	-	-	1
Mailbox	MAILBOX	-	-	2
Spinlock	SPINLOCK	-	-	1
Central Multicore Shared Memory Controller	MSMC (Central)	-	-	1
Local C7/MMA Multicore Shared Memory Controller	C7/MMA MSMC	-	-	4
DDR Subsystem	DDRSS	-	-	4
Peripheral Virtualization Unit	PVU	-	-	2
Navigator Subsystem	NAVSS	-	1	1
Unified DMA Controller	UDMA	-	1	1
Ring Accelerator	RINGACC	-	1	1
Proxy	PROXY	-	1	1
Secure Proxy	SEC_PROXY	-	1	1
Interrupt Aggregator	INTR_AGGR	-	1	3
Data Routing Unit	DRU	-	-	1
Common Platform Time Sync Module	CPTS	-	1	6
Timer Manager	TIMER_MGR	-	-	2
Analog-to-Digital Converter	ADC	-	2	-
General-Purpose Input/Output	GPIO	2	-	4
Inter-Integrated Circuit	I2C	1	2	7
Improved Inter-Integrated Circuit	I3C	-	1	-
Multichannel Serial Peripheral Interface	MCSPI	-	3	8
Universal Asynchronous Receiver/Transmitter	UART	1	1	10
Two-Port Ethernet Switch	CPSW2G	-	1	1
9-Port Gigabit Ethernet Switch	CPSW9G	-	-	1
Peripheral Component Interconnect Express	PCIe	-	-	4
Universal Serial Bus Subsystem	USBSS	-	-	1
Serializer/Deserializer	SERDES	-	-	4
Flash Memory Subsystem	FSS	-	1	-
Octal Serial Peripheral Interface	OSPI	-	2	-
HyperBus Interface	HPB	-	1	-
General-Purpose Memory Controller	GPMC	-	-	1
Error Location Module	ELM	-	-	1
Multimedia Card/Secure Digital Interface	MMCSD	-	-	2
Enhanced Capture Module	ECAP	-	-	3
Enhanced Pulse Width Modulation Module	EPWM	-	-	6
Enhanced Quadrature Encoder Pulse Module	EQEP	-	-	3
Controller Area Network Interface	MCAN	-	2	18
Audio Tracking Logic	ATL	-	-	1
Multichannel Audio Serial Port	MCASP	-	-	5
Display Subsystem	DSS	-	-	1

Table 1-1. Modules Allocation and Instances within Device Domains (continued)

Module Full Name	Module Abbreviation	Domain		
		WKUP	MCU	MAIN
MIPI Display Serial Interface	DSI	-	-	2
Embedded DisplayPort Transmitter	eDP	-	-	1
Camera Streaming Receiver Interface	CSI_RX_IF	-	-	3
Camera Streaming Transmitter Interface	CSI_TX_IF	-	-	2
Shared D-PHY Transmitter	DPHY_TX	-	-	2
Universal Flash Storage	UFS	-	-	1
Global Timer Counter	GTC	-	-	1
Real Time Interrupt Windowed Watchdog Module	RTI	-	2	9
Timers	TIMER	-	10	20
Dual Clock Comparator	DCC	-	3	10
Error Signaling Module	ESM	1	1	1
Memory Cyclic Redundancy Check	MCRC	-	1	1

Note

The supported set of features and peripherals is device part number dependent. For more information, see the device-specific Datasheet.

1.2 Module Descriptions

1.2.1 Arm Cortex-A72 Subsystem

Each core of the quad-core Arm Cortex-A72 Microprocessor Units (MPU) has the following main features:

- Full Armv8-A architecture compliancy
- Advanced Single Instruction Multiple Data (SIMD) and floating point extension (Arm Neon™)
- Armv8 cryptography extensions
- Superscalar, variable length, out-of-order pipeline
- 48KB program and 32KB data Level 1 (L1) Cache
- 2MB shared Level 2 (L2) Cache
- ECC protection for L1 data cache and L2 Cache
- Parity protection for L1 Instruction Cache
- Dynamic branch prediction with Branch Target Buffer (BTB) and Global History Buffer (GHB) RAMs, return stack, and indirect predictor
- Arm General Interrupt Controller (GICv3) architecture
- Support timers for each Cortex-A72 core
- 512-bit wide, synchronous or asynchronous VBUSM.C master interface
- Arm CoreSight™ Debug and Trace Architecture
- Advanced power management for low power optimization
- SoC level dedicated RTI windowed watchdog timer per core

1.2.2 Arm Cortex-R5F Processor

Each instance of the dual-core Arm Cortex-R5F processor supports the following main features:

- Armv7-R architecture
- Two modes of operation, boot-time configurable:
  - Split mode: two independently operating cores (asymmetric multi processing, no coherence)
  - Lock (lockstep) mode: one main operating core with the other operating in lockstep
  - Boot-time configurable to be in split or lock mode
- 32KB instruction and 32KB data SECDED ECC protected L1 cache per core
- 64KB of Tightly Coupled Memory (TCM) per core in a split mode
- 128KB of TCM for CPU0 in lock mode

- Full-Precision Floating Point (VFPv3)
- 8 breakpoints, 8 watch points
- 16-region Memory Protection Unit (MPU)
- CoreSight Debug Access Port (DAP)
- CoreSight ETM-R5 interface
- Performance Monitoring Unit (PMU)
- 32-bit to 48-bit Region-based Address Translation (RAT) on memory access masters
- Integrated Vectored Interrupt Manager (VIM)
- Interfaces:
  - 64-bit VBUSM master pair (1 read, 1 write) for L3 memory accesses (per core)
  - 64-bit VBUSM slave for TCM access (per core)
  - 32-bit VBUSM master pair (1 read, 1 write) for peripheral access
  - 32-bit VBUSP master for peripheral access (per core)
  - 32-bit VBUSP slave configuration port (per core)
  - 32-bit VBUSP slave debug port

1.2.3 C71x DSP Subsystem

Each instance of the C71x DSP supports the following main features:

- True 64-bit C7120 CPU core with:
  - Instruction fetch unit
  - Instruction dispatch unit
  - Instruction decode unit
  - CPU dual data path with one 64-bit scalar side (side A) and one 512-bit vector side (side B)
  - CPU control logic
  - Test, debug, and interrupt logic
  - Enhanced Instruction Set Architecture (ISA)
  - OpenCL features
- Matrix Multiply Accelerator (MMA) as a special functional unit in C71x CorePac CPUs
- L1 Program Memory Controller (PMC) with 32KB L1P memory, all cache
- L1 Data Memory Controller (DMC) with 48KB L1D memory, configurable as cache and/or SRAM
- L2 Unified Memory Controller (UMC) with 512KB L2 memory, configurable as cache and/or SRAM
- Multi-dimensional Streaming Engine (SE) - flexible, high bandwidth mechanism for reading large quantities of data into C71x DSP
- CorePac Memory Management Unit (CMMU)
- Power-down controller
- Debug capabilities

1.2.4 Graphics Processing Unit

The Graphics Processing Unit (GPU) which accelerates 2-dimensional (2D) and 3-dimensional (3D) graphics and compute applications. It supports the following main features:

- Architecture based on IMG BXS-64-4 with 256KB cache
- OpenGL 3.x and Vulkan API support
- Up to 50 GFLOPS
- Support for GPU virtualization
- Support for HyperLane Technology, with 8 HyperLanes available

1.2.5 Video Accelerator

The Video Accelerator (CODEC) has the following main features, among others:

- Encode/Decode:
- – H.265/HEVC – Main and Main Still Picture Profile @L5.1 High-tier
  - H.264/AVC – Baseline/Constrained Baseline/Main/High Profiles Level @L5.2
  - Max resolution: 8192x8192
  - YUV420 video format
  - YUV422 video format (only encoder)

  - 8-bit depth
- Encode, Decode or combination up to 4k60 total rate
- Up to 8x separate concurrent video encode, decode or combination (8x1080p30)

1.2.6 Vision Pre-processing Accelerator

The Vision Pre-processing Accelerator (VPAC) provides a set of common vision primitive functions, performing various pixel data processing tasks, such as: color processing and enhancement, noise filtering, wide dynamic range (WDR) processing, lens distortion correction, pixel remap for de-warping, on-the-fly scale generation, on-the-fly pyramid generation, and offloads these common tasks from the main SoC processors (ARM, DSP, etc.). The VPAC includes the following processing and infrastructure sub-modules:

- Vision Imaging Sub-System (VISS) which provides raw data image processing such as:
  - Wide Dynamic Range (WDR) merge
  - Defect Pixel Correction (DPC)
  - Lens Shading Correction (LSC)
  - Global/Local Brightness and Contrast Enhancement (GLBCE)
  - Advanced Spatial Noise Filter (NSF4V)
  - Edge Enhancement (EE)
  - Demosaicing
  - Color conversion
- Lens Distortion Correction (LDC) block, which provides data reading from memory (DDR or on-chip) and applies perspective transformation as well as correction of lens distortion (including fisheye lenses).
- Multi-Scalar (MSC) block reads data from memory (DDR or on-chip) to internal shared level 2 (SL2) memory and generates up to 10 scaled outputs from one or two inputs, with various scaling ratios.
- Noise Filter (NF) block reads data from memory (DDR or on-chip) to internal SL2 memory and does Bilateral filtering to remove noise.
- Hardware Thread Scheduler (HTS) provides inter-processor communication among various VPAC sub-modules (VISS, LDC, MSC and NF) as well as with the local DMA Engine (UTC).
- Internal Shared Level 2 (SL2) memory for data exchange across VPAC sub-modules (VISS, LDC, MSC and NF) and from DDR/MSMC, using the K3 Data Movement Architecture (DMA) mechanism
- Load/Store Engine (LSE) which performs data load and store tasks on a the SL2 memory for the hardware accelerator algorithm cores
- VISS to LDC direct OTF (On-the-Fly) for multi-camera
- YUV422 10 and 12 bit format support on all units except NF (e.g. LDC/MSC)
- Simultaneous visual (HV) and analytics (MV) output to system memory including L3 flex connect, saving need for additional read from system memory for HV+MV processing.
- Chromatic Aberration Correction (CAC) to support lower cost lens
- RGBIR support

1.2.7 Depth and Motion Perception Accelerator

The Depth and Motion Perception Accelerator (DMPAC) computes dense stereo depth maps (*depth*) and dense optical flow vectors (*motion*) from camera inputs. The stereo and optical flow processing is partitioned into two top level sub-blocks: the Dense Optical Flow (DOF) engine and the Stereo Disparity Engine (SDE). The DOF and SDE blocks share a common local memory, DMA, external messaging and control infrastructure. The DMPAC provides the following main features, among others:

- Image resolution up to 2MPix (maximum horizontal resolution up to 2048 pixels; maximum vertical resolution up to 1024 pixels)
- Maximum throughput up to 220MPix/sec for DOF, and up to 84-100MPix/sec for SDE
- Simultaneous operation of Stereo (1MPix@30fps) and Optical flow (1MP@30fps)
- 12-bit fully packed luminance data input pixel data format (other formats supported through conversion)
- Packed 16-bit (disparity) or 32-bit (flow vector) output data formats
- Shared Level 2 (SL2) memory sub-system, which serves the data transfer of the DOF and SDE blocks
- Unified Transfer Controller (UTC), which serves as a DMA engine
- Hardware Thread Scheduler (HTS) block for messaging and control mechanism
- Counter, Timer and System Event Trace (CTSET) module, which provides event tracing capability for the Stereo and Optical Flow hardware threads

1.2.8 Navigator Subsystem

The Navigator subsystem (NAVSS) can be used for efficient transfer of data support between software, firmware and hardware in all combinations. It consists of the following main modules:

- Unified DMA Controller with the following main modes and features:
  - K3 DMA Architecture compliant Tx/Rx port implementation
  - K3 DMA Architecture compliant Packet-Oriented DMA Functionality (UDMA-P)
  - K3 DMA Architecture compliant Third Party Channel Controller
  - K3 DMA Architecture compliant Unified Transfer Controller
  - K3 DMA Architecture compliant Unified DMA channels which all share the execution hardware using time division multiplexing
- Ring Accelerator provides hardware acceleration to enable straightforward passing of work between a producer and a consumer and has the following main features:
  - Supports 1024 independent memory-mapped ring structures
  - Supports various modes for each ring based on usage and compatibility
  - Provides 2-words deep shared incoming Transfer Response FIFO
  - Provides bit-wide source VBUSM read/write slave interface for accesses from DMA controller entities
- Proxy module with the following main features:
  - Provides proxy buffers to store large data bursts that a host can only access in smaller amounts
  - Keeps the large data coherent until the complete data has been accessed
  - Allows interleaved access between multiple hosts using multiple proxies
  - Supports a pre-configured number of target resources to proxy with pre-configured number of channels, size of each channel, and address offset per each target
- Secure proxy module is a modified version of the proxy module and in addition has the following main features:
  - Supports a number of threads, where each has their own independent proxy function
  - Supports a programmable fixed queue for each proxy thread
  - Supports multiple producers all writing to the same queue
  - Supports programmable thresholds for when to generate events
  - Supports a max message count for outbound proxy threads limiting the number of messages a thread can produce
- Interrupt Aggregator modules provide a centralized machine which handles the termination of system events to that they can be coherently processed by the host(s) in the system. Main features are as follows:
  - 64-bit VBUSP slave using 64-bit registers
  - Provide a set of TI Interrupt Architecture compliant interrupt status and mask registers which are used to pass specific event status to one or more host blocks.
  - Provide a set of Global Event Input (GEVI) counters which can count events delivered via an ingress Event Transport Lane (ETL)
  - Provides a set of Local Event Input (LEVI) to Global event registers which can be used to convert pulsed discrete interrupt inputs or clock synchronous rising edge events into Global events on an egress ETL
  - Provides a set of GEVI 'Multicast' registers which can take a Global event from an ingress ETL and generate two egress Global events on two egress ETL interfaces
- Peripheral Virtualization Unit (PVU) module which provides TLBs (Translation Look-aside Buffers) for static virtual address translation on a CBA VBUSM bus with the following main features:
  - Implements a channelized TLB for virtual address translation
  - Supports a pre-configured number of entries per TLB channel
  - Supports TLB chaining to extend the search but at a latency penalty
  - Supports a 48-bit address size
  - Supports page sizes of 4KB, 16KB, 64KB, 2MB, 32MB, 512MB, 1GB, and 16GB
  - Support TLBs in software mode, where they are maintained by software only
  - Produces a fault interrupt when the TLB misses or upon a permission error
- Mailbox module to facilitate the communication between the various on-chip processors of the device by providing a queued mailbox-interrupt mechanism with the following main features:
  - 12 clusters

  - 32-bit message width
  - Message reception and queue-not-full notification using interrupts
  - Non-intrusive emulation
- Spinlock module (256 hardware semaphores) for synchronizing the processes running on multiple processors in the device.
- Timer Manager modules to support timing operations for the processes running on multiple processors, with the following main features:
  - 1024 × 32-bit RAM-based independent timers (2048 in total)
  - Event interface to an interrupt aggregation module in the NAVSS subsystem with events triggering when a timer expires or when an expired timer is reset or deactivated
  - Host access to determine which timer(s) expired
  - 32 registers with individual timeout status (one bit per timer)
  - Groups of 16 timers separated into pages of 4-K address space
  - Timer bits within each page to read expiration status for each timer when software only has access to that page
  - 10 µs time to cycle through all of the timers
  - Host access to reset individual timers
  - Periodic hardware timers – a timer may be set to automatically reprogram itself upon expiration without software intervention.
- Time Sync modules to facilitate host control of time sync operations, each with the following main features:
  - Supports a selection of multiple external clock sources
  - Software control of time sync events via interrupt or polling
  - Supports 8 hardware timestamp push inputs
  - Supports timestamp counter compare output
  - Supports timestamp counter bit output
  - Supports 6 timestamp generator function outputs
  - 32-bit and 64-bit timestamp modes
- Memory Cyclic Redundancy Check module used to perform CRC to verify the integrity of a memory system with the following main features:
  - Four channels to perform background signature verification on any memory subsystem
  - Data compression on 8-, 16-, 32-, and 64-bit data size
  - Dedicated CRC value register per channel which contains the pre-determined CRC value
  - Timed base event trigger from timer to initiate DMA data transfer
  - Programmable 20-bit pattern counter per channel to count the number of data patterns for compression
  - Three modes of operation: Auto, Semi-CPU, and Full-CPU
  - Timeout interrupt generation if CRC is not performed within the time limit
  - Per channel DMA request generation to initiate CRC value transfer

1.2.9 Region-based Address Translation Module

The Region-based Address Translation (RAT) module performs a region based address translation of a 32-bit input address into a 48-bit output address. The RAT provides the following main features:

- 16 regions with dedicated registers for attributes configuration:
  - Region base address
  - Region size
  - Translated base address
- Address translation for only enabled regions
- Region boundary crossing transactions error generation

1.2.10 Data Routing Unit

The Data Routing Unit (DRU) is a high bandwidth, flexible routing engine with programmable DMA transfer requests which enables performing of high speed data transfers between memory mapped slave endpoints, processor caches and shared caches. It behaves like a DMA transfer controller, moving data at MPU frequency and has the following main features:

- Programmable configuration registers for direct transfer request submission

- Read and write command queues
- Programmable priority for each queue
- Two dedicated ports (one read and one write) to generate independent read and write commands
- Support for region based and channelized firewall
- Independent 48-bit address fields for source and destinations
- Up to four dimensional data transfers
- Error detection and Correction
- CMMU support for IO virtualization
- Compression for DDR bandwidth reduction in CNN application and video stream data from VPAC

1.2.11 Display Subsystem

The Display Subsystem (DSS) is a flexible composition-enabled display subsystem that supports multiple high resolution display outputs. It consists of the following main modules:

- Display Controller (DISPC), with the following main features:
  - Support of multi-layer blending and transparency for each of display outputs
  - Supports write-back pipeline with scaling to enable memory-to-memory composition and/or to capture a display output for Ethernet video encoding
  - Supports gamma correction and programmable color control in both source and destination pipelines
  - Embedded DMA Controller with the following main features:
    - Support for 1D-only DMA transfers
    - Support for 48b addressable memory space
    - Support for memory fragmentation through external PAT at SoC level
    - Integrated shared buffer management for pipelines within the same DMA controller group
    - Programmable DMA requests management
    - Support for source image flip along X and Y-axis
    - Support for secure access to firewall protected frame buffer in DDR memory
  - Two input display processing Video Pipelines, each supporting:
    - Wide range of input RGB source pixel formats
    - Wide range of input YUV source pixel formats
    - Programmable poly-phase filter (scaler)
    - Programmable color space conversion
    - Programmable Brightness/Contrast/Hue/Saturation
    - Programmable Gamma Correction LUT
    - Luma Key generation
    - 10-bit processing pipeline
  - Two input display processing Video Lite Pipelines, each supporting:
    - Wide range of input RGB source pixel formats
    - Wide range of input YUV source pixel formats
    - YUV420 to YUV422 chroma up-sampling using an average filter
    - YUV422 to YUV444 chroma up-sampling using a 4-tap filter based on Catmull-Rom algorithm
    - Programmable color space conversion
    - Programmable Brightness/Contrast/Hue/Saturation
    - Programmable Gamma Correction LUT
    - Luma Key generation
    - 10-bit processing pipeline
  - One Write-back (WB) pipeline, supporting:
    - Wide range of destination RGB pixel formats
    - Wide range of destination YUV pixel formats
    - Programmable poly-phase filter (scaler)
    - Output capture and Memory-to-memory (M2M) operation modes
  - Four Overlay Managers (OVR), each supporting:
    - Input pixel format: ARGB48-12121212
    - Output pixel format: ARGB48-12121212

    - Overlay of the input pipelines
    - Up to 5 input layers blending
    - Transparency color key
    - Alpha blending support: Embedded pixel alpha (ARGB and RGBA), global pixel, and combination of global pixel and pixel alpha
    - Z-order programmable (full flexibility)
    - Color bar test pattern insertion
    - Any overlay output can be selected to drive the Write-back pipeline
  - Four Video Port (VP) display outputs, each supporting:
    - 36-bit per pixel on the RGB output interface
    - Independent programmable timing generator, supporting up to 600 MHz pixel clock video formats
    - Independent programmable 10-bit gamma correction
    - Independent programmable multiple cycles output format on 8/9/12/16-bit interface
    - Selection between RGB and YUV422 output pixel
    - Configurable VP output mode
  - Internal diagnostic features:
    - Supports up to 4 programmable (position/size) check regions on the DISPC video port display outputs
    - Support for 1 check region on each input video pipeline output
    - MISR (Multiple Input Signature Register) used on each check region to perform data correctness check and/or freeze frame detection
  - Local power features:
    - Low power saving modes
    - On-the-fly Dynamic Frequency Scaling (DFS) support
    - Capability to associate all buffers a single pipeline for a display self-refresh
  - System interconnect ports:
    - Two 128-bit VBUSM master interfaces for data read/write
    - One 32-bit VBUSP slave interface for configuration
- Fram Buffer Decompression Core (FBDC), that performs a decompression on lossless compressed images on a tile-by-tile basis.
- MIPI Display Serial Interface (DSI) transmitter host controller, with the following main features:
  - Compliance with MIPI DSI 1.3.1 and previous protocol specifications
  - Compliance with Stereoscopic Display Format (SDF) specification
  - Video and command operational modes
  - Both burst and non-burst modes for video mode data transmission
  - Up to 4 virtual channels via command mode
  - Bi-directional communication and escape mode
  - Pixel clock rate range: 25-330 MHz
  - Programmable display resolutions
  - 16/18/24/30/36-bit RGB input data formats for video mode
  - RGB16, RGB18 packed, and RGB24 input data formats for command mode
  - All generic data types defined by MIPI
  - Display Command Set (DCS) transparent to the protocol engine
  - ECC on the APB interface
  - Data splitter for 2-,3-, or 4-data lane configuration
  - Connection to a single MIPI D-PHY complex I/O through an 8-bit Protocol Peripheral Interface (PPI)
  - Tearing effect (TE) input signals for command mode display
  - Bus contention recovery
  - Video mode pattern generator: color bar pattern image and D-PHY BET testing pattern
  - APB slave interface with 32-bit data and address for configuration
- The MIPI DSI Physical Layer (D-PHY) module with the following main features:
  - Compliance with MIPI D-PHY 1.2 physical layer interface specification and features
  - 1, 2 or 4 data lanes, in addition to clock signaling
  - Maximum data rate up to 2.5 Gbps per data lane
  - Protocol Peripheral Interface (PPI)

  - HS continuous and burst mode
  - Low-Power (LP), Ultra-Lower Power Mode (ULPM), and Shutdown modes
  - Forward direction and reverse direction escape modes
  - Automatic termination control in both high-speed and low-power modes
  - Single 32-bit VBUSP slave interface
- Embedded DisplayPort (eDP) transmitter host controller with the following main features:
  - Compliance with VESA® DisplayPort™ (DP) 1.3 (with 1.4 DSC/FEC support) specification
  - Compliance with VESA Embedded DisplayPort (eDP) 1.4 specification
  - Static configuration of either DP or eDP mode
  - Link rates up to High Bit Rate 3 (HBR3)
  - Pixel clock rate range: 25-600 MHz
  - 8, 10, and 12 bpc (bits per component), in RGB/YCbCr444 colorimetry formats (CEA-861 compliant) and YCbCr422 (via simple decimation)
  - Data splitter for 1-, 2-, or 4-data lane configuration
  - Single Stream Transport (SST)
  - Multiple Stream Transport (MST)
  - High-bandwidth Digital Content Protection (HDCP) data encryption via an embedded HDCP core
  - Display Stream Compression (DSC) encoded stream data transport via an embedded DSC core
  - Forward Error Correction (FEC) encoder with/without DSC enabled in DP mode
  - Single Stream Transport (SST)
  - Audio transport features
  - Metadata transport via Main Stream Attribute (MSA) packet or via SDP
  - APB slave ports for TX/PHY controller configuration
  - SAPB (secure) slave port for secure connection
  - Video source muxing options
  - One 32-bit VBUSP slave interface used for configuration
  - ECC on the critical memories
  - Parity check on the configuration interface
  - Encoder self-check diagnostics support in the DSC core
  - Injection of ECC and parity errors
- eDP (Physical Layer) SERDES and Aux PHY modules with the following main features:
  - DP1.3, HBR3 and eDP1.4a HBR3 throughput
  - 1, 2, or 4 lanes at 1.62Gbps, 2.7Gbps, 5.4Gbps, and 8.1Gbps per lane
  - Additional link rates (2.16, 2.43, 3.24, 4.32Gbps) per lane in eDP mode
  - Reduced differential voltage swing (0.2/0.25/0.30/0.35/0.40/0.45) in eDP mode
  - Hot Plug Detect (HPD) for connection detection and interrupt from sink
  - Integrated Low Jitter, Fixed Bandwidth PLL
  - DisplayPort physical layer functionalities:
    - Scrambler
    - 8/10-bit encoder (within the eDP transmitter)
    - Inter Lane Skew Insertion
    - Training Pattern Generation – TPS1,2,3,4 PRBS7 and 80-bit custom training pattern generation (bypassing the scrambler and encoder)
- 1 Mbps AUX PHY for link training, DPCD register access, HDCP authentication and EDID access

1.2.12 Camera Subsystem

Camera Subsystem unites three camera streaming interfaces – receiver and transmitter, allowing the device to stream video inputs from multiple cameras to the video processing accelerator (VPAC) or to internal memory and to output CSI-2 protocol image data to any device that supports MIPI CSI-2 protocol. Main modules are as follows:

- Camera Streaming Interface Receiver (CSI_RX_IF) with the following main features:
  - Compliant to MIPI CSI-2 v1.3+ and MIPI CSI-2 v2.0
  - Supports up to 16 virtual channels per input
  - Supports one 4MP camera or eight 2MP camera streams

  - Supports data rate up to 2.5 Gbps per lane (wire rate)
  - Supports 1, 2, 3, or 4 Data Lane connections to MIPI D-PHY Receiver (DPHY_RX)
  - Over 25 different programmable formats including YUV420, YUV422, RGB, Raw, and User Defined
  - Supports four independent (simultaneous) output streams:
    - Two VP 32-bit streams to VISS inputs of VPAC image processing accelerator
    - One (up to 4 channels) PPI 16-bit pixel retransmission interface to Camera Streaming Interface Transmitter (CSI_TX_IF)
    - One (up to 32 Channels) DMA interface through a 128-bit Packet Streaming Interface Link (PSI_L) connection to NAVSS for transfers to memory:
- Functional and data path error interrupts
- ECC support
- MIPI D-PHY Receiver (DPHY_RX) with the following main features:
  - Allows the device to input video streams from external sensor cameras and other CSI2 compliant sources
  - Compliant to MIPI D-PHY standard v1.2
  - Supports up to 4 data and 1 clock lanes
  - Supports up to 2.5 Gbps (with deskew) and 1.5 Gbps (without deskew) per data lane
  - Clock lane Control / Interface logic type: CIL-SCNN for HS and low power receiving
  - Data lane Control / Interface logic type: CIL-SFAN for HS and low power receiving
  - Data lanes can be independently operated in HS or ULP mode
  - Swapping of DP/DN signals within each clock/data pair
- Camera Streaming Interface Transmitter (CSI_TX_IF) with the following main features:
  - Compliant to MIPI CSI-2 v1.3+, MIPI CSI-2 v2.0, and MIPI D-PHY v1.2
  - Data rate up to 2.5 Gbps per lane (wire rate)
  - Supports 1, 2, 3, or 4 Data Lane connections to MIPI D-PHY Transmitter (DPHY_TX)
  - Over 25 different programmable formats including YUV420, YUV422, RGB, Raw, and User Defined
  - Support of 16 virtual channels
  - Support of four configurable input streams

1.2.13 Shared D-PHY Transmitter

The DPHY_TX module provides an option for video output interfacing by implementing a four lane, MIPI D-PHY Transmitter. DPHY_TX module supports the following main features:

- Compliancy to MIPI D-PHY Standard version 1.2
- Supports up to 4 data lanes
- Supports up to 2.5 Gbps (with deskew) and 1.5 Gbps (without deskew) per data lane
- Supports Escape mode
- Data Lanes can be independently operated in HS or ULP mode
- Includes a CMN block with reference generators / resistor calibration and an integrated PLL
- Fault detection

1.2.14 Central Multicore Shared Memory Controller

Central Multicore Shared Memory Controller (MSMC) provides high-bandwidth resource access both to and from all of the connected processing elements and the rest of the system and supports the following main features:

- 8MB (4 banks x 2MB) SRAM with ECC
- 512-bit processor port bus and 40-bit physical address bus
- Coherent unified bi-directional interfaces to connect to processors or device masters
- One infrastructure master interface
- Single external memory master interface
- Support of distributed virtual system
- Bandwidth management with starvation bound
- Two-level Quality-of-Service (QoS) support for real-time/non-real-time split
- Security firewall for SRAM/cache and external memory
- ECC error protection
- Trace and debug features
- Support of dynamic clock gating on all logic units

1.2.15 Local C7/MMA Multicore Shared Memory Controller

Local C7/MMA Multicore Shared Memory Controller (C7/MMA MSMC) provides high-bandwidth resource access both to and from each C7/MMA instance and the Central MSMC system and supports the following main features:

- 3MB Extended L2 SRAM with ECC
- 512-bit processor port bus and 40-bit physical address bus
- Closely coupled to C1/MMA with one local MSMC per C7/MMA instance
- All local MSMC instances connect to simple 512b MSMC crossbar (with no memory) to connect all C7/MMA instances to one Central MSMC port

1.2.16 DDR Subsystem

The DDR Subsystem (DDRSS) is used as an interface to external SDRAM devices which can be utilized for storing program or data. DDRSS provides the following main features:

- Support of LPDDR4 memory type
- 32-bit memory bus interface with in-line ECC
- Up to 8 GB per DDRSS across 2 ranks (4 GB per rank)
- System bus interface: little endian only with 256-bit data width
- Configuration bus Interface: little endian only with 32-bit data width
- Support of dual rank configuration
- Support of automatic idle power saving mode when no or low activity is detected
- Class of Service (CoS) - three latency classes supported
- Prioritized refresh scheduling
- Statistical counters for performance management

1.2.17 General Purpose Input/Output Interface

The General Purpose Input/Output (GPIO) modules provide dedicated general-purpose pins that can be configured as either inputs or outputs. Modules main features are:

- Support of 9 banks x 16 GPIO pins
- Support of up to 9 banks of interrupt capable GPIOs
- Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO pin
- Set/clear functionality per individual GPIO pin

1.2.18 Inter-Integrated Circuit Interface

The multi-master Inter-Integrated Circuit (I2C) interfaces support the following main features:

- Compliancy to the Philips I2C-bus specification version 2.1
- Support of standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Support of 7-bit and 10-bit device addressing modes
- Support of multi-master transmitter/slave receiver and receiver/slave transmitter modes
- Built-in FIFOs with programmable size of 8 to 64 bytes for buffered read or write
- 8-bit-wide data access
- Support of Auto Idle, Idle Request/Idle Acknowledge handshake, and Asynchronous Wakeup mechanisms
- Low power consumption

1.2.19 Improved Inter-Integrated Circuit Interface

The multi-master Improved Inter-Integrated Circuit (I3C) module supports the following main features:

- Supports Single Data Rate (SDR) and High Data Rate – Dual Data Rate (HD-DDR) communication modes
- Support of Common Command Codes (CCC)
- Hot-Join capability
- In Band Interrupts (IBI)
- Support of Dynamic Address Assignment (DAA)
- Support of Static Addressing (SA)
- FIFO Buffers
- Registers to store the parameters for the response to an IBI interrupt from a number of slaves

1.2.20 Multi-channel Serial Peripheral Interface

The Multi-channel Serial Peripheral Interface (MCSPI) module supports the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of MCSPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode
- Support of different master multichannel modes
- Single interrupt line for multiple interrupt source events
- Support of start-bit write command
- Support of start-bit pause and break sequence
- Built-in FIFO available for a single channel

1.2.21 Universal Asynchronous Receiver/Transmitter

The configurable Universal Asynchronous Receiver/Transmitter (UART) interface supports the following main features:

- 16C750-compatible
- Support of RS-485 external transceiver auto flow control
- Dual 64-byte FIFOs – one per each received and transmitted data paths
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Programmable sleep mode
- Baud rates up to 3.6 Mbps with 48 MHz functional clock
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Support of IrDA 1.4 Slow Infrared (SIR), Medium Infrared (MIR), and Fast Infrared (FIR) communications
- Support of Consumer Infrared Remote control mode (CIR) with programmable data encoding

1.2.22 Peripheral Component Interconnect Express Subsystem

The Peripheral Component Interconnect express (PCIe) subsystem with shared SerDes lines provides the following main features:

- Compliant to PCI-Express® Base Specification, Revision 4.0 (Version 0.7)
- 4-lane configuration with up to 8.0 Gbps/lane (Gen3). Can support up to 4x2 or 2x4 lanes.
- Gen3 (8 Gbps 128/130-bit encoding), Gen2 (5 Gbps 8/10-bit encoding), and Gen1 (2.5 Gbps 8/10-bit encoding) with auto-negotiation
- Dual mode: Root Port (RP) or End Point (EP) operation modes, selectable via bootstrap pins
- Dynamic PIPE width change when switching between Gen1/2/3 modes
- Constant 32-bit PIPE width for Gen1/2/3 modes
- Maximum payload size of 256 bytes
- Maximum remote read request size of 4KB
- Single-root I/O Virtualization (SR-IOV) with Physical Functions (PF) and Virtual Functions (VF) in End Point mode
- Maximum number of non-posted outstanding transactions: 32
- Resizable Base Address Registers (BAR) capability
- Separate Reference Clock with Independent Spread (SRIS)
- Legacy, MSI and MSI-X Interrupt Support
- 32 outbound address translation regions
- Precision time measurement (PTM)

1.2.23 Universal Serial Bus (USB) Subsystem

The Universal Serial Bus (USB) subsystem with integrated PHY has the following main features:

- Dual-Role Device (DRD) capability
- Compliance with USB 3.1 Gen1 Specification
- Support of Peripheral (aka Device) mode at Super Speed (SS at 5 Gbps), High Speed (HS at 480 Mbps), and Full Speed (FS at 12 Mbps)
- Support of Host mode at SS (5 Gbps), HS (480 Mbps), FS (12 Mbps), and Low Speed (LS at 1.5 Mbps)
- Support of Host Negotiation Protocol (HNP)
- Support of USB3 low power protocol states (U0, U1, U2, and U3)

- USB instance contains a single xHCI compliant with xHCI 1.0 specification with internal DMA controller
- ECC on internal RAMs
- Embedded USB 2.0 PHY

1.2.24 SerDes

The Serializer/Deserializer (SERDES) Multi-protocol Multi-link modules support the following main blocks:

- Quad lane PHY with common module for peripheral and Tx clocking handling
- Physical coding sub-block for data translation from/to the parallel interface, as well as data encoding/ decoding and ymbol alignment
- MUX module for device interfaces multiplexing into three SERDES lanes (Tx and Rx)
- A wrapper for sending control and reporting status signals from the SerDes and muxes

1.2.25 General Purpose Memory Controller with Error Location Module

The General-Purpose Memory Controller (GPMC) with Error Location Module (ELM) is dedicated for interfacing with external memory devices and has the following main features:

- Support of 8- or 16-bit-wide data path to external memory devices
- Supports up to 4 independent chip-select regions of programmable size and programmable base addresses on 16MB, 32MB, 64MB, or 128MB boundary in a total address space of 1GB
- Support of the following wide range of external memories/devices:
  - Asynchronous or synchronous 8-bit wide memory or device (non-burst device)
  - Asynchronous or synchronous 16-bit wide memory or device
  - 16-bit non-multiplexed NOR flash device
  - 16-bit address and data multiplexed NOR flash device
  - 8-bit and 16-bit NAND flash device
  - 16-bit pseudo-SRAM (pSRAM) device
- Supports various interface protocols when communicating with external memory or external devices:
  - Asynchronous read/write access
  - Asynchronous read page access (4, 8, and 16 Word16)
  - Synchronous read/write access
  - Synchronous read burst access without wrap capability (4, 8, and 16 Word16)
  - Synchronous read burst access with wrap capability (4, 8, and 16 Word16)
- Supports on-the-fly error code detection using the Bose-Chaudhuri-Hocquenghem (BCH) or Hamming code to improve the reliability of NAND with a minimum effect on software (NAND flash with 512-byte page size or greater)
- ELM module which used in a conjunction with the GPMC and provides ECC calculation (up to 16-bit) for NAND support and ability to work in both page-based and continuous modes, has the following main features:
  - 4, 8, and 16 bits per 512-byte block error-location, based on BCH algorithms
  - Eight simultaneous processing contexts
  - Page-based and continuous modes
  - Interrupt generation on error-location process completion

1.2.26 Multimedia Card/Secure Digital Interface

The Multimedia Card/Secure Digital (MMCSD) controller supports the following main features:

- 8-bit or 4-bit wide data bus, depending on instance
- Support of eMMC5.1 Host Specification (JESD84-B51)
- Support of SD Host Controller Standard Specification - SDIO 3.00
- Integrated DMA controller supporting SD Advanced DMA - ADMA2 and ADMA3
- eMMC Electrical Standard 5.1 (JESD84-B51)
- Multimedia card features:
  - Backward compatible with earlier eMMC standards
  - Legacy MMC SDR: 1.8 V, 8/4/1-bit bus width, 0-25 MHz, 25/12.5/3.125 MB/s
  - High Speed SDR: 1.8 V, 8/4/1-bit bus width, 0-50 MHz, 50/25/6.25 MB/s
  - High Speed DDR: 1.8 V, 8/4-bit bus width, 0-50 MHz, 100/50 MB/s

  - HS200 SDR: 1.8 V, 0-200 MHz, 8/4-bit bus width, 200/100 MB/s
- SD card support: SDIO, SDR12, SDR25, SDR50, DDR50
- System bus interface: CBA 4.0 VBUSM master port with 64-bit data width and 64-bit address, little endian only
- Configuration bus interface: CBA 4.0 VBUSM with 32-bit data width, 32-bit aligned accesses only, linear incrementing addressing mode, little endian only

1.2.27 Universal Flash Storage Interface

Device MAIN domain supports one standard-based serial interface engine - Universal Flash Storage (UFS) interface with an integrated M-PHY. UFS provides the following main features:

- Support of Universal Flash Storage Host (UFS2.1, JESD220C)
- Support of Universal Flash Storage Host Controller Interface (UFSHCI, JESD223C)
- Support of UFS interconnect - MIPI UniPro (v.1.60, 2013) and MIPI M-PHY (v3.1, 2014)
- Supports speeds 1.46 Gbps (Gear 1), 2.91 Gbps (Gear 2) and 5.83 Gbps (Gear 3), 2-lanes
- Support of all UFS mandatory SCSI commands required by JEDEC specification
- Master bus Interface: one 64-bit master interface for data transfers, 48-bit address width, embedded
- DMA within the host controller with support of little-endian mode only
- Configuration Bus Interface: one 32-bit slave interface for configuration access, support of linear incrementing addressing mode and only aligned accesses
- ECC support on internal RAMs
- M-PHY Features: supports reference clocks of 19.2 MHz and 26 MHz

1.2.28 Enhanced Capture Module

The Enhanced Capture (ECAP) module provides accurate timing for different events. When not being used for event capture, its resources can be used to generate a single channel of asymmetrical PWM waveforms (configurable as either one capture input, or as one auxiliary PWM output). The ECAP module supports the following main features:

- 32-bit time base counter
- 4 x 32 bits event time-stamp capture registers
- 4 stage sequencer (Mod4 counter), synchronized to external events
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Input capture signal pre-scaling (from 1 to 16)
- Interrupt capabilities on any of the four capture events
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or delta mode time-stamp capture)

1.2.29 Enhanced Pulse-Width Modulation Module

The Enhanced Pulse-Width Modulation (EPWM) module supports the following main features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs that can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals through software
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

1.2.30 Enhanced Quadrature Encoder Pulse Module

The 32-bit Enhanced Quadrature Encoder Pulse (EQEP) module for position, speed, and frequency measurements supports the following main features:

- Input synchronization
- Three stage/six stage digital noise filter
- Quadrature decoder unit
- Position counter and control unit for position measurement

- Quadrature edge capture unit for low speed measurement
- Unit time base for speed/frequency measurement
- Watchdog timer for detecting stalls

1.2.31 Controller Area Network

The Controller Area Network (MCAN) interface supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications and has the following main features:

- Conforms with CAN Protocol version 2.0 part A, B and ISO 11898-1:2015
- Full CAN FD (up to 64 data bytes) support
- SAE J1939 support
- AUTOSAR support
- Up to 32 dedicated transmit buffers and 64 dedicated receive buffers
- Two configurable receive FIFOs, up to 64 elements each
- Configurable transmit FIFO, up to 32 elements
- Configurable transmit queue, up to 32 elements
- Configurable transmit event FIFO, up to 32 elements
- Up to 128 filter elements
- Maskable interrupts, two interrupt lines
- Timestamp Counter

1.2.32 Audio Tracking Logic

The Audio Tracking Logic (ATL) module, which is used by HD Radio™ applications to synchronize the digital audio output to the baseband clock, supports the following main features:

- Contains four ATL instances, for HD Radio support and asynchronous sample rate conversion assistance
- Each instance tracks the time error between two syncs (local Audio Word Select [AWS] and Baseband Word Select [BWS])
- Each instance selects between 8 mux choices for BWS and 8 mux choices for AWS
- Each instance generates modulated ATCLK clock signals with software-initiated pulse stealing
- Selection between interface or functional clock to run error counting timers and to derive modulated clock outputs
- Clock and reset management: receives clock and reset signals from the device PSC module
- Hardware reset
- Local software reset

1.2.33 Multi-channel Audio Serial Port

The Multi-channel Audio Serial Ports (MCASP) is a general purpose audio serial port, useful for Time-Division Multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component Digital audio Interface Transmission (DIT). The MCASP module has the following main features:

- Connection to audio Analog-to-Digital Converters (ADC), Digital-to-Analog Converters (DAC), codec, digital audio interface receiver (DIR), and Sony/Philips Digital Interface (S/PDIF) transmit physical layer components
- Support of Time Division Multiplexed (TDM) interface, Inter-IC Sound (I2S) standard, and similar bit stream formats
- Integrated Digital Audio Interface Transmitter (DIT) with enhanced channel status/user data RAM and support of S/PDIF, IEC60958-1, and AES-3 formats
- Independent serializer for each AXRx channel of each MCASP module
- A single 32-bit buffer per serializer for transmit and receive operations
- Support for two DMA requests (one per direction)
- One transmit and one receive interrupt requests common for all serializers
- Two independent clock generator modules for transmit and receive allowing the MCASP to receive and transmit at different rates
- Support of up to 16 serial data pins

1.2.34 Timers

There are three different types of timer modules:

- The Global Time Counter (GTC) module can be used for time synchronization and debug trace time stamping with the following main features:
  - 64-bit up counter
  - No rollover during the lifetime of the device
  - Compatible with Armv8 system counter requirements
  - Outputs reflected binary (Gray) encoded timer value for system timer bus distribution to other modules
  - Selectable counter bit output as a push event that can be used by CPTS modules, timers or interface protocols
- The Windowed Watchdog Timer (WWDT), implemented by using the Digital Windowed Watchdog (DWWD) function of the Real Time Interrupt (RTI) module providing timer functionality for operation systems and benchmarking code with the following main features:
  - Two independent 64 bit counter blocks
  - Four configurable compare registers for generating operating system ticks
  - Free running counter 0 can be incremented by either the internal prescale counter or by an external event
  - Selectable RTI clock input (derived from any of the available clock sources)
  - Fast enabling/disabling of events
- The Timer module with support of the following main features:
  - Free running 32-bit upward counter
  - Generates a 1-ms tick with a 32.768 kHz functional clock
  - Interrupts generated on overflow, compare and capture
  - Supported modes of operation: compare and capture, auto-reload and start-stop
  - Programmable divider clock source (2^n, where n = [0-8])
  - Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
  - On-the-fly read/write register (while counting) for systems operation and benchmarking code

1.2.35 Internal Diagnostics Modules

Internal diagnostics modules provide monitoring and diagnostic functions required to achieve certain safety compliance levels:

- Dual Clock Comparator (DCC) modules, used to determine the accuracy of a clock signal during the time execution of an application, each having the following main features:
  - Two independent counter blocks count clock pulses from each clock source
  - Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
  - Configurable time base for error signal
  - Error signal generation when one of the clocks is out of specification
  - Clock frequency measurement
- Error Signaling Module (ESM) for safety-related events and/or errors aggregation from throughout the device into one location supports the following main features:
  - Up to 1024 level or pulse error event inputs
  - Selectable low and high priority interrupt error pin prioritization of each error event
  - Error pin to signal severe device failure
  - Configurable time base for error signal
  - Error forcing capability
  - Internal redundant flops on safety critical fields
- ECC aggregator modules supporting ECC mechanism for providing increased system reliability via reduction of memory software errors by allowing single bit errors to be detected and corrected (SEC) and double bit errors to be detected (DED). Applied to different memories in many of the subsystems, each of the ECC aggregators has the following main features:
  - Reduces memory software errors via single error correction (SEC) and double error detection (DED)
  - Provides a mechanism to control and monitor the ECC RAMs in a module or subsystem
  - Supports software readable status of ECC errors (single and double-bit) and associated info such as RAM address and data bit or bits that are in error
  - Aggregates level pending status from the ECC RAMs in two interrupts to the device CPU – interrupt for correctable error (SEC) and interrupt for uncorrectable error (DED)

  - Supports up to 256 ECC endpoints (either ECC RAM or interconnect ECC component)
  - Single bit error detection via parity checking results in a non-correctable error interrupt
- Memory Cyclic Redundancy Check (MCRC) module used to perform CRC to verify the integrity of a memory system – part of the NAVSS

1.2.36 Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) module contains a single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels) and supports the following main features:

- 4 MSPS rate with a 60 MHz sample clock
- Single-ended or differential input options
- ADC module can be configured and transformed into digital test inputs
- Programmable 16 steps Finite State Machine (FSM) sequencer

1.2.37 Two-Port Gigabit Ethernet Switch

The 2-port Gigabit Ethernet Switch (CPSW2G) subsystem provides Ethernet packet communication for the device, and has the following main features:

- One Ethernet port (port 1) with selectable RGMII and RMII interfaces and an internal Communications Port Programming Interface (CPPI) port (port 0)
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Eight priority level Quality Of Service (QOS) support (802.1p)
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
- DSCP Priority Mapping (IPv4 and IPv6)
- IPV4/IPV6 UDP/TCP checksum offload
- Energy Efficient Ethernet (EEE) support (802.3az)
- Priority-Based Flow Control (802.1QBB) and Flow Control (802.3x) Support
- Wire rate switching (802.1d)
- Non-Blocking switch fabric
- Time Sensitive Network Support
- Address Lookup Engine (ALE)
- EtherStats and 802.3Stats Remote Network Monitoring (RMON) statistics gathering (per port statistics)
- Ethernet Mac transmit to Ethernet Mac receive Loopback mode (digital loopback) supported
- CPSGMII Loopback Modes (transmit to receive)
- Maximum frame size of 2024 bytes
- Management Data Input/Output (MDIO) module for PHY Management with Clause 45 support
- Programmable interrupt control with selected interrupt pacing
- Host port CPPI Streaming Packet Interface (CPPI_GCLK)
- Digital loopback and FIFO loopback modes supported
- Emulation support
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps modes only
- RAM Error Detection and Correction (SECDED)

1.2.38 Nine-Port Gigabit Ethernet Switch

The 9-port Gigabit Ethernet Switch (CPSW9G) subsystem provides Ethernet packet communication for the device, and has the following main features:

- Eight Ethernet ports with selectable SGMII, XFI, QSGMII and USXGMII interfaces and an internal Communications Port Programming Interface (CPPI) port
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Eight priority level Quality Of Service (QOS) support (802.1p)
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
- Ethernet port reset isolation

- DSCP Priority Mapping (IPv4 and IPv6)
- IPV4/IPV6 UDP/TCP checksum offload
- Energy Efficient Ethernet (EEE) support (802.3az)
- Priority-Based Flow Control (802.1QBB) and Flow Control (802.3x) Support
- Wire rate switching (802.1d)
- Non-Blocking switch fabric
- Time Sensitive Network Support
- Address Lookup Engine (ALE)
- EtherStats and 802.3Stats Remote Network Monitoring (RMON) statistics gathering (per port statistics)
- CPSGMII Loopback Modes (transmit to receive)
- Maximum frame size of 2020 bytes
- Host port CPPI Streaming Packet Interface (CPPI_GCLK)
- Digital loopback and FIFO loopback modes supported
- Emulation support
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps modes only
- RAM Error Detection and Correction (SECDED)

1.2.39 Octal Serial Peripheral Interface and HyperBus Memory Controller as a Flash Subsystem

The Flash Subsystem (FSS) provides access to external flash devices via Octal Serial Peripheral Interface (OSPI) and HyperBus interface along with encryption/decryption, authentication, and in-line ECC protection. FSS supports the following main features:

- Provides two OSPIs or one OSPI and one HyperBus flash interfaces
- OSPI0/HyperBus interface supports:
  - Execute in place (XIP) operation
  - 32-byte Block Copy (BC) operation
  - ECC and/or authentication with four configurable authentication regions and authentication on 32-byte blocks
- OSPI supports up to 4 devices
- OSPI supports single, dual, quad, or octal SPI devices
- HyperBus interface supports up to 2 devices
- The OSPI and HyperBus interface have independent power management for low power operations

1.2.40 Security Management Subsystem

The Security Management Subsystem (SMS) which provides control over the device boot sequencing, device management, and security. With the factory-sealed firmware, SMS main functions include:

- Device management (security only)
- Device boot configuration and sequence
- Secure boot setup
- Decryption routines
- Firewall control for isolation and Security
- Runtime Security Management and resource allocation

Arm Cortex-M4F based SMS acts as a system security master and protects critical security assets during run-time. As part of booting a High Security (HS) device, SMS uses on-chip keys to establish root-of-trust and authenticate images to reinforce trust. SMS acts also as main boot processor and as such is the very first subsystem that is brought out of reset after device power-on-reset.

Main components of the SMS are:

- Two independent M4F processor cores with floating point extension (primary and secondary)
- M4F primary core features include:
  - RTI/WDT (only digital watchdog (non-windowed) feature is supported in SMS primary core context)
  - 128KB IMEM and 48KB DMEM, accessible from M4F primary core and system masters via firewall
  - Messaging between M4F core and host processors using Secure Proxy and RA located in MCU_NAVSS and MAIN NAVSS.

  - 160KB ROM for boot of M4F core
- M4F secondary core features include:
  - Dedicated RTI/WWDT (with windowed watchdog mode, disabled by default)
  - 192KB IMEM and 64KB DMEM, accessible from M4F secondary core and system masters via firewall
  - Messaging between M4F secondary core and up to five host cores (including primary core and 4 other device level cores) using Secure Proxy and RA
- Common features of both M4F primary and secondary cores:
  - Following resources can be accessed from either primary or secondary core with permissions via firewall:
    - Four 32-bit Timers - same as SOC level timers
    - AES engine with 128, 192 and 256-bit support
    - Security Manager
    - SMS control module - contains various control, configuration and status MMRs including firewall management for the full device
  - Other core features:
    - Ability to execute code from unified memory or external memories
    - Up to 240 input interrupts, level or pulse interrupts, capable of waking up the SMS cores from low power mode
    - Two interrupt outputs (per M4F core) to host SOC; support of both level and pulse interrupts
    - One fault detected interrupt output (per M4F core); support of both level and pulse interrupts
    - DAP based debug interface to the M4F core
    - ITM trace to chip level trace framework
    - Support of double detection and single error correction
    - Support of Little Endian mode only
    - In addition to local SMS RAM, the SMS M4F cores may utilize MSMC memory space as secure RAM via firewall

1.3 Device Identification

The JTAGID and JTAG_USER_ID can be used to identify the J784S4 and J742S2 devices. The register values are summarized in Table 1-2.

Table 1-2. Device Identifcation Mapping

Register	Address	Bitfield	Value	Description
CTRL_MMR_CFG0_JTAGID	4300 0014h	[31-28] VARIANT	0x0	Silicon Revision 1.0
		[27-12] PARTNO	0xBB80	Boundary Scan identifier for J784S4 and J742S2
		[11-1] MFG	0x17	Manufacturer - TI
		[0] LSB	0x1	Always Reads 1
CTRL_MMR_CFG0_JTAG_USER_ID	4300 0018h	[2-0] PKG	0x5	J784S4 device in ALY 31mm package
			0x7	J742S2 device in AND 27mm package

2 Device Comparison

Table 2-1 shows the features of the SoC.

Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the TDA4VH Software Build Sheet (PROCESSOR-SDK-J784S4).

Table 2-1. Device Comparison

FEATURES	REFERENCE NAME	J784S4 TDA4VH88	J742S2 TDA4VPE4
PROCESSORS AND ACCELERATORS			
Speed Grades		T	T
Arm Cortex-A72 Microprocessor Subsystem	Arm A72	Octal Core	Quad Core
Arm Cortex-R5F	Arm R5F	Octal Core	
	Lockstep	Optional	
Security Management	SMS	Yes	
Security Accelerators	SA	Yes	
C7x Floating Point, Vector DSP	C7x DSP	Quad Core	Tri Core
Deep Learning Accelerator	MMA	Quad Core	Dual Core
Graphics Accelerator IMG BXS-4-64	GPU	Yes	
Depth and Motion Processing Accelerators	DMPAC	Yes	
Vision Processing Accelerators	VPAC	2	
Video Encoder / Decoder	VENC/ VDEC	Enc/Dec 960 MP/s	
SAFETY AND SECURITY			
Safety Targeted	Safety	Optional	
Device Security	Security	Optional	
AEC-Q100 Qualified	Q1	Optional	
PROGRAM AND DATA STORAGE			
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	3x512KB SRAM	
On-Chip Shared Memory (RAM) in MCU Domain	MCU_MSRAM	1MB SRAM	
Multicore Shared Memory Controller	MSMC	8MB (On-Chip SRAM with ECC)	4MB (On-Chip SRAM with ECC)
LPDDR4 DDR Subsystem	DDRSS0	32-b w/ inline ECC	
	DDRSS1	32-b w/ inline ECC	
	DDRSS2	32-b w/ inline ECC	No
	DDRSS3	32-b w/ inline ECC	No
	SECDED	7-Bit	
General-Purpose Memory Controller	GPMC	Yes	
PERIPHERALS			
Display Subsystem	DSS	Yes	
	DSI 4L TX	2	
	eDP 4L	1	
	DPI	1	
Modular Controller Area Network Interface with Full CAN-FD Support	MCAN	20	
General-Purpose I/O	GPIO	155	
Inter-Integrated Circuit Interface	I2C	10	
Improved Inter-Integrated Circuit Interface	I3C	1	
Analog-to-Digital Converter	ADC	2	

Table 2-1. Device Comparison (continued)

FEATURES	REFERENCE NAME	J784S4 TDA4VH88	J742S2 TDA4VPE4
Capture Subsystem with Camera Serial Interface (CSI2)	CSI2.0 4L RX	3	
	CSI2.0 4L TX	2	
Multichannel Serial Peripheral Interface	MCSPI	11	
Multichannel Audio Serial Port	MCASP0	16 Serializers	
	MCASP1	5 Serializers	
	MCASP2	5 Serializers	
	MCASP3	3 Serializers	
	MCASP4	5 Serializers	
MultiMedia Card/ Secure Digital Interface	MMCSD0	eMMC (8-bits)	
	MMCSD1	SD/SDIO (4-bits)	
Universal Flash Storage	UFS 2L	Yes	
Flash Subsystem (FSS)	OSPI0	8-bits	
	OSPI1	4-bits	
	HyperBus	Yes	
4x PCI Express Port with Integrated PHY	PCIE	2x4L or 4x2L	1x4L or 2x2L
Ethernet Interfaces	MCU CPSW2G	RMII or RGMII	
	MAIN CPSW2G	RMII or RGMII	
	CPSW9G	8 port SERDES	4 port SERDES
General-Purpose Timers	TIMER	30	
Enhanced High Resolution Pulse-Width Modulator Module	eHRPWM	6	
Enhanced Capture Module	eCAP	3	
Enhanced Quadrature Encoder Pulse Module	eQEP	3	
Universal Asynchronous Receiver and Transmitter	UART	12	
Universal Serial Bus (USB3.1) SuperSpeed Dual-Role-Device (DRD) Ports with SS PHY	USB0	Yes	

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