Test Report: PMP23146

45-W High-Power-Density Active Clamp Flyback With GaN Reference Design for Server Auxiliary Power

Description

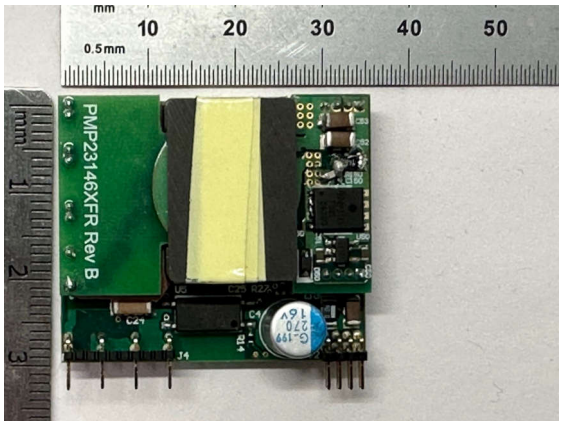
This reference design is a GaN-based 45-W active clamp flyback (ACF) providing auxiliary power in server and telecom power supply units (PSU). The UCC28782 ACF controller and LMG2610 GaN half-bridge drive a planar transformer with synchronous rectification using the UCC24612. This supply operates using the PFC bus voltage as an input, and generates an isolated 12-V, 3.7-A output, and a non-isolated 18-V, 400-mA output. The main 12-V output is protected by the TPS74800 ORing controller. Multiple PMP23146 units can be operated in parallel for higher power capability.

Features

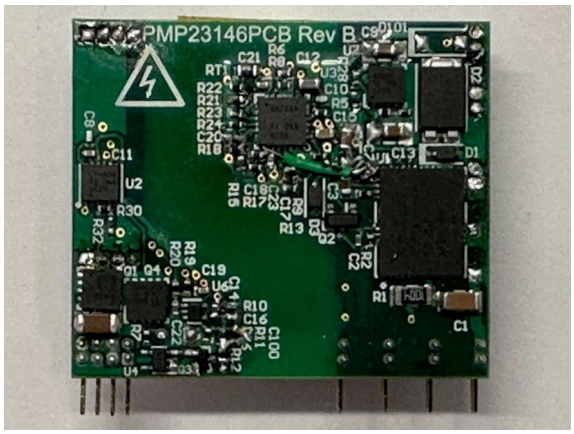
- High-frequency (400 kHz) GaN ACF design with planar transformer
- Compact size (30 mm × 35 mm × 12 mm) and high power density (60 W/in^3)
- Parallel design is possible for higher power capability
- Low standby power consumption (< 100 mW)
- Additional non-isolated 18-V output provided

Applications

- Merchant network and server PSU



Top Photo



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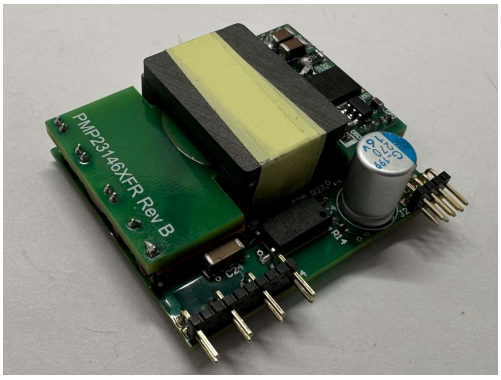

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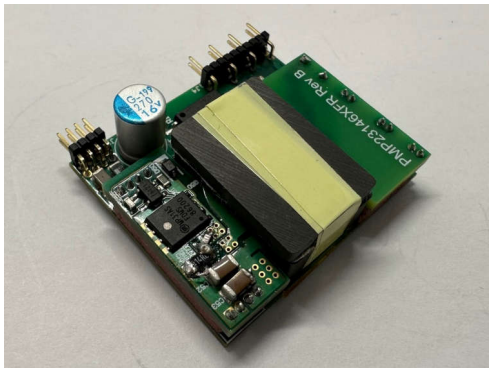

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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage range (Full rated power)	250 VDC–410 VDC
Extended input voltage range (50% Rated power)	100 VDC–410 VDC
12VSB and S12V maximum load current (combined)	3.7 A
P18V maximum load current (see Figure 1-1 for minimum load requirements on 12VSB and S12V)	400 mA
Worst-case 12VSB load current mismatch between 2 paralleled units (calculated)	30%

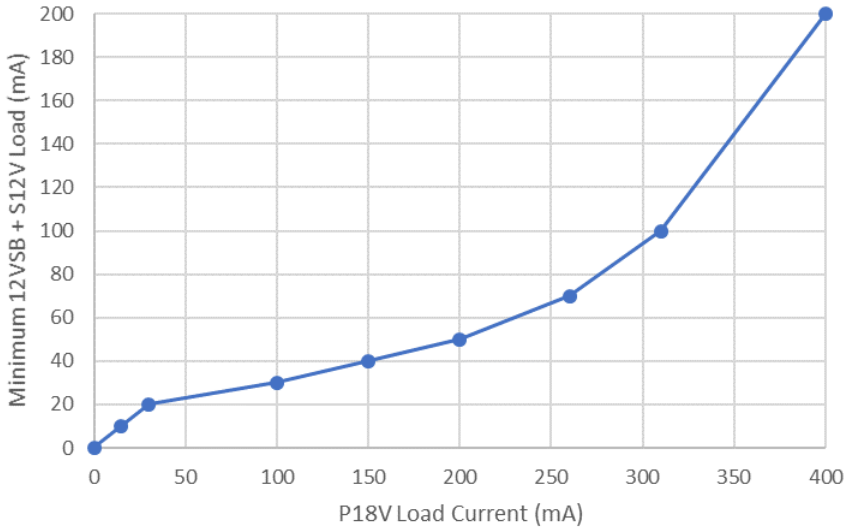

Figure 1-1. P18V Minimum Load Requirements

1.2 Functional Block Diagram

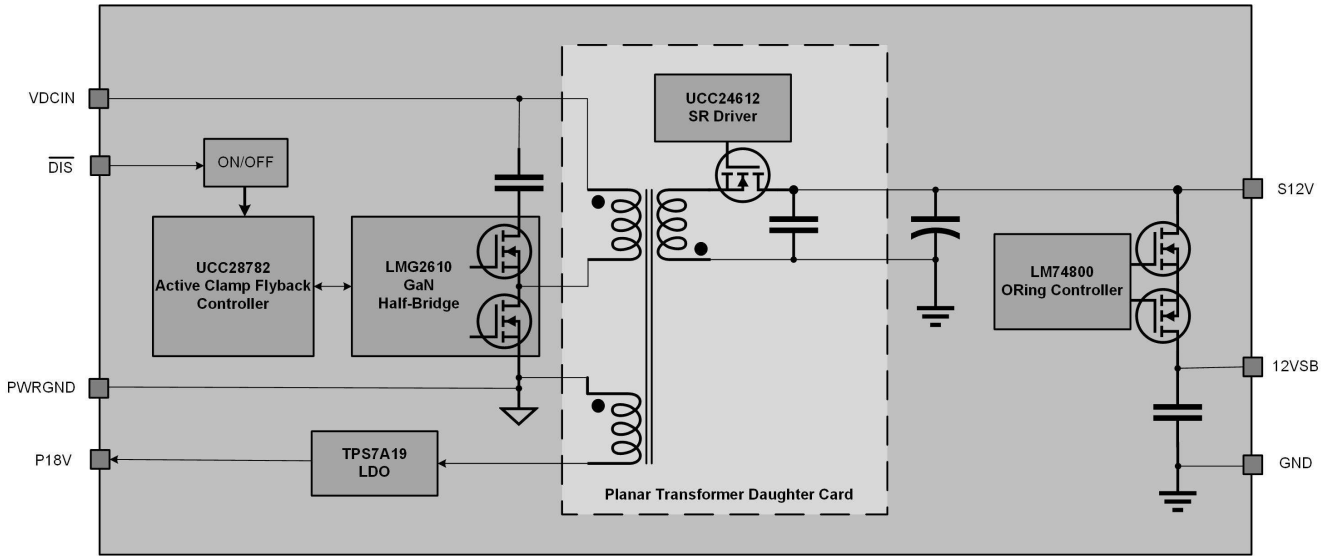

Figure 1-2. Functional Block Diagram

1.3 Pin Functions

Table 1-2 provides the functional descriptions of the pins.

Table 1-2. Pin Functional Descriptions

Pin Name	Pin Number	Description
12VSB	J2: pins 3, 4, 6	Main 12-V output. The combination of 12VSB and S12V are capable of supplying up to 3.7 A. The 12VSB output is separated from the S12V output by back-to-back FET controlled by the TPS74800 ORing controller, allowing the 12VSB outputs from multiple supplies to be connected in parallel.
DIS	J4: pin 14	Disable signal. This is an active-low, open-drain signal. Connecting this pin to PWRGND disables switching of the UCC28782 and turns off all outputs.
GND	J2: pins 5, 7, 8	Return path for 12VSB and S12V and all secondary referenced circuits.
P18V	J4: pin 20	Auxiliary 18-V output referenced to PWRGND. This output is capable of supplying up to 400 mA, but does require some minimum load on the 12VSB and S12V outputs to avoid abnormal operation. The P18V output voltage can range between 15 V and 18 V.
PWRGND	J4: pins 7, 13, 19	Return path for VDCIN and all primary referenced circuits.
S12V	J2: pin 2	Auxiliary 12-V output referenced to GND. The combination of 12VSB and S12V are capable of supplying up to 3.7 A.
VDCIN	J4: pins 1, 2	DC input. Connect these pins to the input power source, normally the output of a PFC pre-regulator.

2 Waveforms

2.1 Switching Frequency and Operating Modes

The UCC28782 device has several operating modes that are dependent on the loading conditions. These different operating modes are optimized to provide high efficiency across the entire load range. A brief description of the different operating modes is provided here, along with associated waveforms measured on this reference design. For more details, see the *UCC28782 High-Density Active-Clamp Flyback Controller with EMI Dithering, X-Cap Discharge, and Bias Power Management* data sheet.

At maximum load, the UCC28782 is operating in Adaptive Amplitude Modulation (AAM) mode. In this mode, the converter is basically in transition mode and provides ZVS on every switching cycle.

As the load is decreased in AAM, the switching frequency increases due to the transition mode of operation. Once the frequency reaches a programmed maximum frequency, the converter enters Adaptive Burst Mode (ABM) operation. In ABM, the switching frequency remain fixed, and is sub-modulated at a lower burst frequency. In ABM, the first pulse in a burst packet is non-ZVS, but all other switching pulses are ZVS.

As the load is decreased in ABM, the number of switching pulses per burst packet are reduced to keep the burst frequency from entering the audible range. Once the number of pulses reaches two per packet, a further reduction in load causes the converter to enter Low Power Mode (LPM). In LPM, the active clamp switch is disabled to save power consumption, the number of pulses per burst packet is fixed at two, and the peak current is reduced. The reduction in peak current causes the switching frequency to increase as the load is decreased.

As the load continues to decrease in LPM, once the switching frequency reaches another clamping level, the converter enters Standby Power 1 (SBP1) mode of operation. In SBP1, the peak current once again becomes fixed, the number of pulses are fixed at two per burst packet, and the burst frequency is allowed to reduce lower.

At near-no-load operation, the converter transitions from SBP1 to Standby Power 2 (SBP2) mode of operation. In SBP2 mode, the number of pulses per burst packet is increased to four, and the peak current is increased. This allows the converter to operate at extremely low burst frequencies to minimize the no load power consumption.

In all the following figures, the input voltage was 390 VDC, and no load was applied to P18V and S12V.

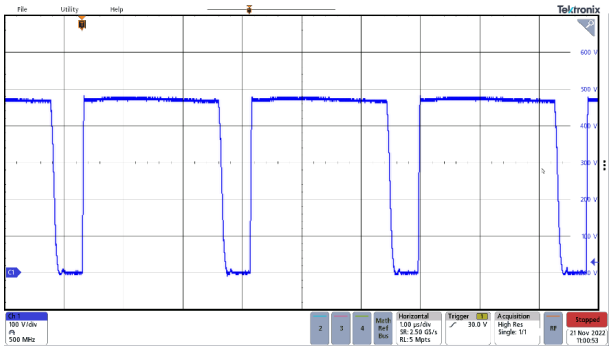

Figure 2-1. Primary Switch Node Voltage in AAM (3.7 A on 12VSB)

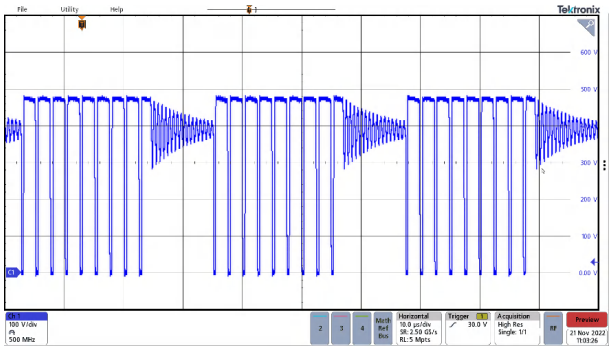

Figure 2-2. Primary Switch Node Voltage in ABM, Near ABM-AAM Boundary (2.0 A on 12VSB)

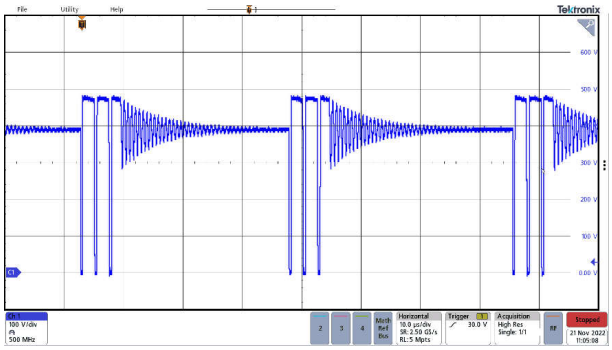

Figure 2-3. Primary Switch Node Voltage in ABM, Near LPM-ABM Boundary (600 mA on 12VSB)

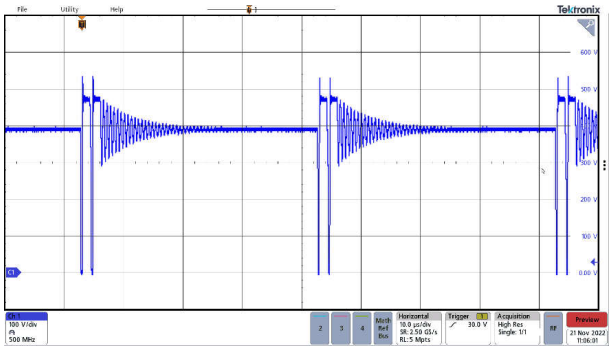

Figure 2-4. Primary Switch Node Voltage in LPM (250 mA on 12VSB)

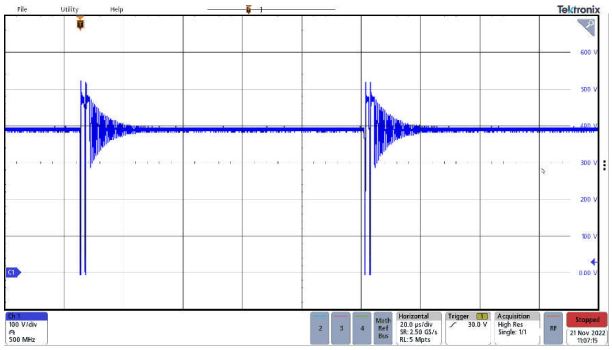

Figure 2-5. Primary Switch Node Voltage in SBP1 (100 mA on 12VSB)

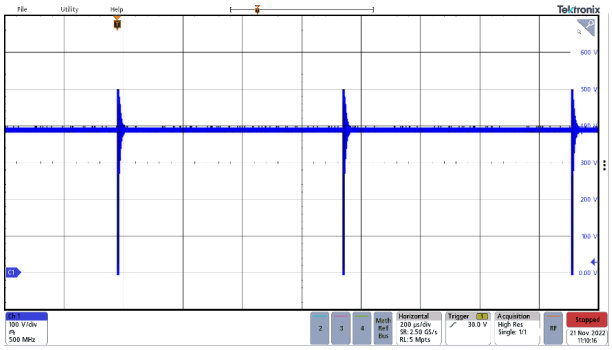

Figure 2-6. Primary Switch Node Voltage in SBP2 (20 mA on 12VSB)

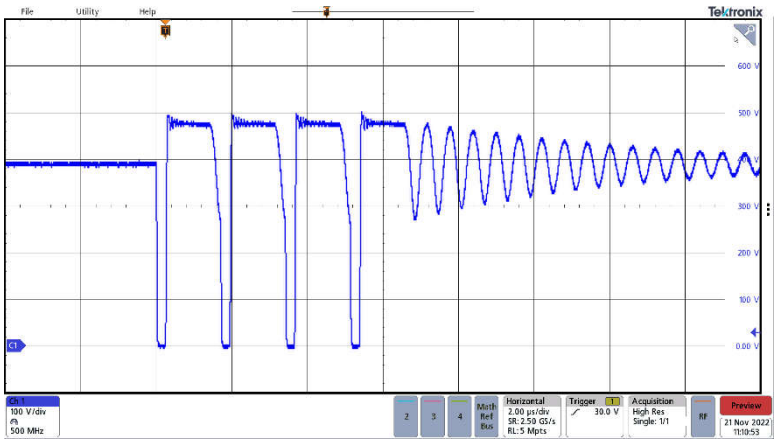

Figure 2-7. Primary Switch Node Voltage in SBP2 (Zoom) (20 mA on 12VSB)

2.2 Output Voltage Ripple

The output ripple voltage has a high frequency component due to the switching frequency and a lower frequency component due to the burst frequency in all operating modes except AAM. The following figures show the output ripple in the different modes of operation. A system capacitance of 1000-µF was connected to 12VSB, and 100-µF was connected to P18V, respectively. For all figures, the input was 390 VDC and no load was applied to P18V and S12V.

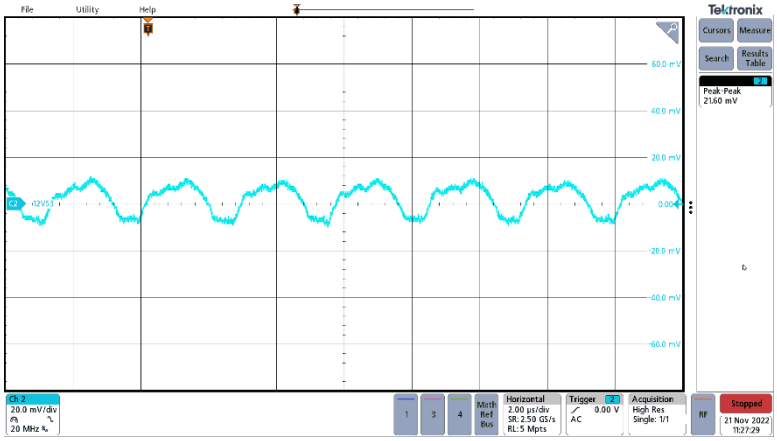

Figure 2-8. Output Voltage Ripple in AAM (3.7 A on 12VSB)

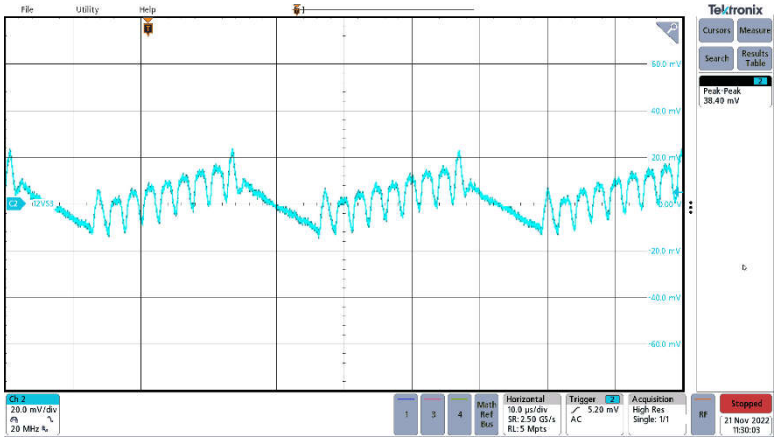

Figure 2-9. Output Voltage Ripple in ABM (2.0 A on 12VSB)

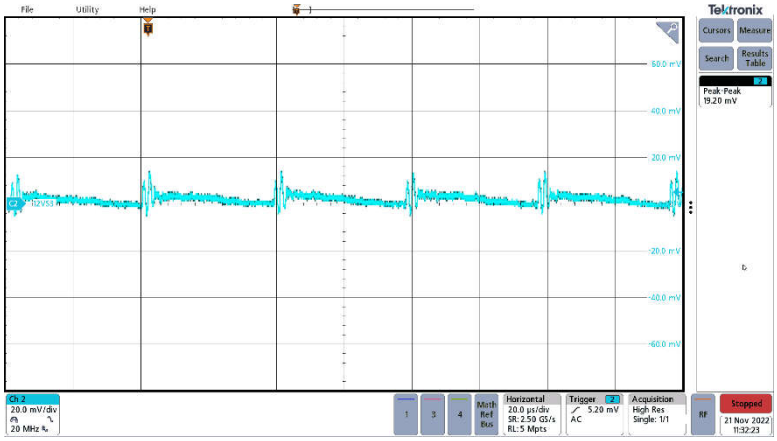

Figure 2-10. Output Voltage Ripple in LPM (250 mA on 12VSB)

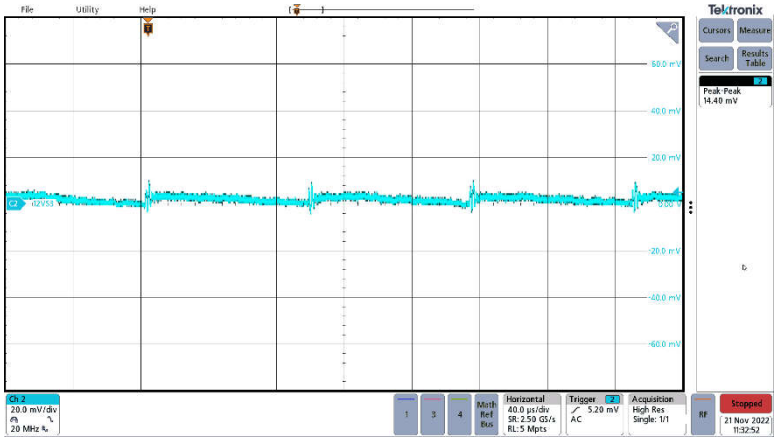

Figure 2-11. Output Voltage Ripple in SBP1 (100 mA on 12VSB)

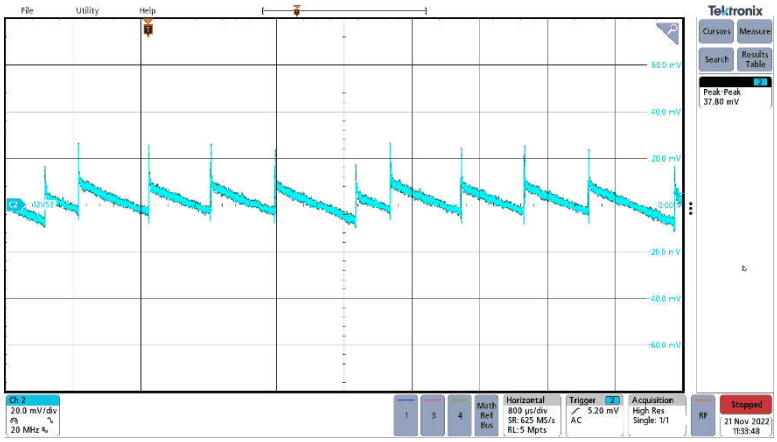

Figure 2-12. Output Voltage Ripple in SBP2 (20 mA on 12VSB)

2.3 Load Transients

Load transient response is shown in the following figures. The load step was applied to the 12VSB output. The input voltage was 390 VDC, and both P18V and S12V were unloaded. A system capacitance of 1000-µF was connected to 12VSB, and 100-µF was connected to P18V, respectively. Channel 2 shows the 12VSB output voltage, AC coupled. Channel 4 shows the 12VSB load current.

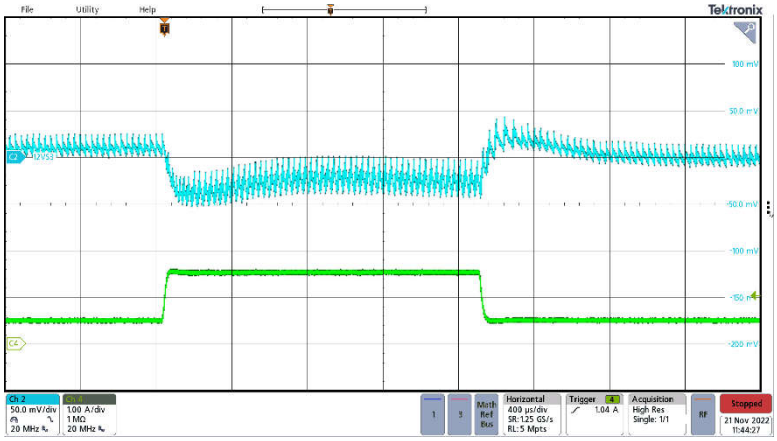

Figure 2-13. Load Transient (500 mA to 1.5 A)

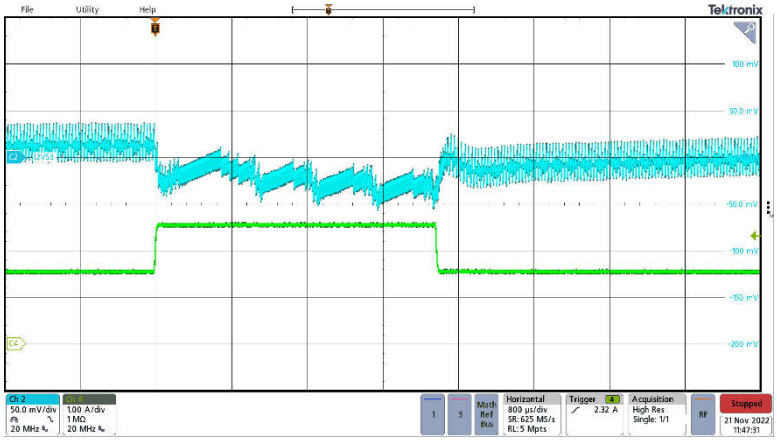

Figure 2-14. Load Transient (1.5 A to 2.5 A)

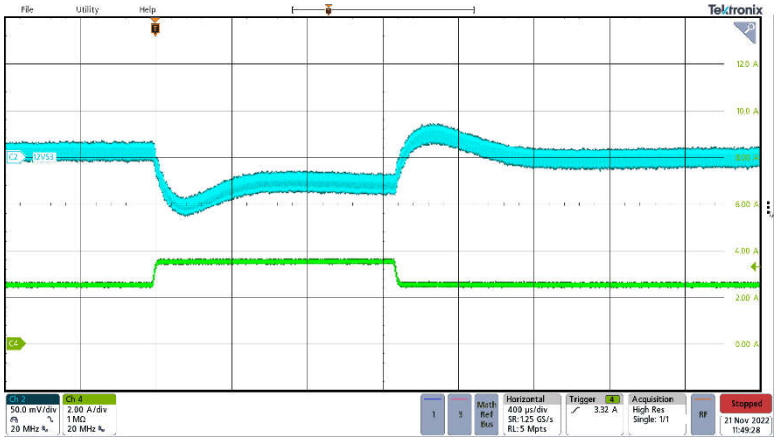

Figure 2-15. Load Transient (2.5 A to 3.5 A)

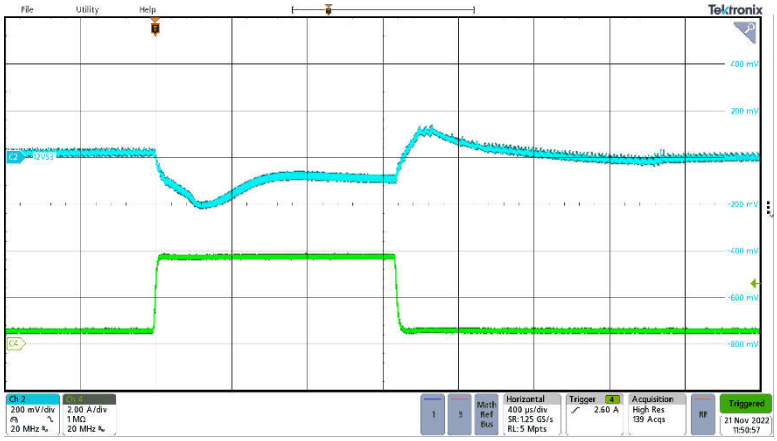

Figure 2-16. Load Transient (500 mA to 3.7 A)

2.4 Start-Up Sequence

Start-up behavior is shown in the following figures. No load was applied on all outputs, and the input voltage was set to 390 VDC. A system capacitance of 1000-µF was connected to 12VSB, and 100-µF was connected to P18V, respectively. Channel 1 shows the P18V output voltage. Channel 2 shows the 12VSB output voltage. Channel 3 shows the S12V output voltage. Channel 4 shows either the input voltage in Figure 2-17 and the DIS pin voltage in Figure 2-18.

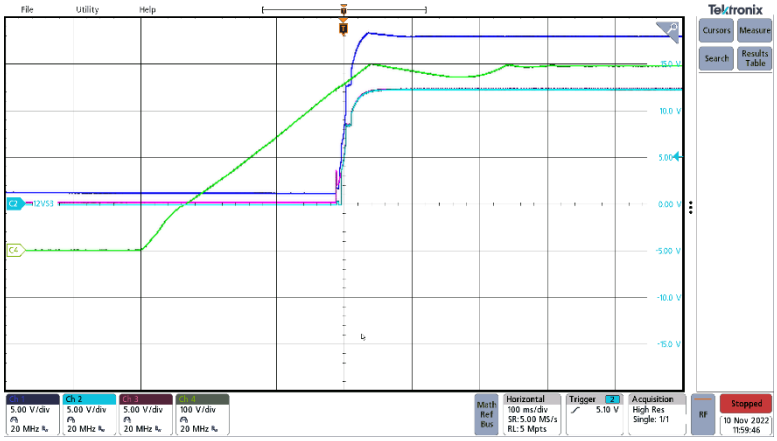

Figure 2-17. Start-Up (DIS Pin Floating When Input Voltage is Applied)

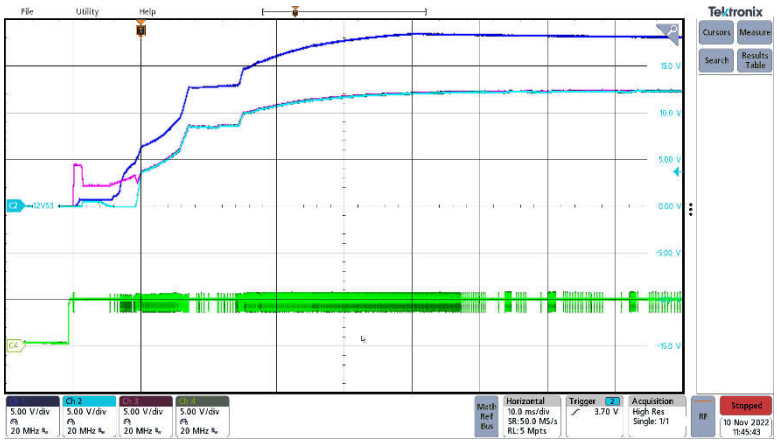

Figure 2-18. Start-Up (Input Voltage Present When DIS Pin Toggled From 0 V to High-Z)

3 Testing and Results

3.1 Efficiency Graphs

Efficiency was measured with a DC input source and loading only the 12VSB output. Efficiency was recorded with input voltages of 100 VDC, 170 VDC, 310 VDC, 390 VDC, and 410 VDC. Table 3-1 describes the system-level conditions represented by these DC input voltages.

Table 3-1. Rated System-Level Conditions

DC Input Voltage	Representative System Condition
410 V	PFC pre-regulator maximum output voltage
390 V	PFC pre-regulator nominal output voltage
310 V	Bridge-rectified 230 VAC input voltage
170 V	Bridge-rectified 120 VAC input voltage
100 V	Minimum operating input voltage

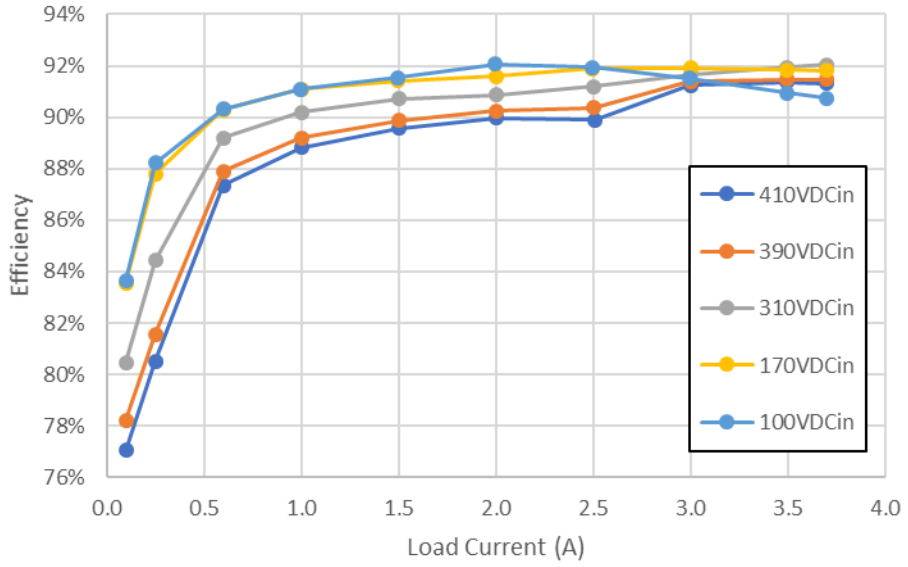

Figure 3-1. Efficiency Graph

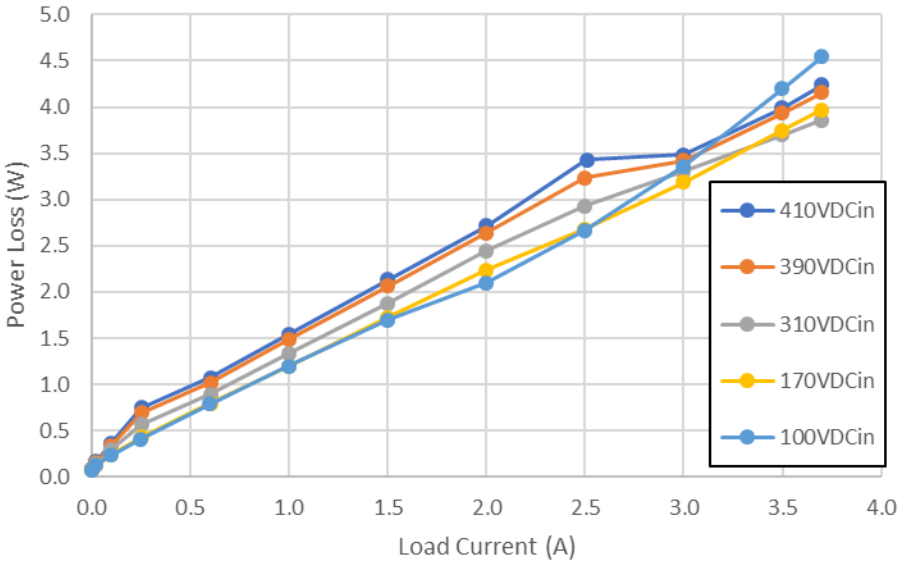

Figure 3-2. Power Loss Graph

3.2 Efficiency Data

Efficiency data is shown in the following tables.

Table 3-2. 410 VDC Input Raw Efficiency Data

I_{OUT} (A)	12VSB (V)	V_{IN} (V)	P_{IN} (W)	P_{loss} (W)	Efficiency
3.698	12.079	409.8	48.78	4.24	91.3%
3.499	12.093	409.8	46.19	3.99	91.4%
2.999	12.136	409.8	39.79	3.48	91.2%
2.509	12.179	409.9	33.92	3.43	89.9%
1.999	12.224	409.9	27.10	2.72	90.0%
1.499	12.269	409.9	20.50	2.14	89.6%
0.998	12.314	409.9	13.817	1.546	88.8%
0.599	12.350	409.9	8.459	1.071	87.3%
0.249	12.382	409.9	3.826	0.746	80.5%
0.099	12.396	410.0	1.591	0.365	77.1%
0.020	12.404	410.0	0.415	0.167	59.8%
0.000	12.406	410.0	0.082	0.082	0.0%

Table 3-3. 390 VDC Input Raw Efficiency Data

I_{OUT} (A)	12VSB (V)	V_{IN} (V)	P_{IN} (W)	P_{loss} (W)	Efficiency
3.698	12.074	389.8	48.68	4.15	91.5%
3.498	12.091	389.8	46.11	3.93	91.5%
2.999	12.134	389.8	39.72	3.42	91.4%
2.499	12.178	389.9	33.60	3.24	90.4%
1.999	12.222	389.9	27.02	2.64	90.2%
1.499	12.267	389.9	20.42	2.07	89.9%
0.998	12.312	389.9	13.756	1.487	89.2%
0.599	12.349	389.9	8.406	1.018	87.9%
0.249	12.381	389.9	3.776	0.696	81.6%
0.099	12.396	389.9	1.568	0.342	78.2%
0.020	12.404	389.9	0.402	0.154	61.7%
0.000	12.406	390.0	0.080	0.080	0.0%

Table 3-4. 310 VDC Input Raw Efficiency Data

I_{OUT} (A)	12VSB (V)	V_{IN} (V)	P_{IN} (W)	P_{loss} (W)	Efficiency
3.699	12.076	309.7	48.39	3.86	92.0%
3.498	12.091	309.7	45.88	3.70	91.9%
2.999	12.135	309.7	39.60	3.30	91.7%
2.499	12.179	309.8	33.30	2.93	91.2%
1.999	12.223	309.8	26.83	2.45	90.9%
1.499	12.268	309.8	20.24	1.88	90.7%
0.998	12.313	309.8	13.604	1.334	90.2%
0.599	12.350	309.8	8.283	0.895	89.2%
0.249	12.382	309.9	3.648	0.568	84.4%
0.099	12.396	309.9	1.524	0.297	80.5%
0.020	12.404	309.9	0.387	0.139	64.1%

Table 3-4. 310 VDC Input Raw Efficiency Data (continued)

I_{OUT} (A)	12VSB (V)	V_{IN} (V)	P_{IN} (W)	P_{loss} (W)	Efficiency
0.000	12.406	309.9	0.080	0.080	0.0%

Table 3-5. 170VDC Input Raw Efficiency Data

I_{OUT} (A)	12VSB (V)	V_{IN} (V)	P_{IN} (W)	P_{loss} (W)	Efficiency
3.698	12.074	169.6	48.49	3.97	91.8%
3.498	12.088	169.6	45.91	3.75	91.8%
2.999	12.132	169.7	39.48	3.19	91.9%
2.498	12.176	169.7	33.03	2.68	91.9%
1.999	12.222	169.7	26.62	2.24	91.6%
1.498	12.268	169.8	20.07	1.72	91.4%
0.998	12.312	169.8	13.469	1.200	91.1%
0.599	12.348	169.9	8.181	0.794	90.3%
0.249	12.381	169.9	3.508	0.428	87.8%
0.099	12.395	169.9	1.467	0.241	83.6%
0.020	12.403	169.9	0.375	0.127	66.2%
0.000	12.405	169.9	0.076	0.076	0.0%

Table 3-6. 100VDC Input Raw Efficiency Data

I_{OUT} (A)	12VSB (V)	V_{IN} (V)	P_{IN} (W)	P_{loss} (W)	Efficiency
3.698	12.076	99.4	49.07	4.55	90.7%
3.497	12.092	99.4	46.36	4.20	90.9%
2.998	12.135	99.5	39.65	3.36	91.5%
2.498	12.179	99.6	33.02	2.66	91.9%
1.998	12.224	99.7	26.48	2.10	92.1%
1.498	12.269	99.7	20.04	1.69	91.5%
0.997	12.314	99.8	13.458	1.199	91.1%
0.598	12.350	99.8	8.167	0.790	90.3%
0.248	12.382	99.9	3.478	0.410	88.2%
0.098	12.396	99.9	1.451	0.237	83.6%
0.019	12.404	99.9	0.368	0.132	64.1%
0.000	12.406	99.9	0.072	0.072	0.0%

3.3 No Load and OFF State Power Consumption

For no load power consumption, input voltage was applied with all outputs unloaded. For OFF state power consumption, input voltage was applied while the DIS pin was shorted to PGND.

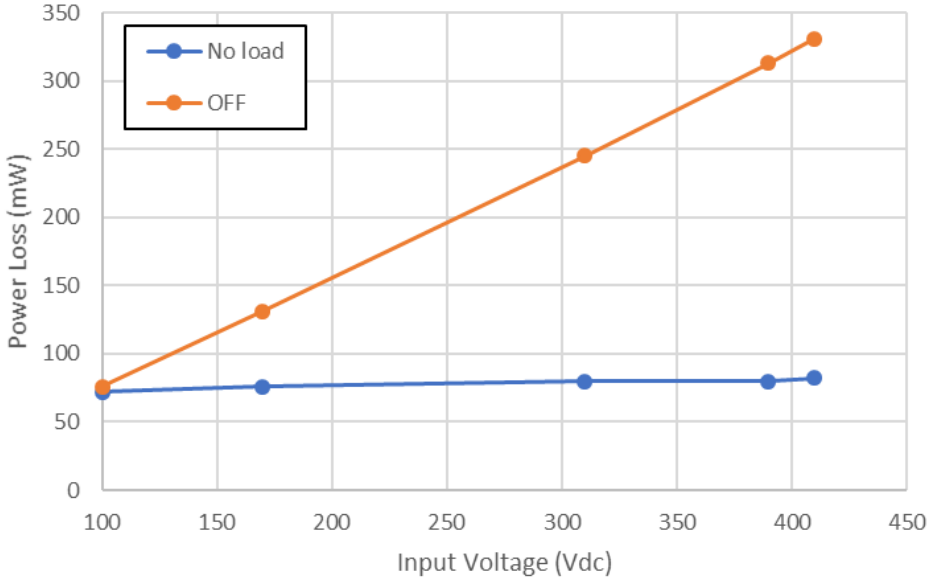

Figure 3-3. No Load and OFF State Power Loss Graph

Table 3-7. No Load and OFF State Power Loss Raw Data

Input Voltage (VDC)	No Load Input Power (mW)	OFF State Input Power (mW)
100	72	76
170	76	131
310	80	245
390	80	313
410	82	331

3.4 Thermal Images

Thermal images are shown in the following figures. All images were captured with the unit under test (UUT) enclosed in a 30-cm × 45-cm × 20-cm Plexiglas box at 25ºC ambient, after a 30-minute warm up. For the full load images, the unit was tested with 390-VDC input, 3.7-A load on 12VSB and no load on P18V and S12V. Forced air was used, with the fan current limited to 200 mA. Table 3-8 summarizes the results of the full load images. In the OFF state image, the unit was tested with a 310-VDC input and DIS shorted to PGND. No forced air flow was used. The maximum temperature was 65.3°C, measured on the depletion mode start-up or sensing FET Q2.

Table 3-8. Full Load Thermal Summary

Reference Designator	Description	Maximum Temperature (°C)
U1	LMG2610 GaN half-bridge	52.1
U3	UCC28782 ACF controller	48.5
N/A	Planar transformer PCB near core on primary side	53.0
CORE50	Planar transformer core	49.5
N/A	Planar transformer PCB near core on secondary side	51.7
Q50	Synchronous rectifier FET	52.4
U50	UCC24612 SR driver	57.6
R3	Secondary current sense resistor	48.8

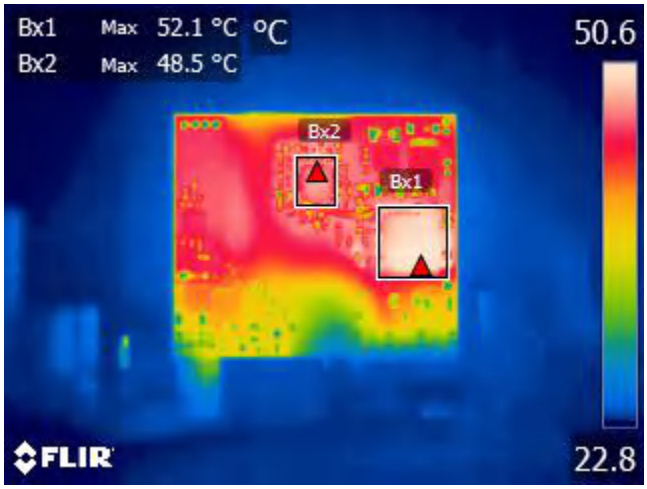

Figure 3-4. Thermal Image Full Load (GaN-Side of Assembly)

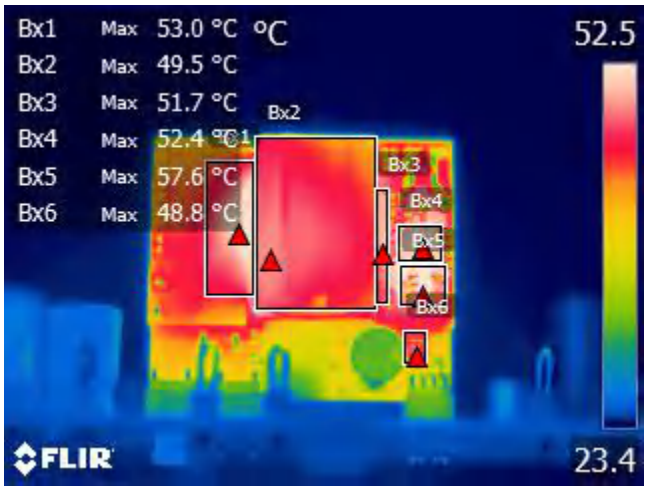

Figure 3-5. Thermal Image Full Load (Transformer-Side of Assembly)

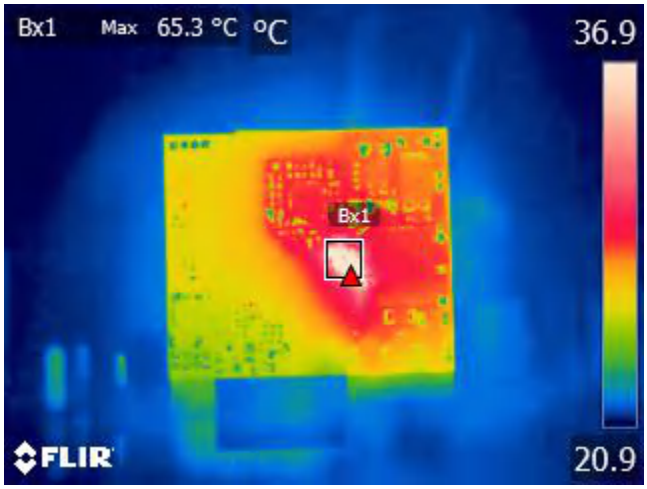

Figure 3-6. Thermal Image OFF State(GaN-Side of Assembly)

3.5 Bode Plots

The feedback loop frequency response was measured with 390 VDC input, 3.7-A load on 12VSB and no load on P18V and S12V. Separate measurements were taken with 270 µF of system capacitance and 4700 µF of system capacitance and are shown in the following figures.

Table 3-9. Bode Plot Summary

System Capacitance (µF)	Phase Margin (°)	Gain Margin (dB)
270	48.9	11.9
4700	116	14.3

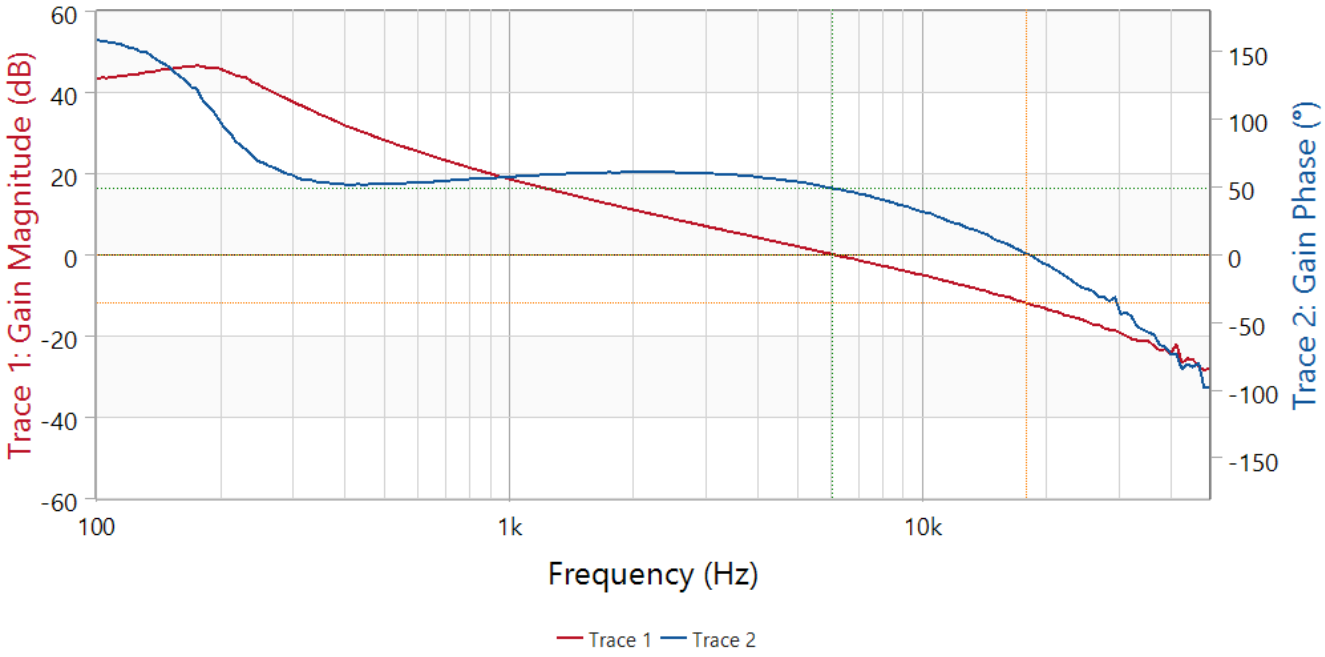

Figure 3-7. Bode Plot 270-µF System Capacitance

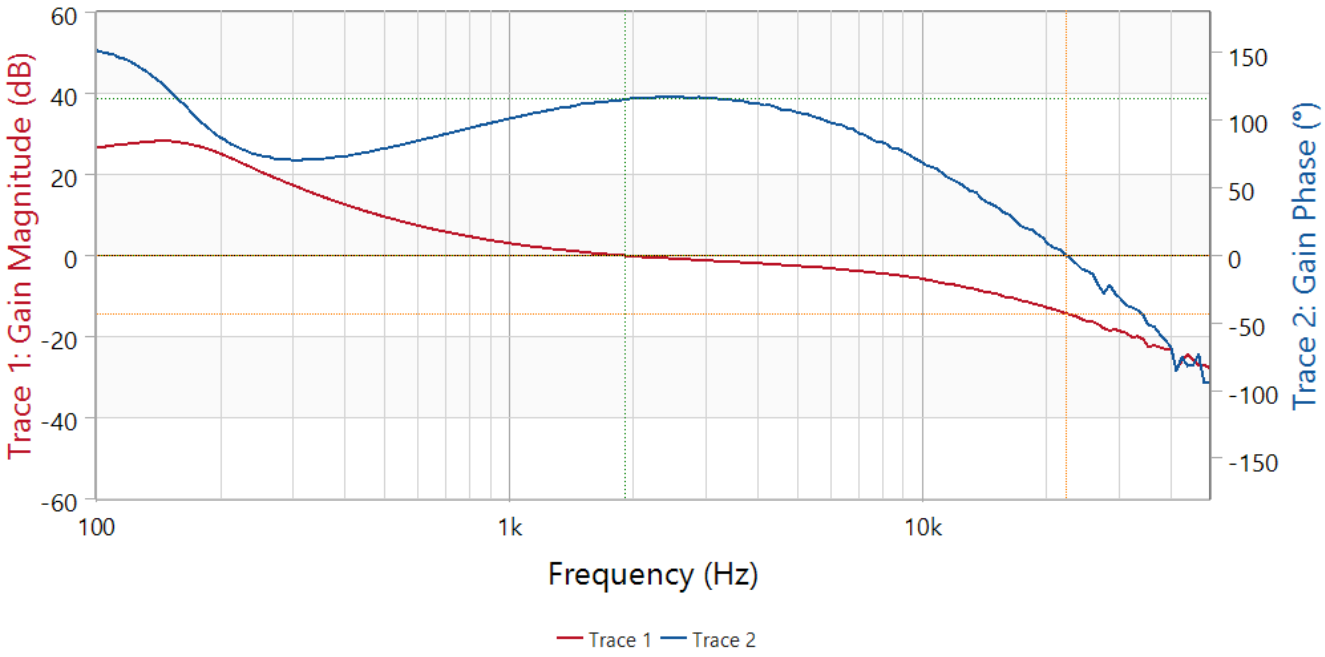

Figure 3-8. Bode Plot 4700-µF System Capacitance

3.6 Load Regulation

The data from the 390 VDC input efficiency measurements was used to generate the 12VSB and S12V regulation plot shown in Figure 3-9. No additional loading was applied to P18V and S12V.

The second plot (Figure 3-10) shows the voltage measured on P18V for different loading combinations on all outputs.

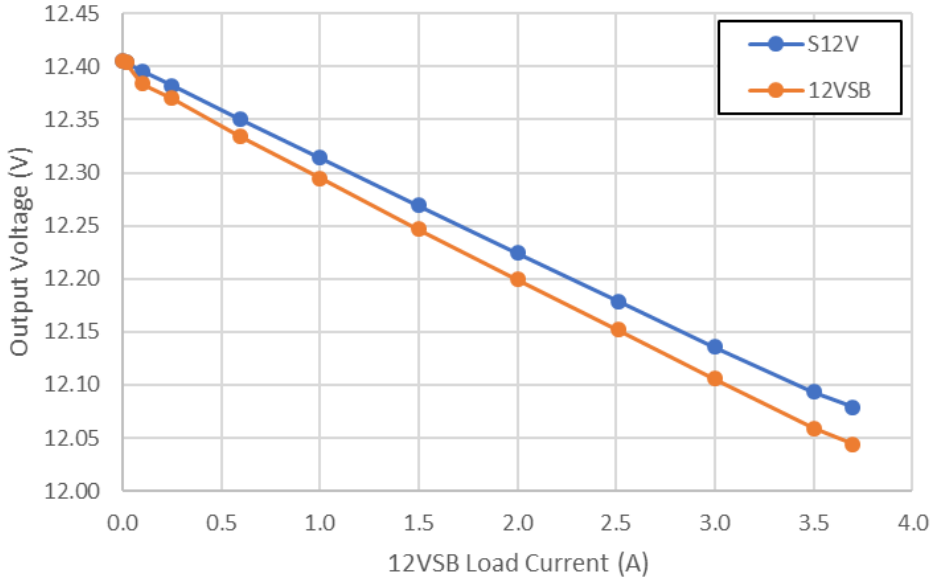

Figure 3-9. 12VSB and S12V Output Voltage Regulation

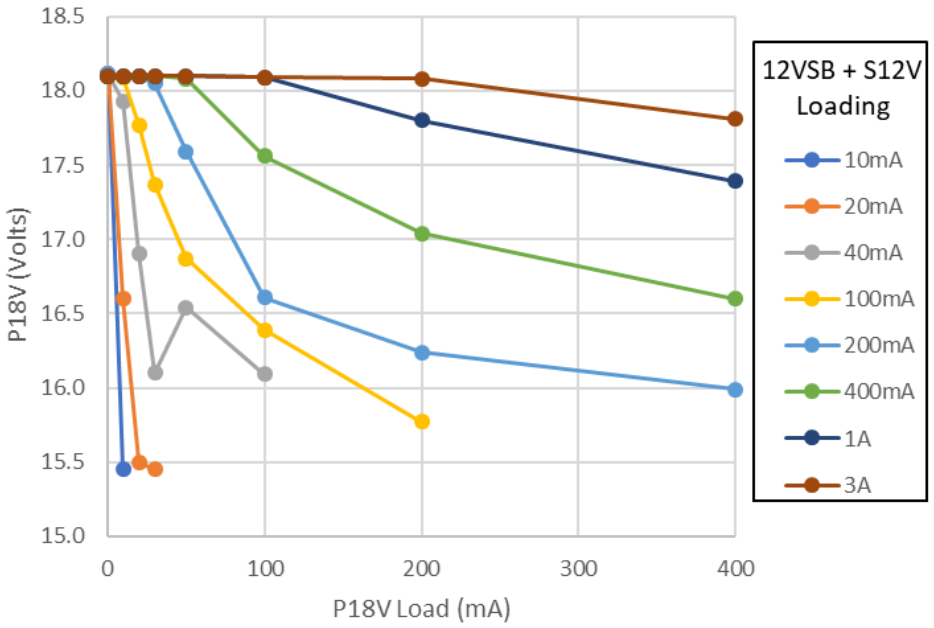

Figure 3-10. P18V Output Voltage Regulation

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