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TI Designs
Optimizing the LMH6554 to Drive High-Speed ADCs

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LMH6554	Product Folder
ADS4449	Product Folder

Design Overview

This reference design discusses the use and performance of the high-speed amplifier, the LMH6554 device, to drive the high-speed analog-to-digital convert (ADC), the ADS4449 device. Different options for common-mode voltages, power supplies, and interfaces are discussed and measured, including AC-coupling and DC-coupling, to meet the requirements of a variety of applications.

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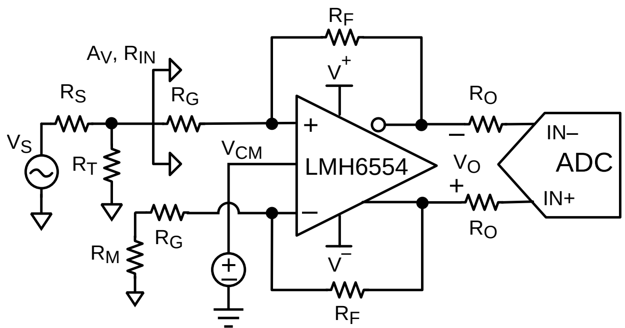

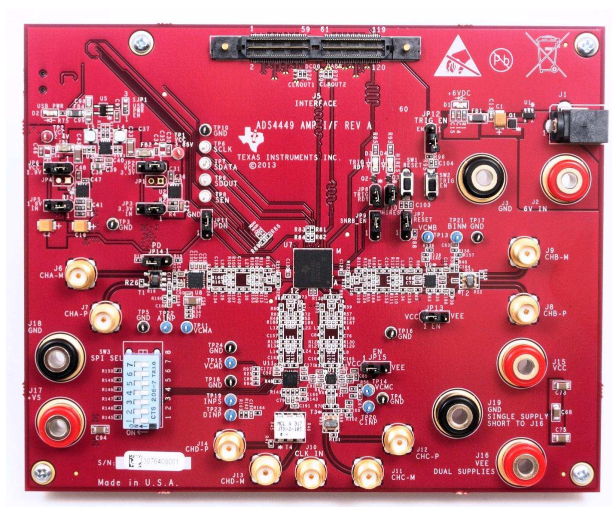

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1 Introduction

This reference design serves as a comprehensive summary of the performance and trade-offs when driving an ADC with high-speed operational amplifiers (op-amps). A printed-circuit board was developed in order to test different setups. This board consists of an ADS4449 device, which is a quad-channel, 14-Bit, 250-MSPS ADC, and four high-speed fully-differential amplifiers. The following op-amp devices are used in order to compare the performance of each: LMH6881, LMH6554, THS770006, and THS4509.

This reference design focuses on the operation of the LMH6554 device. Included in this document are general considerations when driving an ADC with an amplifier, such as common-mode voltages, power supplies, AC-coupling and DC-coupling, and filter interfaces. This document also includes a discussion of the measured performance based on different circuit topologies.

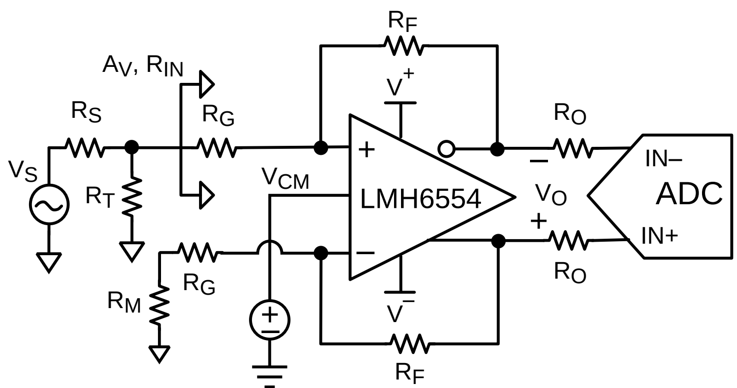
2 General Considerations

2.1 Single-Ended Input to Differential-Output Operation

Many applications require a single-ended source to drive a differential-input ADC. In general, transformers are used to provide single-to-differential conversion, but these transformers are inherently band-pass in nature and cannot be used for DC-coupled applications. As a result, a common solution is to use a high-speed amplifier in order to enable DC-coupling without affecting ADC performance at higher frequencies. Op-amps offer a flexible and cost-effective solution when the application requires gain, a flat pass-band with low ripple, DC-level shifts, or a DC-coupled signal path.

2.1.1 DC-Coupled Configuration

The LMH6554 device provides excellent performance as a single-ended input-to-differential output converter down to DC. Figure 1 shows a typical DC-coupled configuration where an LMH6554 device is used to produce a balanced differential output signal from a single-ended source.



$$A_V = \left(\frac{2(1-\beta_1)}{\beta_1+\beta_2}\right) \qquad \beta_1 = \left(\frac{R_G}{R_G+R_F}\right) \qquad R_S = R_T \parallel R_{IN}$$

$$R_{IN} = \left(\frac{2R_G+R_M(1-\beta_2)}{1+\beta_2}\right) \qquad \beta_2 = \left(\frac{R_G+R_M}{R_G+R_F+R_M}\right) \qquad R_M = R_T \parallel R_S$$

Figure 1. Single-Ended Input With Differential Output

To match the input impedance of the circuit in Figure 1 to a specified source resistance R_S, the following is required: $R_T \parallel R_{IN} = R_S$. Figure 1 also shows the equations to calculate A_V and R_{IN} for a single-to-differential operation. These equations, along with the source matching condition, must be solved iteratively to achieve the desired gain with the proper input termination.

Assume that a 50-Ω source is used and therefore R_S = 50 Ω. The voltage divider created by the source impedance, R_S, and the input impedance, $R_T \parallel R_{IN}$, has a gain of ½ or –6 dB. The amplifier gain can be set to 6 dB to compensate for the input circuit attenuation so the output of the amplifier has the same voltage swing as V_S. Table 1 lists the resistors values selected to match these conditions.

Table 1. Component Values for 50-Ω System

Gain	R_F	R_G	R_T	R_M
6 dB	200 Ω	91 Ω	76.8 Ω	30.3 Ω

2.1.2 AC-Coupled Configuration

AC-coupling is the recommended configuration if the application requires operating in a Nyquist zone other than the first one, or if a DC signal is not required. Figure 2 shows a typical schematic of the LMH6554 device. Note that the impedance seen on each pin must be balanced with no DC offset voltage. Also, in single-to-differential operation, the unused pin must be AC-coupled to ground or DC-coupled to V_{CM}.

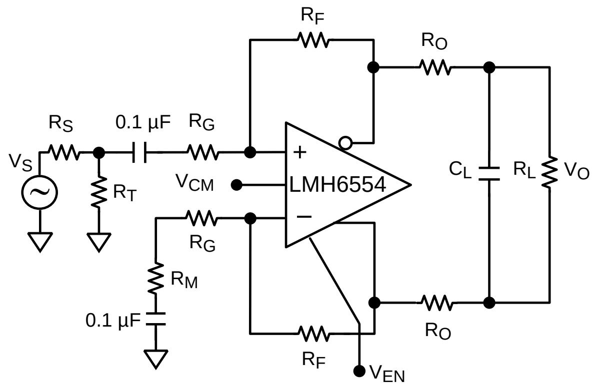


Figure 2. AC-Coupled Configuration

2.2 *Common-Mode Level Consideration*

For most ADCs, the common mode voltage must be set to a particular value to realize the full dynamic range of the ADC. The LMH6554 device uses an internal common-mode feedback circuit to set the precise level of common-mode output voltage. Because a differential amplifier only amplifies the difference of the inputs, the output common mode can be set independently with no impact on the gain or the differential output signal.

The output common-mode level of the LMH6554 device is set at the V_{CM} pin. The drive at the V_{CM} pin can be one of the following:

- A resistive divider circuit that uses the existing supply voltages (generally ½V_+)
- A reference level defined by an ADC output pin
- A dedicated voltage reference

The V_{CM} pin must be decoupled to ground as close as possible to the chip in order to avoid coupling any noise that appears at the output common mode. The maximum-allowed common-mode range is ±1.25 V for the LMH6554 device relative to the common-mode level of the supply voltages show in Equation 1 .

$$V_{CM} = (V_+ + V_-) / 2) \qquad (1)$$

To avoid distortion issues, centering the V_{CM} voltage is recommended. The further away V_{CM} is from the center the more the performance of HD2 and HD3 decreases as shown in Figure 3 (provided that this method is allowed by the application).

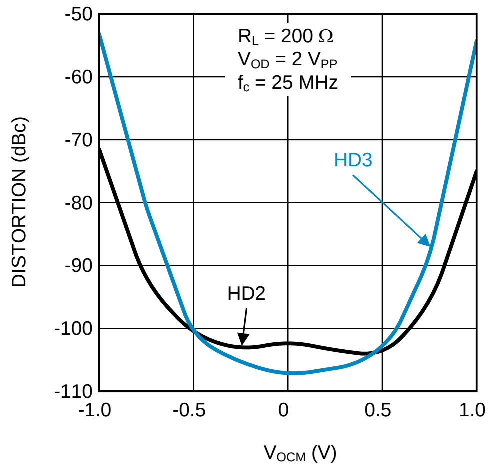


Figure 3. Distortion Versus Output Common-Mode voltage

2.3 Power Supply Consideration

The LMH6554 device can operate with either a single or dual supply, and with either DC coupling or AC coupling. The advantage of AC-coupling over DC-coupling is to offer more freedom of choice in regard to power supply. The main concern with DC coupling is ensuring that the input common-mode voltage does not violate the device operating conditions. By AC-coupling the input of the driver, the input self-biases at the level set by the V_{CM} pin which ensures optimal operation.

If a single supply is used, AC-coupling the op-amp when driving an ADC is easier in relation to common-mode settings. Figure 4 shows a 5-V single supply configuration for an AC-coupled driver followed by a filter to remove out-of-band noise or to be used for Nyquist filtering. The circuit is then appropriately biased to match the ADC common-mode level because of the V_{CM} output being connected to the common mode termination.

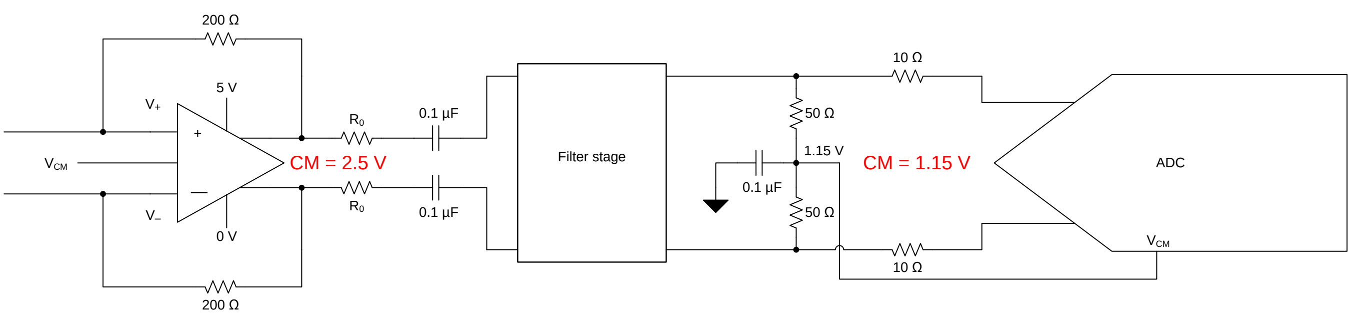


Figure 4. Interfacing With AC-Coupled Configuration

If DC-coupling must be used with a single supply, the common-mode output of the driver must operate at V+ / 2 (in this case, 2.5 V). However, shifting the DC level to match the common mode of the ADC with the interface is possible (see Figure 5). The appropriate common mode is set by using the voltage divider between R_0 and R_1. Unfortunately, this method results in loss of signal power because the op-amp must drive a larger voltage to overcome the attenuation of the voltage divider formed by R_0 and R_1, which results in degraded performance.

The input common-mode voltage (V_{ICM}) of the DC-coupled driver input must also be considered. While the output common-mode voltage (V_{OCM}) is set at V_{CM}, V_{ICM} can have a small delta compared to V_{OCM} based on the feedback resistors. This delta can generate a flow-back current that wastes power. Also, based on the signal source, the delta can cause issues in some applications that may require a buffer amplifier before the fully-differential amplifier.

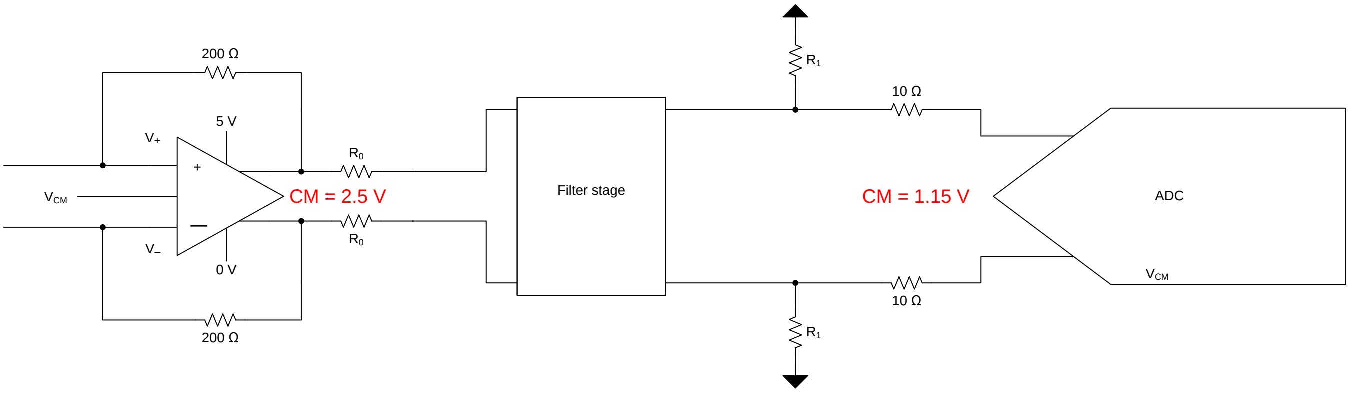


Figure 5. Interfacing With DC-Coupled Configuration

If the application uses a split supply, an advantageous approach is to use a non-symmetric supply operation. For example, non-symmetric supply operation is an alternative solution in a DC-coupled application driving an ADC that requires an input common mode different from 2.5 V. In this reference design, the LMH6554 device drives an ADS4449 device that requires a 1.15-V input common mode. Selecting V+ and V- to center the amplifier input common mode range to suit the application is possible (using Equation 2).

$$V+ = 3.65 \text{ V and } V– = –1.35 \text{ V so that } V_{CM} = (V_+ + V_–) / 2 = 1.15 \text{ V}) \quad (2)$$

A more standard +2.5-V and –2.5-V symmetrical supply can also be used but with degraded performance because V_{CM}, is no longer centered, as shown in Figure 3.

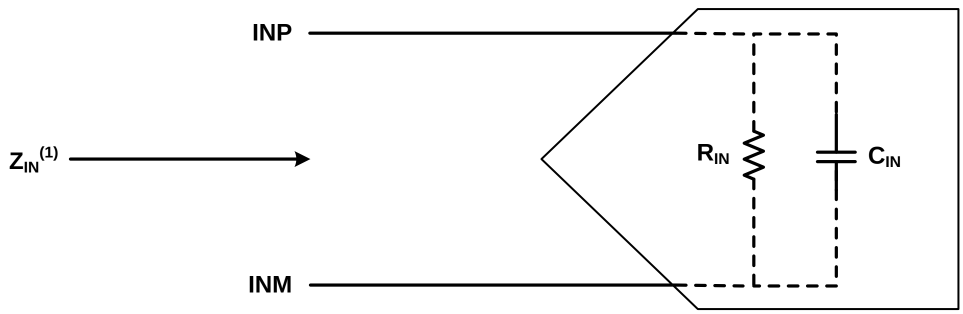
The following summarizes the AC-coupling and DC-coupling differences between a single-supply operation and a split-supply operation.

- **Single supply operation (0 to 5 V)**
  - AC-coupling:
    - The CM is biased at 2.5 V at the op-amp
    - Easily adapts to any required ADC input CM
  - DC-coupling:
    - The input CM of the op-amp can differ from the output CM which leads to current leakages
    - Adapting to the input CM of the ADC requires a voltage divider which leads to losses in signal power and potential distortions issues.
- **Split-supply operation**
  - AC-coupling:
    - The CM is biased at the op-amp
    - Easily adapts to any required ADC input CM
  - DC-coupling:
    - Best solution if the supply can be set to match the required input CM of the ADC
    - Voltage divider is not required which leads to easier interface configuration

2.4 Connecting the Amplifier to the ADC

Analog-to-digital converters (ADCs) often present challenging load conditions. ADCs typically have high impedance inputs with variable capacitive components. Current spikes associated with a switched capacitor or sample-and-hold circuits can also occur. These characteristics result in an ADC input that is a challenge to drive. Using an amplifier provides value to the design because the output stage of a differential amplifier correct for glitches by providing a low-impedance, fast-settling source for accurate sampling.

The first aspect to consider is the ADC-equivalent input impedance. Figure 6 shows that the input of the ADS4449 can be represented by a differential resistor (R_{IN} ≈ 700 to 1000 Ω for the first two Nyquist zones, 0 to 250 MHz) and capacitor (C_{IN} ≈ 3.5 pF) in parallel. The ADS4449 does not have a buffered input and therefore noise from the switched capacitor can also occur.



(1) $Z_{IN} = R_{IN} \parallel (1 / j\omega C_{IN})$.

Figure 6. ADS4449 Equivalent-Input Impedance

The interface between the op-amp and the ADC must be optimized. Figure 7 shows a typical circuit for driving an ADC. The two R_0 resistors isolate the capacitive loading of the ADC from the amplifier to ensure stability. The resistors form part of a low-pass filter with L_1 and C_1, which helps to provide anti-alias and noise reduction functions. The two C_1 capacitors help to smooth the current spikes associated with the internal switching circuits of the ADC. Note that the ADC input capacitance must be factored into the frequency response of the input filter. A 5 to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by the package parasitics. The input circuit (and notably these resistors) must initially be optimized in the lab because up to a 4-dB SFDR and 2-dB SNR improvement has been observed.

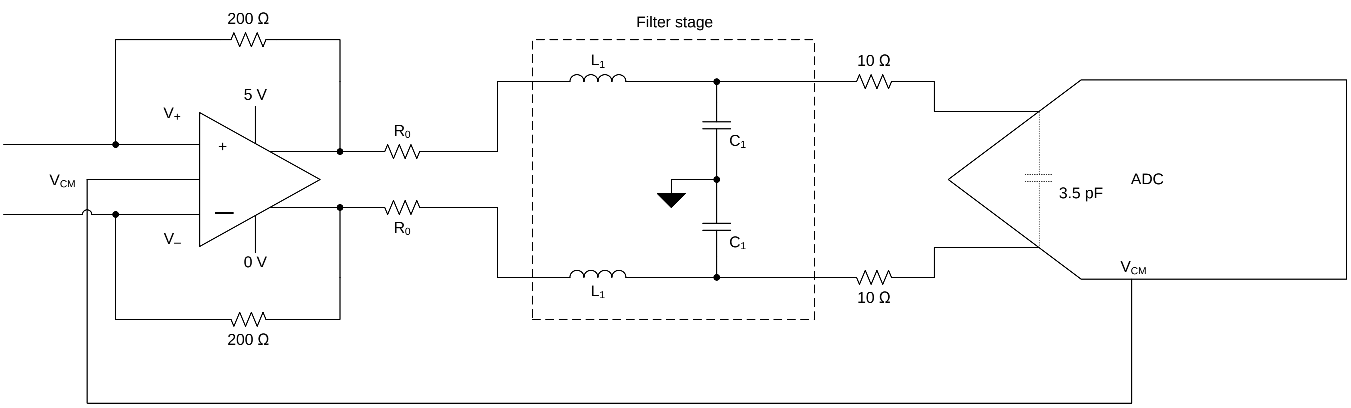


Figure 7. Typical Interface Circuit Driving an ADC

2.5 Layout Considerations

Board layout is critical for typical high-speed circuits. To achieve a proper layout, TI recommends the following:

- The amplifier and ADC must be located as close together as possible.
- Both the amplifier and the ADC require that the filter components be located in close proximity.
- The amplifier must have minimal parasitic loading on the output traces as the ADC is sensitive to high frequency noise that can couple in on the input lines.
- The ADC digital outputs must be well isolated from the ADC input as well as from the amplifier inputs.
- The amplifier and the ADC input pins must not be placed over power or ground planes.
- Power-supply bypass capacitors must be low ESR and placed within 2 mm of the associated pins.
- When vias are used, using multiple vias is recommended.
- To optimize balance and, therefore, common-mode rejection, 0.1% resistors must be used for the feedback path of the amplifier.

2.5.1 Board Layout

Figure 8, Figure 9, and Figure 10 show the board and board layout.

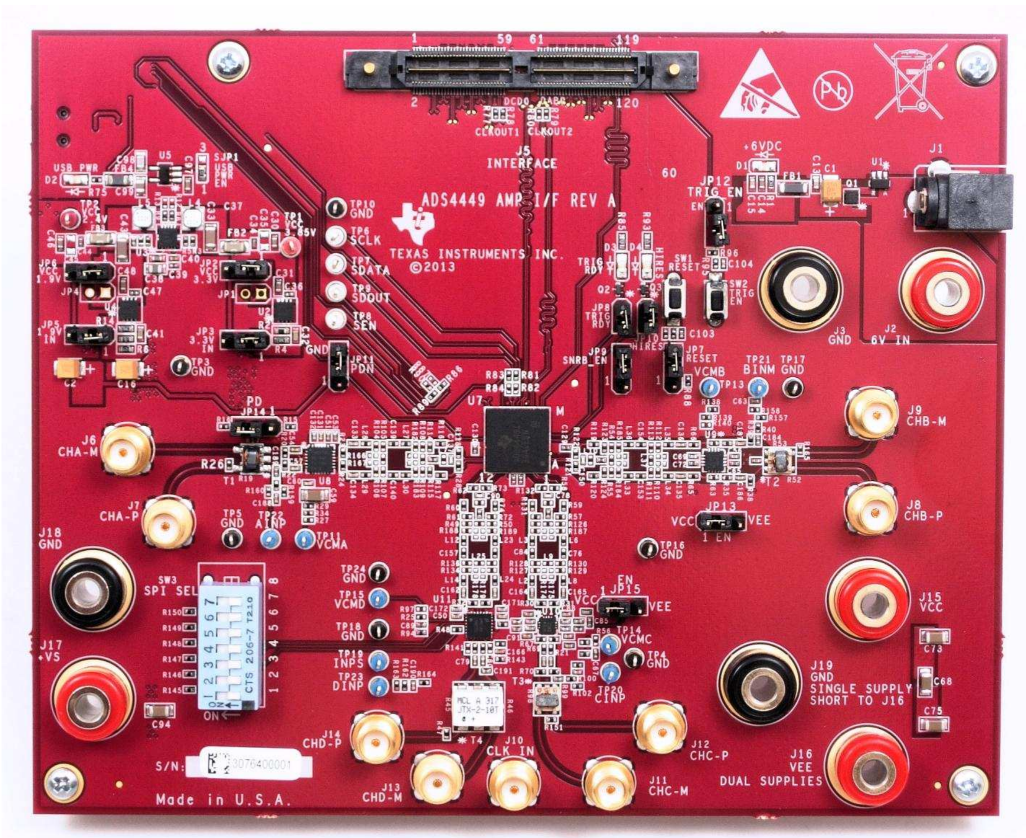


Figure 8. ADS4449 AMP I/F Board

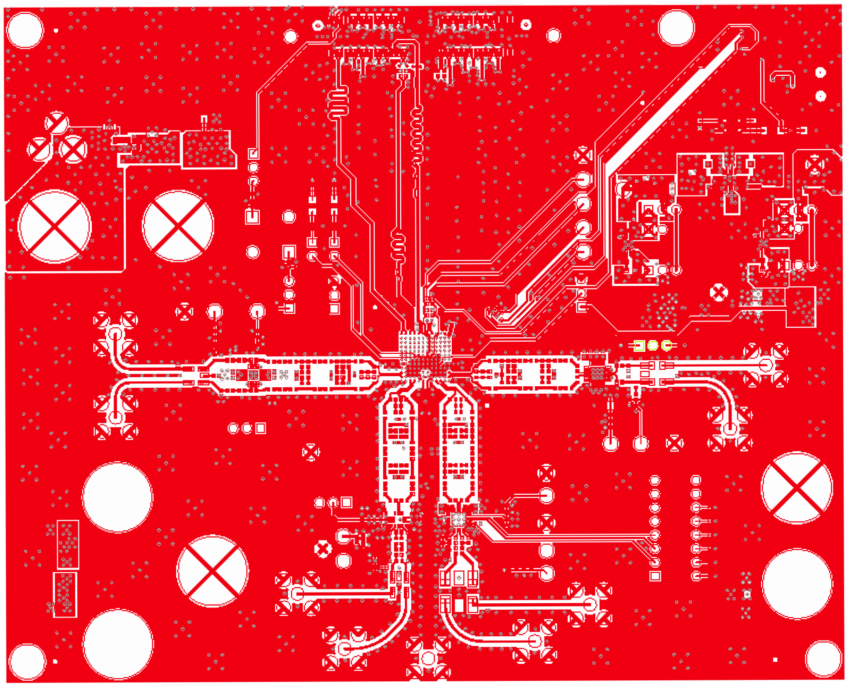


Figure 9. Top-Side Layer

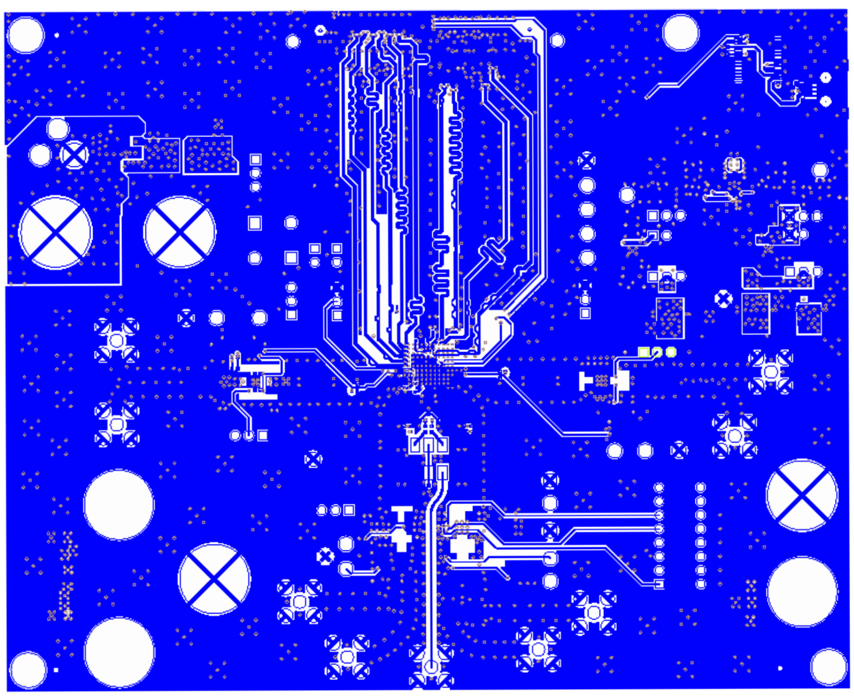


Figure 10. Bottom-Side Layer

3 Tests and Measurements

Three design options have been explored and optimized: AC-coupling for signals in the first Nyquist zone, AC-coupling for signals in the second Nyquist zone, and DC-coupling for signals in the first Nyquist zone. The schematics of the circuits, and the SNR and SFDR measurement results are presented in this section.

3.1 *Test setup*

The board used for these measurements is the ADS4449 amplifier I/F which was specifically created for these tests. The board comprises an ADS4449 ADC with the following different op-amp on the channels:

- Channel A: THS770006
- Channel B: THS4509
- Channel C: LMH6554
- Channel D: LMH6881

This section only covers the measurements and different circuits concerned with Channel C. All SNR and SFDR measurements are taken at –1 dBFS.

The clock used for all these measurements is set at 245.76 MHz with a 10-dBm amplitude.

3.2 *AC-Coupled Scenario*

3.2.1 First Nyquist Zone

Figure 11 shows the circuit used in the first Nyquist Zone in an AC-coupled scenario.

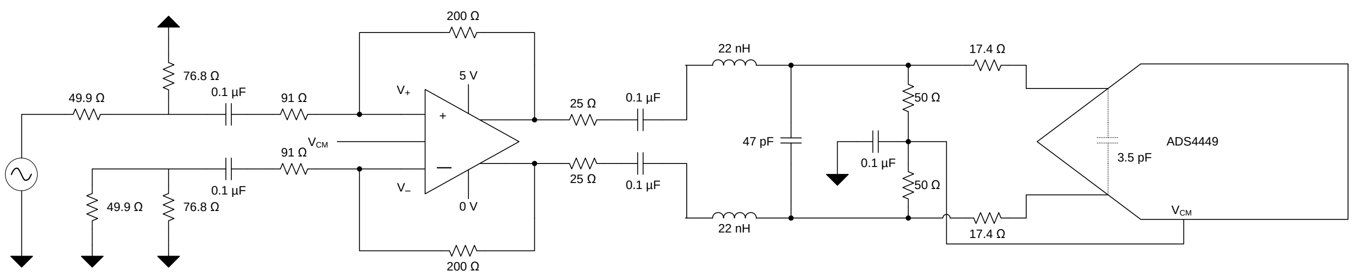


Figure 11. Circuit Used for the AC-coupled First Nyquist Zone Measurements

An LC filter was designed in order for a second-order low-pass filter to restrict the application to the first Nyquist zone. Figure 12 shows the measured filter response. The corner frequency is located at 105 MHz.

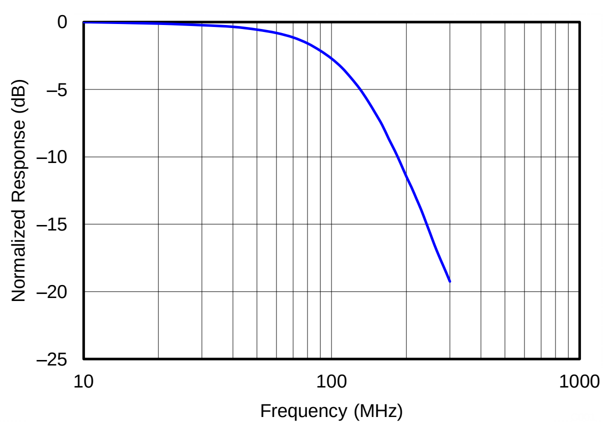


Figure 12. Normalized Gain Response — AC-Coupled First Nyquist Zone

Table 2 and Table 3 list the SNR and SFDR results.

Table 2. SNR Result — AC-Coupled First Nyquist Zone

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
10	70.24	72
20	70.33	71.97
30	70.22	71.99
40	70.09	72.02
50	70.16	71.89
60	70.05	71.85
70	69.99	71.84
80	69.8	71.77
90	69.77	71.67
100	69.78	71.6

Table 3. SFDR Result — AC-Coupled First Nyquist Zone

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
10	84	90.4
20	84.49	85.79
30	86.29	85.04
40	84.15	84.65
50	81.58	83.05
60	78.76	82.48
70	77.06	82.63
80	75.23	82.77
90	74.29	83.64
100	73.72	86.83

3.2.2 Second Nyquist Zone

Figure 13 shows the circuit used in the second Nyquist Zone in an AC-coupled scenario.

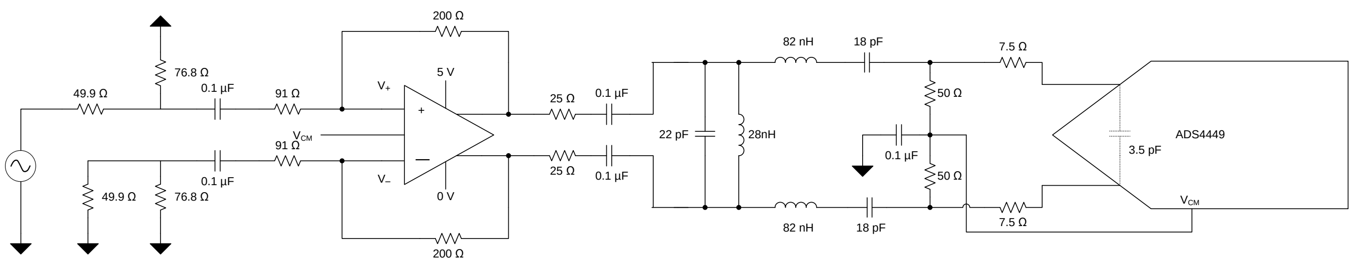


Figure 13. Circuit Used for the AC-Coupled Second Nyquist Zone Measurements

An LC filter was been designed in order for a second-order band-pass filter to restrict the application to the second Nyquist zone. Figure 14 shows the measured filter response. The corner frequencies are located at 105 MHz and 250 MHz.

NOTE: In a real application, the band-pass filter must be designed for a specific frequency in the second Nyquist zone, thus giving a narrower selectivity and better results.

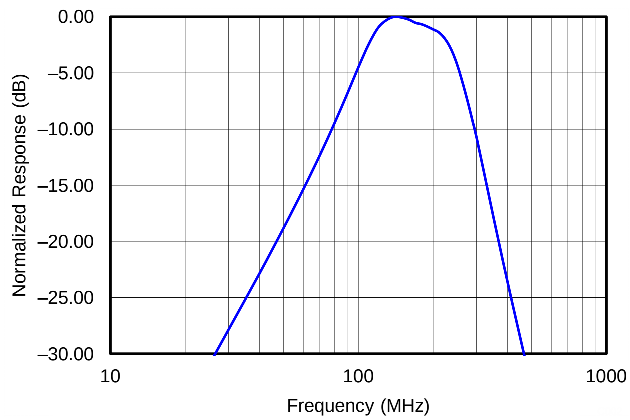


Figure 14. Normalized Gain Response — AC-Coupled Second Nyquist Zone

Table 4 and Table 5 list the SNR and SFDR results.

Table 4. SNR Result — AC-Coupled Second Nyquist Zone

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
130	69.5	68.74
170	69.19	68.5
230	68.67	68.42

Table 5. SFDR Result — AC-Coupled Second Nyquist Zone

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
130	74.9	82.21
170	74.12	82.02
230	67.61	80.12

3.3 *DC-Coupled Scenario*

Figure 15 shows the circuit used in the first Nyquist Zone in a DC-coupled scenario.

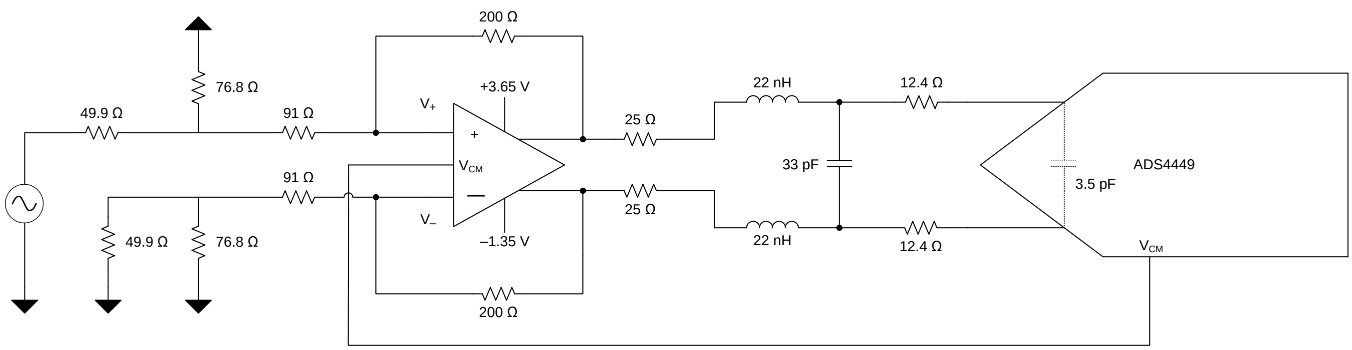


Figure 15. Circuit Used for the DC-Coupled First Nyquist Zone Measurements

When using the DC-coupled configuration, check the input common mode. In this case, the input common mode was measured at 432 mV. With the split-supply configuration being V+ = 3.65 V and V– = –1.35 V, the minimum recommended input common-mode voltage is –0.15 V while the ideal voltage is 1.15 V. Therefore biasing the input common mode at 432 mV is a good margin from the V_{ICM} limit.

An LC filter was designed as a second-order low-pass filter to restrict the application to the first Nyquist zone. Figure 16 shows the measured filter response. The corner frequency is located at 115 MHz.

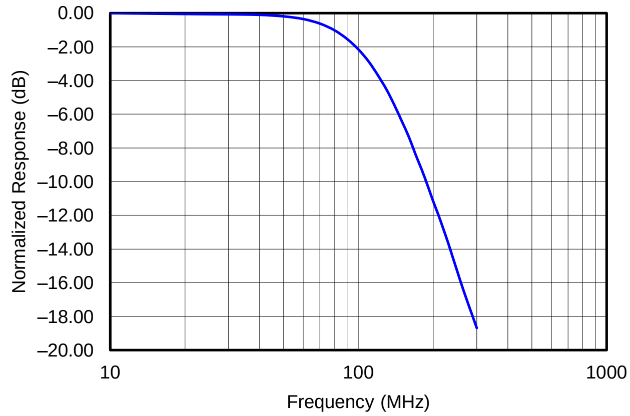


Figure 16. Normalized Gain Response — DC-Coupled First Nyquist Zone

Table 6 and Table 7 list the SNR and SFDR results.

Table 6. SNR Result — DC-Coupled First Nyquist Zone

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
10	68.38	71.14
20	68.31	71.17
30	68.38	71.13
40	68.31	71.11
50	68.18	71.04
60	68.03	71.02
70	67.99	70.99
80	67.93	70.97
90	67.73	70.88
100	67.72	70.83

Table 7. SFDR Result — DC-Coupled First Nyquist Zone

Frequency (MHz)	No Filter (dBFs)	LC Filter (dBFs)
10	74.67	86.22
20	75.2	85.07
30	76.11	84.52
40	76.49	84.25
50	76.92	83.21
60	76.87	83.87
70	77.08	83.66
80	78.12	82.98
90	77.11	82.27
100	77.66	83.62

3.4 Comparison Between Op-Amps and Raw ADC Performance

Table 8 and Table 9 list a general summary of the performance measured on the ADS4449 amplifier I/F board. These tables include measurements using the THS4509 device, the LMH6881 device, and the LMH6554 device to drive the ADS4449 device. For additional information on how to drive high-speed ADC using the THS4509 device and the LMH6881 device, please see TIDU173 and TIDU174 (respectively). Typical values from the ADS4449 datasheet (SBAS603) are shown as a benchmark.

Table 8. Performance Measured in AC-Coupling Configuration

	Frequency (MHz)	THS4509	LMH6881	LMH6554	ADS4449
SNR (dBFs)	40	71.65	69.44	72.02	71.1
	70	71.49	69.3	71.84	71
	130	68.12	67.34	68.74	69.5
	170	67.89	67.21	68.5	69
	230	67.9	67.34	68.42	68.5
SFDR (dBFs)	40	84.03	81.79	84.65	84
	70	78.55	71.76	82.63	87
	130	71.03	53.25	82.21	85
	170	69.24	58.34	82.02	86
	230	75.34	64.07	80.12	84

Table 9. Performance Measured in DC-Coupling Configuration

	Frequency (MHz)	THS4509	LMH6881	LMH6554	ADS4449
SNR (dBFs)	40	70.83	70.39	71.11	71.1
	70	70.66	70.21	70.99	71
SFDR (dBFs)	40	88.55	75.86	84.25	84
	70	80.1	69.32	83.66	87

4 Conclusion

Based on both theory and actual measurement, the LMH6554 device is a good solution to drive a high-speed ADC such as the ADS4449 device. The LMH6554 device can be set in either DC-coupled or AC-coupled configuration. An important consideration is proper common-mode biasing based on power supply choices.

In terms of SNR and SFDR, performance can improve greatly if time is spent to optimize the interface circuit and filtering. The test results provided in this document show that using the LMH6554 can achieve performance almost as good as when driving the ADC directly.

5 References

1. LMH6554 data sheet, SNOSB30
2. ADS4449 data sheet, SBAS603
3. Application report, *Driving High-Speed Analog-to-Digital Converters: Circuit Topologies and System-Level Parameters*, SLAA416
4. Application note, *AN-1393 Using High Speed Differential Amplifiers to Drive Analog-to-Digital Converters*, SNOA461
5. Application note, *AN-2177 Using the LMH6554 as an ADC Driver*, SNOA565

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