*TI Designs*

# *Digitally Isolated 2-Channel, Wide AC/DC Binary Input Module*

## TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

## Design Resources

| | |
|---|---|
| TIDA-00490 | Design Folder |
| MSP430G2332IPW20 | Product Folder |
| ISO1541D | Product Folder |
| SN6501DBV | Product Folder |
| OPA4314 | Product Folder |
| LM4041 | Product Folder |
| LMV551 | Product Folder |
| ISO7220A | Product Folder |

TI E2E™ Community

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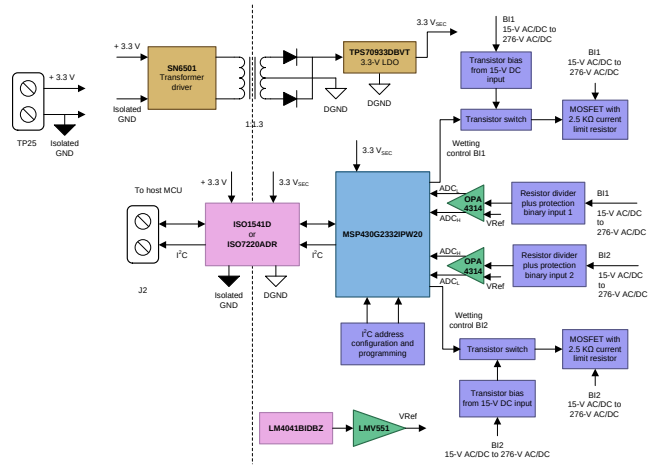
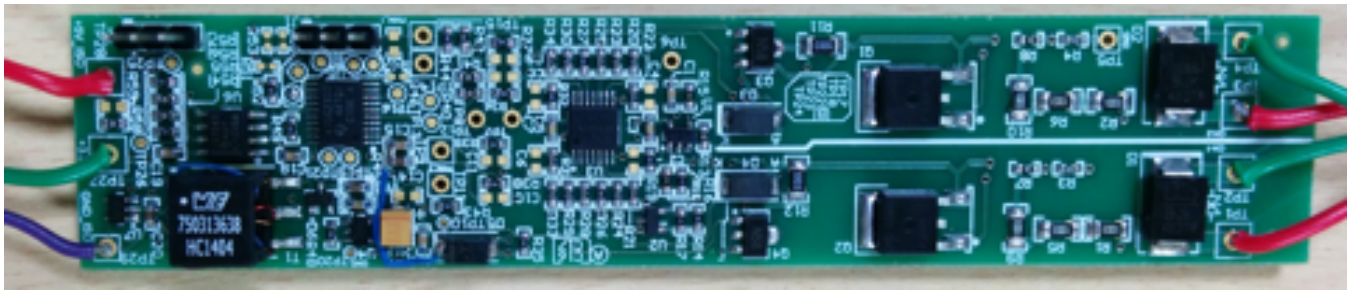



## Design Features

- Accurate Sensing of Input Voltage Over Wide Temperature Range
  - Accuracy < ±3% of Measured Value ±1 V (Programming Resolution or Step Size)
- MCU-Based 2-Channel AC/DC Binary Input Voltage Sensing
- Isolator Rated for 2500-$V_{RMS}$ Isolation for 1 Minute per UL 1577
- Two Gain Stages for Improved Measurement Accuracy Over Wide Input Range (×1 and ×3.5)
- Independent Wetting Current Control for Both Inputs When Used in DC Input Configuration
- Wide AC/DC Input Measurement: Rated up to 276-V AC/DC Including Positive and Negative DC Input
- Inputs Rated up to 300-V AC/DC
- Can be Interfaced to the Host MCU Using $I^2C$ Interface or Digital Output Type of Isolators
- ≥2.5-KΩ Impedance for Wetting and >300-KΩ Impedance for Binary Input
- Less Than 1-mA Consumption at 276-V AC/DC Input
- Measurement Resolution Better Than 1 V
- PCB Width ≤ 1 inch

## Featured Applications

- Multifunction Protection Relays
- Remote Terminal Unit
- Bay Controller
- Remote I/O
- Merging Unit
- Circuit Breaker Digital Input Module
- FTU/DTU/FRTU



# 1 System Description

## 1.1 Introduction to IED and Subsystems in Grid Applications

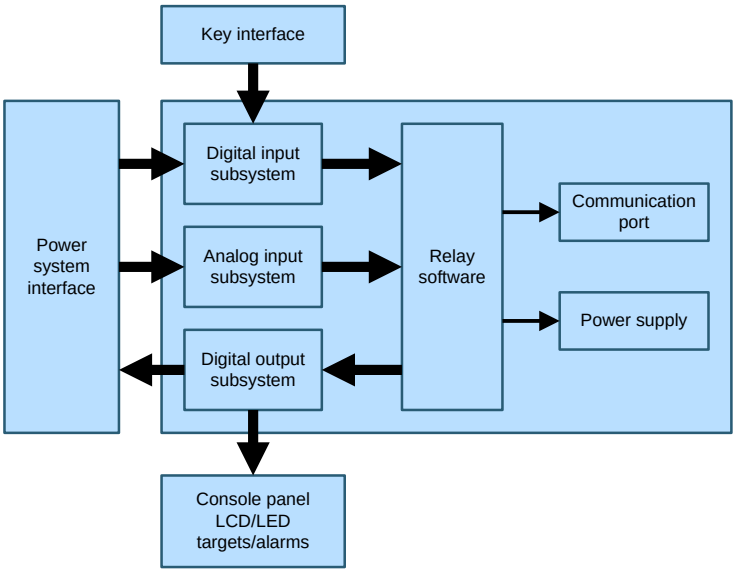



**Figure 1. Generic Block Diagram of a Protection Relay**

The protection relay, intelligent electronic device (IED), or substation controllers used in grid applications have the following generic subsystems. The subsystems are based on the functionality and are as follows:

- CPU or DSP module
  - This module handles all protection functions and logic. Additionally, the HMI and communication functions are also handled by this module.
- Power supply
  - Nominal auxiliary voltage: 24-V DC, 48 to 60-V DC, 110 to 125-V DC, 220-V DC, and 230-V AC, 50 or 60 Hz, ± 20%, and 40-W max. admissible consumption
  - Stored energy for up to 50 ms power supply interruption
  - Dual source power supply (optional)
- AC measurement inputs
  - Nominal frequency (FNOM): 50 or 60 Hz
  - Operating range: 45 to 66 Hz
  - Accuracy: 0.2% $F_S$ at FNOM
- CT measurements inputs
  - Nominal current: 1 or 5 A (IN)
  - Nominal consumption per phase: < 0.15 A at IN
  - Load rating: 20 A in continuous; 30 A for 3 s; 100 A for 1 s
- VT measurements inputs
  - Nominal voltage: 57.7 to 500 V
  - Nominal consumption per phase: < 0.1 VA at 130 V
  - Maximum measurable voltage: 577 $V_{RMS}$

- DC analog input range (independently configurable):
  - ±1.25, ±2.5, ±5, and ±10 V
  - ±1, ±5, ±10, and ±20 mA
  - 0 to 1, 0 to 5, 0 to 10, 0 to 20, and 4 to 20 mA
- DC analog output range (independently configurable):
  - ±5, ±10, ±20 mA, and 4 to 20 mA
- Digital inputs
  - Nominal voltage: 24-V DC, 48 to 60-V DC, 110 to 125-V DC/AC and 220-V DC/AC, ±20% or multi-voltage (24 to 250-V DC/AC)
  - Power consumption per input: 2 to 6 mA, maximum power dissipation is 0.45 W ±20% per input or short peak-current (> 25 mA)
  - Groups of 4, 8, 12, 16, or 32
- Digital output relays
  - Continuous current: 5 A
  - Short-duration current: 30 A for 500 ms; 100 A for 30 ms
  - Breaking capacity: DC: 50 W resistive, 15 W inductive (L/R = 20 ms); AC: 1250 VA (cos PF = 0,7)
- Control output relays
  - Continuous current: 5 A
  - Short-duration current: 30 A for 4 s; 250 A for 30 ms
  - Breaking capacity (Double pole contacts wired in serial): DC: 100 W resistive, 30 W inductive (L/R = 40 ms); AC: 2000 VA (cos F = 0.7)
- Time synchronization
  - by an IRIG–B GPS clock (through the IRIG-B input)
  - by an Ethernet SNTP server
  - by a time telegram message issued by remote Scada (DNP3.0, IEC 60870-5-101 or IEC 60870-5-104)
- Communication capabilities
  - Ethernet communication
    - 10/100BASE-TX, auto-crossing or 100BASE-FX
    - Protocols include UCA2 or IEC 61850, IEC 60870-5-104 (multi-client) or DNP3.0 IP
    - Embedded Ethernet switch module with up to six ports (permitting a compact connection of various devices or I/O extensions)
  - Serial communication
    - Up to two SCADA or four IED links per device
    - SCADA protocol can be switched between DNP3.0, IEC 60870-5-101 and MODBUS
    - IED Protocol can be switched between DNP3.0, IEC 60870-5-103, MODBUS and IEC 60870-5-101
    - Transmission rate is configurable up to 38.4 kbps

## 1.2 Binary Inputs or Digital Inputs

The inputs to the protection relay or substation controllers are called under different names:

- Binary input
- Digital input
- Control input
- Indication input

The names are based on the function performed. These inputs will be referred as binary inputs in this design guide. Binary inputs have wide applications. The binary input module specifications differ with OEMs. The binary inputs are designed as modules and based on application one or more modules are used. Below is the summary of some of the Applications, functionalities, and specifications. These inputs have galvanic isolation from internal circuits, generally opto-coupler are used for isolation. Number of binary inputs per module can vary as 4, 8, 16, or 32. *The binary inputs are organized in groups (depending upon application) with a common wire. In some of the applications the inputs are channel isolated.*

### 1.2.1 Binary Input Applications

Some of the grip applications use binary inputs for the following functionalities:

- Substation battery monitoring
- Bay or substation interlocking
- Breaker status indication
- General interrogations
- LED test
- Diagnostics (self-test)
- Fault indication (alarm)
- Configuration change (operated with new settings to perform different functionality)

### 1.2.2 Specifications

***Key Specification***

- Input voltage range
- Threshold for guarantee operation
- Threshold for uncertain operation
- Response or reset time (software provides de-bounce time)
- Power consumption, energized

***General Specification***

- Inputs are jumper selectable for low range (nominal system voltages of up to 100 V) or high range (from 100 to 300 V)
- Tolerance: ±10%
- Common input voltage ranges:
  - 24-V DC
  - 48-V DC
  - 110-V AC/DC
  - 230-V AC/DC
- Frequency: 50 or 60 Hz
- Contacts per common return: Four or more
- Recognition (processing of the inputs) time: ≥ 20 ms
- Inputs protected against continuous overload up to 300-V AC/DC
- All I/O terminals protected with internal transient limiting devices
- Continuous current draw: < 5 mA
- Auto-burnish impulse current: 20 to 50 mA
- Duration of auto-burnish impulse: 25 to 50 ms

### 1.2.3 Wetting or Auto Burnishing

The binary inputs sense a change of the state of the external device. When these external devices are located in a harsh industrial environments (either outdoor or indoor), their contacts can be exposed to various types of contamination. Normally, there is a thin film of insulating sulfidation, oxidation, or contaminates on the surface of the contacts, sometimes making it difficult or impossible to detect a change of the state. This film must be removed to establish circuit continuity; an impulse of higher than normal current can accomplish this.

The contact inputs with auto-burnish create a high current impulse when the threshold is reached to burn off this oxidation layer as maintenance to the contacts. Afterwards, the contact input current is reduced to a steady-state current. Contact inputs with auto burnishing allow currents up to 50 mA at the first instance when the change of state was sensed. Then, within 25 to 50 ms, this current is slowly reduced to 5 mA. The 50-mA peak current burns any film on the contacts, allowing for proper sensing of state changes.

### 1.2.4 Miscellaneous Features

#### *Filter*

Filters prevent the input signal from being detected erroneously. The following types of input filters can be used:

- The hardware input filter is used to suppress contact bounce (1 to 64 ms).
- Change-of-state delay is used to suppress short signal interruptions.
- Chatter blocking is used to suppress huge bursts of indications in case of defective battery or intermediate relays.

#### *Processing*

The detected changes of state can be processed further in the following ways:

- Single-point indication: Each incoming or outgoing input signal causes data to be entered in the event buffer and the process image to be updated.
- Transient indication: Each change in the input signal causes the process image to be updated. However, only an incoming input signal causes data to be entered in the event buffer.
- Double-point indication: Two defined states of an operational device (for example, on/off) and two undefined states (for example, intermediate state information) can be represented with two inputs. Each change in the double-point indication causes data to be entered in the event buffer. Each new state of the two inputs is entered in the process image.
- Bit patterns: Several inputs are used to detect freely definable states of an operating device. This information can be transferred to the event buffer by an internal event signal (change in the bit pattern) or an external event signal (impulse through a fixed external input).
- Transformer tap indication: Several inputs are used to detect the states of a transformer tap generator. This information is transferred according to the moving contact. The transformer taps can be entered in variable codes.
- Metered-value acquisition: Signal changes are interpreted as metering pulses and totalized. The metered value is transferred to the event buffer by means of a transfer job.

## 1.3 Isolation

**Table 1. Key Methods of Isolation**

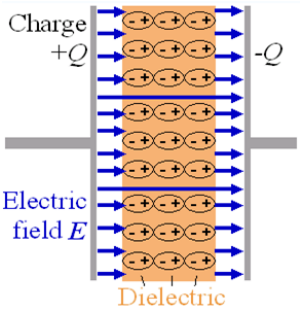
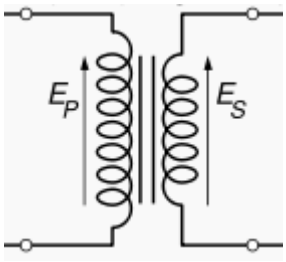
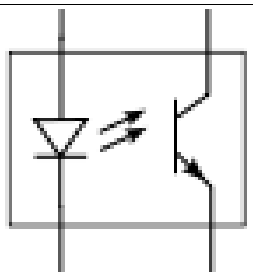
| | |
|---|---|
|  | SiO2: ISO72x; Typical BV is $V_{PEAK}$/µm<br>• Inorganic<br>• Highly stable (over temperature, moisture, time), high quality<br>• Used extensively and for a long time as dielectric in semiconductor (low defunct rates)<br>• Deposited in a controlled semiconductor process |
|  | Polymide: ADI transformer core; Typical BV is 250 $V_{PEAK}$/µm<br>• Organic<br>• Retains moisture — affects lifetime especially at high voltages<br>• Used in semiconductor mainly for stress relief and now as isolation barrier |
|  | Epoxy: Opto-couplers; Typical BV is 50 $V_{PEAK}$/µm<br>• Uses filler materials<br>• Leaky (higher partial discharge)<br>• Applied at packaging as mold compound<br>• Voids and anomalies are common |

**Table 2. Isolation Solutions Reliability**

| PARAMETER | OPTO | MAGNETIC | CAPACITIVE |
|---|---|---|---|
| Signaling rate (Mbps) | 50 | 150 | 150 |
| Propagation delay time (ns) | 20 | 32 | 12 |
| Pulse width distortion (ns) | 2 | 2 | 1.5 |
| Channel-to-channel skew (ns) | 16 | 2 | 1.6 |
| Part-to-part skew (ns) | 20 | 10 | 2 |
| ESD on all pins (kV) | ±2 | ±2 | ±4 |
| CM transient immunity (kV/µs) | 20 | 25 | 25 |
| Temperature (°C) | –45 to 125 | –40 to 125 | –55 to 125 |
| MTTF @ 125°C, 90% confidence (years) | 8 | 1746 | 2255 |
| FIT @ 125°C, 90% confidence | 14391 | 65 | 50 |
| Magnetic immunity @ 1 kHz ($Wb/m^2$) | — | $10^2$ | $10^8$ |
| Radiated electromagnetic-field immunity<br>IEC61000-4-3 (80 to 1000 MHz)<br>MIL-STD 461E RS103 (30 to 1000 MHz) | <br>—<br>— | <br>Fails<br>Fails | <br>Compiles<br>Compiles |
| High-voltage lifetime expectancy (years) | < 5 | < 10 | > 28 |

## 1.4 EMC — Transient Overvoltage Stress

In industrial applications, lightning strikes, power source fluctuations, inductive switching, and electrostatic discharge (ESD) can cause damage to binary inputs by generating large transient voltages. The following ESD protection and surge protection specifications are relevant to binary input applications:

- IEC 61000-4-2 ESD protection
- IEC 61000-4-5 Surge protection

The level of protection can be further enhanced when using external clamping devices, such as TVS diodes. TVS diodes are normally used to protect silicon devices, like binary inputs, from transients. The protection is accomplished by clamping the voltage spike to a limit, by the low impedance avalanche breakdown of a PN junction. TVS diodes are ideally open-circuit devices. A TVS diode can be modeled as a large resistance in parallel with some capacitance while working below its breakdown voltage. When a transient is generated and the surge voltage is larger than the breakdown voltage of the TVS, the resistance of the TVS decreases to keep the clamping voltage constant. The TVS clamps the pulse to a level that does not damage the device that it is protecting. The transients are clamped instantaneously (< 1 ns) and the damaging current is diverted away from the protected device.

## 1.5 TI Isolator Solutions for Binary Input Module

### 1.5.1 ISO72x Family of High-Speed Digital Isolators

The Texas Instruments ISO72x family of isolators use capacitive coupling. The capacitive coupling solution uses proven and cost-effective manufacturing processes and provides an inherent immunity to magnetic fields.

To provide transfer of steady-state information, the ISO72x uses both a high-signaling rate and low-signaling rate channel to communicate as shown in Figure 2. The high-signaling rate channel is not encoded and it transmits data transitions across the barrier after a single-ended-to-differential conversion. The low-signaling rate channel encodes the data in a pulse-width modulated format and transmits the data across the barrier differentially, ensuring the accurate communication of steady-state conditions (long string of 1s or 0s).

Differential transfer of the single-ended logic signal across the isolation barrier allows low-level signals and small coupling capacitance. This appears as high impedance to common-mode noise and, with the common-mode noise rejection of the receiver, gives excellent transient immunity, the primary concern in capacitive coupling of signals.

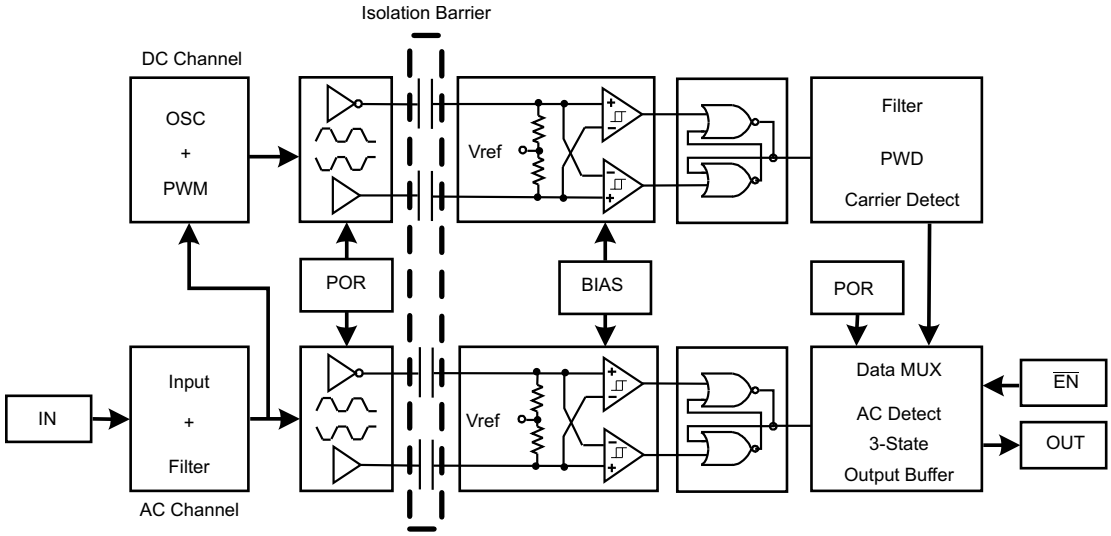



**Figure 2. ISO72x Isolator Internal Diagram**

### 1.5.2 Power Consumption

Beyond the efficiency of the signal transfer across the barrier, the design of the input and output conditioning circuitry has the most to do with power consumption. As shown in Table 3, the opto-couplers use more power than the inductive or capacitive examples.

**Table 3. Quiescent Power Supply Current Table**

| PART | COUPLING TECHNOLOGY | $V_{CC1}$ AND $V_{CC2}$ (V) | $I_{CC1}$ (mA) | $I_{CC2}$ (mA) | POWER (mW) |
|---|---|---|---|---|---|
| ISO721 | Capacitive | 5 | 1 | 11 | 60 |
| | | 3.3 | 0.5 | 6 | 21.5 |
| ADuM1100 | Magnetic | 5 | 0.8 | 0.06 | 4.3 |
| | | 3.3 | 0.3 | 0.04 | 1.2 |
| HCPL-0900 | Magnetic | 5 | 0.018 | 6 | 30 |
| | | 3.3 | 0.01 | 4 | 13.2 |
| HCPL-0721 | Optical | 5 only | 10 (1) | 9 | 95 |
| HCPL-0723 | Optical | 5 only | 10 (1) | 17.5 (2) | 137.5 |

(1) 10 mA is for the logic-low input state. When the logic input state is high, then the current consumption drops to 3 mA.
(2) 17.5 mA is for the logic-low input state. When the logic input state is high, then the current consumption drops to 16.5 mA.

### 1.5.3 Reliability

Mean time to failure (MTTF) is a standard measure for reliability of semiconductor devices. For digital isolators, this measure represents the reliability of both the integrated circuit and the isolation mechanism. Table 4 shows the MTTF of an optical, inductive, and capacitive digital isolator. The ISO721 is very reliable when compared to inductive and optical solutions.

**Table 4. MTTF Reliability Measurement**

| PART | COUPLING TECHNOLOGY | AMBIENT TEMPERATURE (°C) | TYPICAL, 60% CONFIDENCE | | TYPICAL, 90% CONFIDENCE | |
|---|---|---|---|---|---|---|
| | | | MTTF (Hr/Fail) | FITs (Fail/$10^9$ Hr) | MTTF (Hr/Fail) | FITs (Fail/$10^9$ Hr) |
| ISO721 | Capacitive | 125 | 1,246,889 | 802 | 504,408 | 1983 |
| HCPL-0900 | Inductive | 125 | 288,118 | 3471 | 114,654 | 8722 |
| HCPL-0721 | Optical | 125 | 174,617 | 5727 | 69,487 | 14.391 |

## *1.6 Isolated 2-Channel, Wide AC/DC Binary Input Module TI Design Advantages*

Some of the advantage of the AC/DC binary input module is as follows:

- Allows for measurement of wide AC/DC input
- Uses MCU to allow flexibility in terms of input voltage processing and measurement accuracy
- Reduces any error that could be caused due to bridge rectifier at the input (no bridge rectifier used)
- Improves voltage input measurement accuracy by using multiple gains
- Provides provision for programmable threshold on the host side
- Uses digital isolator to increase reliability
- Uses MCU capabilities to control of wetting current
- Costs optimized solution

## 2 Design Features

The AC/DC binary module measures the input voltage in terms of ADC counts. To ensure wide input AC/DC voltages are measured within the required accuracy, two gain stages have been used for each input: High gain and Low gain. ADC counts after subtracting the DC offset is averaged for 30 ms. ADC counts for each channel (High and Low) are communicated to the host. The host converts the ADC count into voltage for further processing. The conversion factor changes for DC and AC voltages. The conversion factor also changes for high gain and low gain.

**Table 5. AC/DC Binary Input — Electrical Specifications**

| SERIAL NUMBER | PARAMETER | DESCRIPTION | COMMENT |
|---|---|---|---|
| 1 | Number of inputs | 2 | Both inputs share common ground |
| 2 | Input voltage range | 15-V to 276-V AC/DC | Maximum permissible voltage input is ≤ 300-V AC/DC |
| 3 | Input voltage frequency | DC or AC (50 or 60 Hz) sinusoidal | |
| 4 | Measurement resolution | <1 V for input values between 24-V to 230-V AC/DC | Binary module communicates measured voltage as ADC counts using $I^2C$ interface to the host |
| 5 | Input voltage measurement accuracy | ±3% of measured value ±1 V (programmable step size) | |
| 6 | Input voltage resistance | ≥ 300 KΩ | |
| 7 | Current drain at voltage input | < 1 mA | |
| 8 | Response time | ≥ 30 ms | Measurement averaged over 30 ms |
| 9 | Binary input wetting resistance for DC input | ≥ 2.5 KΩ | Default wetting is off<br>Binary wetting pulse width is based on nominal voltage (24 V, 110 V, 230 V) |
| 10 | Isolator type | • $I^2C$ isolator<br>• Digital isolators (replaces $I^2C$ isolator) | 3.3-V isolated voltage is generated internally on the module. |
| 11 | Binary input contact type | External wetting type | Tested with DC input |
| 12 | Voltage reference | 1.65-V DC | |
| 13 | Reference temperature | 25°C | |
| 14 | Isolation of binary inputs | Group isolated | |
| 14 | Electrical isolation level | > 2 $kV_{RMS}$ | |
| 16 | Protection against ESD, surge (EMC requirements) | ESD: 2 kV, contact<br>Surge: 2 kV , 42-Ω differential mode | |

**NOTE:** Do not apply AC voltage when the module is configured for DC input and wetting current functionality. This can damage the board.

## 3 Block Diagram

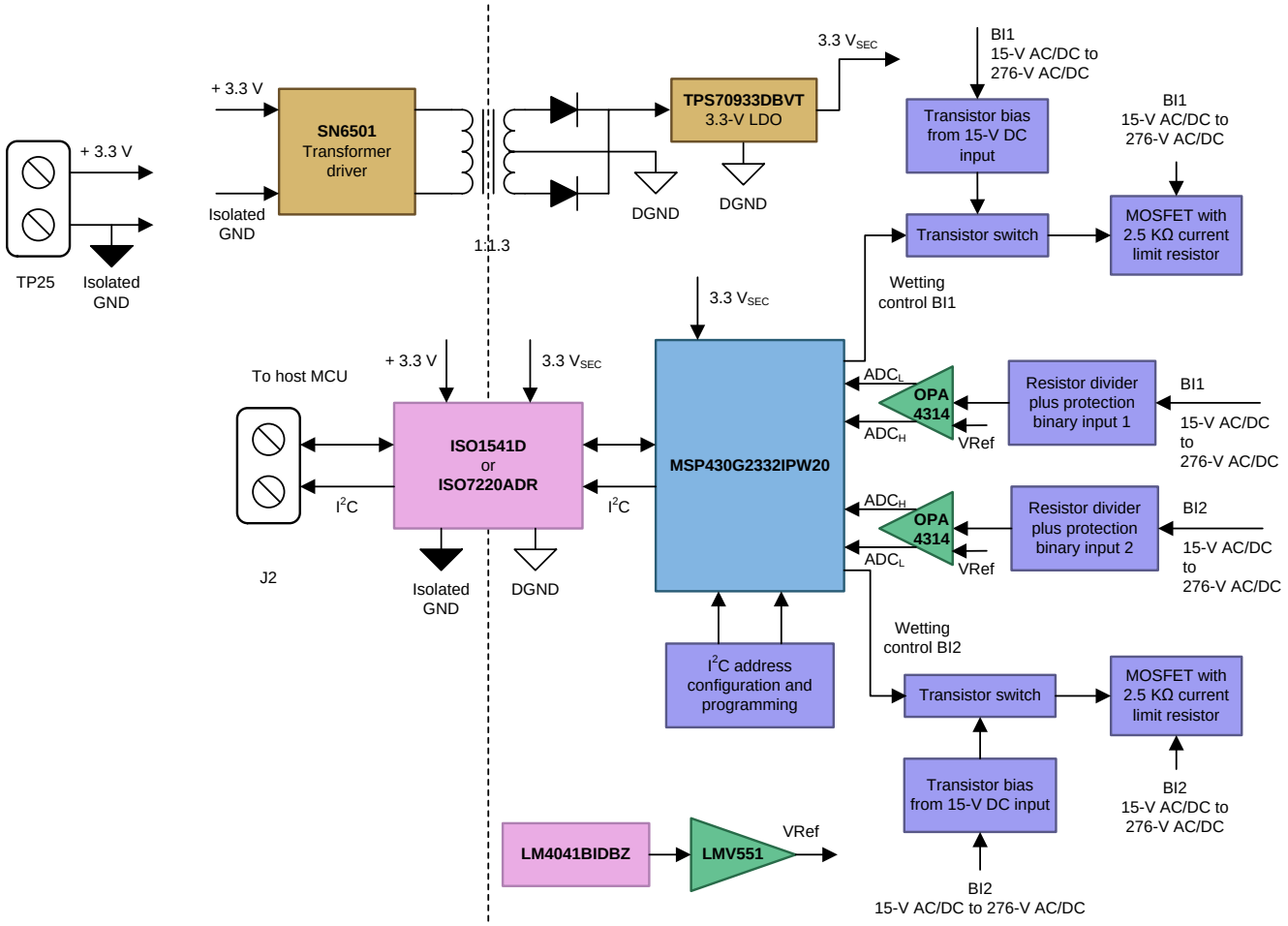



**Figure 3. Block Diagram of AC/DC Binary Input Module**

### 3.1 MCU With Internal ADC

The MSP430 family of ultra-low-power microcontrollers has been considered for this TI design. The MCU considered is MSP430G2332IPW20. The MCU has an internal 10-bit ADC.

Other features include:

- Low supply voltage range: 1.8 to 3.6 V
- Ultra-low power consumption
  - Active mode: 220 µA at 1 MHz, 2.2 V
- Internal very-low-power low-frequency (LF) oscillator
- One 16-bit Timer_A with three capture/compare registers

### 3.2 Digital Isolator

To meet safety requirements, the binary input module is isolated from the host interface. Digital isolators have been considered for isolation. The binary inputs status information is communicated to the host MCU using the following options:

- I$^2$C isolator: ISO1541D low-power bidirectional I$^2$C isolators The status information is communicated as ADC counts that can be converted to voltage
- Digital isolator: ISO7220ADR dual-channel digital isolators. The status information is conveyed as above (high) or below (low) a set value

## 3.3 Isolated Power Supply

The isolated power for the MCU, digital isolator, and the signal conditioning circuit used for sensing the binary inputs are generated using a Push-Pull Driver for Isolated Power Supplies SN6501DBV. The transformer used for this application is 750313638. The transformer package is selected to have isolation voltage of > 5 kV. Choosing a bigger transformer package facilitates easy migration to reinforced isolators. Zener diode PTZTE253.9B is used for protecting the power supply against overvoltage and ESD. The Isolated power supply operates with a single 3.3-V input. The host interface provides the required power supply for the binary module operation. An LDO TPS70933DBVT is used to improve the ADC dynamic range and accuracy of the output supply voltage.

## 3.4 Host Interface

The status of the binary output can be communicated as voltage otuput ($I^2C$ output) or digital output. The status is communicated to a host MCU. Tiva™ C Series TM4C123G LaunchPad™ Evaluation Board is used as the host MCU.

**NOTE:** The host MCU (LaunchPad) is not part of the binary module.

## 3.5 Input Voltage Divider, Signal Conditioning, and Protection

- Input protection: TVS SMCJ400CA is used for protecting binary input module against overvoltage and transient inputs. Package selection is critical to ensure the device has low leakage with temperature variation.
- Resistor divider: The AC/DC binary input voltage applied is divided by a resistor divider, which presents a constant resistance to the binary input. Multiple resistors are used to ensure the resistors withstand the maximum input voltage reliably. The output of the resistor divider is measured by the ADC, and the output voltage range is within the ADC measurement range at maximum input. A Zener diode PTZTE255.1B is used to protect the electronic circuit from overvoltage.
- Reference: For measuring AC/DC inputs, the input is level shifted by ADC_reference/2. The 1.65-V DC reference is generated using LM4041. The LMV551 Micropower RRO, a high-performance, low-power operational amplifier, is used as buffer for the reference output.
- Gain: To measure wide input AC/DC accurately, an amplifier gain stage is provided. The gain stages are unity gain and a gain of 3.5. These gains are chosen to cover input range of 15 to 276 V. The OPA4314 amplifier stage is used.

## 3.6 Wetting Current Control

### 3.6.1 Transistor Drive for MOSFET Gate driver

A transistor is used to drive the MOSFET that controls the wetting current. The bias voltage of 15 V max for the MOSFET operation is generated from the binary input using a Zener regulator. The bias current for the Zener must be in µA and care should be taken during selection of the Zener. Voltage Vz versus Iz characteristics is critical.

### 3.6.2 Wetting Current Limiting Resistor and MOSFET

Four resistors, 10 KΩ each connected in parallel, are used as current limit for wetting current. A D-PAK MOSFET with a 600-V rating AOD2N60A is used that ensures reliability of the MOSFET. *The short time overload capability of the resistor is being used and care should be taken to not test the wetting current for test > 100 ms (typically 50 ms).*

# 4 Circuit Design and Component Selection

## 4.1 MCU With Internal ADC

The binary input modules are cost sensitive and to ensure the overall solution cost is optimal, MCU with internal ADC has been selected. The internal ADC is a 10-bit SAR ADC.

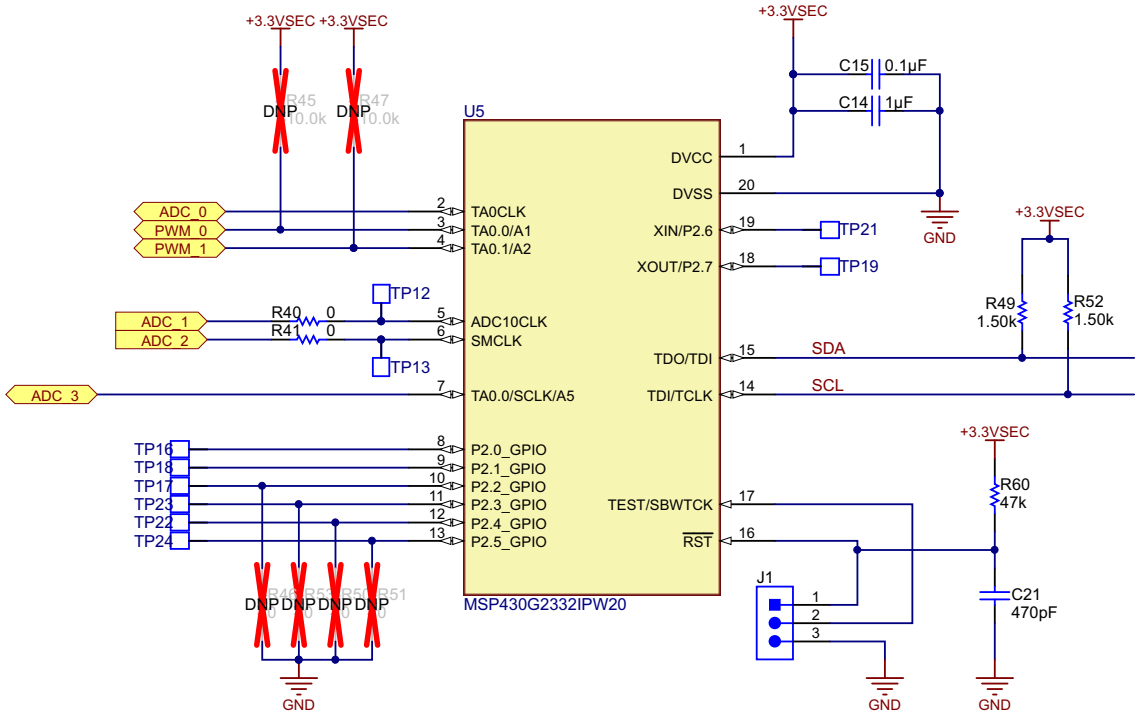



**Figure 4. MCU Functionality Configuration**

The MCU considered is MSP430G2332IPW20. Texas Instruments MSP430 family of ultra-low-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430G2332IPW20 is a ultra-low-power mixed signal microcontroller with a built-in 16-bit timer. The device has up to 16 I/O capacitive-touch enabled pins and built-in communication capability using the universal serial communication interface. TheMSP430G2332IPW20 has a 10-bit A/D converter.

### 4.1.1 Features

- Low supply voltage range: 1.8 to 3.6 V
- Ultra-low power consumption
  - Active mode: 220 µA at 1 MHz, 2.2 V
  - Standby mode: 0.5 µA
  - Off mode (RAM retention): 0.1 µA
- Five power-saving modes
- Ultra-fast wake-up from standby mode in less than 1 µs
- 16-bit RISC architecture, 62.5-ns instruction cycle time
- Basic clock module configurations
  - Internal frequencies up to 16 MHz with four calibrated frequencies
  - Internal very-low-power LF oscillator
  - 32-kHz crystal
  - External digital clock source
- One 16-bit Timer_A with three capture/compare registers
- Universal serial interface (USI) supporting SPI and $I^2C$
- 10-bit 200-ksps A/D converter with internal reference, sample-and-hold, and Autoscan (MSP430G2x32 only)
- Brownout detector
- Serial onboard programming, no external programming voltage needed, programmable code protection by security fuse
- On-chip emulation logic with Spy-Bi-Wire interface
- Package
  - TSSOP: 20-pin

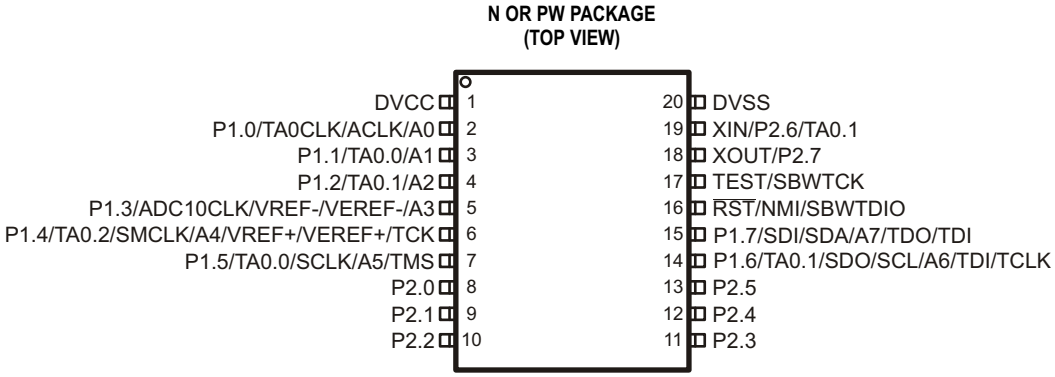



**Figure 5. MCU Pinout Description**

### 4.1.2 MCU Resources

**Table 6. MCU RAM and Flash Size**

| PIN NUMBER | DESCRIPTION | SIZE |
|---|---|---|
| 1 | Flash | 4 KB |
| 2 | RAM | 256 bytes |
| 3 | ADC10 | 8 channels |
| 4 | Package and pin count | 20-TSSOP |

### 4.1.3 MCU Configuration

**Table 7. MCU Pin Configuration for the AC/DC Binary Module**

| PIN NUMBER | PIN FUNCTION | CONFIGURATION |
|---|---|---|
| 1 | DVCC | 3.3 $V_{SEC}$ |
| 2 | A0 | ADC_0 (Binary Input1 – Low Gain) |
| 3 | TA0.0 | PWM_0 (Control of Binary Input1 wetting current) |
| 4 | TA0.1 | PWM_1 (Control of Binary Input2 wetting current) |
| 5 | A3 | ADC_1 (Binary Input1 — High Gain) |
| 6 | A4 | ADC_2 (Binary Input2 — High Gain) |
| 7 | A5 | ADC_3 (Binary Input2 — Low Gain) |
| 8 | P2.0 | Not used — configured as output |
| 9 | P2.1 | Not used — configured as output |
| 10 | P2.2 | Can be used to set $I^2C$ address — configured as output |
| 11 | P2.3 | Can be used to set $I^2C$ address — configured as output |
| 12 | P2.4 | Can be used to set $I^2C$ address — configured as output |
| 13 | P2.5 | Can be used to set $I^2C$ address — configured as output |
| 14 | SCL | $I^2C$ clock |
| 15 | SDA | $I^2C$ data |
| 16 | /RST | Programming |
| 17 | SBWTCK | Programming |
| 18 | P2.7 | Not used — configured as output |
| 19 | P2.6 | Not used — configured as output |
| 20 | DVSS | GND |

### 4.1.4 ADC Features

The ADC used is a 10-bit, 8-channel ADC with Autoscan and DMA capabilities.

**Table 8. 10-Bit ADC, Timing Parameters (MSP430G2x32 Only)[1]**

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{ADC10CLK}$ | ADC input clock frequency | For specified performance of ADC10 linearity parameters | ADC10SR = 0 | 3 V | 0.45 | | 6.3 | MHz |
| | | | ADC10SR = 1 | | 0.45 | | 1.5 | |
| $f_{ADC10OSC}$ | ADC10 built-in oscillator frequency | ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$ | | 3 V | 3.7 | | 6.3 | MHz |
| $t_{CONVERT}$ | Conversion time | ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$ | | 3 V | 2.06 | | 3.51 | µs |
| | | $f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0 | | | 13 × ADC10DIV × $1/f_{ADC10CLK}$ | | | |
| $t_{ADC10ON}$ | Turn-on setting time of the ADC | [2] | | | | | 100 | ns |

(1) Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(2) The condition is that the error in a conversion started after tADC10ON is less than ±0.5 LSB. The reference and input signal are already settled.

**Table 9. 10-Bit ADC, Linearity Parameters (MSP430G2x32 Only)**

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error | | 3 V | | | ±1 | LSB |
| $E_D$ | Differential linearity error | | 3 V | | | ±1 | LSB |
| $E_O$ | Offset error | Source impedance $R_S$ < 100 Ω | 3 V | | | ±1 | LSB |
| $E_G$ | Gain error | | 3 V | | ±1.1 | ±2 | LSB |
| $E_T$ | Total unadjusted error | | 3 V | | ±2 | ±5 | LSB |

## 4.2 Digital Isolator

The binary input module is isolated from the host MCU. TI digital isolators are used to provide the required isolation. The isolator could be digital output type or $I^2C$ interface type.

An $I^2C$ interface type isolator provides flexibility in terms of functionality. A digital output type is recommended when cost is critical and the binary inputs are a fixed input voltage.

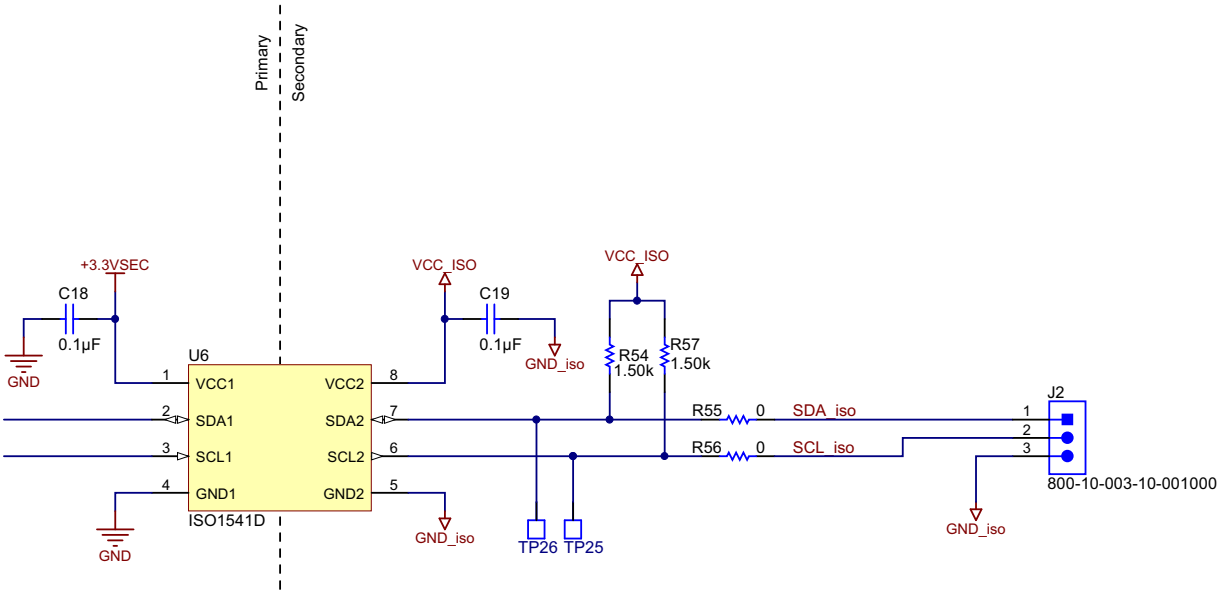



**Figure 6. Digital Isolator for $I^2C$ Interface**

### 4.2.1 $I^2C$ Isolator: ISO1541D Low-Power Bidirectional $I^2C$ Isolators

The ISO1541 are low-power, bidirectional isolators that are compatible with $I^2C$ interfaces. These devices have their logic input and output buffers separated by TI's capacitive isolation technology using a SiO2 barrier. When used in conjunction with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

This isolation technology provides for function, performance, size, and power consumption advantages when compared to opto-couplers. The ISO1541 enable a complete isolated $I^2C$ interface to be implemented within a small form factor. The ISO1541 is useful in applications that have a single master while the ISO1540 is ideally fit for multi-master applications.

Isolated bidirectional communications is accomplished within these devices by offsetting the Side 1 Low-Level Output Voltage to a value greater than the Side 1 High-Level Input Voltage thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

#### 4.2.1.1 Features

- Isolated bidirectional, $I^2C$ compatible, communications
- Supports up to 1-MHz operation
- 3- to 5.5-V supply range
- Open drain outputs with 3.5-mA Side 1 and 35-mA Side 2 sink current capability
- –40°C to 125°C operating temperature
- ±50 kV/µs transient immunity (typical)
- HBM ESD protection of 4 kV on all pins; 8 kV on bus pins

### 4.2.2 Digital Isolator: ISO7220ADR Dual Channel Digital Isolators

The ISO7220 are dual-channel digital isolators. The logic input and output buffer is separated by TI's SiO2 isolation barrier, providing galvanic isolation of up to 4000 VPK per VDE. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received every 4 µs, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state.

The small capacitance and resulting time constant provide fast operation with signaling rates available from 0 Mbps (DC) to 150 Mbps. The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second). The A-, B-, and C-option devices have TTL input thresholds and a noise filter at the input that prevents transient pulses from being passed to the output of the device. The M-option devices have CMOS $V_{CC}$/2 input thresholds and do not have the input noise-filter and the additional propagation delay.

#### *4.2.2.1 Features*

- 1 Mbps signaling rate options
  - Low channel-to-channel output skew; 1-ns max
  - Low pulse-width distortion (PWD); 1-ns max
  - Low jitter content; 1 ns typical at 150 Mbps
- 50 kV/µs typical transient immunity
- Operates with 2.8-V (C-Grade), 3.3-V or 5-V supplies
- 4-kV ESD protection
- High electromagnetic immunity
- –40°C to 125°C operating range
- Typical 28-year life at rated voltage (see *High-Voltage Lifetime of the ISO72x Family of Digital Isolators* [SLLA198])
- VDE basic insulation with 4000-VPK VIOTM, 560 VPK VIORM per DIN EN 60747-5-5 (VDE 0884-5) and DIN EN 61010-1 (VDE 0411-1)
- 2500 $V_{RMS}$ isolation per UL 1577
- CSA approved for component acceptance notice 5 A and IEC 60950-1

**NOTE:** ISO7220ADR is pin compatible to the $I^2C$ isolator and hence is not shown in the schematics. Based on the requirement, the $I^2C$ or digital isolator is mounted.

ISO7320 series isolators provide higher isolation and surge ratings. These devices are pin compatible and can be considered based on application requirement.

## 4.3 Isolated Power Supply

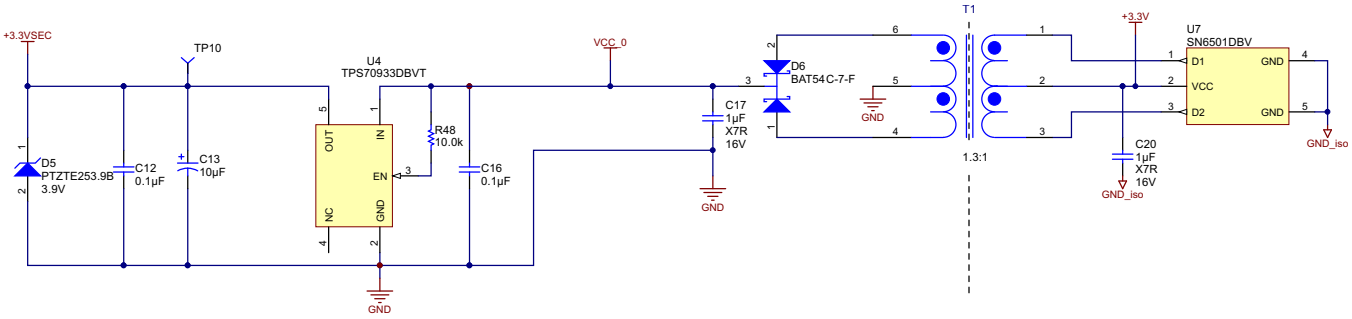



**Figure 7. Isolated Power Supply**

### 4.3.1 Push-Pull Driver for Isolated Power Supplies (SN6501DBV)

The SN6501 is a monolithic oscillator/power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio.

The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches. The SN6501 is available in a small SOT-23 (5) package, and is specified for operation at temperatures from –40°C to 125°C.

#### 4.3.1.1 Features

- Push-pull driver for small transformers
- Single 3.3- or 5-V supply
- High primary-side current drive:
  - 5-V supply: 350 mA (max)
  - 3.3-V supply: 150 mA (max)
- Low ripple on rectified output permits small output capacitors
- Small 5-pin SOT-23 package

### 4.3.2 Isolation Transformer

**Table 10. Isolation Transformer 750313638 Specifications**

| PARAMETER | SPECIFICATION |
|---|---|
| Type | DC/DC converter |
| Applications | Forward, push-pull converters |
| Intended chipset | SN6501 |
| Voltage — Primary | — |
| Voltage — Auxillary | — |
| Voltage — Isolation | 5000 $V_{RMS}$ |
| Frequency | — |
| Operating temperature | –40°C to 125°C |
| Mounting type | Surface mount |
| Size and dimension | 9.14 × 8.00 mm (L × W) |
| Height — Seated (max) | 7.62 mm |
| Chipset manufacturer | Texas Instruments |

### 4.3.3 Power Supply Overvoltage and ESD Protection Zener (PTZTE253.9B)

**Table 11. 3.9-V Power Supply Protection Zener Diode Specification**

| PARAMETER | SPECIFICATION |
|---|---|
| Voltage — Zener (Nom; Vz) | 4.1 V |
| Tolerance | ±6% |
| Power — Max | 1 W |
| Impedance (Max; Zzt) | 15 Ω |
| Current — Reverse leakage @ Vr | 40 µA @ 1 V |
| Mounting type | Surface mount |
| Package or case | DO-214AC, SMA |
| Supplier device package | PMDS |

### 4.3.4 LDO

The TPS70933DBVT linear regulator is an ultra-low, quiescent current device designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. A quiescent current of only 1 µA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety.

**Table 12. 3.3-V LDO Specifications**

| PARAMETER | SPECIFICATION |
|---|---|
| Regulator topology | Positive fixed |
| Voltage — Output | 3.3 V |
| Current — Output | 150 mA |
| Voltage — Dropout (Typical) | 0.96 V @ 150 mA |
| Number of regulators | 1 |
| Voltage — Input | Up to 30 V |
| Current — Limit (Min) | 200 mA |
| Operating temperature | –40°C to 125°C |
| Package | SOT23-5 |

## 4.4 Simulation of Host MCU Interface

To test the functionality, the host interface was simulated using an MCU-based system.

### 4.4.1 Tiva C Series LaunchPad Interface

The Tiva C Series LaunchPad (EK-TM4C123GXL) is a low-cost evaluation platform for ARM® Cortex™-M4F-based microcontrollers. The Tiva C Series LaunchPad design highlights the TM4C123GH6PMI microcontroller USB 2.0 device interface, hibernation module, and motion control pulse-width modulator (MC PWM) module. The Tiva C Series LaunchPad also features programmable user buttons and an RGB LED for custom applications. The stackable headers of the Tiva C Series LaunchPad BoosterPack™ XL interface demonstrate how easy it is to expand the functionality of the Tiva C Series LaunchPad when interfacing to other peripherals on many existing BoosterPack add-on boards as well as future products. Figure 8 shows a photo of the Tiva C Series LaunchPad.

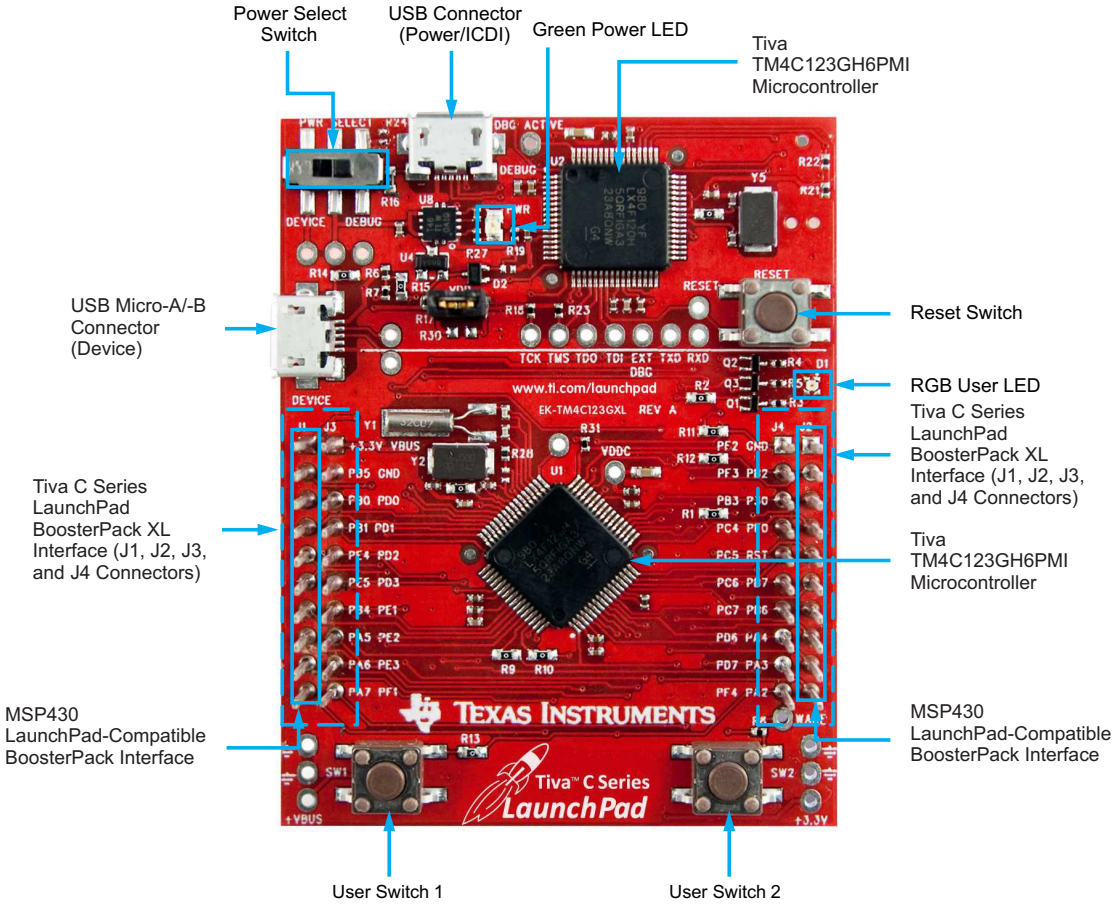



**Figure 8. Tiva C Series TM4C123G LaunchPad Evaluation Board**

## 4.5 Input Voltage Divider, Signal Conditioning, and Protection

### Note on resistor divider

The 300-KΩ resistance was increased to 500 KΩ and 1 MΩ, and voltage measurement accuracy was tested. No variation in accuracy was observed with increase in resistance. The 300-KΩ impedance has been finalized assuming that the binary inputs would be specified with minimum resistance. The ratio of division has to be maintained even with an increase in total resistance.

### Note on gain resistors

Since these modules are expected to measured AC/DC inputs, the resistance value is critical for accuracy. Do not increase the resistance above the values used as shown in Figure 9. In case values are increased, there may be change in accuracy, and these need to be verified.

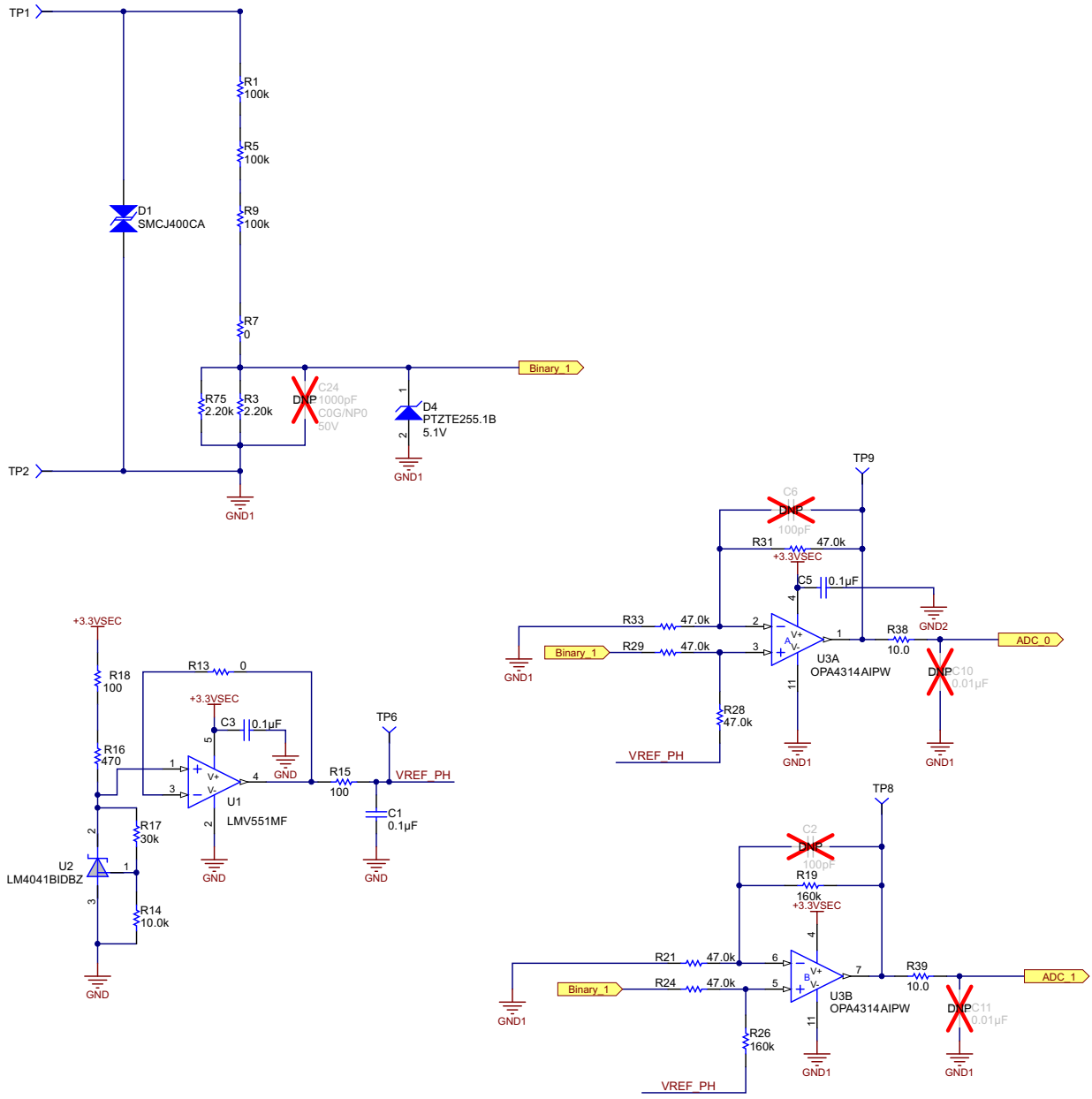



**Figure 9. Analog Input and Gain**

### 4.5.1 Input Protection

The binary input module is protected against overvoltage and transients. The SMCJ400CA is used achieve the required protection.

**Table 13. SMCJ400 Specifications**

| PARAMETER | SPECIFICATION |
|---|---|
| Type | Zener |
| Bidirectional channels | 1 |
| Voltage — Reverse standoff (Typ) | 400 V |
| Voltage — Breakdown (Min) | 447 V |
| Voltage — Clamping (Max) @ $I_{PP}$ | 648 V |
| Current — Peak Pulse (10/1000 µs) | 2.3 A |
| Power — Peak pulse | 1500 W (1.5 kW) |
| Power line protection | No |
| Applications | General Purpose |
| Capacitance @ frequency | — |
| Operating temperature | –55°C to 150°C ($T_J$) |
| Mounting type | Surface mount |
| Package or case | DO-214AB, SMC |

### 4.5.2 Resistor Divider

A 100-KΩ 1206 package resistor, which can withstand a maximum voltage of 200 V, is selected for this application. The resistor tolerance and temperature drift can be selected based on the accuracy requirement.

### 4.5.3 ADC Input Overvoltage Protection (PTZTE255.1B)

A Zener diode is used to protect the electronic circuit from overvoltage and ESD.

**Table 14. 5.1-V Analog Input to ADC Protection Diode Specifications**

| PARAMETER | SPECIFICATION |
|---|---|
| Voltage — Zener (Nom; Vz) | 5.4 V |
| Tolerance | ±6% |
| Power — Max | 1 W |
| Impedance (Max; Zzt) | 8 Ω |
| Current — Reverse leakage @ Vr | 20 µA @ 1 V |
| Mounting type | Surface mount |
| Package or case | DO-214AC, SMA |

### 4.5.4 Amplifier Gain Stage Using OPA4314

The OPA4314 family of single-, dual- and quad-channel operational amplifiers represents a new generation of low-power, general-purpose CMOS amplifiers. Rail-to-rail input and output swings, low-quiescent current (150 µA typ at 5.0 VS) combined with a wide bandwidth of 3 MHz, and very low noise (14 nV/√Hz at 1 kHz) make this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance. The low input bias current supports applications with MΩ source impedances.

The robust design of the OPA314 devices provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 300 pF, an integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high ESD protection (4-kV HBM).

These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V), and are specified over the full extended temperature range of –40°C to 125°C. The quad-channel OPA4314 used is TSSOP-14 package.

**Table 15. OPA4314 Specifications**

| PARAMETER | SPECIFICATION |
|---|---|
| Characteristics | OPA4314 |
| $I_Q$ Total (Max; mA) | 0.720 |
| Number of channels | 4 |
| Rail-to-rail | In/out |
| Operating temperature range (°C) (Package dependent exception exist) | –40 to 125 |
| Vos (Offset voltage @ 25°C) (Max; mV) | 2.5 |
| Offset drift (Typ; µV/°C) | 1 |
| Vn at 1 kHz (Typ; nV/rtHz) | 14 |
| CMRR (Min; dB)/PSRR | 94/92 |
| IBias (Max; pA) | 10 |
| Total supply voltage (Max; 5 V = 5, ±5 V = 10) | 5.5 |
| Total supply voltage (Min; 5 V = 5, ±5 V = 10) | 1.8 |
| Slew rate (Typ; V/µs) | 1.5 |
| GBW (Typ; MHz) | 3 |
| Pin or package | 14TSSOP |
| ESD — Human model (kV) | 4 |
| EMI filter | Internal |
| Vo (Swing) | $V_{CC}$ (60 mV) |
| Vcm (input) | V– (–0.2 V) , V+ (0.2 V) |

**NOTE:** Other devices like LMV614 can also be considered.

### 4.5.5 Reference

The DC reference for level-shifting is generated using LM4041.

#### *4.5.5.1 Adjustable Precision Shunt Voltage Reference*

The LM4041 series of shunt voltage references are versatile, easy-to-use references suitable for a wide array of applications. The reference is used for level shifting the AC voltage input by AVDD/2. 1.65 V is a level by which the input voltage is shifted. This series requires no external capacitors for operation and is stable with all capacitive loads. Additionally, the reference offers low-dynamic impedance, low noise, and a low temperature coefficient to ensure a stable output voltage over a wide range of operating currents and temperatures. The LM4041 uses fuse and Zener-zap reverse breakdown voltage trim during wafer sort to offer four output voltage tolerances, ranging from 0.1% (max) for the A grade to 1% (max) for the D grade. As a result, a great deal of flexibility is offered to designers in choosing the best cost-to-performance ratio for their applications. The LM4041 is available in a fixed (1.225 V nominal) or an adjustable version, which requires an external resistor divider to set the output to a value between 1.225 V and 10 V.

#### *4.5.5.2 Features*

- Small packages: SOT23, SC70-5
- No output capacitor required
- Output voltage tolerance
- LM4041D: ±1% at 25°C
- Low output noise: 20 $\mu V_{RMS}$ (10 Hz to 10 kHz)
- Wide operating current range: 60 µA to 12 mA
- Extended temperature range: –40°C to 125°C
- Low temperature coefficient: 100 ppm/°C (max)

#### *4.5.5.3 Buffer for Reference*

The LMV551 are high-performance, low-power operational amplifiers implemented with TI's advanced VIP50 process. They feature 3 MHz of bandwidth while consuming only 37 µA of current per amplifier, which is an exceptional bandwidth to power ratio in this op-amp class. These amplifiers are unity gain stable and provide an excellent solution for low power applications requiring a wide bandwidth.

**Table 16. Reference Buffer Amplifier Specifications**

| PARAMETER | SPECIFICATION |
|---|---|
| Amplifier type | General purpose |
| Number of circuits | 1 |
| Output type | Rail-to-rail |
| Slew rate | 1 V/µs |
| Gain bandwidth product | 3 MHz |
| –3-db bandwidth | — |
| Current — Input bias | 20 nA |
| Voltage — Input offset | 1 mV |
| Current — Supply | 37 µA |
| Current — Output / channel | 25 mA |
| Voltage — Supply, single or dual (±) | 2.7 to 5.5 V |
| Operating temperature | –40°C to 125°C |
| Mounting type | Surface mount |

## 4.6 Wetting Current Control (Used for DC Inputs Only)

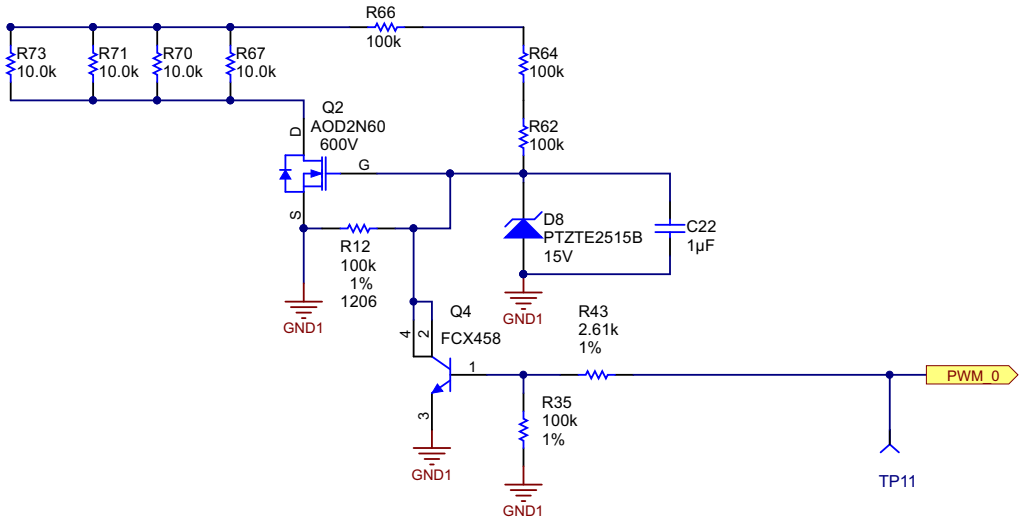



**Figure 10. Wetting Current Control Circuit**

### 4.6.1 Transistor Drive for MOSFET Gate Driver

A transistor is used to drive the MOSFET that controls the wetting current. The bias voltage of 15 V max is generated from the binary input using a Zener PTZTE2515BCT regulator.

**Table 17. 15-V Transistor Bias Voltage Regulation Zener Specification**

| PARAMETER | SPECIFICATION |
|---|---|
| Voltage — Zener (Nom; Vz) | 15.4 V |
| Tolerance | ±6% |
| Power — Max | 1 W |
| Impedance (Max; Zzt) | 10 Ω |
| Current — Reverse leakage @ Vr | 10 µA @ 11 V |
| Mounting type | Surface mount |
| Package or case | DO-214AC, SMA |

**Table 18. FCX458 Transistor Specifications**

| PARAMETER | SPECIFICATION |
|---|---|
| Transistor type | NPN |
| Current — Collector (Ic; Max) | 225 mA |
| Voltage — Collector emitter breakdown (Max) | 400 V |
| Vce saturation (Max) @ Ib, Ic | 500 mV @ 6 mA, 50 mA |
| Current — Collector cutoff (Max) | 100 nA |
| DC current gain (hFE) (Min) @ Ic, Vce | 100 @ 50 mA, 10 V |
| Power (Max) | 1 W |
| Frequency — Transition | 50 MHz |
| Mounting type | Surface mount |
| Package or case | TO-243AA |

### 4.6.2 Current Limiting Resistors and MOSFET (AOD2N60A)

**Table 19. Wetting Current Control MOSFET Specifications**

| PARAMETER | SPECIFICATION |
|---|---|
| FET type | MOSFET N-channel, metal oxide |
| FET feature | Standard |
| Drain-to-source Voltage ($V_{DS}$) | 600 V |
| Current — Continuous drain (Id) @ 25°C | 2 A (Tc) |
| Rds On (Max) @ Id, Vgs | 4.7 Ω @ 1 A, 10 V |
| $V_{GS(th)}$ (Max) @ Id | 4.5 V @ 250 µA |
| Gate charge (Qg) @ Vgs | 11 nC @ 10 V |
| Input capacitance (Ciss) @ $V_{DS}$ | 295 pF @ 25 V |
| Power (Max) | 57 W |
| Mounting type | Surface mount |
| Package or case | TO-252-3, DPak (Two Leads + Tab), SC-63 |
| Supplier device package | TO-252 (D-Pak) |

Four resistors, 1206 package 10 KΩ each in parallel, are used as current limit for wetting current. A D-PAK MOSFET with a 600-V rating is used for enhanced reliability.

## 4.7 Hardware Design Guidelines

- Input voltage divider selection: Ensure the resistors are de-rated 30% for the maximum withstand voltage rating.
- Wetting current control resistor selection: The short time overload capability must be greater than 2.5 times the normal voltage withstand capability for one second.
- 15-V Zener selection for MOSFET switching: Vz must be constant for wide bias currents. The Zener current must be as less as possible to reduce power loss.
- Zener selection for ADC input overvoltage protection: At lower biasing, current Vz reduces and this will clip the input voltage affecting accuracy. The Vz at low bias current must be selected such that at the lowest input voltage, the voltage would be sufficient to bias the MOSFET.

## 4.8 Enhancements — Migration of Digital Isolator From Basic to Reinforced Isolation Type

TI has a reinforced isolator as part of the isolator roadmap that is package and pin compatible. With this design, the migration to reinforce would need minimal efforts of digital isolator replacement and testing. There may not be any design efforts required.

# 5 Software Description

## 5.1 Initialization

**Table 20. MCU Peripherals Initialization for AC/DC Binary Module Functionality**

| FUNCTIONALITY | DESCRIPTION |
|---|---|
| MCU clock | SMCLK and DCO are initialized to 1 MHz |
| Timer | 1. Configure the timer capture control register (TA0CCTL0) to select no capture CMx as 0, compare/capture input selected as CCIxA, output mode OUTMODx as 0 and enable compare interrupt CCIE.<br>2. Timer A programmed to provide interrupt every 200 µs (or any other sampling interval desired). Set the sampling interval (TA0CCR0)<br>3. Configure the Timer A control register (TA0CTL) to choose SMCLK, divider as 1 and up/down mode. |
| ADC – Four channels | 1. Disable conversion.<br>2. Configure the following options for the ADC control register0 (ADC10CTL0):<br>(a) Enable ADC interrupt.<br>(b) Switch ON ADC.<br>(c) Set the sample and hold time to 16 x ADC10CLKs.<br>(d) Set the reference voltages for ADC: VR+ = $V_{CC}$ and VR– = VSS<br>ADC10CTL0, once configured, does not need to be changed to switch between different channels.<br>3. Configure the following options for the ADC control register0 (ADC10CTL1):<br>(a) Set the mode to single channel single conversion.<br>(b) Set the ADC clock to ADC1OSC.<br>(c) Set the divider to 1.<br>(d) Set the sampling trigger to ADC10SC bit.<br>(e) Set the channel to be sampled (A0).<br>4. Enable ADC channels ADC10AE0.<br>5. Enable conversion.<br>6. Once the sampling interval timer issues a trigger, the first ADC channel (A0) is sampled.<br>(a) Once the sample value for channel A0 is read from ADC10MEM, clear the ADC10SC bit.<br>(b) Reinitialize ADC10CTL1 and ADC10AE0 with the other desired ADC channel (A3, A4, or A5).<br>(c) Conversion can be started by making the ADC10SC bit high.<br>(d) Repeat the same process for the other channels (every sampling interval) until all channels have been sampled. |
| Ports | 1. Configure the direction of the ports (P1DIR); 0 as inputs and 1 as outputs.<br>2. Set the default values for outputs (0 as low, 1 as high) |
| $I^2C$ | 1. Set the output pins for $I^2C$ (P1.6 and P1.7) to high.<br>2. Enable the pull up resistors for P1.6 and P1.7 (P1REN).<br>3. Enable the USI function by setting the USIPE6 and USIPE7 bits in USICTL0 register.<br>4. Disable the USI peripheral using software reset (USISWRST bit).<br>5. Enable $I^2C$ mode and USI interrupt enable.<br>6. Set clock polarity.<br>7. Disable automatic clear control (USIIFGCC bit).<br>8. Enable USI peripheral by clearing the (USISWRST bit). |

## 5.2 Functionality

**Table 21. AC/DC Binary Module Functional Description**

| FUNCTIONALITY | DESCRIPTION |
|---|---|
| Power ON | 1. Stop the watchdog timer.<br>2. Initialize the clocks to set SMCLK to 1 MHz.<br>3. Disable all interrupts.<br>4. Set the direction of port pins to default values.<br>5. Initialize $I^2C$ in master mode<br>6. Configure Timer A to provide an interval based interrupt using compare register. The timer interrupt can be used to periodically trigger ADC sampling.<br>7. Initialize ADC to sample one ADC channel. Re-initialize ADC10CTL1 and ADC10AE0 to sample a different ADC channel.<br>8. Enable all interrupts. |
| ADC sample capturing for all four channels | • Samples are triggered by setting ADC10SC bit. (From the timer interrupt for the first channel, meaning A0)<br>• When conversion is complete, it triggers an interrupt. The result is obtained by reading the register ADC10MEM.<br>• Reinitialize the ADC to read the other ADC channels and issue ADC10SC trigger. Repeat this step to read the other ADC channels. |
| ADC samples integration | • After the value is read from ADC10MEM, the offset has to be corrected.<br>• For each ADC channel, the sample values are added over a timer period (1 ms) and then averaged by dividing with the number of sample counts. |
| 30- and 60-ms ADC count calculation | Calculation of 1-ms average (for each channel)<br>• The 1-ms average for each channel can be stored for three iterations (that is, three such 1-ms average values). |
| | Calculation of 3-ms average (for each channel)<br>• 3-ms average can be calculated using the three counts of 1-ms averages and is stored for 10 or 20 counts. |
| | Calculation of 30- or 60-ms average (for each channel)<br>• 10 or 20 counts of 3-ms average is stored and can be averaged to provide 30 or 60 ms average. |
| $I^2C$ interface for communicating ADC count to host | • The 30-ms average values for all four channels can be transmitted over $I^2C$ to the host processor.<br>• A pre-requisite for this is to have a host processor (for example, LaunchPad) that runs as an $I^2C$ slave.<br>• The master sends 30-ms averages for each channel on $I^2C$. |

## 5.3 Calculations

**Table 22. Maximum DC Input Allowed**

| PARAMETER | SPECIFICATION |
|---|---|
| DC offset in ADC counts | 511 |
| ADC range in counts | 1023 – 511 = 512 |
| Resistor divider ratio | 301.1 KΩ / 1.1 KΩ = 273.72 |
| DC input ADC reference span | ADCref = 1.65 V |
| Maximum input voltage | ADCref × Resistor divider ratio = > 300 V |

**Table 23. Maximum AC Input Allowed**

| PARAMETER | SPECIFICATION |
|---|---|
| DC offset in ADC counts | 511 |
| Peak ADC range in counts | 1023 – 511 = 512 |
| RMS ADC range in counts | 512 / (1.414) = 362 |
| Resistor divider ratio | 301.1 KΩ / 1.1 KΩ = 273.72 |
| AC RMS ADC reference span | AvgRef = 1.65 V / (1.414) = 1.1668 |
| Maximum input voltage | AvgRef × Resistor divider ratio = > 300 V |

**Table 24. Converting ADC Count to Voltage — DC Input Low Gain**

| PARAMETER | SPECIFICATION |
|---|---|
| ADCref | 1.65 V |
| Maximum input | 450 V |
| Gain factor | 1 |
| Max ADC count for DC input | 512 |
| DC voltage equivalent for one ADC count | Maximum input / (ADC count × Gain factor) = 0.878 V |

The minimum ADC resolution of 1 count equals approximately 1 V. To improve the resolution, a gain stage of 3.4 is used.

**Table 25. Converting ADC Count to Voltage — DC Input High Gain**

| PARAMETER | SPECIFICATION |
|---|---|
| ADCref | 1.65 V |
| Maximum input | 450 V |
| Gain factor | 3.4 |
| Max ADC count for DC input | 512 |
| DC voltage equivalent for one ADC count | Maximum input / (ADC count × Gain factor) = 0.2582 |

**Table 26. Converting ADC Count to Voltage — AC Input Low Gain**

| PARAMETER | SPECIFICATION |
|---|---|
| ADCref - peak | 1.65 V |
| Maximum input | 315 V |
| Gain factor | 1 |
| Max ADC count for RMS input | 512 / 1.414 = 362 |
| RMS voltage equivalent for one ADC count | Maximum input / (ADC count × Gain factor) = 0.870 |

The minimum ADC resolution of 1 count equals approximately 1 V. To overcome this issue, a gain stage of 3.4 is used.

**Table 27. Converting ADC Count to Voltage — AC Input High Gain**

| PARAMETER | SPECIFICATION |
|---|---|
| ADCref - peak | 1.65 V |
| Maximum input | 315 V |
| Gain factor | 3.4 |
| Max ADC count for RMS input | 512 / 1.414 = 362 |
| RMS voltage equivalent for one ADC count | Maximum input / (ADC count × Gain factor) = 0.260 |

## 5.4 Programming

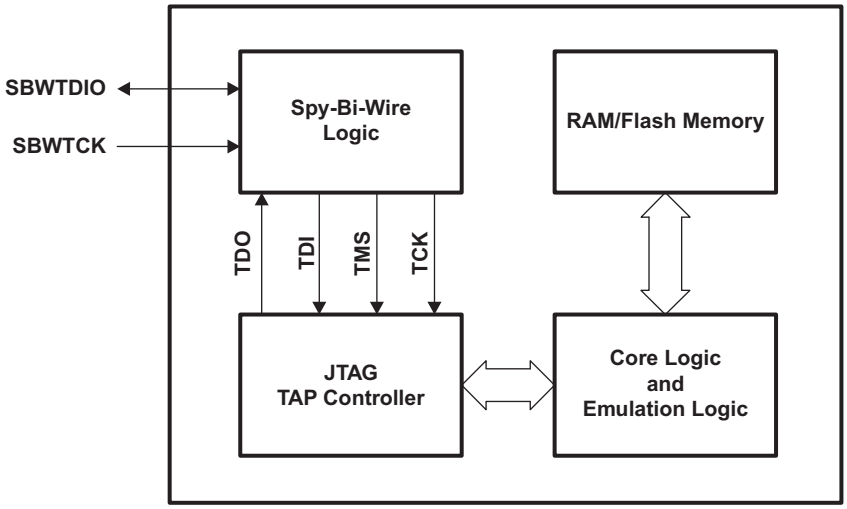



**Figure 11. Spy-Bi-Wire Basic Concept**

The 2-wire interface is made up of the SBWTCK (Spy-Bi-Wire test clock) and SBWTDIO (Spy-Bi-Wire test data I/O) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the $\overline{\text{RST}}$/NMI pin of the device.

# 6 Testing

## 6.1 Functional Testing

**Table 28. Measurements**

| PARAMETER | SPECIFICATION | MEASUREMENT |
|---|---|---|
| Isolated supply and reference | 3.3 V, 1.65 V | 3.31 V, 1.645 V |
| MCU programming | Spy-Bi-Wire | OK |

## 6.2 Voltage Measurement Accuracy Testing

**NOTE:** The reading in the following tables are the measurements taken without any calibration. The errors include component tolerances and ADC error. The accuracy can be improved by introducing software calibration.

The errors observed can be further improved by doing a gain calibration. To ensure that the results are less than ±3.0% of measured value ±1 V (programmable step size), applying gain calibration is recommended. The gain calibration can be applied on the host side.

For initial testing, averaging was done for 10, 30, and 60 ms. The measurement was repeatable at 30 and 60 ms, and there was no difference observed in the measured values. In case measurements are expected to be done faster than 30 ms, characterization has be done for accuracy before implementation.

### 6.2.1 Testing with 30-ms Averaging

**Table 29. AC Input Voltage versus Measured Voltage Difference**

| INPUT PARAMETERS | | | A0 AND A3 | | A4 AND A5 | |
|---|---|---|---|---|---|---|
| APPLIED VOLTAGE @ 50 Hz | ALLOWED VOLTAGE LIMIT (±V) | GAIN | MEASURED VOLTAGE | DIFF | MEASURED VOLTAGE | DIFF |
| 15 | 1.45 | High | 14.764 | –0.236 | 15.042 | 0.042 |
| 23 | 1.69 | | 22.285 | –0.715 | 22.842 | –0.158 |
| 24 | 1.72 | | 23.399 | –0.601 | 23.677 | –0.323 |
| 48 | 2.44 | | 46.519 | –1.481 | 46.798 | –1.202 |
| 108 | 4.24 | Low | 107.705 | –0.295 | 107.705 | –0.295 |
| 109 | 4.27 | | 106.735 | –2.265 | 108.675 | –0.325 |
| 110 | 4.3 | | 107.705 | –2.295 | 109.646 | –0.354 |
| 111 | 4.33 | | 110.616 | –0.384 | 110.616 | –0.384 |
| 112 | 4.36 | | 110.616 | –1.384 | 111.586 | –0.414 |
| 228 | 7.84 | | 224.143 | –3.857 | 225.113 | –2.887 |
| 229 | 7.87 | | 224.143 | –4.857 | 225.113 | –3.887 |
| 230 | 7.9 | | 224.143 | –5.857 | 227.054 | –2.946 |
| 231 | 7.93 | | 225.113 | –5.887 | 228.024 | –2.976 |
| 232 | 7.96 | | 227.054 | –4.946 | 227.054 | –4.946 |
| 264 | 8.92 | | 256.163 | –7.837 | 258.104 | –5.896 |
| 276 | 9.28 | | 269.748 | –6.252 | 268.778 | –7.222 |

**Table 30. DC Input Voltage versus Measured Voltage Difference**

| INPUT PARAMETERS | | | A0 AND A3 | | A4 AND A5 | |
|---|---|---|---|---|---|---|
| APPLIED VOLTAGE | ALLOWED VOLTAGE LIMIT (±V) | GAIN | MEASURED VOLTAGE | DIFF | MEASURED VOLTAGE | DIFF |
| 10 | 1.3 | High | 9.876 | –0.124 | 9.876 | –0.124 |
| 15 | 1.45 | | 14.941 | –0.059 | 14.941 | –0.059 |
| 23 | 1.69 | | 22.791 | –0.209 | 22.791 | –0.209 |
| 24 | 1.72 | | 23.804 | –0.196 | 23.804 | –0.196 |
| 25 | 1.75 | | 24.564 | –0.436 | 24.817 | –0.183 |
| 48 | 2.44 | | 47.355 | –0.645 | 47.355 | –0.645 |
| 108 | 4.24 | Low | 106.735 | –1.265 | 107.617 | –0.383 |
| 109 | 4.27 | | 108.499 | –0.501 | 108.499 | –0.501 |
| 110 | 4.3 | | 109.381 | –0.619 | 109.381 | –0.619 |
| 111 | 4.33 | | 110.263 | –0.737 | 110.263 | –0.737 |
| 112 | 4.36 | | 111.145 | –0.855 | 111.145 | –0.855 |
| 228 | 7.84 | | 225.819 | –2.181 | 225.819 | –2.181 |
| 229 | 7.87 | | 226.701 | –2.299 | 226.701 | –2.299 |
| 230 | 7.9 | | 228.465 | –1.535 | 228.465 | –1.535 |
| 231 | 7.93 | | 229.347 | –1.653 | 229.347 | –1.653 |
| 232 | 7.96 | | 230.23 | –1.77 | 231.112 | –0.888 |
| 264 | 8.92 | | 260.221 | –3.779 | 260.221 | –3.779 |
| 320 | 10.6 | | 316.676 | –3.324 | 315.794 | –4.206 |

### 6.2.2 Error in % of the Measured Value

**Table 31. AC Input Voltage versus Measured Voltage Error (% of the Reading)**

| INPUT PARAMETERS | | A0 AND A3 | A4 AND A5 |
|---|---|---|---|
| APPLIED VOLTAGE @ 50 Hz | GAIN | ERROR (%) | ERROR (%) |
| 15 | High | –1.58 | 0.28 |
| 23 | | –3.11 | –0.69 |
| 24 | | –2.51 | –1.34 |
| 48 | | –3.09 | –2.51 |
| 108 | Low | –0.27 | –0.27 |
| 109 | | –2.08 | –0.30 |
| 110 | | –2.09 | –0.32 |
| 111 | | –0.35 | –0.35 |
| 112 | | –1.24 | –0.37 |
| 228 | | –1.69 | –1.27 |
| 229 | | –2.12 | –1.70 |
| 230 | | –2.55 | –1.28 |
| 231 | | –2.55 | –1.29 |
| 232 | | –2.13 | –2.13 |
| 264 | | –2.97 | –2.23 |
| 276 | | –2.27 | –2.62 |

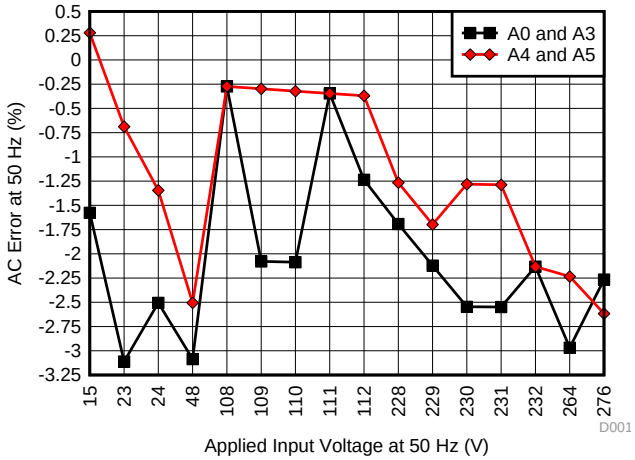



**Figure 12. Input Voltage versus Measured Voltage Error (% of the Reading)**

**Table 32. Input Voltage versus Measured Voltage Error (% of the Reading)**

| INPUT PARAMETERS | | A0 AND A3 | A4 AND A5 |
|---|---|---|---|
| APPLIED VOLTAGE DC INPUT | GAIN | ERROR (%) | ERROR (%) |
| 10 | High | –1.24 | –1.24 |
| 15 | | –0.39 | –0.39 |
| 23 | | –0.91 | –0.91 |
| 24 | | –0.82 | –0.82 |
| 25 | | –1.75 | –0.73 |
| 48 | | –1.34 | –1.34 |
| 108 | Low | –1.17 | –0.35 |
| 109 | | –0.46 | –0.46 |
| 110 | | –0.56 | –0.56 |
| 111 | | –0.66 | –0.66 |
| 112 | | –0.76 | –0.76 |
| 228 | | –0.96 | –0.96 |
| 229 | | –1.00 | –1.00 |
| 230 | | –0.67 | –0.67 |
| 231 | | –0.72 | –0.72 |
| 232 | | –0.76 | –0.38 |
| 264 | | –1.43 | –1.43 |
| 320 | | –1.04 | –1.31 |

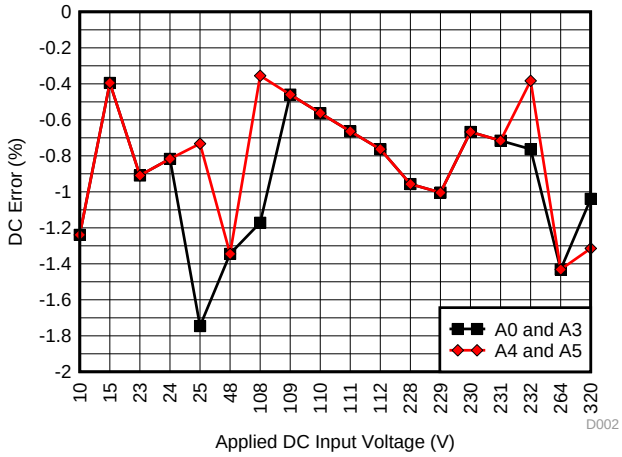



**Figure 13. DC Input Voltage versus Measured Voltage Error (% of the Reading)**

### 6.2.3 Frequency Variation

**Table 33. Voltage Measurement Error With Frequency**

| GAIN | INPUT VOLTAGE | MEASURED VOLTAGE @ 50 Hz | ERROR (%) | MEASURED VOLTAGE @ 60 Hz | ERROR (%) |
|---|---|---|---|---|---|
| High | 48 | 46.79758 | –2.50505 | 47.07613 | –1.92472 |
| Low | 240 | 231.9055 | –3.3727 | 231.9055 | –3.3727 |

**NOTE:** Variation between reading at 50 and 60 Hz was observed to be within 1%.

## *6.3 Wetting Current Measurement*

**Table 34. Wetting Current Measurement at Different Voltage Inputs (DC Only)**

| DC VOLTAGE INPUT SWITCHED ON FOR 50 ms | IMPEDANCE | INPUT 1 CURRENT (mA) | DUTY CYCLE | INPUT 2 CURRENT (mA) | DUTY CYCLE |
|---|---|---|---|---|---|
| 24 V | 2.5 K | ~9 | N/A | ~9 | N/A |
| 110 V | 2.5 K | ~44 | N/A | ~44 | N/A |
| 230 V | 2.5 K | ~44 | 50% | ~44 | 50% |

## 6.4 Drift Due to Temperature Variation of Signal Conditioning Circuit

The signal conditioning circuit consisting of the resistor divider, the 400-V input TVS, 5.1-V ADC input protection Zener, was tested for temperature variation. The leakage current for the 400-V TVS is < 1 µA at rated voltage for SMCJ package. The following results indicate that the effect of leakage current does not significantly influence the voltage input to ADC.

**Table 35. Voltage Drift With Temperature at 300-V Input**

| TEMPERATURE (°C) | MEASURED VOLTAGE (V) | DIFFERENCE (–V) |
|---|---|---|
| –10 | 298.92 | –1.082 |
| 12 | 299.01 | –0.986 |
| 40 | 299.01 | –0.986 |
| 70 | 299.11 | –0.890 |

**Table 36. Voltage Drift With Temperature at 110-V Input**

| TEMPERATURE (°C) | MEASURED VOLTAGE (V) | DIFFERENCE (–V) |
|---|---|---|
| –10 | 109.84 | –0.160 |
| 10 | 109.74 | –0.256 |
| 40 | 109.84 | –0.160 |
| 70 | 109.84 | –0.160 |

**Table 37. Voltage Drift With Temperature at 24-V Input**

| TEMPERATURE (°C) | MEASURED VOLTAGE (V) | DIFFERENCE (–V) |
|---|---|---|
| –10 | 23.98 | –0.018 |
| 10 | 23.89 | –0.113 |
| 40 | 23.98 | –0.018 |
| 70 | 23.98 | –0.018 |

## 6.5 Binary Input Testing With Digital Output (ISO7220ADR)

The binary module uses an $I^2C$ isolator to communicate the voltage reading to the host MCU. Alternatively, digital isolator can be used with the module to sense fixed voltages.

**Table 38. Results With Digital Isolator Mounted**

| DC INPUT $V_{IN}$ | APPLIED VOLTAGE | TOLERANCE | BINARY INPUT 1 OBSERVATION | BINARY INPUT 2 OBSERVATION |
|---|---|---|---|---|
| 24 | 22 | ±3% of $V_{IN}$ ±1 V | Low | Low |
| 24 | 26 | ±3% of $V_{IN}$ ±1 V | High | High |
| 110 | 106 | ±3% of $V_{IN}$ ±1 V | Low | Low |
| 110 | 114 | ±3% of $V_{IN}$ ±1 V | High | High |
| 240 | 230 | ±3% of $V_{IN}$ ±1 V | Low | Low |
| 240 | 250 | ±3% of $V_{IN}$ ±1 V | High | High |

## 6.6 IEC Pre-Compliance Testing

The following EMC tests have been performed.

**Table 39. EMC Tests**

| TEST | STANDARD |
|---|---|
| ESD | IEC61000-4-2 |
| Surge | IEC61000-4-5 |

**Table 40. Performance Criteria**

| CRITERIA | ACCEPTANCE (PASS) CRITERIA |
|---|---|
| A | The analog output module must continue to operate as intended. No loss of function or performance occur even during the test. |
| B | Temporary degradation of performance is accepted.<br>After the test, the analog output module must continue to operate as intended without manual intervention. |
| C | During the test, a loss of functions accepted, but no destruction of hardware or software.<br>After the test, the analog output module must continue to operate as intended automatically after manual restart or power off/power on. |

### 6.6.1 IEC61000-4-2 ESD Test

The IEC610004-2 ESD test simulates the electrostatic discharge of an operator directly onto an adjacent electronic component. Electrostatic charge usually develops in low relative humidity, and on low-conductivity carpets, or vinyl garments. To simulate a discharge event, an ESD generator applies ESD pulses to the equipment under test (EUT), which can happen through direct contact with the EUT (contact discharge), or through an air-gap (air-discharge). This was applied across signal inputs only. A series of 10 negative and positive pulses were applied directly on the binary inputs during the test (contact discharge). After the test, the binary input module was attached to TM4C123GXL LaunchPad to verify functionality. The test results show the EUT was able to withstand the required discharge . The EUT was not permanently damaged.

**Table 41. ESD Test Steps**

| TEST NO | TEST MODE | OBSERVATION |
|---|---|---|
| 1 | Contact 1 kV | Pass |
| 2 | Contact –1 kV | Pass |
| 3 | Contact 2 kV | Pass |
| 4 | Contact –2 kV | Pass |

**Table 42. ESD Test Observations**

| IMMUNITY TEST | STANDARD | PORT | TARGET VOLTAGE | RESULT |
|---|---|---|---|---|
| ESD | IEC 61000-4-2, contact | Binary input | ±2 kV | Meets Criteria B (After the test, the module continued to operate as intended.) |

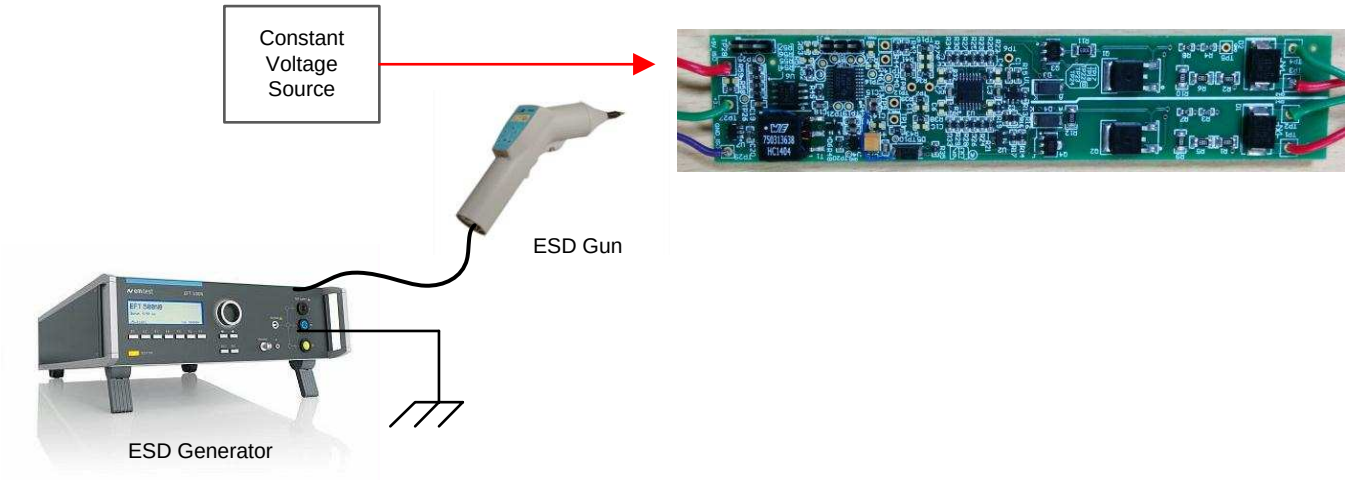



**Figure 14. ESD Setup for Binary Input Module**

### 6.6.2 IEC61000-4-5 Surge Test

The IEC61000-4-5 surge test simulates switching transients caused by lightning strikes or the switching of power systems including load changes and short circuits. The test requires five positive and five negative surge pulses with a time interval between successive pulses of one minute or less. The unshielded symmetrical data line setup as defined by the IEC61000-4-5 specification was used for this test. The test generator was configured for 1.2/50-µs surges and diode clamps were used for line-to-ground coupling. A series of five negative and positive pulses, with 10 seconds spacing between each pulse, were applied during the test. After the test, the binary input module was attached to TM4C123GXL LaunchPad to verify functionality. The test results show the EUT was able to withstand up to ±500-V bursts. The EUT was able to perform normally after each test. Because functionality could not be verified during the test, the result was noted as passing with Class B.

**Table 43. Surge Test Steps**

| TEST NO | TEST MODE | OBSERVATION |
|---|---|---|
| 1 | 0.5 kV | Pass |
| 2 | –0.5 kV | Pass |
| 3 | 1 kV | Pass |
| 4 | –1 kV | Pass |
| 5 | 2 kV | Pass |
| 6 | –2 kV | Pass |

**Table 44. Surge Test Observations**

| IMMUNITY TEST | STANDARD | PORT | TARGET VOLTAGE | RESULT |
|---|---|---|---|---|
| Surge, DM | IEC 61000-4-5:<br>1.2 / 20-µs voltage waveform<br>8 / 20-µs current waveform<br>42-Ω impedance | Binary input | ± 1 kV | Meets Criteria B<br>(After the test, the module continued to operate as intended.) |

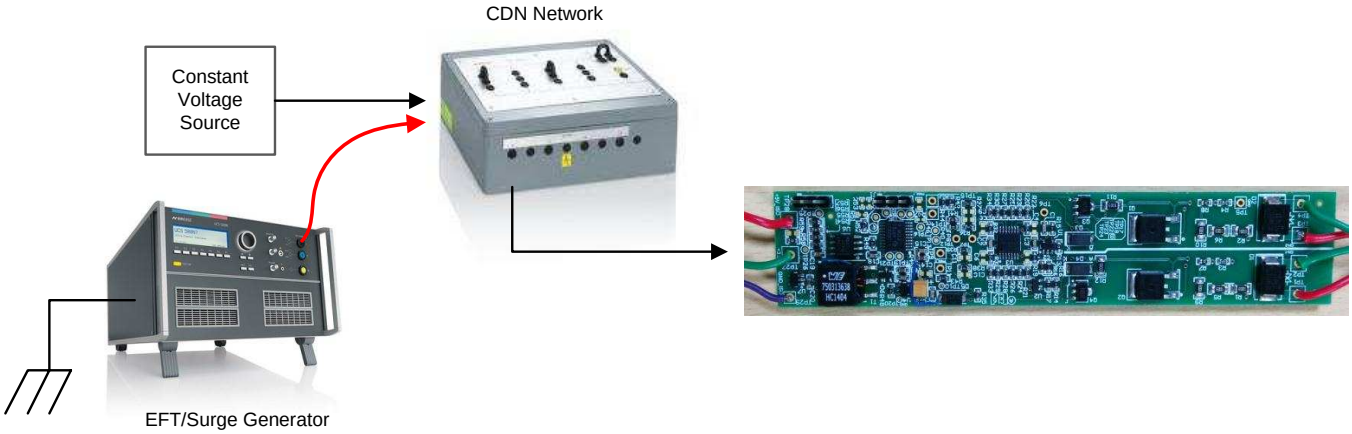



**Figure 15. Surge Setup for Binary Input Module**

## 6.7 Test Results Summary

**Table 45. Test Results Summary for AC/DC Binary Input Module**

| TEST | OBSERVATION |
|---|---|
| Power supply | OK |
| MCU programming | OK |
| Measurement of AC/DC voltage input | OK |
| AC/DC input voltage measurement accuracy | < ±3% of measured value ±1 V (programmable step size) |
| EMC pre-compliance tests | OK |

# 7 Design Files

## 7.1 Schematics

To download the schematics, see the design files at TIDA-00490.

## 7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00490.

**NOTE:** The BOM configuration is for a DC input type. If the board is required to be assembled as AC input, do not populate Q1, Q2, Q3, Q4, D3, D4, D7, D8, C23, or C22.

## 7.3 Layer Plots

To download the layer plots, see the design files at TIDA-00490.

## 7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00490.

## 7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00490.

## 8 Terminology

**External clearance—** The shortest distance through air between conductive input and output leads; measured in mm.

**Comparative tracking index (CTI)—** Outer molding material characterization in the presence of aqueous contaminants. The higher the CTI value, the more resistant the material is to electrical arc tracking. CTI is often used with creepage by safety agencies to determine working voltage.

**External creepage—** The shortest distance along the outside surface between input and output leads; measured in mm.

**Dielectric insulation voltage withstand rating—** The ability to withstand without breakdown a 60-second application of a defined dielectric insulation voltage between input and output leads.

**Installation class—**

1. Equipment in closed systems (for example, telecom) protected against overvoltage with devices such as diverters, filters, capacitors, and so on.
2. Energy consuming equipment (for example, appliances) supplied through a fixed installation.
3. Primarily equipment in fixed installations (for example, fixed industrial equipment).
4. Primary supply level for industrial factories.

**Insulation—**

- Operational — Required for correct equipment operation but not as a protection against electric shock.
- Basic — Protects against electric shock.
- Supplementary — Independently applied to basic insulation to protect against shock in the event of its failure.
- Double — Composed of both basic and supplementary.
- Reinforced — A single insulation system composed of several layers (for example, single and supplementary).

**Material group (see Comparative Tracking Index) —**

1. 600 < CTI
2. 400 < CTI < 600
3. 175 < CTI < 400
4. 100 < CTI <175

**Partial discharge—** Electric discharge that partially bridges the insulation between two electrodes. Agilent supports partial discharge measurements per VDE0884, a technique developed to evaluate the integrity of insulating materials

**Pollution degree—**

1. Nonconductive pollution only.
2. Only occasional, temporary conductivity due to condensation.
3. Frequent conductive pollution due to condensation.
4. Persistent conductive pollution due to dust, rain, or snow.

**Rated mains voltage—** Primary power voltage declared by manufacturer. Used to categorize opto-coupler maximum allowable working voltage.

**Common-mode transient rejection (CMTR)—** CMTR describes the maximum tolerable rate-of-rise (or fall) of a common-mode voltage (given in volts per microsecond). The specification for CMTR also includes the amplitude of the common-mode voltage (VCM) that can be tolerated. Common-mode interference that exceeds the maximum specification might result in abnormal voltage transitions or excessive noise on the output signal.

## 9 References

1. Texas Instruments, *MSP430™ Programming Via the JTAG Interface*, User's Guide (SLAU320).
2. Texas Instruments, *The ISO72x Family of High-Speed Digital Isolators*, Application Report (SLLA198).

## 10 About the Author

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# Revision History

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