TI Designs: TIDA-00527
RS-485 Power Over Bus

TI Designs

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Design Resources

SN65HVD75	Product Folder
SN65HVD82	Product Folder
SLLA336	Application Report

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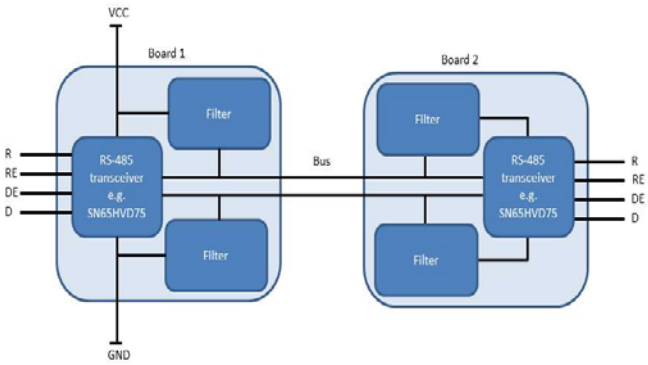
Design Features

- Power over Bus evaluation
- Quick and easy tests of different bus power filters
- Configurable modules for master or slave application
- DC blocking bus capacitors
- Onboard receiver / transmitter enable / disable pull-up / pull-down resistors

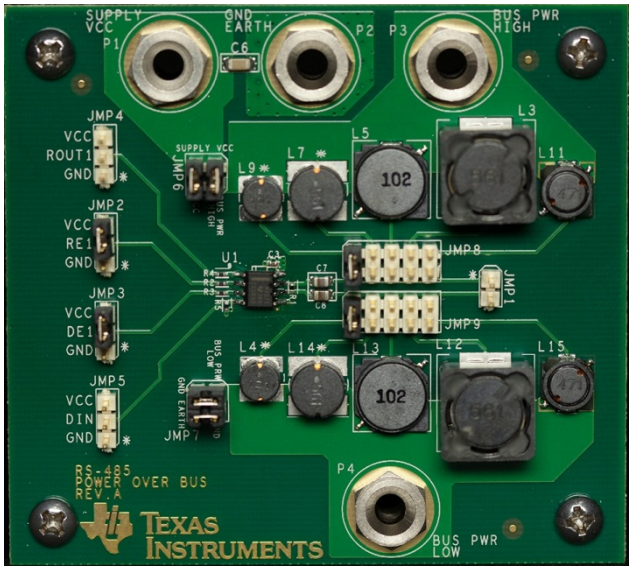
Featured Applications

- Elevators
- Industrial robots

Block Diagram



Board Image



1 Design Overview

Many industrial communications networks require the distribution of both power and data lines between master and remote (slave) nodes. As the distance between nodes increases, the cost of cabling tends to increase as well. Combining power and data communication onto a common pair of wires reduces the overall number of wires connecting each node, and can provide significant system cost savings. It also can help when installing new systems into applications with an existing cable infrastructure that were designed for data-only or power-only distribution.

This reference design uses a bias-tee structure in order to combine power and data. High-frequency data (in this case from an RS-485 transceiver) is connected to the distribution line through a series capacitor, which allows data to pass through while protecting the transceiver from large DC potentials on the bus. A power supply is connected to the line through an inductor, which allows for DC power to be distributed through the line and filtered out on the other end.

Note that this technique requires that the data signals being transmitted do not have content at DC or at very low frequencies. The series capacitance will form a single-pole high-pass filter with the shunt termination resistances at each end of the bus, and the lowest signal frequency should be higher than the filter cut-off. Manchester encoding is a common way to eliminate the DC portions of a data signal, although other encoding schemes (like 8b/10b) could be used as well.

2 Schematic

The schematic for the Power-over-Bus reference design is shown below.

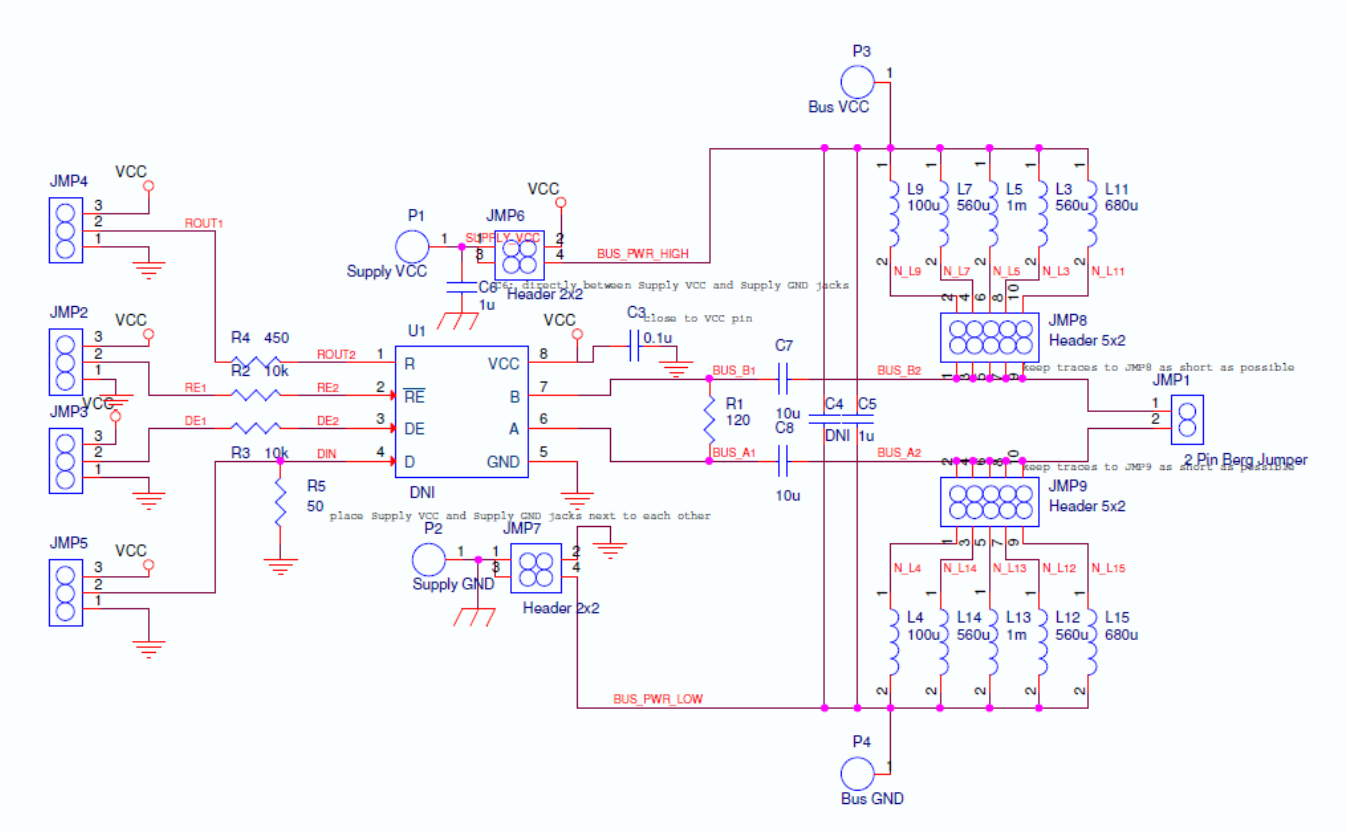


Figure 1. Power-over-Bus schematic

The jumpers at the left side of the schematic allow for connectivity to the host-side interface of the transceiver (i.e., the R, /RE, DE, and D pins). At the far right side, JMP1 is used to connect to the bus. Power can be inserted into the differential bus through the P3 and P4 banana jacks. Two 5x2 headers allow for testing with various different inductances in the bias-T. The bias-T capacitor is fixed at 10 uF, although this can be modified by the end user in order to test at different operating rates or with different encoding/modulation schemes. It is possible to independently power the transceiver using the P1 and P2 banana jacks.

Note that the same schematic can be used as either a master node (sending power) or a slave node (receiving power).

3 Test Waveforms

The following waveforms were recorded using the SN65HVD78 3.3-V RS-485 transceiver and a distributed DC power supply of 3.3 V.

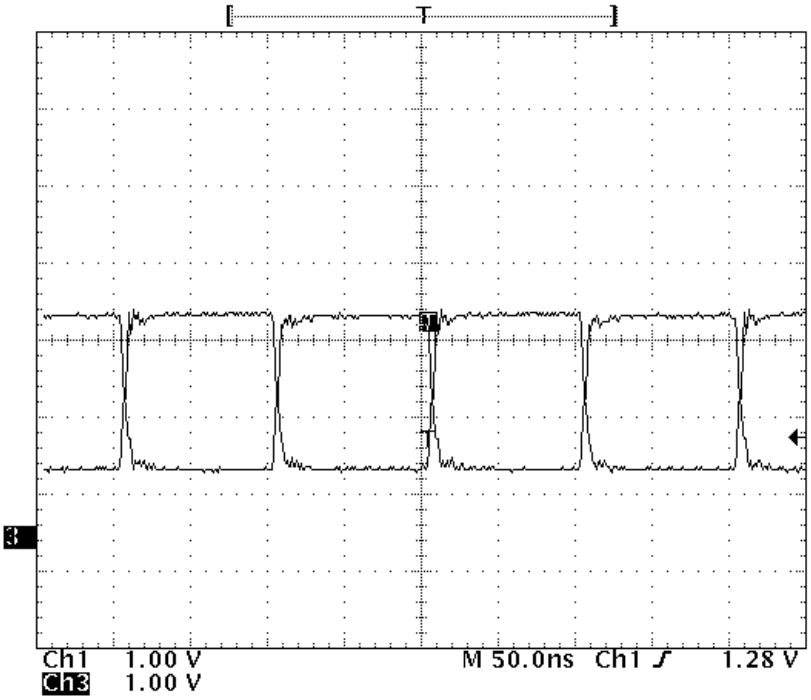


Figure 2. Differential signal at RS-485 transceiver output

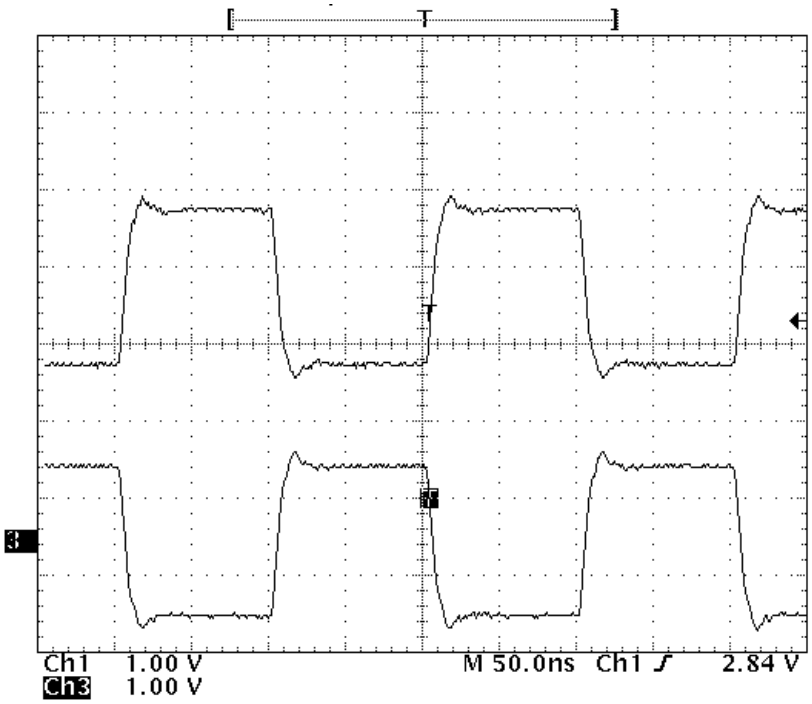


Figure 3. Differential signal on bus (with 3.3-V DC supply)

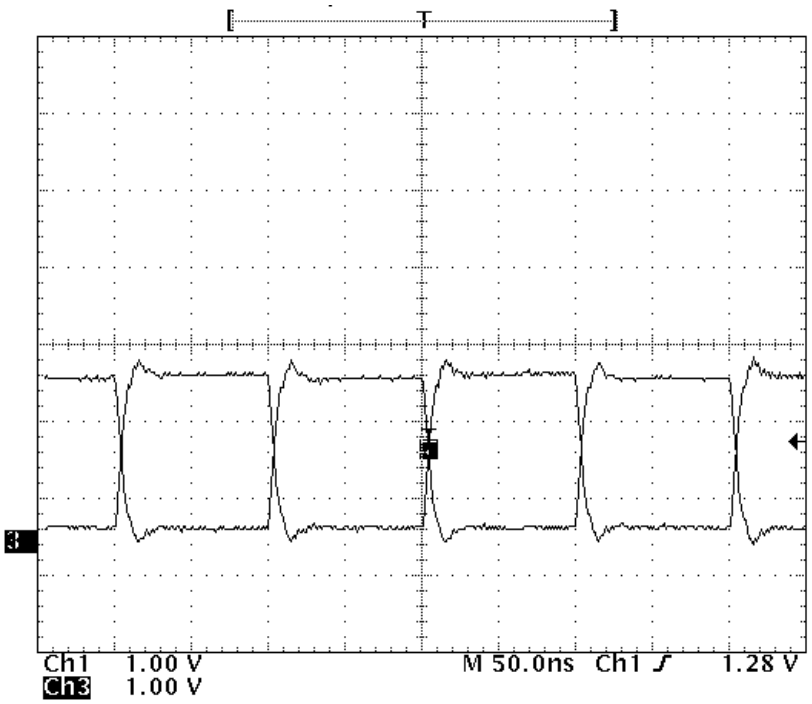


Figure 4. Differential signal at remote receiver input (after bias-tee)

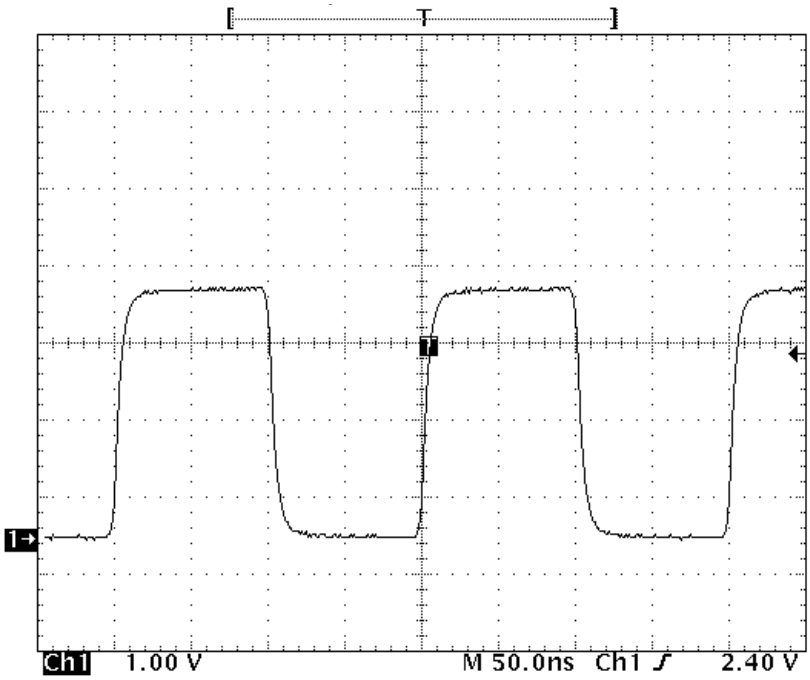


Figure 5. Remote receiver output signal

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