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Dual Sensor Measurement Using Single Current-Loop With FSK Modulation

TEXAS INSTRUMENTS

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Design Resources

|	
TIDA-00483	Tool Folder Containing Design Files
DAC161S997	Product Folder
OPT3001	Product Folder
HDC1000	Product Folder
TPS7A4901	Product Folder
LMV342	Product Folder
MSP430FR5969	Product Folder

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Design Features

- Transmits Two Variable Parameters Simultaneously
- Normal 4- to 20-mA Operation
- Expandable to Multiple Parameters Through FSK-Modulated Digital Data Stream
- Reduce Cabling and Installation Costs
- Dual Op-Amp Fourth-Order Butterworth Filter for FSK Generation
- Ultralow-Power (ULP) TI MSP430™ MCU Allows Higher Current Sensors in Loop

Featured Applications

- Heating, Ventilating, and Air Conditioning (HVAC)
- Building Automation
- Factory Automation
- Field Sensors
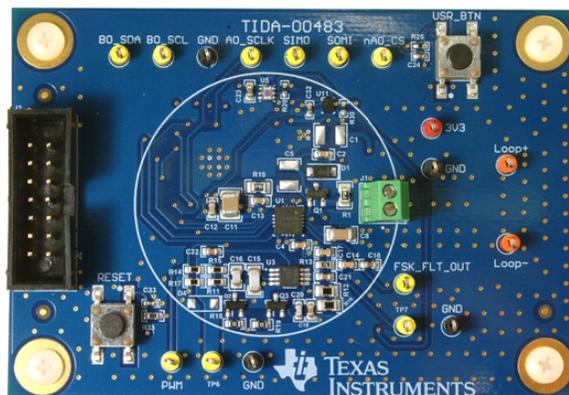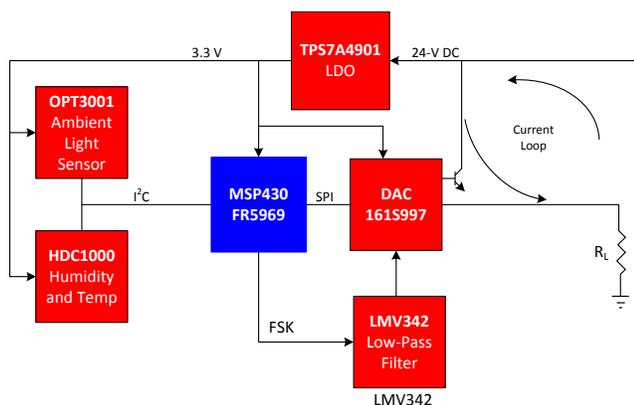
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1 Key System Specifications

Table 1. Key Specifications Table

PARAMETER	SPECIFICATION	DETAILS
Sensor type	Ambient light sensor, humidity sensor, and temperature sensor	Section 3
Input voltage	10- to 35-V DC; 24-V DC nominal	Section 3
Output	4 mA to 20 mA and FSK modulation	Section 4.5
Output resolution	16 bits,0.85 μA	Section 7.3
Maximum measured error	Total combined error: ±0.3°C	Section 7.7
FSK modulation	1200 Hz (Logic 1), 2200 Hz (Logic 0)	Section 4.5
Operating temperature	−40°C to 85°C	Section 3
Working environment	Indoor building automation	—
Debug communication port	Universal asynchronous receiver and transmitter (UART) through a USB to UART dongle	—

2   System Description

This TIDA-00483 reference design brings together several devices to create a subsystem capable of measuring the surrounding environment and communicating the temperature, humidity, and ambient light over a 4- to 20-mA current loop. The small foot print of the design contains all sensors, filters, and control circuitry to calculate and communicate the sensor data. The reference design is intended for process measurement applications in factory automation, field transmitters, and building automation. The sensors, MCU, and communication modules all run off power from the current loop, which requires less than 3.5 mA to achieve. This power configuration allows the rest of the current to be dynamically adjustable for the 4- to 20-mA loop communication protocol standard.

2.1   DAC161S997

This DAC161S997 digital-to-analog converter (DAC) from Texas Instruments (TI) is designed to easily control the current in an industry standard 4- to 20-mA current loop. The DAC161S997 is a very low power DAC that allows higher current sensors and devices onto the current loop. The DAC also has the capability to simultaneously interface with an FSK modulator to allow the injection of digital data onto the current loop. In this reference design, the DAC implements the current loop control and injects a digital bit stream onto the loop, allowing two or more sensor parameters to be transmitted through one current loop.

2.2   Ambient Light Sensor

An ambient light sensor allows the system to measure and react to changes in the lighting environment. The OPT3001 is an ambient light sensor from Texas Instruments. The sensor measures the intensity of visible light. The light data that the OPT3001 device collects is transmitted on the 4- to 20-mA current loop. The current in the loop is proportional to the light intensity measured by the light sensor.

2.3   Humidity and Temperature Sensor

An integrated humidity and temperature sensor decreases the complexity of system design and overall footprint of the finished product. The user can collect temperature and humidity data with one read command. The use of a single device saves power and decreases the communication time and cycles required to collect necessary information.

The HDC1000 is a dual sensor device that contains a temperature and humidity sensor in a compact package. The temperature and humidity data can be transmitted on the 4- to 20-mA current loop through FSK modulation. Digital bit stream FSK allows the reference design to transmit multiple sensor parameters alongside the standard 4- to 20-mA protocol.

2.4   TPS7A4901

Texas Instruments offers a wide range of linear regulators. The TPS7A4901 is a very high-voltage tolerant regulator with a single output. The regulator is set to regulate the 3.3-V rail in this reference design. The 3.3-V rail powers the sensors and the MSP430.

2.5   Operational Amplifier

Many amplifiers are available for the designer to choose. A relatively quick amplifier with low current consumption is key to an efficient subsystem. The LMV342 dual, rail-to-rail output CMOS operational amplifier has been chosen because it is designed for low-voltage applications and has low-voltage noise with a small SOT-23 package.

2.6   Microcontroller Selection

This reference design requires a low power MCU to handle the computation and communication aspects of the design. Because the total current consumption is important for 4- to 20-mA designs, a low power MCU is a very critical component to this design. The total current consumption of the sensor and control circuitry must be below 3.5 mA to be within the 4- to 20-mA IEEE standard operating specifications. A low-power MCU allows more current to be available for sensors and filtering circuitry. The TI MSP430FR5969 device is selected for this design because of the ultralow-power (ULP) operating current of this particular MCU.
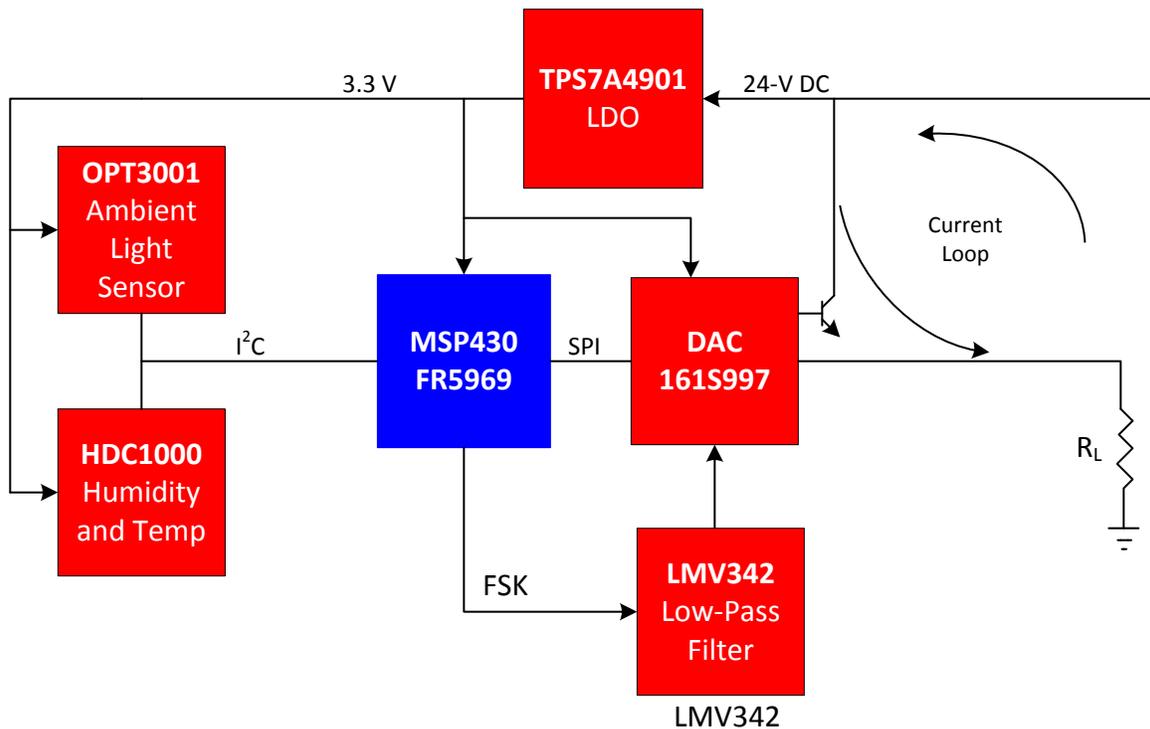
3 Block Diagram

Figure 1. TIDA-00483 Block Diagram

3.1 Highlighted Products

The dual sensor measurement reference design features the following devices:

- DAC161S997: 16-bit precision DAC for 4- to 20-mA loops with serial peripheral interface (SPI)
- OPT3001: Single-chip lux meter, which measures light intensity as is visible by the human eye with infrared (IR) rejection
- HDC1000: Digital humidity sensor with integrated temperature sensor
- TPS7A4901: positive, high-voltage ultralow-noise linear regulator
- LMV342: Low-power, dual, rail-to-rail output CMOS operational amplifier
- MSP430FR5969: 16-MHz ULP MCU featuring 64-KB FRAM, 2-KB SRAM, and 40 input and outputs (I/O)

3.1.1 DAC161S997

The DAC161S997 is a very low power 16-bit ΣΔ digital-to-analog converter (DAC) for transmitting an analog output current over an industry standard 4- to 20-mA current loop. The DAC161S997 has a simple four-wire serial peripheral interface (SPI) for data transfer and configuration of the DAC functions. To reduce power and component count in compact loop-powered applications, the DAC161S997 contains an internal ultralow power voltage reference and an internal oscillator. The low power consumption of the DAC161S997 device results in additional current being available for the remaining portion of the system. The loop drive of the DAC161S997 interfaces to a Highway Addressable Remote Transducer (HART) modulator, allowing injection of FSK-modulated digital data into the 4- to 20-mA current loop. This combination of specifications and features makes the DAC161S997 device ideal for two- and four-wire industrial transmitters. The DAC161S997 is available in a 16-pin, 4-mm × 4-mm WQFN package and is specified over the extended industrial temperature range of –40°C to +105°C. Figure 2 shows the DAC161S997 block diagram.

The DAC161S997 device has the following features:

- 16-bit resolution
- Very-low supply current of 100 µA
- 5 ppmFS/°C gain error
- Pin-programmable power-up condition
- Loop-error detection and reporting
- Programmable output-current error levels
- Simple HART modulator interfacing
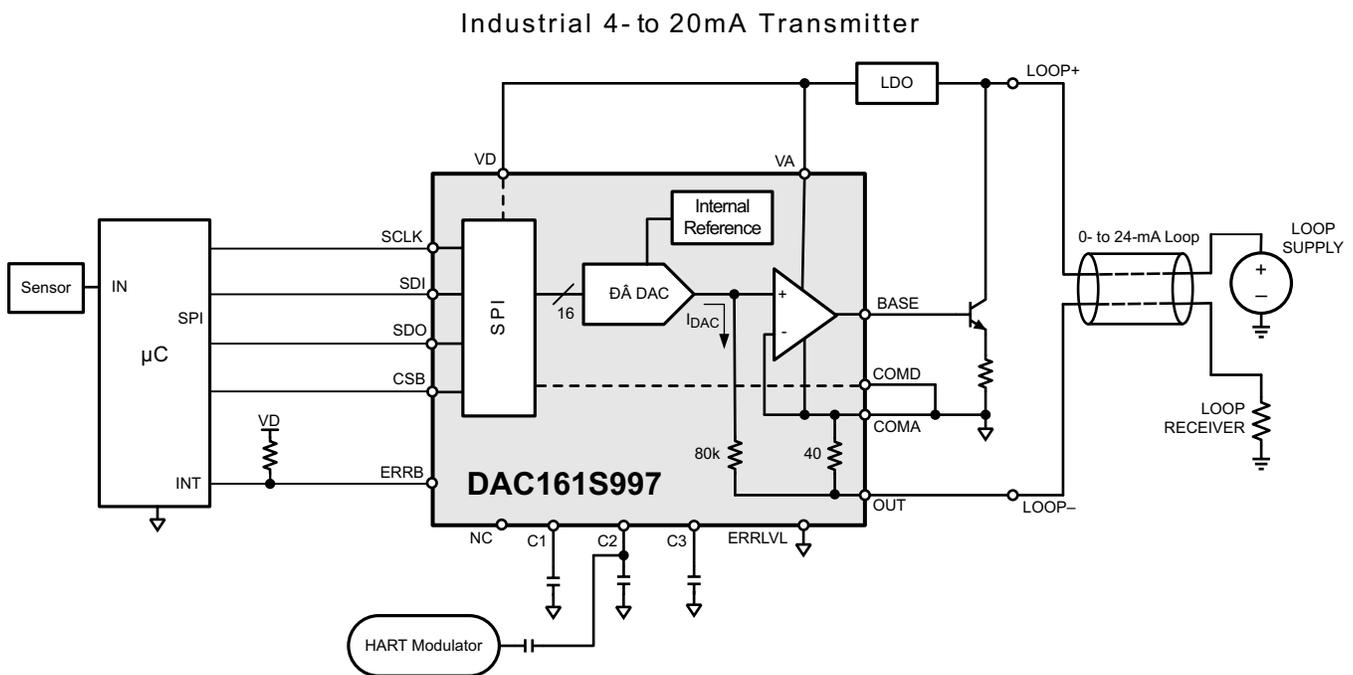- Highly integrated feature set in a small-footprint WQFN-16 (4 × 4 mm, 0.5-mm pitch)

Industrial 4- to 20mA Transmitter

Figure 2. DAC161S997 Block Diagram

3.1.2 OPT3001

The OPT3001 device is a sensor that measures the intensity of light. The spectral response of the sensor is tightly matched to the photopic response of the human eye and includes significant infrared (IR) rejection. The OPT3001 is a single-chip lux meter that measures the intensity of light as seen by the human eye. The precision spectral response and strong IR rejection of the device enables the OPT3001 to accurately measure the intensity of light, regardless of its source. The strong IR rejection also aids in maintaining a high accuracy when an industrial design requires mounting the sensor under dark glass for aesthetics. The OPT3001 device is designed for systems that create light-based experiences for humans and an ideal, preferred replacement for photodiodes, photoresistors, or other ambient light sensors with less human eye matching and IR rejection. The small form factor (2.0 mm × 2.0 mm × 0.65 mm) allows the device to fit almost anywhere. Figure 3 shows the OPT3001 block diagram.
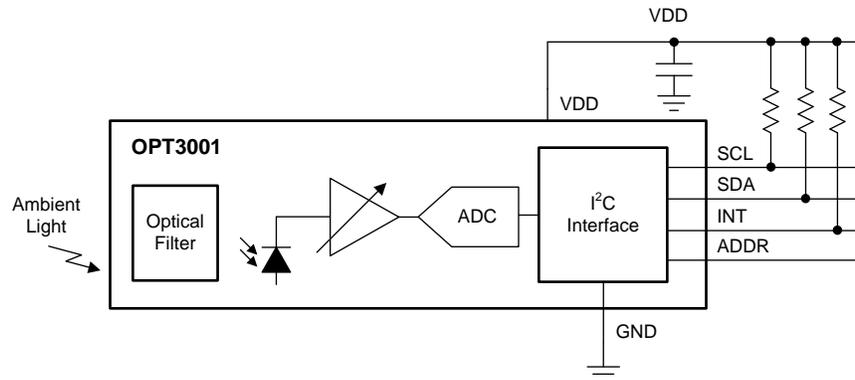

Figure 3. OPT3001 Block Diagram

3.1.3 HDC1000

The HDC1000 is a digital humidity sensor with an integrated temperature sensor that provides excellent measurement accuracy at very low power. The device measures humidity based on a novel capacitive sensor. The humidity and temperature sensors are factory calibrated. The innovative Wafer Level Chip Scale Package (WLCSP) simplifies board design with the use of an ultra-compact package. The sensor element of the HDC1000 is placed on the bottom part of the device, which makes the HDC1000 more robust against dirt, dust, and other environmental contaminants. The HDC1000 sensor is functional within the full –40°C to 125°C temperature range. Figure 4 shows the HDC1000 block diagram.
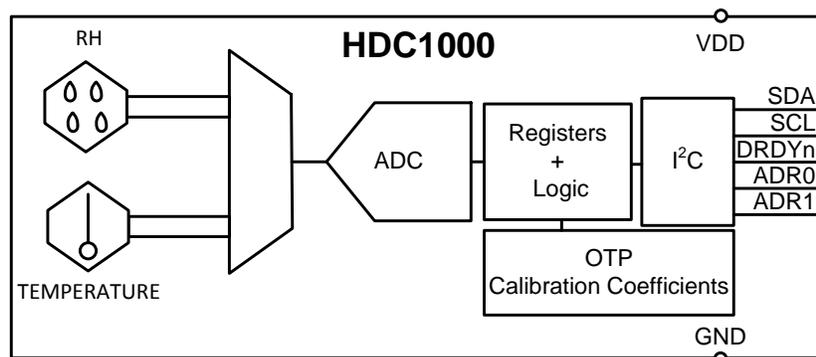

Figure 4. HDC1000 Block Diagram

3.1.4   TPS7A4901

The TPS7A49 series of devices are positive, high-voltage (36 V), ultralow-noise (15.4 μV_{RMS}, 72-dB PSRR) linear regulators that can source a 150-mA load.

These linear regulators include a CMOS logic-level compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other available features include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A49 family is designed using bipolar technology and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes the device an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A49 family of linear regulators is suitable for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications. Figure 5 shows the TPS7A4901 block diagram.
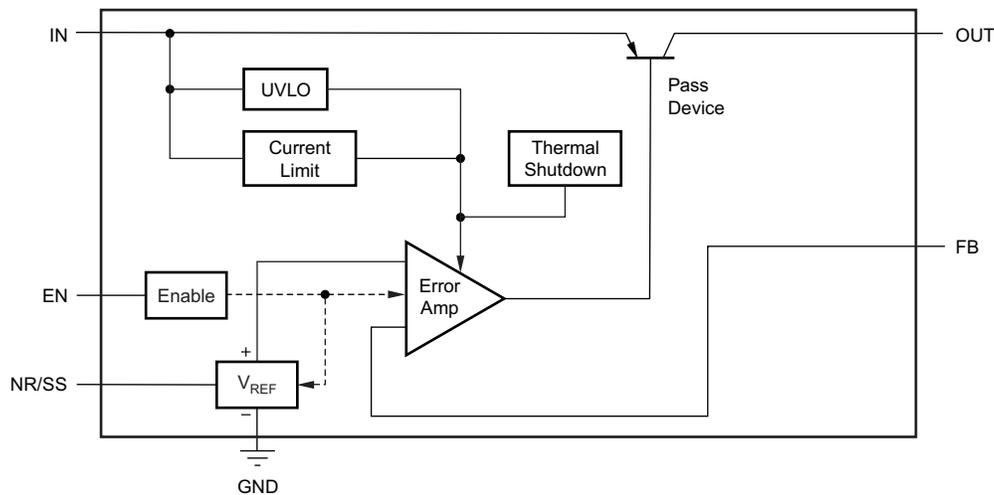
Figure 5. TPS7A4901 Block Diagram

3.1.5   LMV342

The LMV342 device is a dual-CMOS operational amplifier with low voltage, low power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultralow input bias current of 1 pA (typically) and an offset voltage of 0.25 mV (typically). The single-supply amplifier is designed specifically for low-voltage (2.7 V to 5 V) operation, with a wide common-mode input voltage range that typically extends from –0.2 V to 0.8 V from the positive supply rail. In shutdown mode, the supply current is reduced to 33 nA (typically). Additional features of this device family are a 20-nV/$\sqrt{Hz}$ voltage noise at 10 KHz, 1-MHz unity-gain bandwidth, 1-V/µs slew rate, and 100-µA current consumption per channel.

The LMV342 dual device is offered in the standard SOIC and MSOP packages. An extended industrial temperature range from –40°C to 125°C makes this device suitable in a wide variety of commercial and industrial environments. Figure 6 shows the LMV342 block diagram.

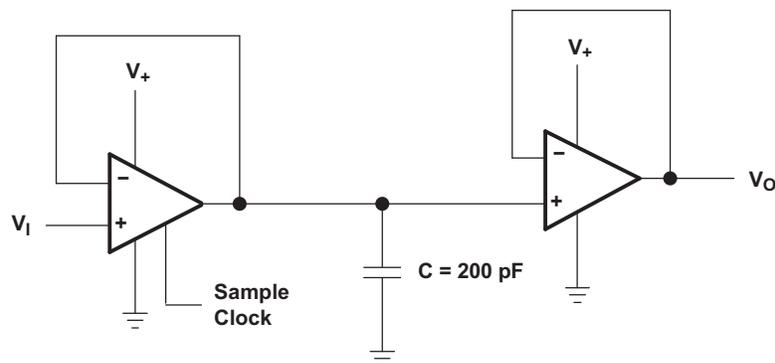**Figure 6. LMV342 Block Diagram**

3.1.6   MSP430FR5969

The MSP430 ULP FRAM platform combines uniquely embedded FRAM and a holistic ULP system architecture that allows innovators to increase performance at lowered energy budgets. FRAM technology combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash with much lower power.

The MSP430 ULP FRAM portfolio consists of a diverse set of devices featuring FRAM, the ULP 16-bit MSP430 central processing unit (CPU), and intelligent peripherals targeted for various applications. The ULP architecture showcases seven low-power modes that are optimized to achieve extended battery life in energy-challenged applications. Figure 7 shows the MSP430FR5969 block diagram.
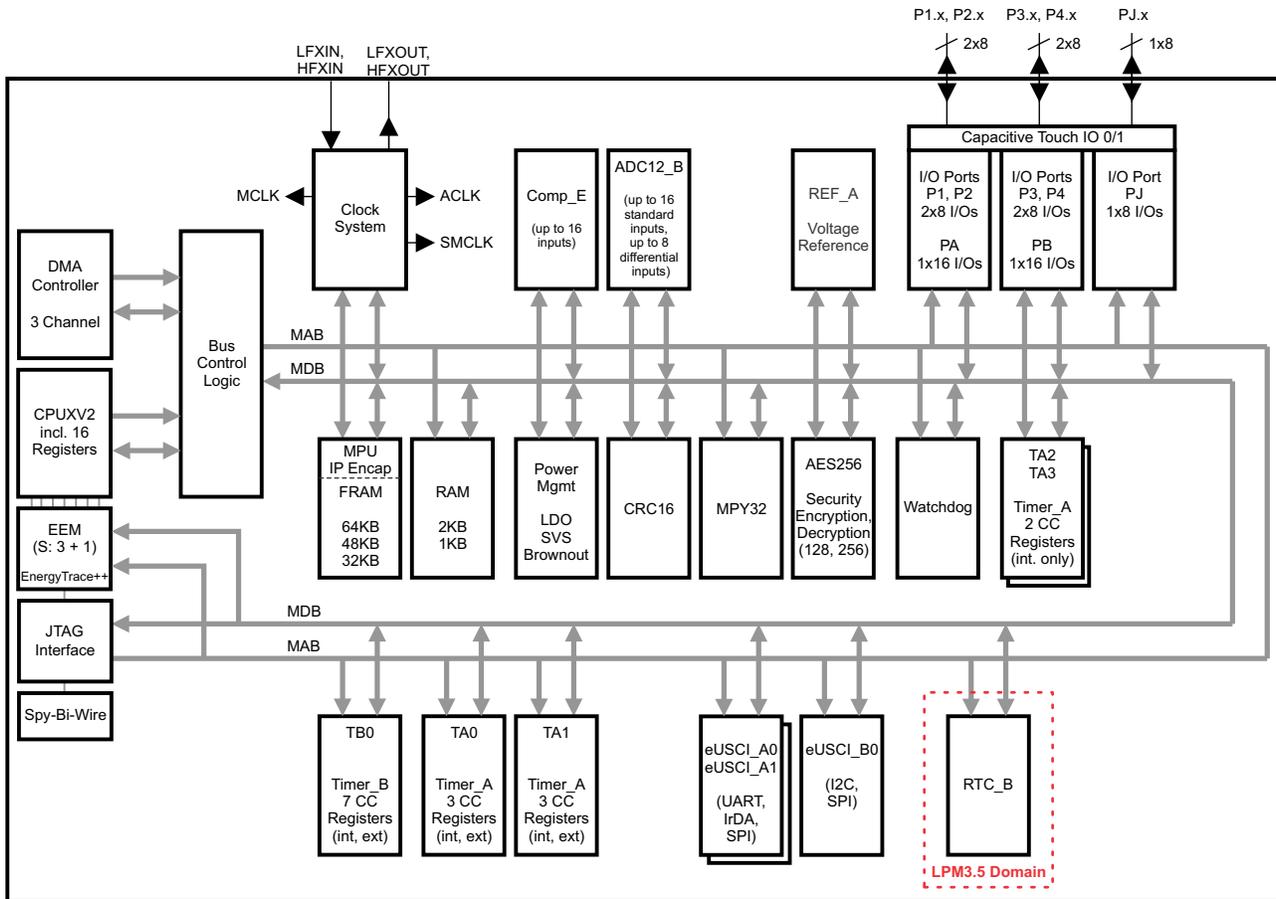

Figure 7. MSP430FR5969 Block Diagram

4 System Design Theory

4.1 Current Loop Basic Theory—4 mA to 20 mA

The basic current loop consists of three main parts: a power supply, transmitter, and receiver. All of the devices and sensors in the TIDA-00483 reference design are driven by a DC power supply; this design utilizes the most common supply voltage of 24-V DC. The supply voltage must be higher than the voltage required for the transmitter, IR drop in the receiver, and IR drop in the transmission line.

The 4- to 20-mA current loop communication protocol is very robust because the current in the wire carries the information, not the voltage. Voltage is more prone to noise and can be accidentally altered by other outside sources, which causes the readings to fluctuate. The current in the loop is the same for all devices in the loop and is controlled the transmitter. In this design, the transmitter is the DAC161S997. The DAC transmitter just regulates the amount of current in the loop and does not actually generate or source the current.

The receiver is the device at the end of the loop that receives the signal. A precision sense resistor is often used as part of the receiver, because voltage is easier to measure than current. Use a simple analog-to-digital converter (ADC) along with the sense resistor to calculate loop current. One benefit of current loops is that multiple sense resistors can be used in series at different positions in the loop with each experiencing the same current. The wire that makes up the current loop can be thousands of feet long and can add extra resistance to the loop as well. Remember, if the transmission line is long, or if extra resistance is added to the loop, the user may have to increase the supply voltage. One downfall of current loops is that only one parameter can be transmitted on the current loop because current in the loop is directly related to the percentage of the parameter's range. Equation 1 shows the relationship between current and sensor reading.

$$\text{Linear mA out} = 4 + \left(16 \times \left(\frac{\text{Reading} - \text{Min Reading}}{\text{Max reading} - \text{Min Reading}} \right) \right)$$

(1)

4.2 DAC Theory of Operation

The DAC converts the 16-bit input code in the DACCODE registers to an equivalent current output. The $\Sigma\Delta$ DAC output is a current pulse, which is then filtered by a third-order RC low-pass filter and boosted to produce the loop current (I_{LOOP}) at the device OUT pin.

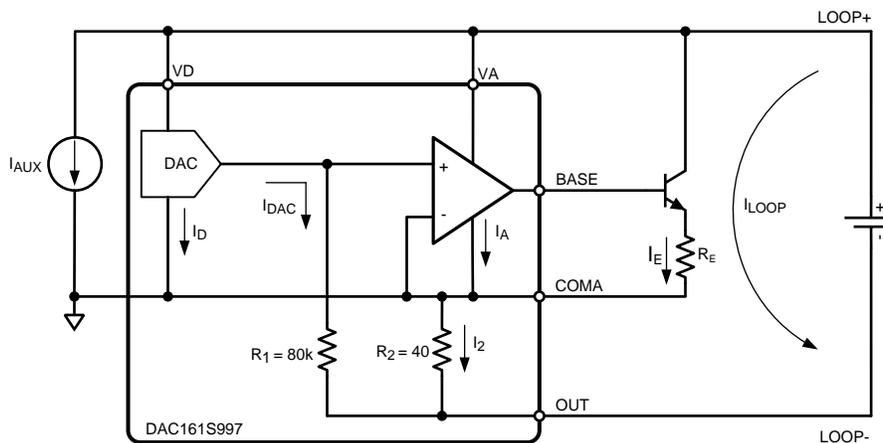Figure 8 shows the principle of operation of the DAC161S997 in the loop-powered transmitter.

Figure 8. Loop-Powered Transmitter

In Figure 8, I_D and I_A represent the supply (quiescent) currents of the internal digital and analog blocks. I_{AUX} represents supply (quiescent) current of companion devices present in the system, such as the voltage regulator and the digital interface The control loop formed by the amplifier and the bipolar transistor force the voltage across R_1 and R_2 to be equal (under normal conditions). So, the value of I_{LOOP} depends only on the I_{DAC} through the following relationship that Equation 2 and Figure 9 show:

$$I_{LOOP} = (1 + R_1 / R_2) \times I_{DAC}$$

where

- $I_{DAC} = f \times (DACCODE)$ (2)
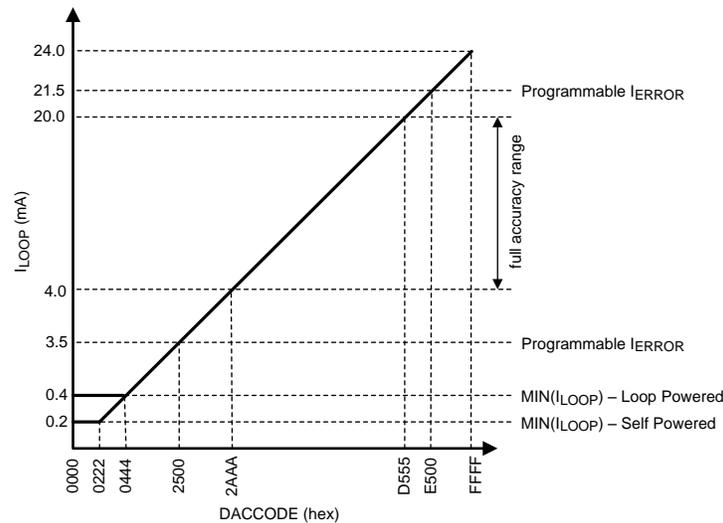


Figure 9. DAC-DC Transfer Function

The DAC161S997 cannot directly interface to the typical 4- to 20-mA loop because of the high supply voltage. The loop interface must provide the means of stepping down the LOOP supply to approximately 3.3 V. The second component of the loop interface is the external NPN transistor (BJT). This device is part of the control circuit that regulates the transmitter's output current (I_{LOOP}). Because the BJT operates over the wide current range (spanning at least 4 mA to 200 mA), degenerating the emitter to stabilize the transconductance (gm) of the transistor is not necessary. A degeneration resistor of 20 Ω is suggested in typical applications.

4.3 DAC Offset Error

The DAC161S997 may require some calibration depending on the system upon which it is installed to achieve the correct current loop output. A slightly improved output curve was attained upon the completion of the characterization that Section 7.2 discusses. A small correction factor in the software corrected the amount of error that was noticeable in the DAC output stage of the design. Refer to the software for more information on how to emulate the DAC offset configurations. The factor applied to the current output in the software is 0.99954.

4.4 Gain Error

The gain error that Figure 10 shows is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For a DAC, the gain error is the step value when the digital input is in full scale. This error represents a difference in the slope of the actual and ideal transfer functions, and as such, corresponds to the same percentage error in each step. This error can usually be adjusted to zero by trimming, as well.
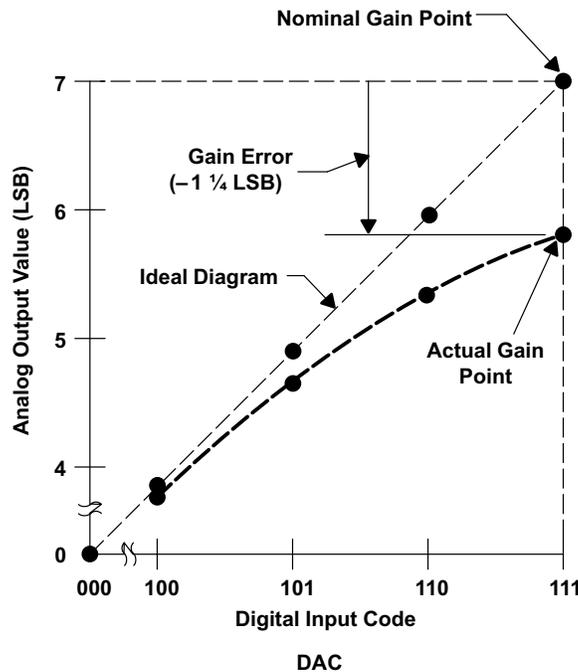
Gain Error of a Linear 3-Bit Natural Binary Code Converter
(Specified at Step 111), After Correction of the Offset Error

Figure 10. DAC Gain Error

Customers can perform the DAC gain calibration measurement on a given system by removing the *#DAC_test*, recompiling the firmware, and then using SW 1 (see board Image in hardware overview), which outputs 4 mA to 20 mA in 2-mA steps for each button push. Using these values, the user can locate a new DAC error correction value. For a higher precision gain correction, the user may implement a look-up table.

4.5   *Frequency Shift Keying (FSK) Modulation*

To transmit more than one parameter, a form of frequency-shift keying is employed on top of the current loop on the same wire. The DAC161S997 can add Highway Addressable Remote Transducer (HART) protocol modulation into the current loop. However, to create a simpler software solution, a custom communications interface has been developed to showcase the abilities and simple nature of the design. The modulation is very similar to HART, but this communications interface does not use a modem to communicate. The MSP430 MCU generates a square-wave output that resembles HART conventions. The modulation then passes through a filter network to create sine waves that are passed to the modulator input on the DAC. A "1" is represented by one period of a 1200-Hz sine wave and a "0" is represented with two periods of a 2200-Hz sine wave. The following Section 4.6 discusses the modulation filter in more detail. Section 5.2 discusses the MSP430 software that handles the modulation.

Figure 11 shows the path of the sensor data in the reference design. The HDC1000 temperature data transmits through the standard 4- to 20-mA standard. The light sensor data and humidity data can be transmitted by following the modulation scheme that this section describes. Section 5 includes a more in-depth discussion about the communication and parameter handling.
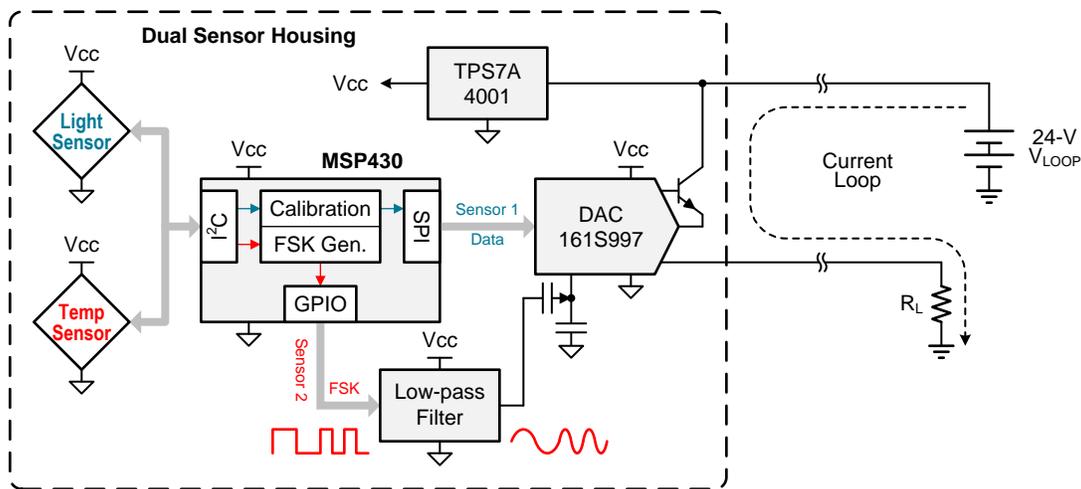

Figure 11. TIDA-00483 Functional Block Diagram

4.6   *FSK Modulation Filter*

The purpose of the FSK modulation filter is to convert the modulated digital data stream from the MSP430 device into a scaled sinusoidal version of the modulated digital-input signal, which can be used as a HART-compatible input to the DAC. Converting the modulated digital data stream into a modulated sinusoidal signal poses a couple of challenges. The first challenge is creating a constant amplitude output for the two data symbols, which use two cycles of a 2.2-KHz carrier to represent logic 0 and one cycle of a 1.2-KHz carrier to represent logic 1. The second challenge is minimizing phase distortion in the modulated output at the transitions of logic 0 to logic 1 symbols and at the transitions of logic 1 to logic 0 symbols. The following subsections describe the design of the filter in more detail to address the challenge of constant amplitude for both carrier frequencies. The phase distortion challenge is addressed by adjusting the timing of the filter cutoff frequency control signal (Filter_sel signal in Figure 12) with respect to the modulated data stream. This timing is adjustable in firmware and features independent control of the timing relationship for both digital data transitions (that is logic 0 to logic 1 and logic 1 to logic 0). Section 5.2 describes the details of the phase distortion timing adjustment.

4.6.1 Filter Details

The filter used for this design is a fourth-order, low-pass Butterworth response, which is implemented using two cascaded, second-order, low-pass Sallen-Key sections. The filter design includes a switchable capacitor in each section, which is used to switch the filter cutoff frequency based on the carrier frequency that the MSP430 device sends. The switches are therefore controlled by the unmodulated digital data, which is a second output from the MSP430 into the filter. Because only a single capacitor is switched in each section, the filter Q is reduced compared to the ideal Butterworth response for logic 1 symbols, for the sake of simplicity. The following Figure 12 shows a schematic for the filter section.
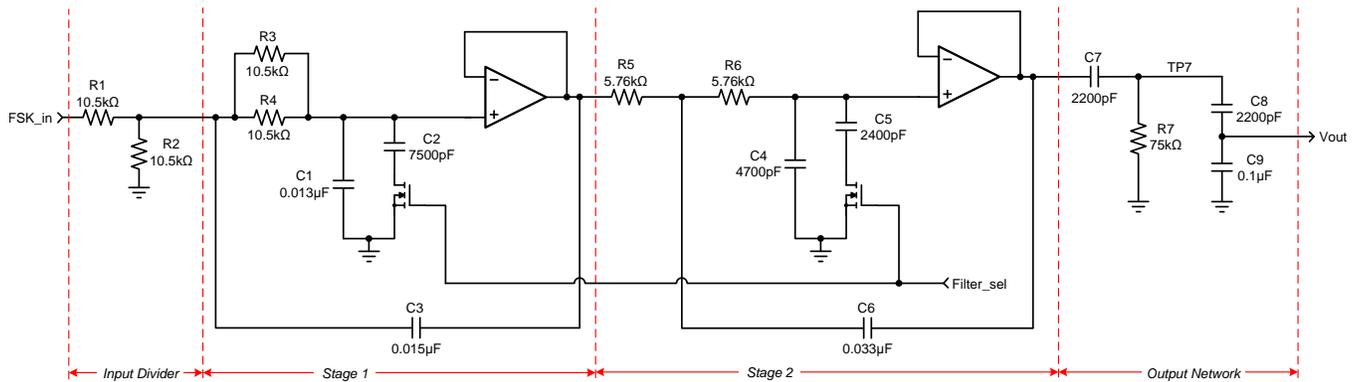

Figure 12. FSK Modulation Filter Schematic

To obtain a reasonably clean sinusoid output (that is, low harmonic distortion) from a square wave input, an attenuation of the third harmonic must be at least 20 dB more than the attenuation of the fundamental frequency. This requirement means that the third harmonic will be at least an order of magnitude smaller than the fundamental frequency. Conceptually, a fourth-order, low-pass filter is to have an attenuation of 24 dB/octave, which means there is a sufficient amount of attenuation present at the third harmonic. Because of the reduced filter Q for logic 1 symbols, which translates into a wider filter transition region and lower attenuation at the third harmonic, more attenuation margin is required for the filter response at the third harmonic for logic 0 symbols to have more than 20-dB attenuation of the third harmonic for both logic symbols. If not for this constraint (where the same filter response with the same filter Q is implemented for both logic symbols), a third-order response would be sufficient for this application. The effect of the modified filter Q in this implementation is visible in the simulated frequency response for a normalized low-pass filter in the following Figure 13.
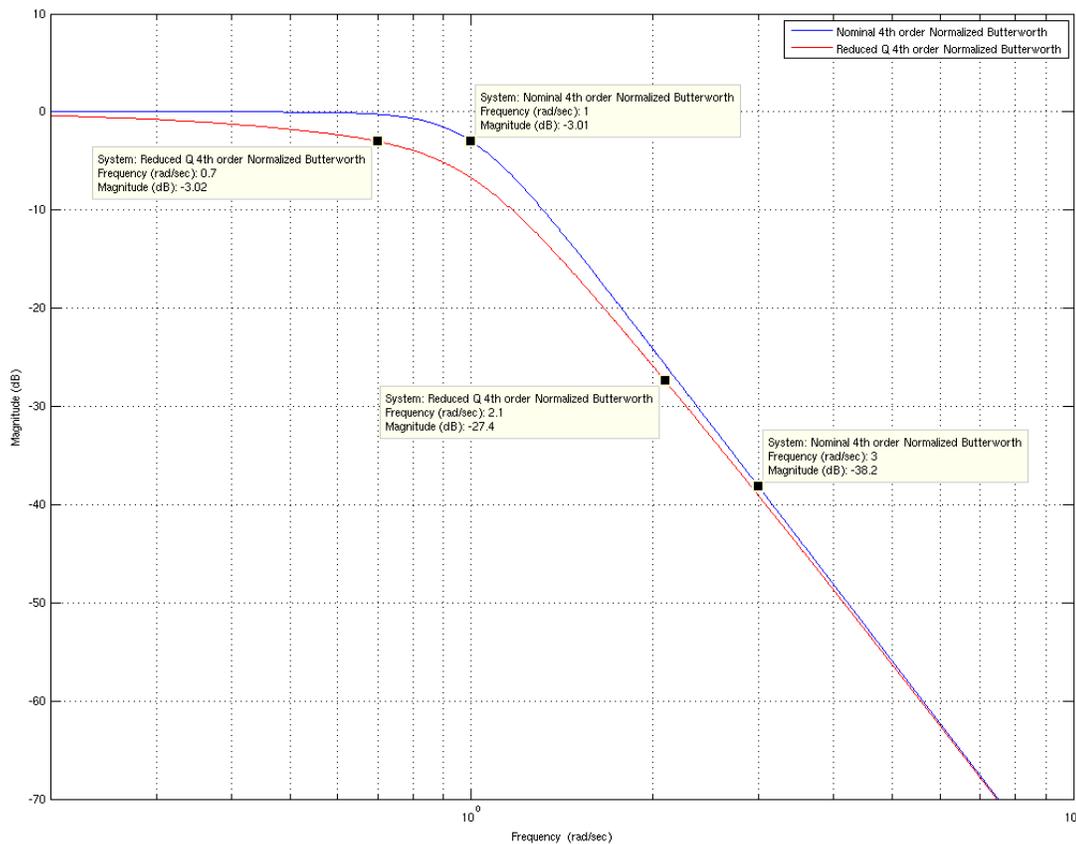
Figure 13. Comparison of Normalized Fourth-Order Filter Response

The choice of filter response is due to the desire to have a flat magnitude response in the filter passband and stopband, as well as efficient transition band attenuation versus filter order. A Bessel response also fits the requirements for the magnitude response; however, the Butterworth response features a steeper filter rolloff for a given order compared to that of a Bessel response. If the timing adjustment from the MSP430 is not available and the filter has been implemented such that the same filter response with the same filter Q was implemented for both logic symbols, using the Bessel response is preferable, even at the expense of higher order, so that its property of linear passband phase (and, therefore, constant group delay) can be utilized to minimize phase distortion in the modulated sinusoidal output signal.

The Sallen-Key architecture has been chosen for its ease of use compared to other possible architectures and the availability of multiple optimization choices provided by this filter architecture. Another benefit of the Sallen-Key architecture is the fact that it does not require a separate mid-supply bias for single supply operation. These benefits translate directly into a cost effective and flexible filter design.

4.6.2 Filter Design

The characteristics of the filter for this design for achieving equal amplitude for the two logic symbols in theory can be implemented with a band pass filter where the upper and lower cutoff frequencies correspond to the carries frequencies for a logic 1 symbol and for a logic 0 symbol, respectively. The drawback with this implementation is that the attenuation at the third harmonic is not the same for both symbols, as Figure 14 shows.
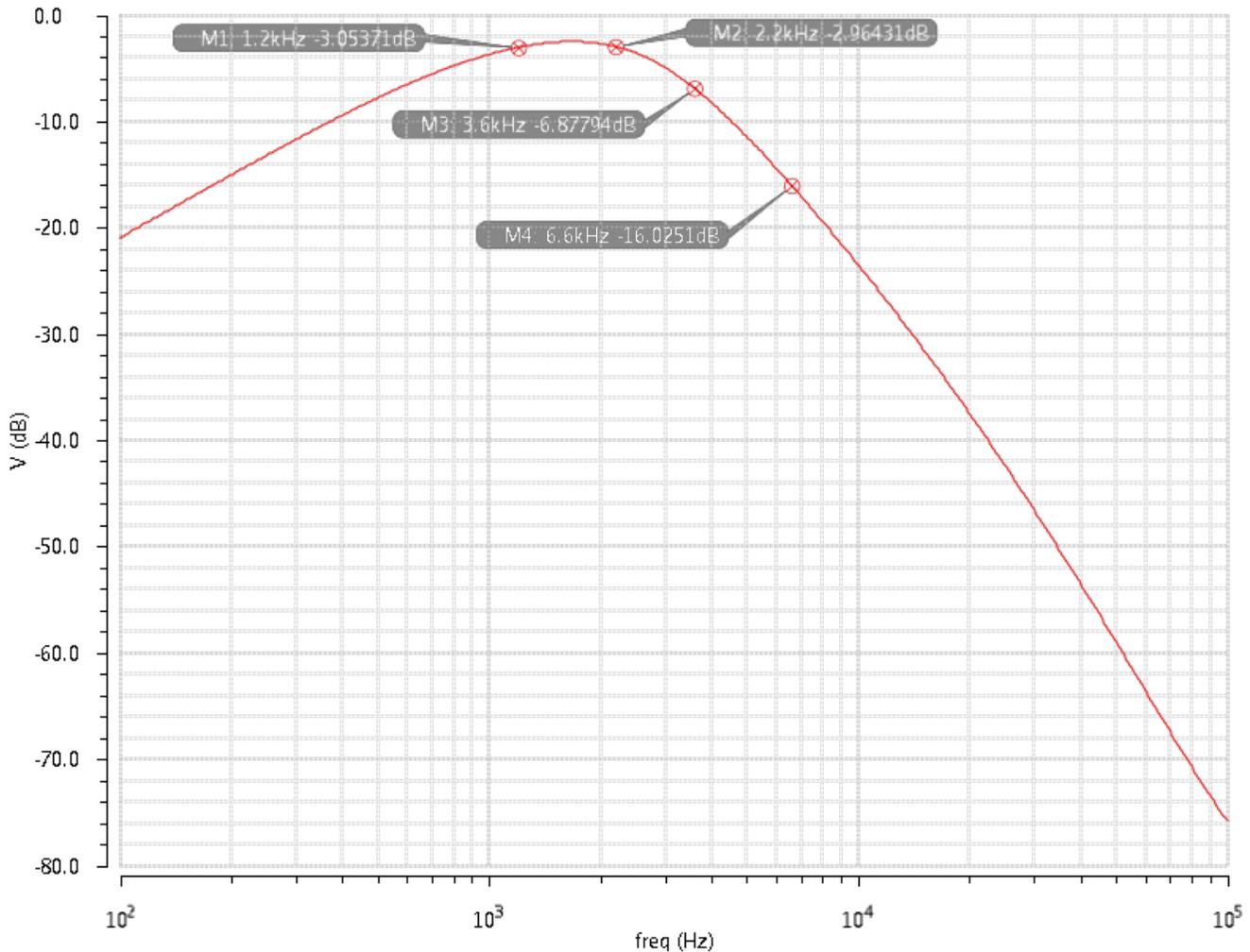

Figure 14. Drawbacks for Implementing Band-Pass Filter Response

The design requires a low-pass filter, which has a cutoff frequency that changes based on the logic symbol being transmitted. An additional simple RC filter can then be added as a final stage to remove the DC content before being converted to loop current. The difficulty with implementing this type of filter lies in the number of components that must be switched based on the logic symbol to maintain the filter Q. One possible alternative implementation is to use a switched-capacitor filter implementation. This kind of implementation requires an accurate clock that can scale with the logic symbol, but must operate at a low enough quiescent current so that regulation of the 4- to 20-mA loop can be maintained. For these reasons, a compromise has been made in this design where the filter Q is reduced for a logic 1 symbol to minimize the number of components that must be switched based on the logic symbol and to maintain a low quiescent current.

The synthesis of the filter component values starts with the normalized transfer function for the desired response followed by mapping the response coefficients to normalized component values for the specific filter circuit implementation. The normalized component values are then frequency scaled and magnitude scaled to achieve a desirable range of component values. Finally, this set of scaled component values must be rounded to standard component values followed by simulation to verify proper operation. For this design, the normalized transfer function for a fourth-order, low-pass Butterworth response is calculated as Equation 3 shows:

$$T(s) = \frac{vo}{vi} = \frac{1}{\left(s^2 + 0.765367s + 1\right) \times \left(s^2 + 1.847759s + 1\right)} = \frac{1}{\left(s^2 + \dfrac{s}{Q_1} + 1\right) \times \left(s^2 + \dfrac{s}{Q_2} + 1\right)}$$

(3)

The following Figure 15 shows a general, second-order, Sallen-Key filter stage, which implements the transfer function in Equation 4.

$$T(s) = \frac{vo}{vi} = \frac{\dfrac{1}{R1 \times R2 \times C1 \times C2}}{s^2 + \left(\dfrac{1}{R1 \times C1} + \dfrac{1}{R2 \times C2}\right) \times s + \dfrac{1}{R1 \times R2 \times C1 \times C2}}$$
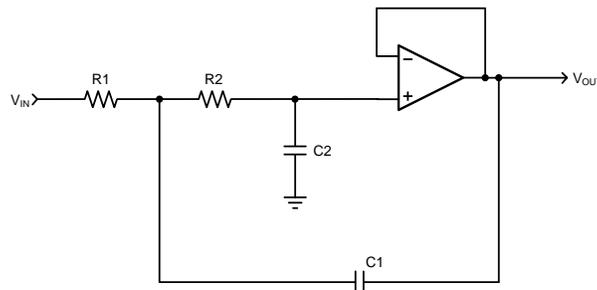
(4)

Figure 15. Second-Order Low-Pass Sallen-Key Filter Circuit

Equation 4 shows four component values to satisfy two equations, namely fc and Q. For this design, the choice was made to have R1 = R2 = 1. This optimization choice produces the minimum sensitivity of filter characteristics to component variations at the expense of a large capacitance spread between C1 and C2. However, because the Q values for this filter implementation are not too large, this is a fair trade-off. Mapping the coefficients of Equation 3 with those of Equation 4 and taking R1 = R2 = 1 yields C1 = 2Q and C2 = 1 / (2Q). Equation 5 and Equation 6 are used to scale the normalized component values. Note that the magnitude scaling factor can be different for the two filter stages because stage 2 is driven by the low output impedance of the op-amp in stage 1. The scaling factors used are:
kf = 2 × π × 2200 = 13823.01, km1 = 5250, and km2 = 5760. Table 2 tabulates the component values through the different steps of the design process.

$$C_{scaled} = \frac{C_{norm}}{kf \times km}$$

(5)

$$R_{scaled} = km \times R_{norm}$$

(6)

Table 2. Tabulation of Filter Component Design Values

FILTER STAGE	NORMALIZED	FREQ SCALED	MAG SCALED	FINAL (2.2 KHz)	1.2-KHz CALCULATION	FINAL (1.2 KHz)
R1_stage1	1	1	5.25k	10.5k || 10.5k	5.25k	10.5k || 10.5k
R2_stage1	1	1	5.25k	10.5k || 10.5k	5.25k	10.5k || 10.5k
Q_stage1		0.5412		0.5371	0.433	0.4277
C1_stage1	1.0824	7.8304E-05	14.915e-9	0.015 µF	0.015 µF	0.015 µF
C2_stage1	0.9239	6.6836E-05	12.7307e-9	0.013 µF	20.0057e-9	0.013 µF + 7500 pF
R1_stage2	1	1	5.76k	5.76k	5.76k	5.76k

Table 2. Tabulation of Filter Component Design Values (continued)

FILTER STAGE	NORMALIZED	FREQ SCALED	MAG SCALED	FINAL (2.2 KHz)	1.2-KHz CALCULATION	FINAL (1.2 KHz)
R2_stage2	1	1	5.76k	5.76k	5.76k	5.76k
Q_stage2		1.3066		1.3249	1.045	1.0779
C1_stage2	2.6131	1.8904E-04	32.82e-9	0.033 µF	0.033 µF	0.033 µF
C2_stage2	0.3827	2.7685E-05	4.8063e-9	4700 pF	7.5545e-9	4700 pF + 2400 pF

The final values in the preceding Table 2 show the design for a filter cutoff of 2.2 KHz corresponding to the carrier frequency for a logic 0 symbol. The design for the 1.2-KHz filter cutoff corresponding to the carrier frequency for a logic 1 symbol involves re-calculating the value of C2 using Equation 7. The capacitor value placed in series with the MOS switch (see Figure 12) is simply the difference between the two calculated C2 values for the two different filter cutoff frequencies. The additional factor in the frequency term of the following Equation 7 is because of the reduction in Q for the logic 1 symbol. This reduction in Q means that the –3-dB frequency is not equal to the natural frequency of the second-order terms. The scaling factor here has been determined through a simulation, such that the attenuation at fc is –3 dB (see Figure 13). As the preceding Table 2 shows, further adjustment of the final values for the new C2 values is necessary to obtain a 3-dB attenuation at 1.2 KHz in the final design.

$$C2_{new} = \frac{1}{R1 \times R2 \times C1 \times \left(2\pi fc \times 1.458333\right)^2}$$

(7)

The last pieces of the design are the voltage divider at the input to the filter (R1 and R2 in Figure 12) and the output network (C7, C8, C9, and R7 in Figure 12). The voltage divider is necessary to keep the input signal for both filter stages within the common-mode range of the op-amps. If a rail-to-rail, input stage op-amp is used, then this voltage divider is not necessary; however, this option requires that the op-amps swing rail-to-rail on the output as well. The output network is required to filter the DC component of the filter output signal and scale the final output to the 15-mVpp nominal amplitude required by the DAC to generate the nominal 1-mApp loop current. Equation 8 and Equation 9 provide the design equations for the output network. Figure 12 shows the final filter. Figure 16 shows the simulation results for the final filter design.

$$T(s) = \frac{vo_{tp7}}{vi} = \frac{\left(\frac{C7}{C7 + CT}\right) \times s}{s + \frac{1}{R7 \times (C7 + CT)}}$$

where

$$CT = \frac{C8 \times C9}{C8 + C9}$$

$$fc = \frac{1}{2\pi R7 \times (C7 + CT)}$$

(8)

$$\left(1 + \frac{C9}{C8}\right) = \frac{\left(\frac{3.3}{4 \times \sqrt{2}}\right)}{15 \text{ mVpp}} \cong 39 \text{ assuming that C8 = C7}$$
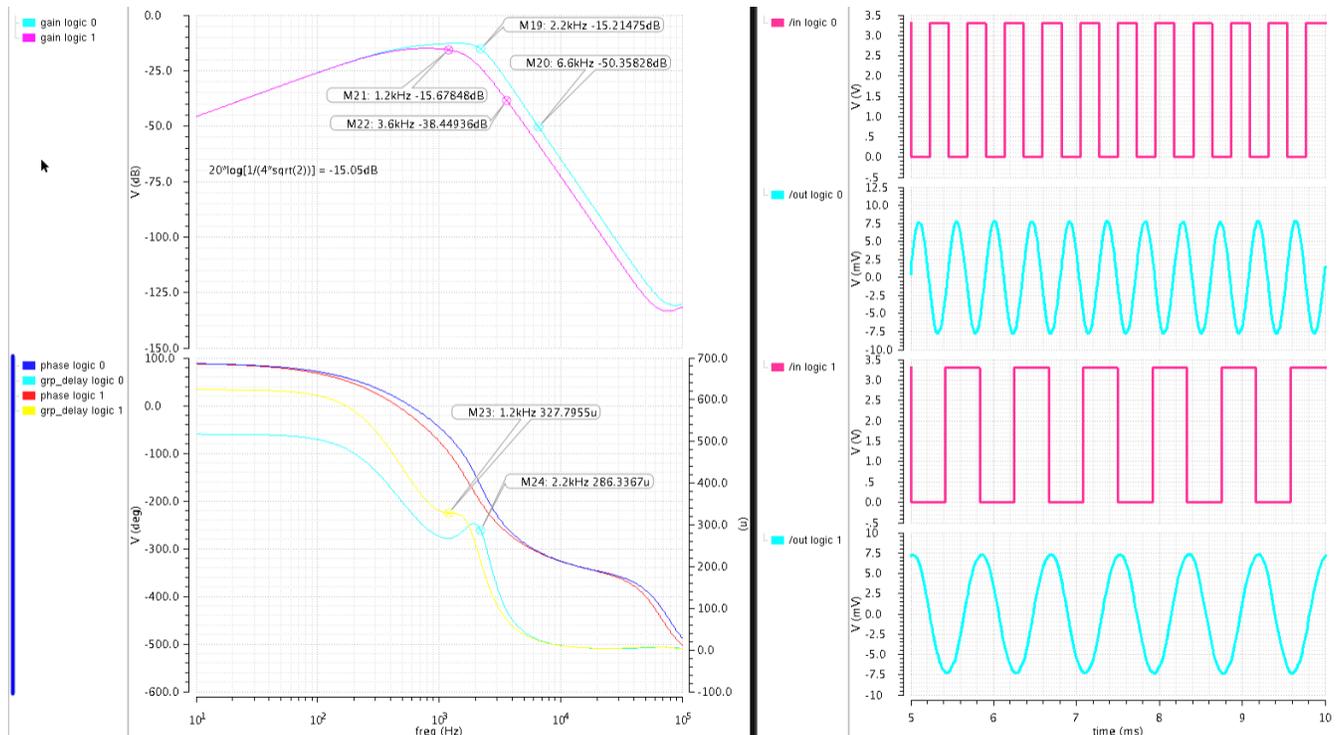
(9)

Figure 16. Simulation Results of Final Filter Design—Performance With Both Logic Symbols

While the previously outlined steps are generally applicable to any active RC filter implementation, be advised that filter design tool software programs are available that feature GUI-based input for filter specifications with these steps and calculations fully automated in the background. One such tool is available from Texas Instruments. Please visit http://www.ti.com/lsds/ti/analog/webench/webench-filters.page for more information on the WEBENCH® filter designer tool.

4.6.3   Alternate Filter Options

As previously mentioned, the design shown is one possible solution for converting a modulated digital data stream into a scaled, constant amplitude-modulated sinusoid with minimum phase distortion at the bit transitions. The rationale for this design choice has been explained, but in summation, the result arises mainly because of the discrete implementation of supply current, in addition to focusing on the overall solution cost. Some other possible solutions are a switched-capacitor filter implementation and an M-bit digital representation of a sinusoid, which is then converted to analog using a DAC (similar to direct digital synthesis (DDS)). Figure 17 and Figure 18 show the block diagrams for these two possible solutions, respectively.
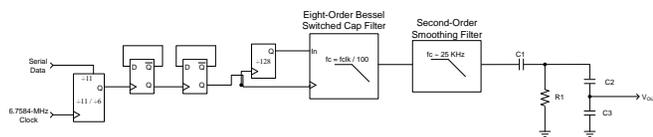

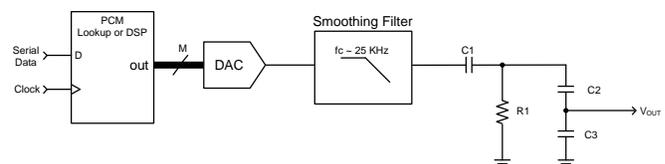**Figure 17. Switched Capacitor Filter Implementation**

Figure 18. Digital Synthesis of Sinusoid Implementation

Both of these implementations offer the benefits of constant amplitude and minimum phase distortion. The switched-capacitor solution accomplishes this by maintaining the same attenuation level of the fundamental frequency and filter Q for both logic symbols, indicating that the attenuation of the harmonics is to be the same for both logic symbols. The DDS approach uses the scaling of the DAC output voltage to accomplish constant amplitude. Because the digital representation is oversampled and generated from either a computed value of the ideal waveform or from a look-up table representation, the phase distortion is also minimized. The DDS approach is generally utilized in commercially-available integrated HART modems. While both of these solutions are elegant, they are both better suited for integrated implementations where cost and supply current (as well as board space) can all be simultaneously minimized to acceptable levels.

4.7 *FSK Modulation DAC Input*

The DAC161S997 is also configured to receive an FSK modulation signal input and inject the signal into the current loop. The output from the FSK modulation filter connects to pin C2 of the DAC. The input signal must be a sine wave with an approximate 15-mV peak-to-peak to create a 1-mA peak-to-peak output on the current loop. This design achieves a 16.8-mV peak-to-peak input to the DAC and a 0.95-mA peak-to-peak output onto the current loop. Figure 19 shows the MSP430 generated PWM and the input signal into the DAC.
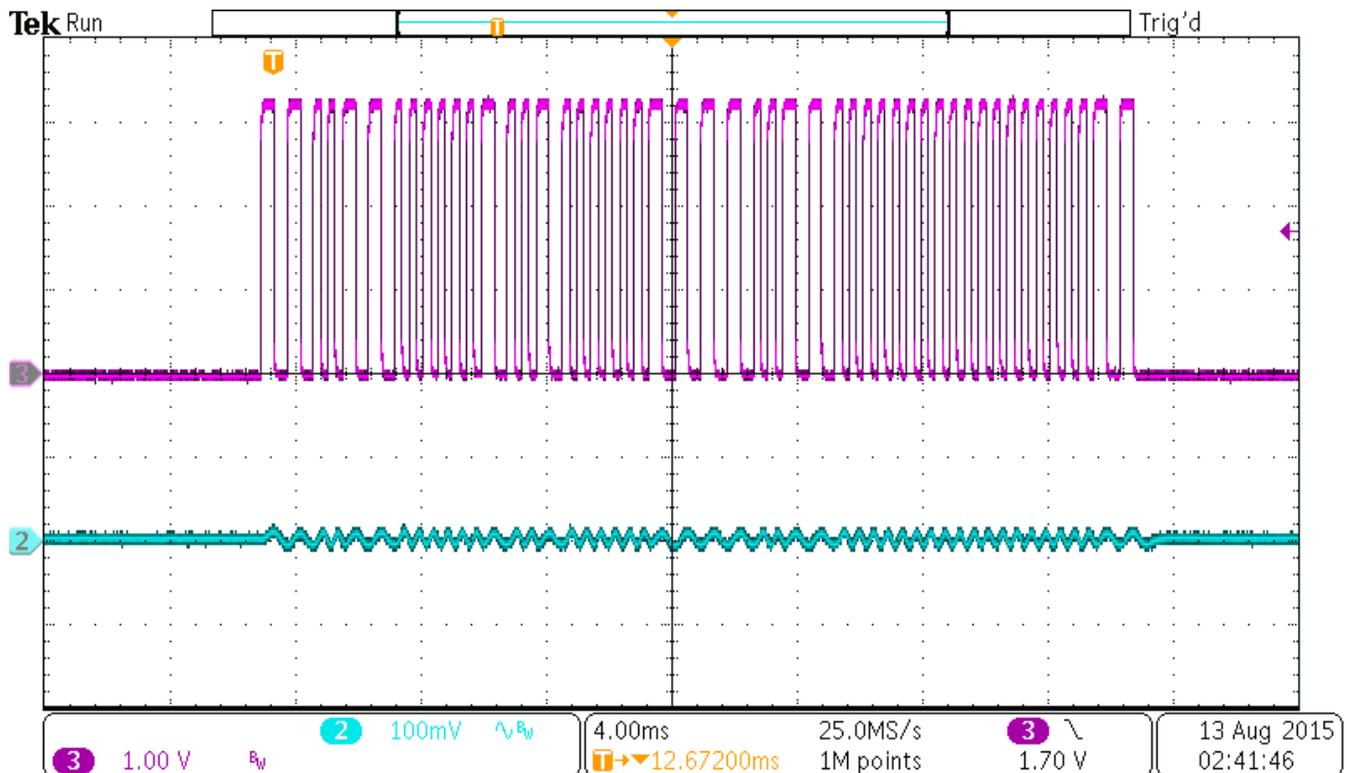

Figure 19. PWM and DAC Input Signals

4.8 Reverse Polarity Protection

To protect the system from accidentally connecting the power to ground and vice versa, place the reverse protection diodes in the path of Loop+ and Loop− as Figure 20 and Figure 21 show.
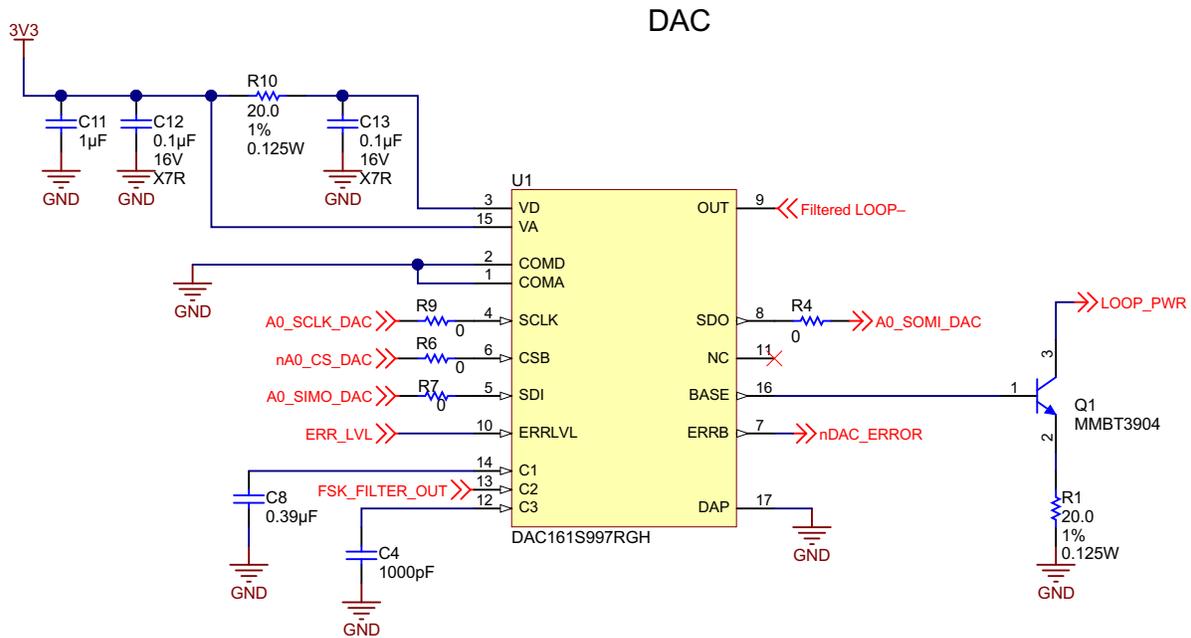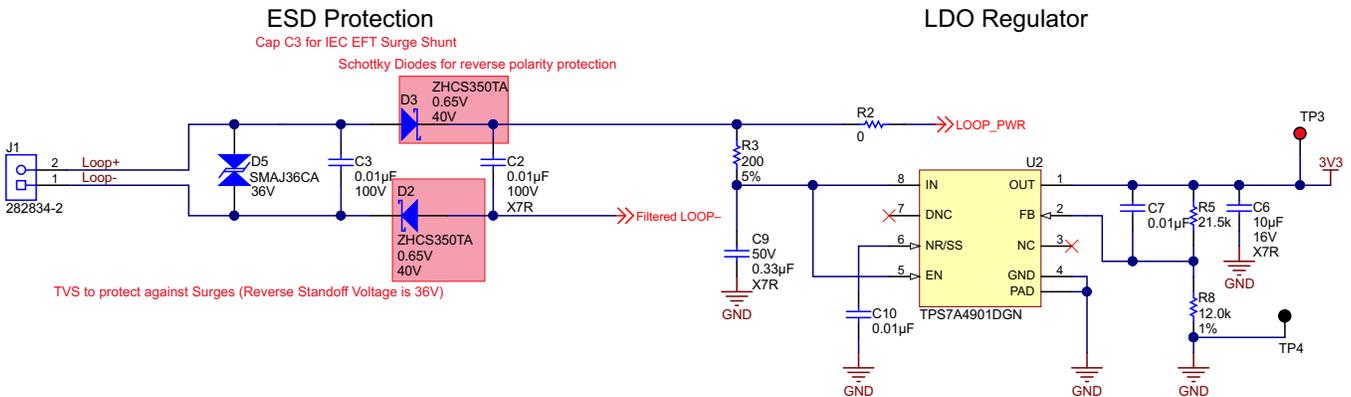

Figure 20. Reverse Polarity Diode

Figure 21. Reverse Polarity Diode at Loop−

5 Software Overview

The MSP430 software was written using TI's Code Composer Studio™ v6.1 (CCSv6) software. A 14-pin JTAG debug interface is required to program the reference design. The MSP-FET and the MSP-FET430UIF are suitable USB debuggers and programmers and were used during the development process of this TIDA-00483 reference design. However, the MSP-FET is the only debugger that allows the TI EnergyTrace™ software feature.

5.1 Sensor Parameters and Communication

The TIDA-00483 reference design has two sensors, the HDC1000 and OPT30001, which produce a total of three different pieces of environmental data. These sensors collect temperature, humidity, and ambient light data. Both devices communicate with the MSP430 through the I^{2}C bus with unique addresses. The temperature data is first converted to the correct mA output that represents the temperature reading. Section 4.1 details the relationship between loop current and the equivalent sensor reading. The equation converts the temperature reading to the equivalent loop current that represents that temperature value in °C. The DAC161S997 then receives a serial peripheral interface (SPI) command from the MSP430 to adjust the current in the loop. Humidity and lux data are transmitted through FSK modulation on the current loop. The previous Section 4.5 and Section 5.2 provide more information regarding the modulation scheme and mechanics.

5.2 FSK Modulation Scheme

The frequency-shift keying executed for the TIDA-00483 reference design begins with collecting sensor data. After collecting a sensor reading, the transmit data frames are created with the data bytes. The transmit protocol is very similar to HART or UART communication protocols. Table 3 shows the breakdown on the transmit frame.

Table 3. Transmit Data Frame (16 Bits)

START	START	ADDR2	ADDR1	ADDR0	DATA BITS(0 TO 7) LSB FIRST	PARITY	STOP	STOP
1	1	—	—	—	—	1 = odd	1	1

The transmit data frame consists of two start bits, three address bits, eight data bits (sent LSB first), a parity bit for error checking, and then two stop bits. Use the address bits to determine which sensor is communicating or to represent a certain register from a given sensor.

After the transmit frames are created, the entire modulation time sequence for the data transfer is created in memory to decrease any chance of error, shorten the interrupt service routine, and ensure that each pulse of the modulation is correct. The MSP430FR5969A square-wave output from the PWM pin 1.2. An interrupt-driven timer controls when the output on pin 1.2 toggles. At each interrupt, the next time interval loads into the timer interrupt count register, enabling a very short interrupt service routine.

The following Figure 22 shows a sample FSK transmission. The pink signal is the square output directly from the MSP430 MCU and the green signal is the sine wave visible on the current loop. Refer to the preceding Section 4.8 for more information regarding the filter design.
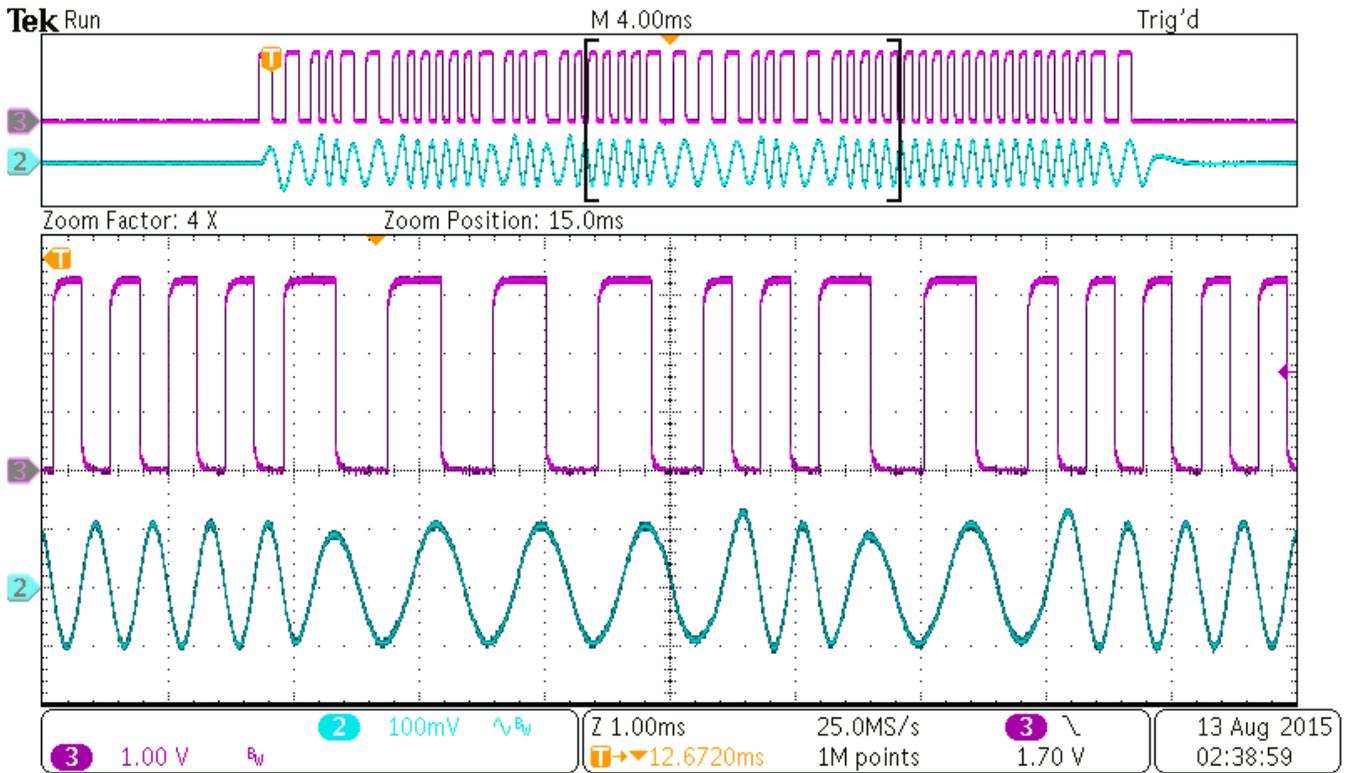
Figure 22. PWM and Loop Signal

Another GPIO pin on the MSP430 is used to toggle a capacitor into the filter design to alter the corner frequency of the Butterworth response. The toggle pin is controlled through an interrupt similar to that of the data frame, but only toggles at the transitions of "0" to "1" or a "1" to "0" transition. This is the only time that the filter must change its corner frequency. To finely customize when each transition happens, delays are added before the GPIO toggle to achieve less phase distortion in the FSK signal. Almost all phase distortion can be removed because a fine granularity clock source is employed.

6 Getting Started

6.1 Hardware Overview

The first critical hardware component to notice is the small 1.5-in (approximately 4-cm) diameter circle that is screen printed in the middle of the board. This shape is the approximate solution size for this design and other 4- to 20-mA sensor boards.

The TIDA-00483 reference design is preprogrammed out-of-the-box to communicate both parameters on the current loop. Temperature values are transmitted through normal 4- to 20-mA operation and the lux measurement on the custom FSK modulation scheme that the previous Section 5.2 details. Two wires are required to connect the dual measurement reference design to a current loop. To make a connection, use the connection points labeled Loop+ and Loop− on the green terminal block J1. Terminal block J1 is near the center of the board and the Loop+ and Loop− test points are located on the right side of the board. Other test points are located near the top and bottom edges of the board for ease of use. Figure 23 shows the top of the finished TIDA-00483 board.
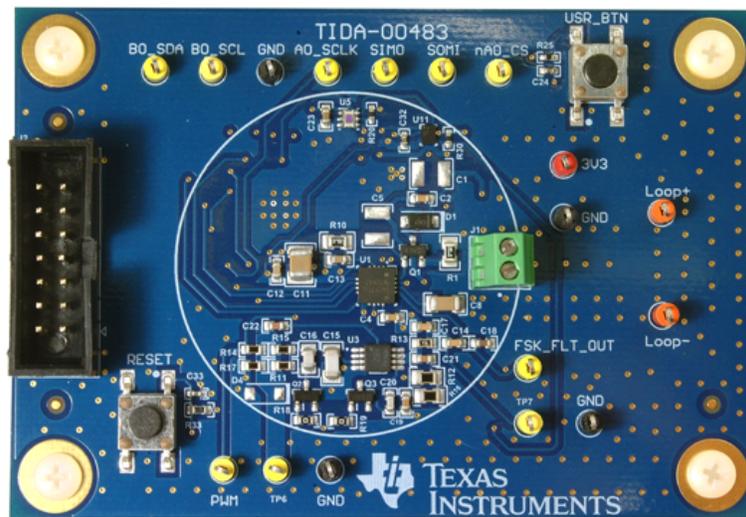

Figure 23. TIDA-00483 Top Board Image

Two push buttons are located on the top of the board, as well. The bottom-left button is the reset and the top-right button is a miscellaneous user button. The OPT3001 optical light sensor is located in the top-middle of the circle outline (U5), whereas the HDC1000 is located just off to the right of the OPT3001 sensor and is labeled U11.

Figure 24 shows the back side of the board. The MSP430 MCU and the LDO are located on the backside of the board along with their supporting components.
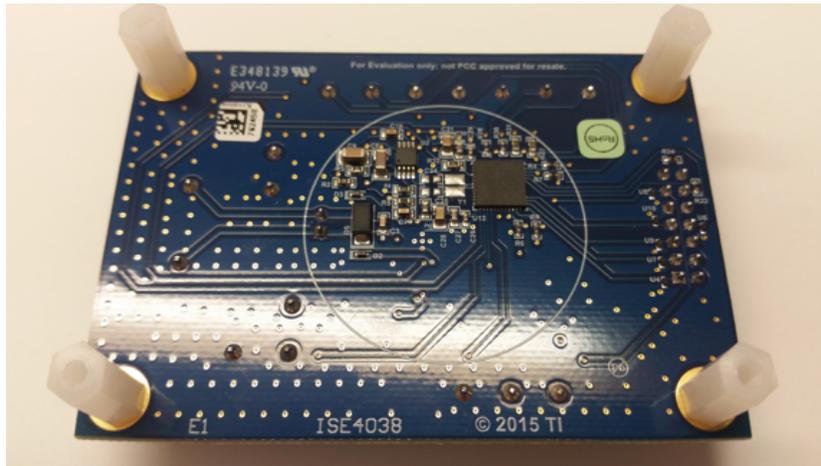

Figure 24. TIDA-00483 Backside Board Image

6.2   Programming

The programming for the TIDA-00483 reference design is fairly simple using CCSv6 or IAR software. The software package available online was created in CCSv6, which includes all of the necessary essential libraries and files. The 14-pin JTAG port located on the left side of the board was used with the MSP-FET during development and testing to load software to the onboard MSP430 MCU.

7 Test Data

> **NOTE:** Unless otherwise noted, the test data in the following subsections were measured with the system at room temperature. All of the measurements in this section were measured with calibrated lab equipment.

7.1 Overview

The major sensing devices of the TIDA-00483 underwent a complete series of testing. Temperature and humidity testing was also performed to verify how the reference design reacts in different environments. The following subsections describe the test setup, procedures, and results.

7.2 DAC Characterization

In this test, Figure 25 shows a 6½ digit multimeter (DMM) connected in series in the current loop. The MSP430 was programmed at fixed current levels: 4 mA, 6 mA, 8 mA, 10 mA, 12 mA, 14 mA, 16 mA, 18 mA, and 20 mA.
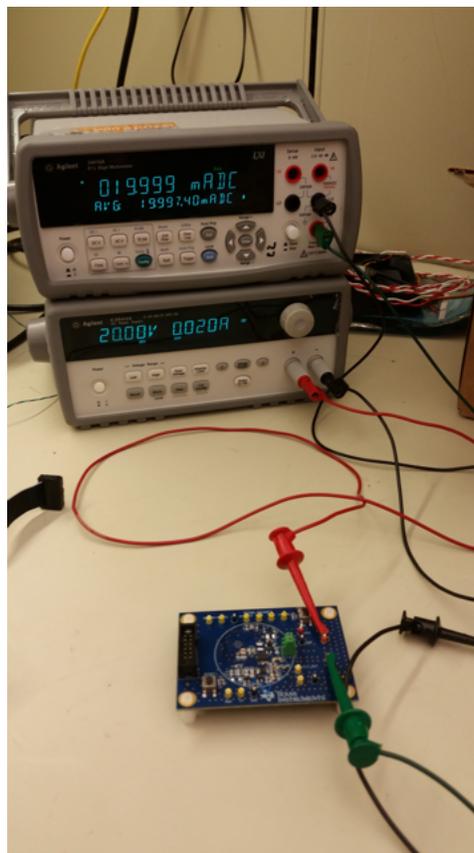

Figure 25. DAC Characterization Setup

The corresponding loop current was measured using the multimeter (see Table 4 and corresponding Figure 26).

Table 4. DAC Current With and Without Gain Calibration

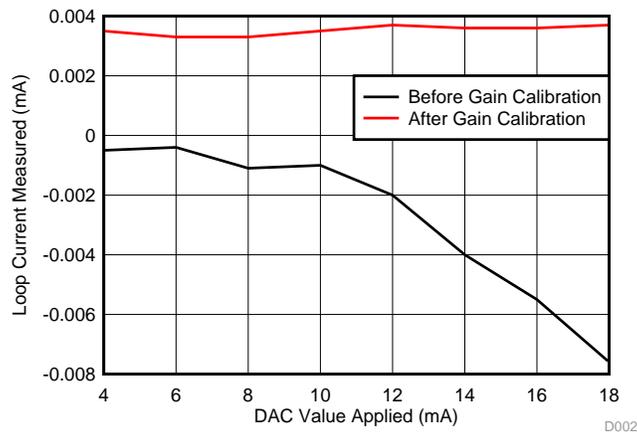| DAC VALUE APPLIED (mA)	LOOP CURRENT MEASURED (mA)	
	PRE-GAIN CALIBRATION	POST-GAIN CALIBRATION
4	3.999	3.9966
6	6.0005	5.9965
8	8.0004	7.9967
10	10.0011	9.9967
12	12.001	11.9965
14	14.002	13.9963
16	16.004	15.9964
18	18.0055	17.9964
20	20.0076	19.9963

Figure 26. DAC Gain and Offset Calibration

The software implements a simple gain correction factor to account for the relatively linear relationship between error and loop current. The gain can be modified further in the MSP430 firmware with a more complex algorithm, as Section 4.3 details.

7.3 Output Resolution

The DAC output was programmed to 4 mA and the maximum and minimum current values were recorded by a 6½ DMM over a 20-minute period to monitor the output resolution. The minimum and maximum currents recorded were 3.995262 mA and 3.9960963 mA, respectively. This result means that the maximum output variation is 0.833 µA. That value is an approximate 0.0208% loss of accuracy in the worst scenario, with the worst case resulting in a minimum current level of 4 mA (4000 µA).

7.4 Power Supply Influence

To complete the power-supply influence test, the power supply was tested from 10 V to 30 V and the corresponding loop-current change was recorded. The output current error versus the transmitter voltage was collected over the current loop range of 4 mA to 20 mA. The transmitter voltage is the power supply voltage minus the voltage drop at the sense resistor. The DAC receives a code to set the loop current at each level for each data point at approximately every 4 mA. During this process, the voltage across the sense resistor was recorded with a 6½ DMM. The loop current was calculated from the sense resistor voltage drop and resistor value. The following Figure 27 shows the results of this calculation. By examining the graph, the user can notice that the output current error is about 25 PPM.
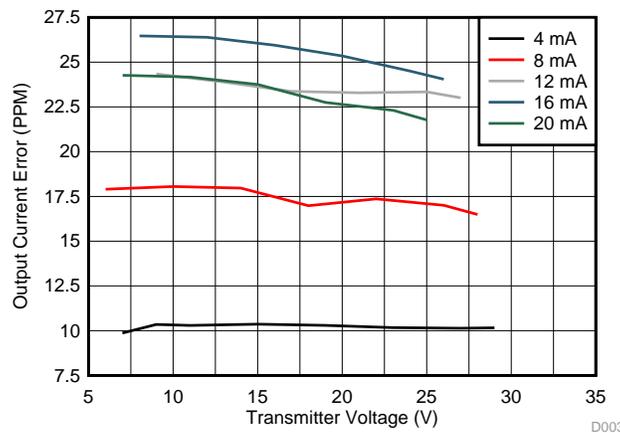

Figure 27. Output Current Error Versus Transmitter Voltage

7.5 Reverse Polarity Test

To conduct the reverse polarity test, swap the connections on Loop+ and Loop–. Figure 28 shows the proper setup for connecting the board before connecting the board up backwards.

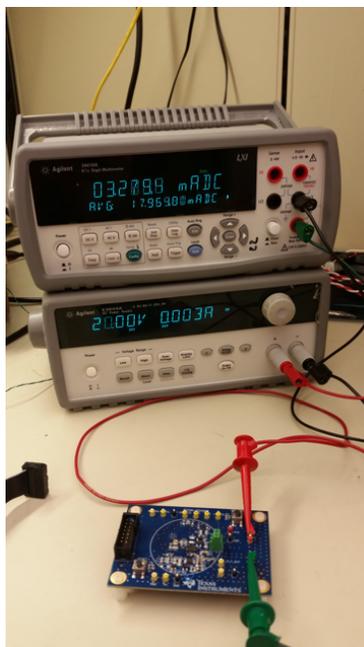Figure 29 shows an image of the setup after reversing the polarity.

Figure 28. Reverse Polarity Setup With Correct Polarity

Figure 29. Reverse Polarity Measurement With Inverted Polarity

7.6 Latch-Up Condition Testing

Rapid power cycling testing was completed to ensure that the DAC161S997 and other devices in the system do not latch up from error conditions relating to quickly disconnecting or losing power during operation. The test was completed by disconnecting one of the loop connectors and reconnecting it to try to force a latch-up condition. The power supply was kept on for the entire duration of this test. No latch-up or errors were seen when disconnecting Loop+ or Loop– from the board and then reconnecting back to its original connection point. Even quickly making a connection with either loop connector caused no damage to the subsystem and no errors were observed. This test proves that this design can be installed into a "hot" current loop system without any harm to the circuitry.

7.7 Temperature Testing

The temperature sensor reading is transmitted through the normal 4- to 20-mA operation. A test was conducted to check the accuracy of the reference design over the temperature range of 15°C to 85°C. A temperature bath was used to control the temperature during testing. At each temperature data point, the board was allowed to soak for 15 minutes after the chamber reached the intended temperature. The temperature bath, HDC sensor temperature reading, DAC code, and sense resistor voltage was recorded at each data point to determine the HDC error, DAC error, and the total combined system error.

The equivalent temperature reading is calculated by Equation 1 in Section 4.1. Some adjustments can be made to the basic equation to achieve a higher level of accuracy. The HDC relative error is below ±0.2°C for the entire testing range. The DAC adds a little error, but the maximum combined system error is visible as ±0.3°C. Figure 30 and Figure 31 show the plots for these respective measurements.
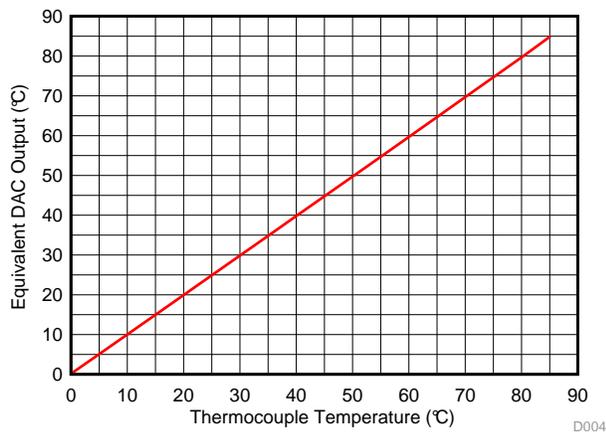

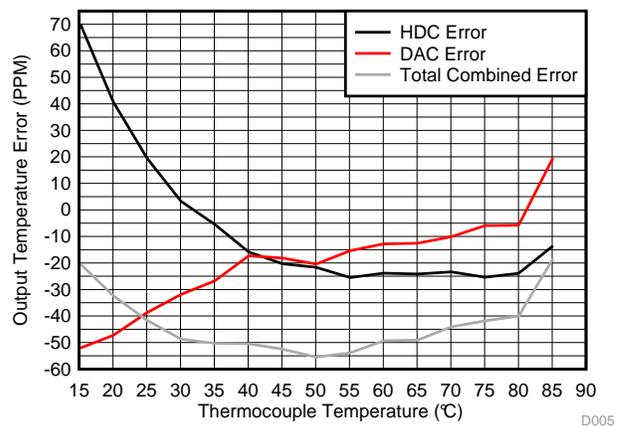**Figure 30. Temperature Versus DAC Output**

Figure 31. Error Across Temperature

7.8 *Humidity Testing*

To better understand how the TIDA-00483 TI Design system responds to varying relative humidity levels, the hardware was placed in a Thunder Scientific® Model 2500 Benchtop Humidity Generator (www.thunderscientific.com/).

The relative humidity was then programmed to run a pre-defined profile. This profile set the initial chamber humidity to 20% and soaked the TI Design hardware for an initial 40 minutes. The relative humidity was then ramped up to 30% at a controlled rate over 10 minutes, followed by soaking at that humidity level for 20 minutes. This process was repeated up to the maximum tested relative humidity of 70%, then decreased similarly to the minimum humidity level of 20%, and finally soaked for 40 minutes to end the test. The temperature during this profile was held to a set-point of 45°C. Figure 32 shows a plot of the HDC1000 measured relative humidity.
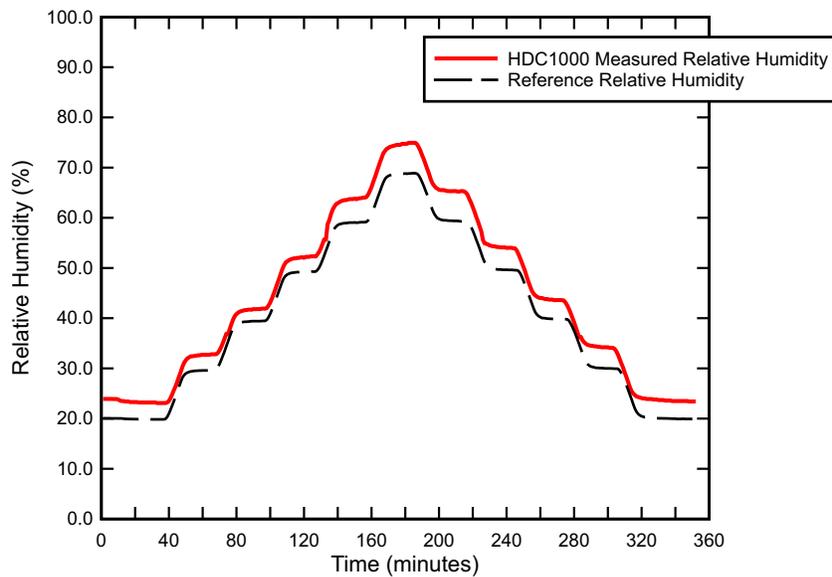

Figure 32. HDC1000 Measured Relative Humidity Data

7.9 *Light Sensor Testing*

The light sensor data was collected on a different reference design with a similar layout. For more information regarding the light sensing test platform and other testing completed on the OPT3001 sensor, refer to the Section 7 *Test Setup* in TIDU781.

The first test completed compares the output response versus the input illuminance of multiple light sources or bulb types. Fluorescent, halogen, and incandescent light were tested. Figure 33 shows a plot of the output response versus the input illuminance with multiple light sources.
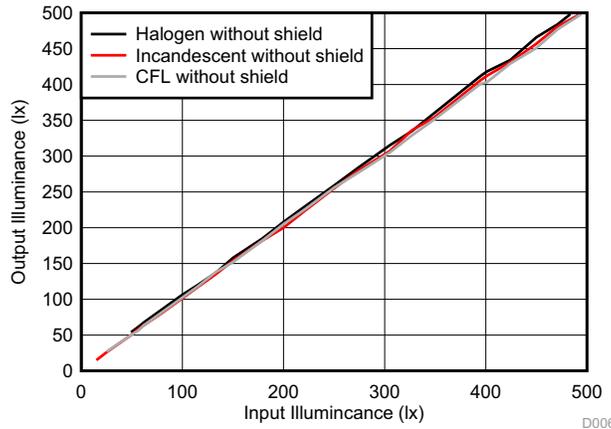

Figure 33. Output Response Versus Input Illuminance—Multiple Light Sources

The test platform was approximately 11 in from the light box during each test. As demonstrated in the test data, various light sources have little effect on the output of the OPT3001. The ambient light sensor is excellent at sensing the intensity of light, regardless of the type of light.

The following test showcases the ability of the OPT3001 sensor to closely measure the intensity of light from 0 lx to 83 klx. This test reveals less than a 4% error at any one point (see Figure 34).
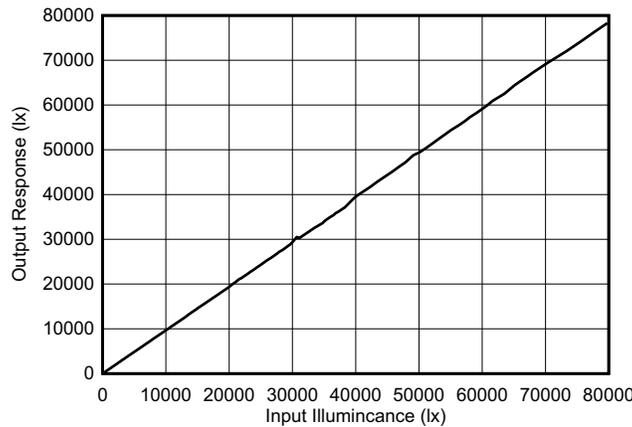

Figure 34. Output Response Versus Input Illuminance—Full Range, White LEDs

8 Design Files

8.1 Schematics

To download the schematics for each board, see the design files at TIDA-00483.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00483.

8.3 Layout Prints

To download the layout prints for each board, see the design files at TIDA-00483.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00483.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00483.

8.6 Assembly Drawings

To download the assembly files, see the design files at TIDA-00483.

9 Software Files

To download the software files, see the design files at TIDA-00483.

10 References

1. Texas Instruments, *Noise Analysis in Operational Amplifier Circuits*, Application Report (SLVA043)
2. Texas Instruments, *HART Field Transmitter for RTD Temperature Design Guide*, TIDM-HRTTRANSMITTER Design Guide (TIDUA04)

11 About the Author

JARROD KREBS is a systems designer at Texas Instruments, where he is responsible for developing reference designs in the industrial segment. Jarrod has experience with software and embedded applications implemented on ARM-based microcontrollers and TI's MSP430 platforms. Jarrod earned his bachelor of science in computer engineering from Kansas State University in Manhattan, KS. Jarrod is also a member of the Institute of Electrical and Electronics Engineers (IEEE).

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