

PMP7154RevB/C Test Results

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Topology: nonsynchronous buck converter, step down converter
 Device: TPS40200; cost effective, no bootstrap diode – needs PMOS FET

RevA: achieved loop exactly as calculated, bw 10kHz
 RevB: tuned loop to bw 15kHz; decreased sense resistor from 68 to 50milliOhm *
 RevC: low noise, added input filter, added RC snubber

**functionality OK, but no startup at full load and low input 8V:*

solution #1:

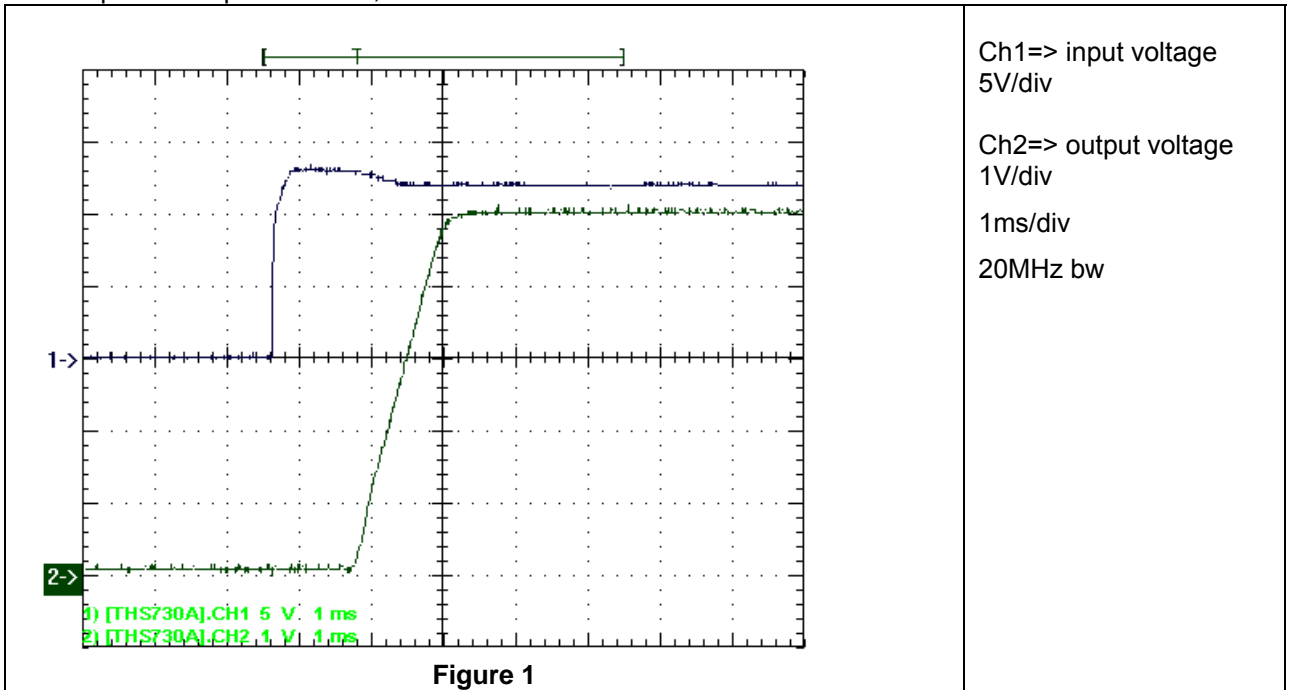
*increase softstart capacitor to lower peak current during startup;
 wanted to keep startup around 2ms.*

solution #2:

*decrease sense resistor to allow more current, here 2Amps DC;
 inductor is OK up to 2Amps, went for 50milliOhm;
 startup at full load 1A and low input 8V OK, current limit 2Amps (200%).*

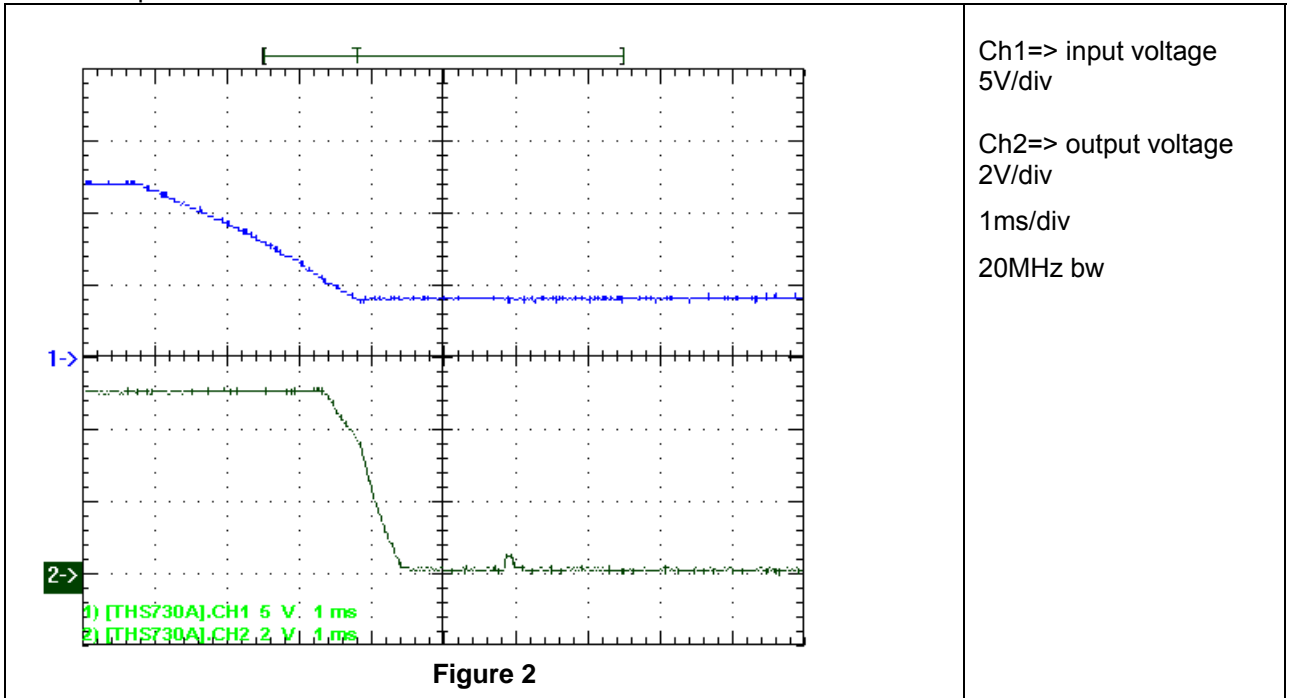
1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 12V, with 1A load at the output. Startup w/in 1.5ms, calculated 2.02ms:



2 Shutdown

The shutdown waveform is shown in the Figure 2. The input voltage was set at 12V, with 1A load on the output.



3 Efficiency

The efficiency is shown in the Figure 3 below. The input voltage was set to 12V

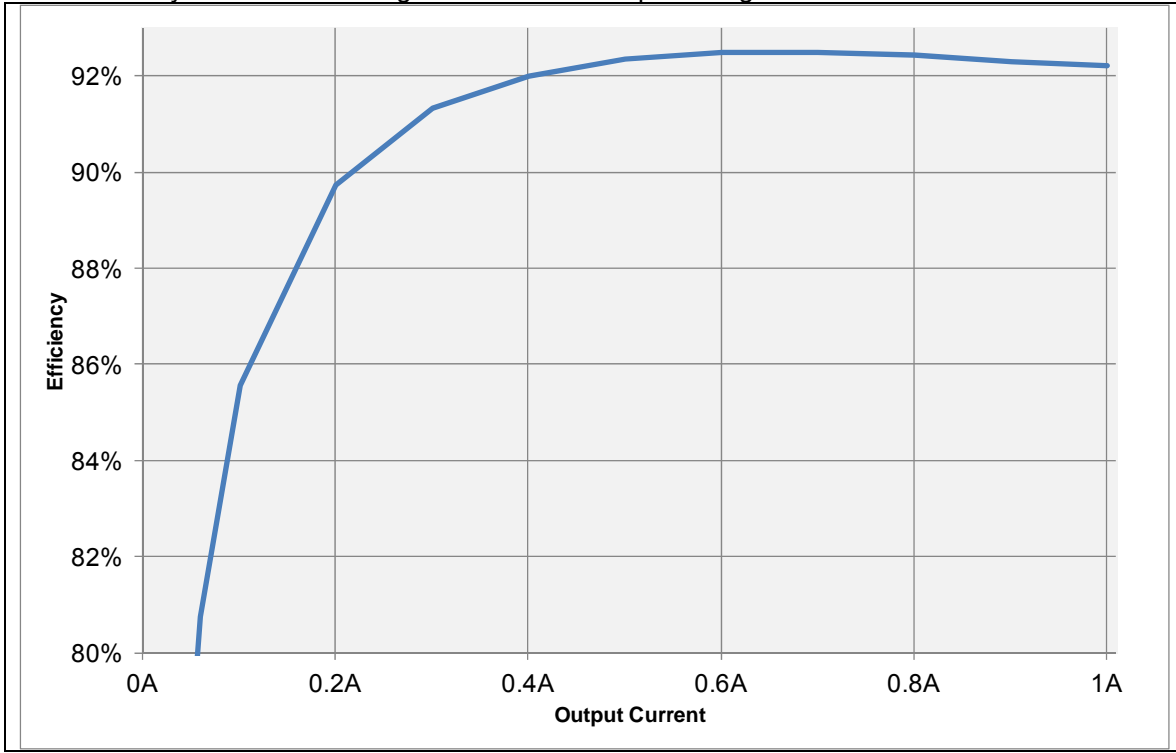
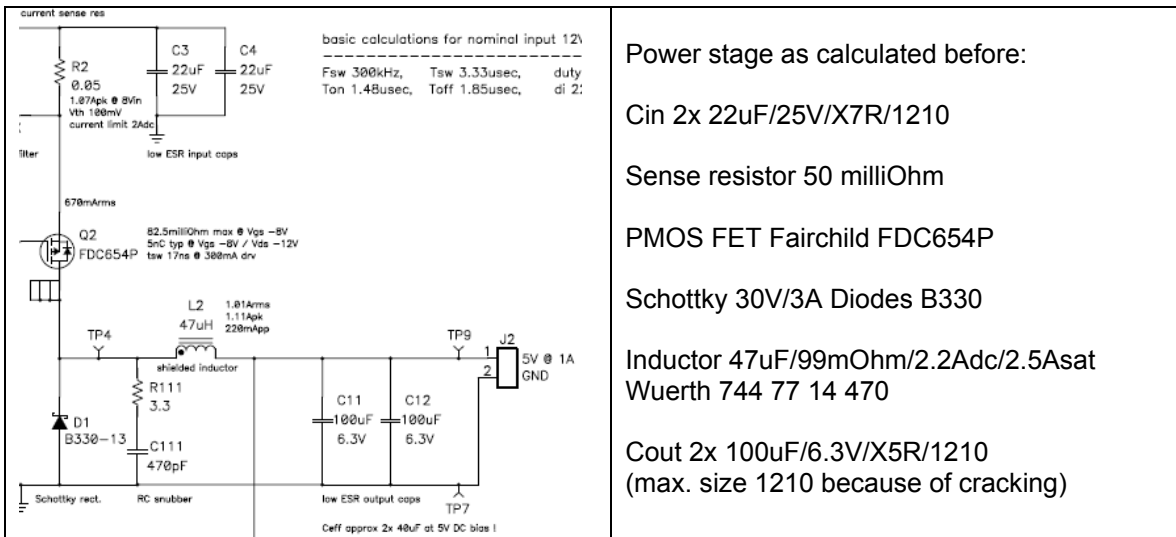


Figure 3

Full load effcy 92.2%, calculated 91.9%;
 deviation by self heating of Schottky rectifier and less switching losses
 (due to rise time/fall time 10ns).

Maximum effcy 92.5% at 600mA..700mA, so around 2/3 of full load 1A, perfect.

Effcy ≥90% in a range 200mA to 1A, so 20% load to 100% load



4 Load Regulation

The load regulation of the output is shown in the Figure 4 below. The input voltage was set to 12V.

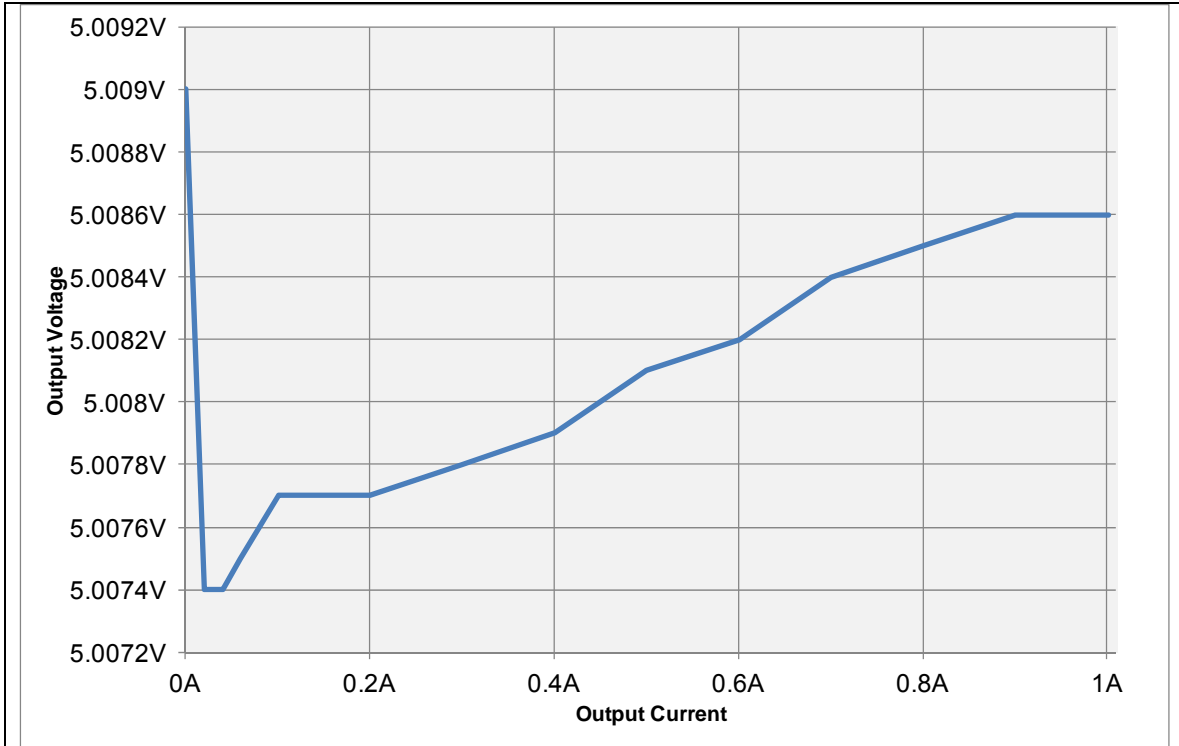


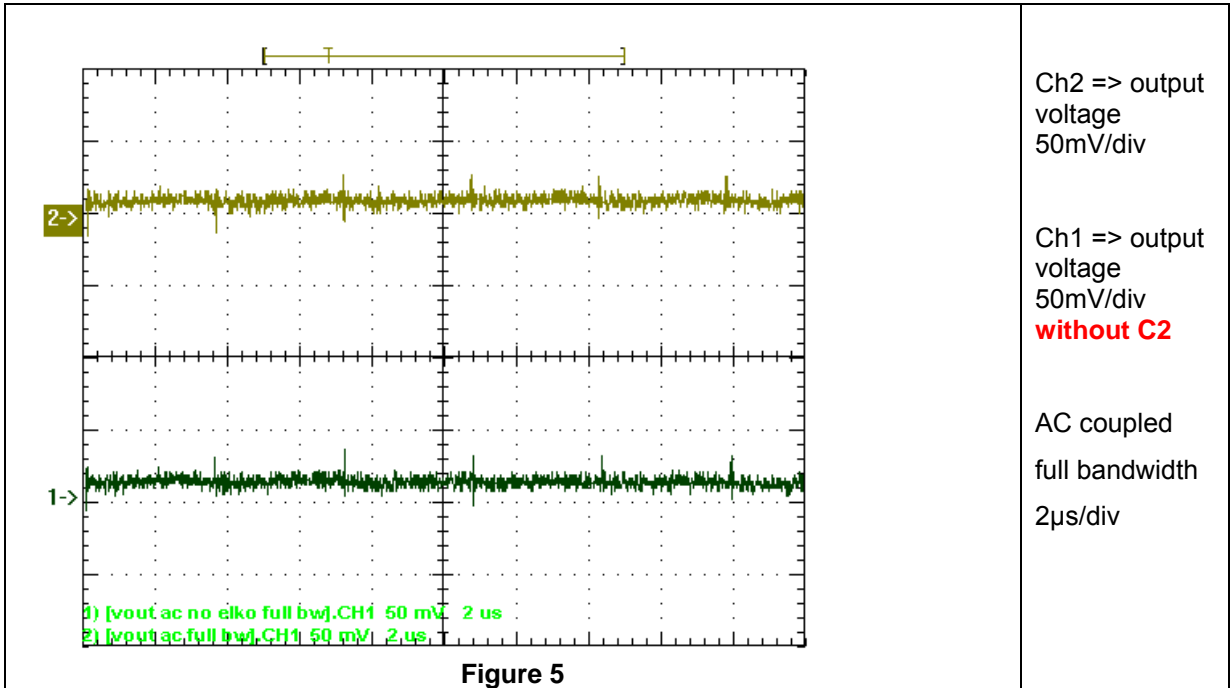
Figure 4

Min. Vout 5.0074V (DCM), max Vout 5.009V (NoLoad, Cout catches noise),

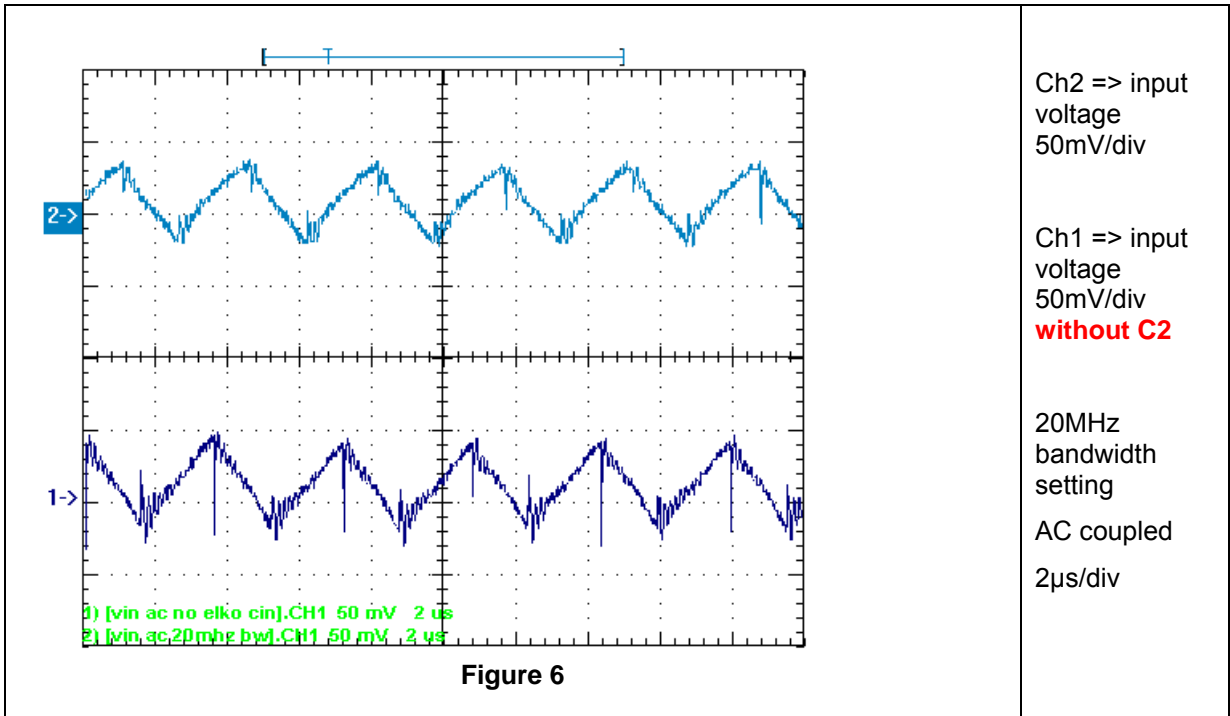
Output voltage variation 1.6mV, so 0.03%, negligible.

5 Ripple Voltage

The output ripple voltage is shown in Figure 5. The image was taken with 1A load 12V at the input. Due to low ESR MLCCs at the output almost no output ripple voltage:

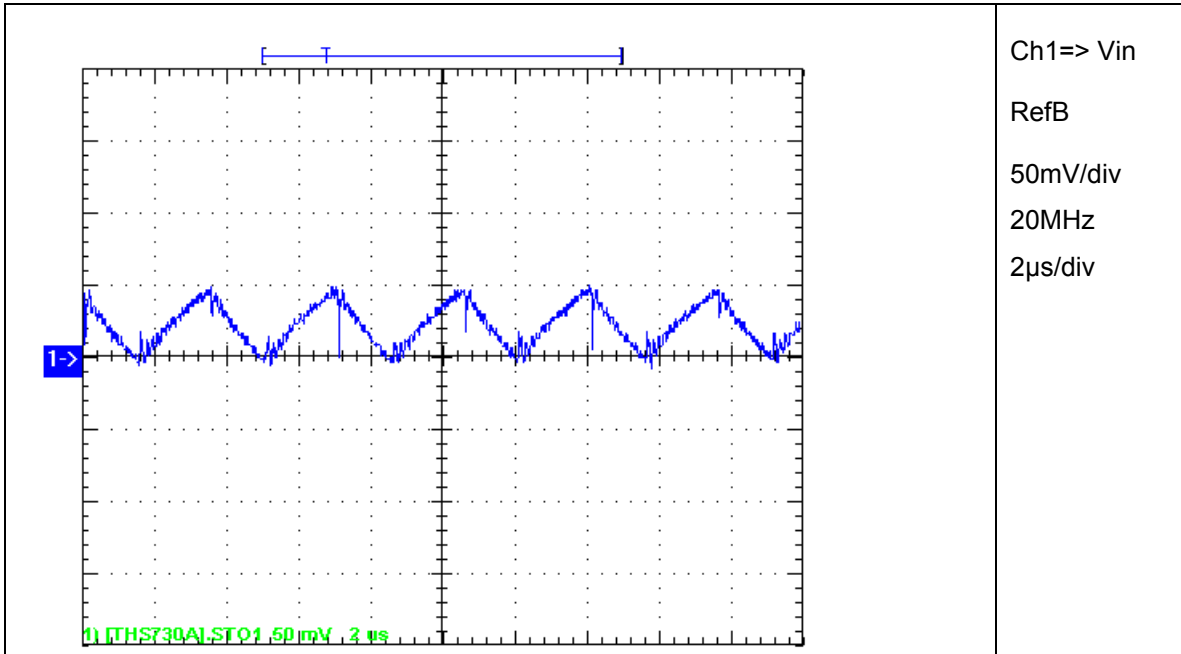


The input ripple voltage is shown in Figure 6. The image was taken with 1A load 12V at the input.

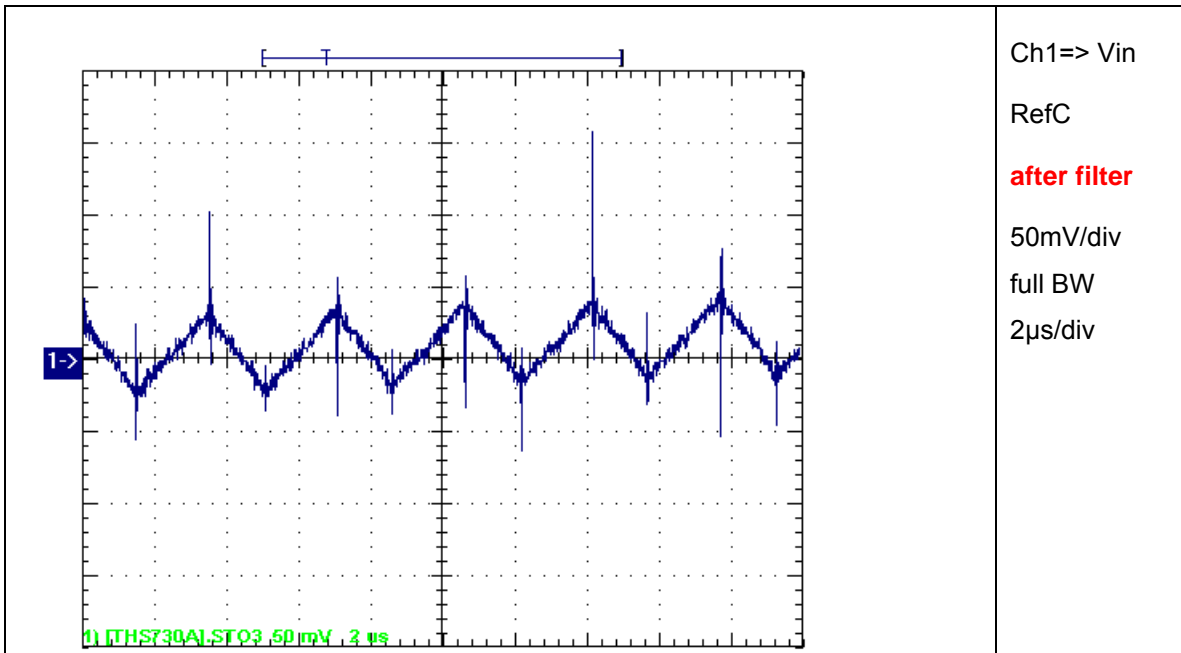


Simply paralleling a bulk capacitor is not a very big benefit – check impedances, use PSPICE !

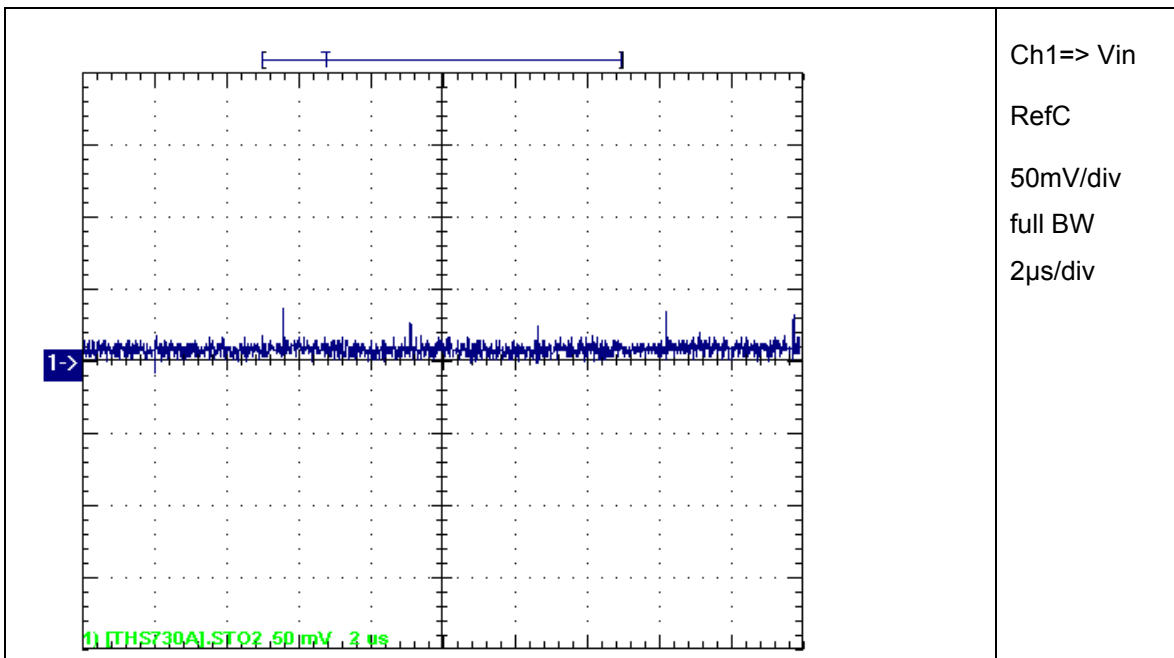
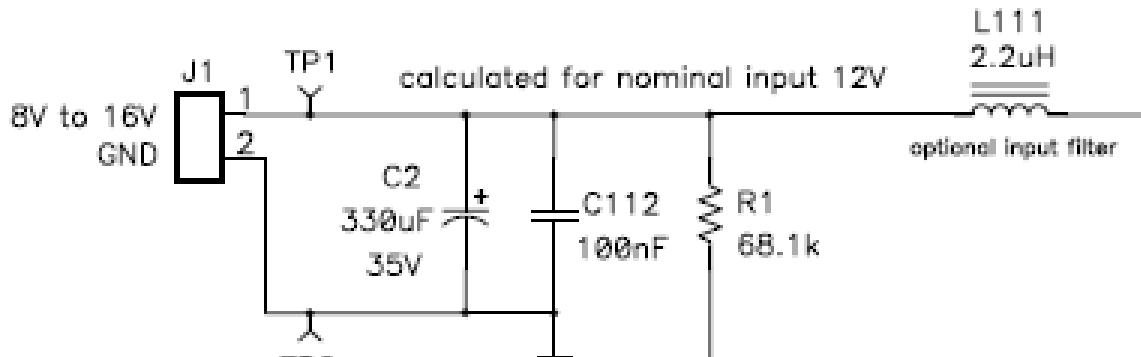
Reflected ripple = conducted emissions, EMI, with 220uF electrolytic & 2x 22uF MLCC: **50mVpp**



Separating electrolytic and MLCCs by filter inductor 2.2uH, decoupling pulsed currents from input;
Ripple voltage across MLCCs:



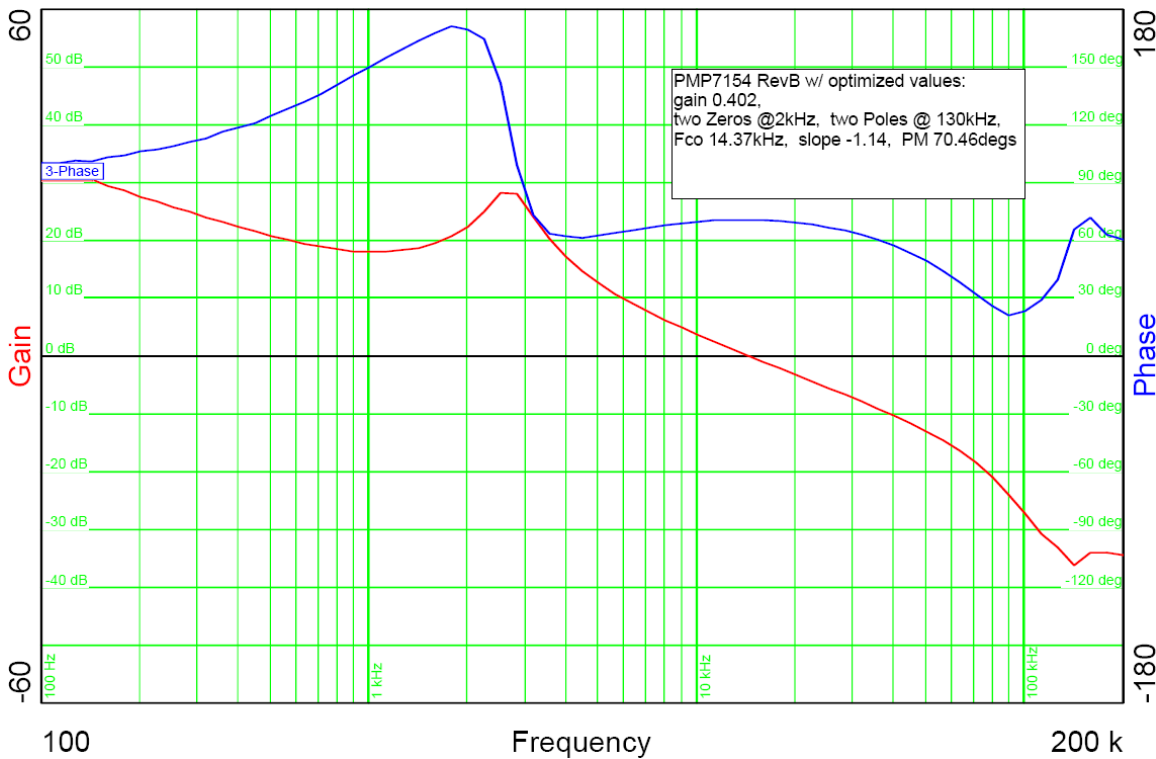
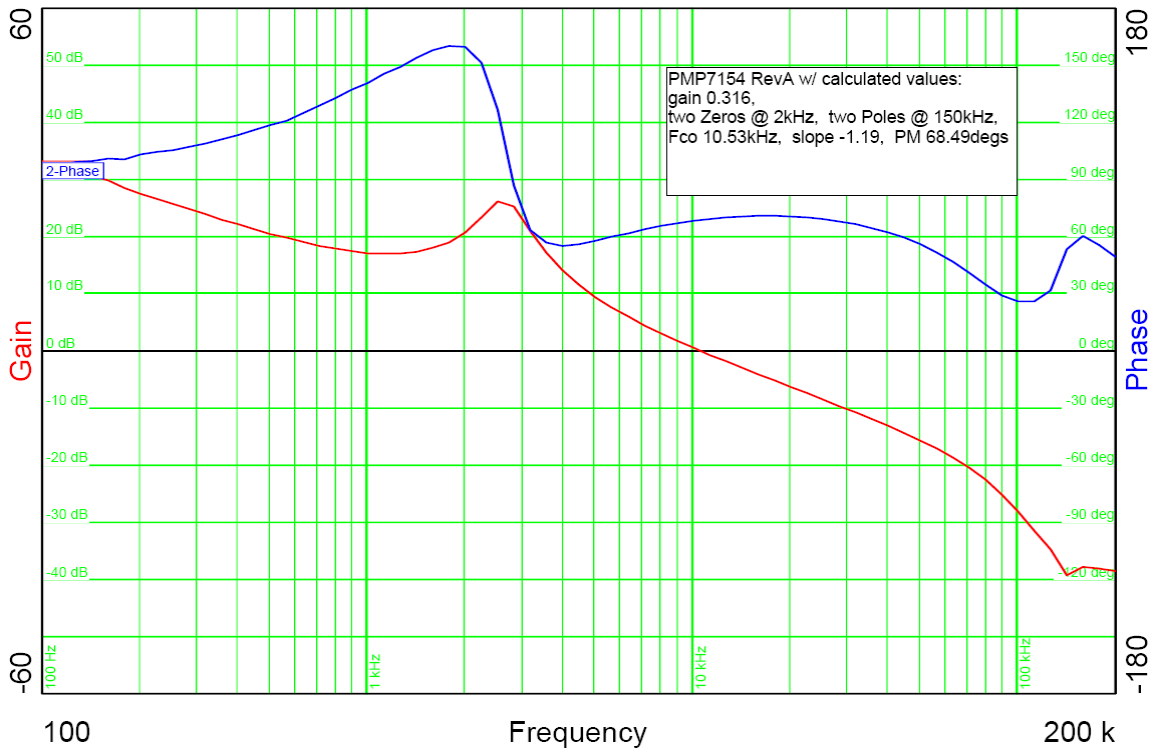
Finally the input voltage by using PI filter 220uF – 3.3uH – 2x 22uF;
A small ceramic capacitor 100nF was added to the electrolytic to suppress glitches:



A tremendous reduction of reflected ripple resulted in better EMI behavior !
The inductor prevents the source from seeing the pulse currents – less conducted emissions.

6 Control Loop Frequency Response

Figures below shows the loop response with 1A load and 12V input – RevA 10kHz, RevB 15kHz:



The bandwidth is measured with NWA Venable #3120. The crossover frequency 10.5kHz for RevA fits exactly to the first calculation by hand, the phase margin is slightly bigger. Slope at crossover is close to -1, here -1.19.

For RevB the bandwidth was optimized to 15kHz, the crossover frequency fits exactly to the calculation and the EXCEL spreadsheet Fco 14.4kHz; again PM is bigger, slope is -1.14.

REMEMBER:

This analysis is a small signal analysis, shows the small signal behavior of the power supply.

The only true analysis is a large signal analysis, the system response on a load transient !

Below the typical test method, load transient 50%, means half the load to full load:

7 Load Transients

The Figure 7 shows the response to load transients. The load is switching from 0.5A to 1A. with 400Hz frequency. The input voltage was set to 12V

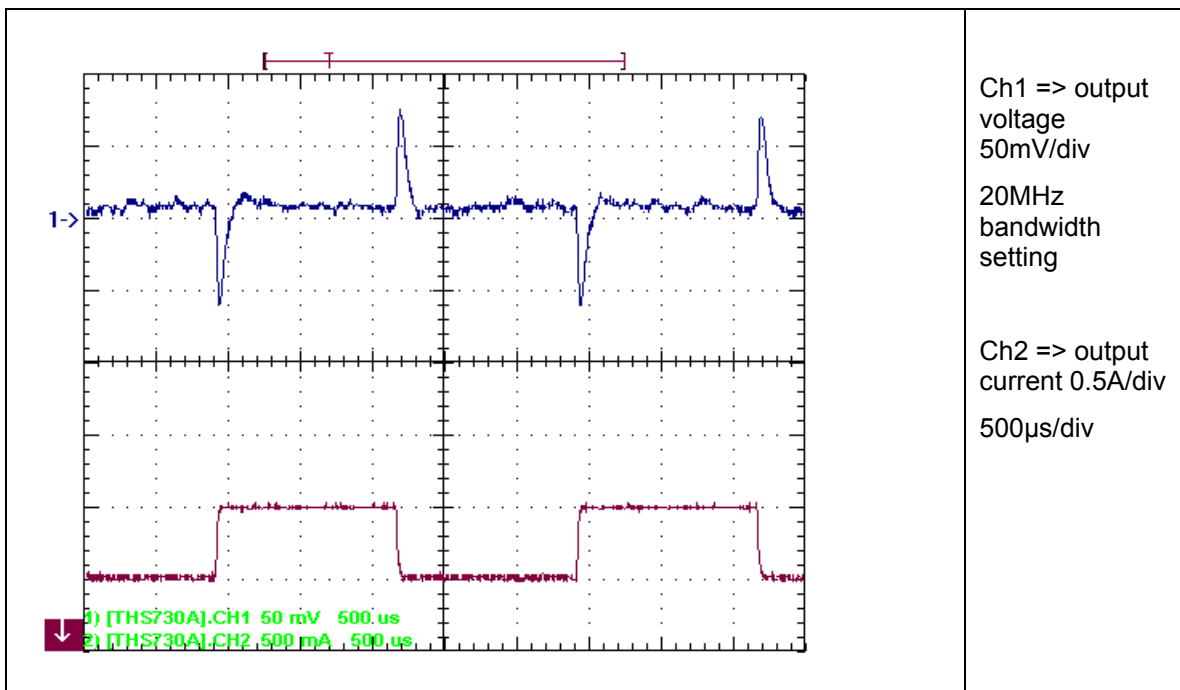


Figure 7

The voltage drop caused by di 500mA is around 70mV, so less than 2% of the output voltage 5V; The combination output capacitor to loop bandwidth matches.

A proper calculation of the error amplifier compensation results in a stable design. For series production a phase margin >60 degrees and a gain margin <-15dB is recommended.

8 Miscellaneous Waveforms

8.1 Switch node (D1)

With input voltage set to 12V and 1A lout results in the waveform shown in Figure 8

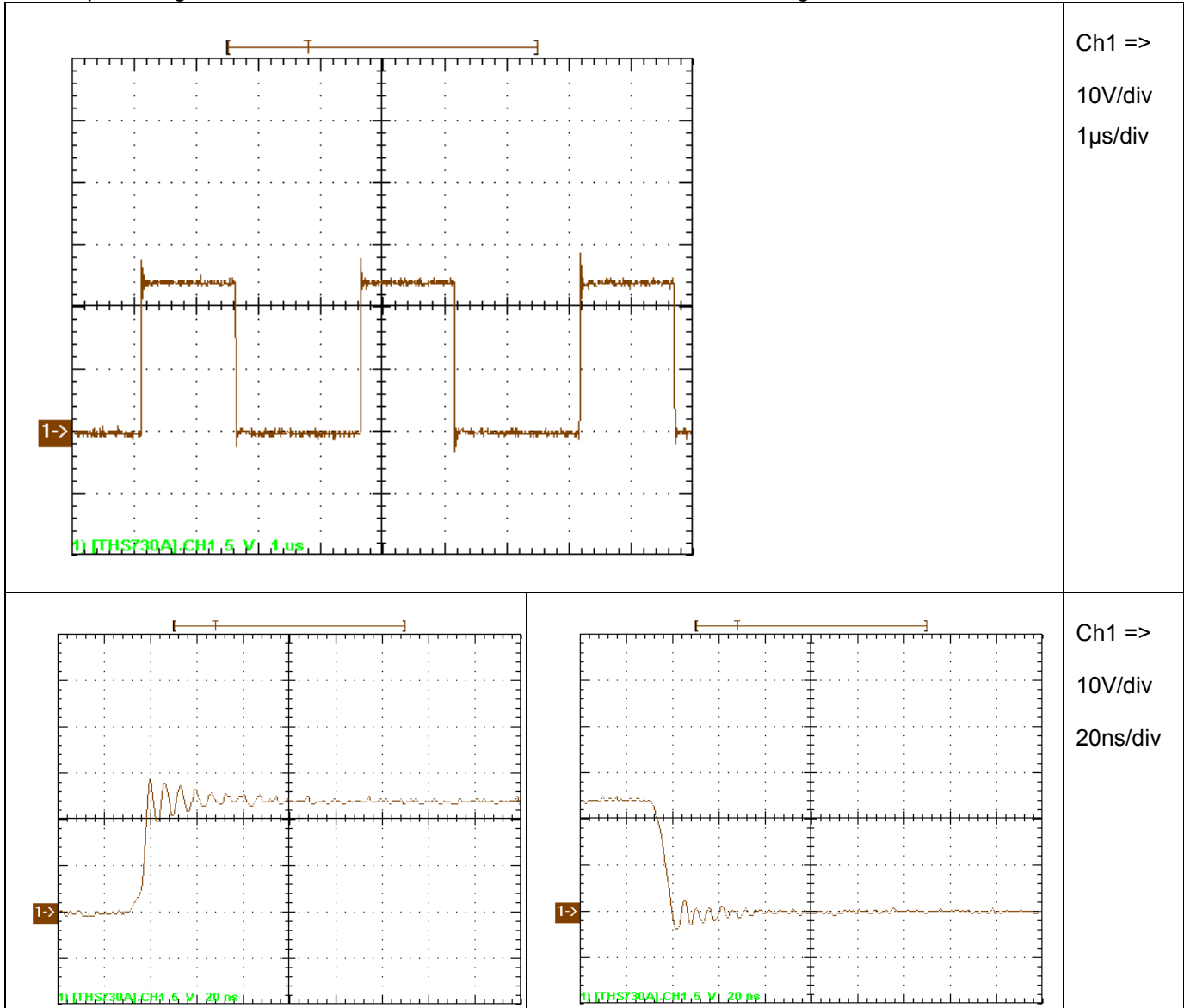
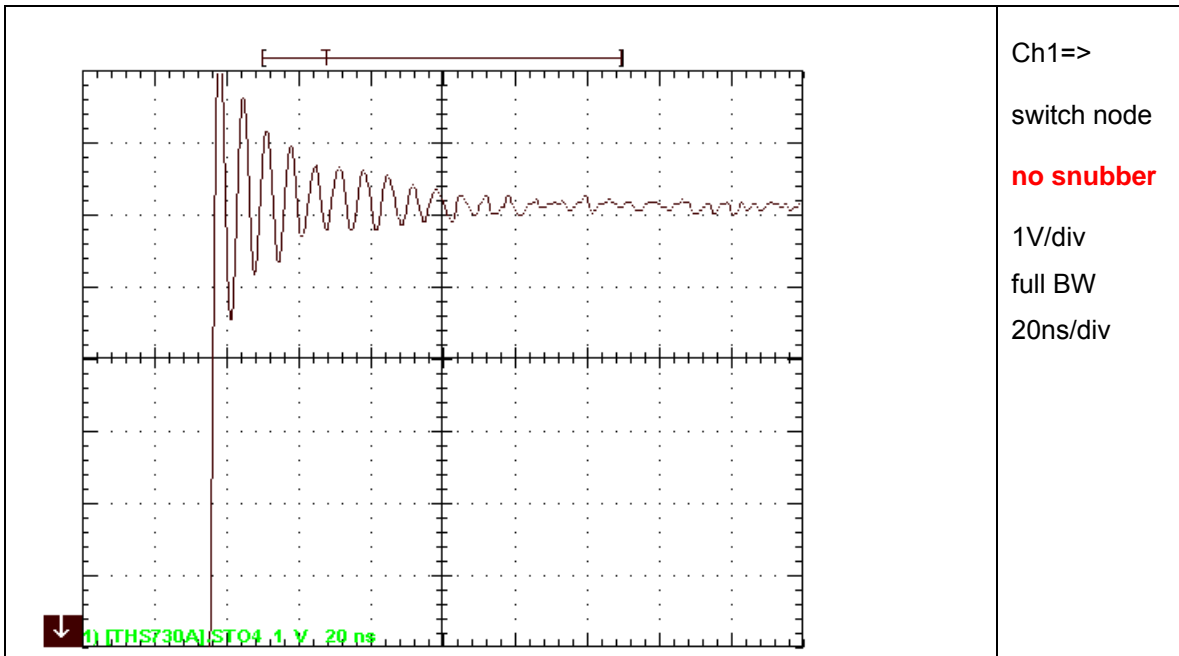


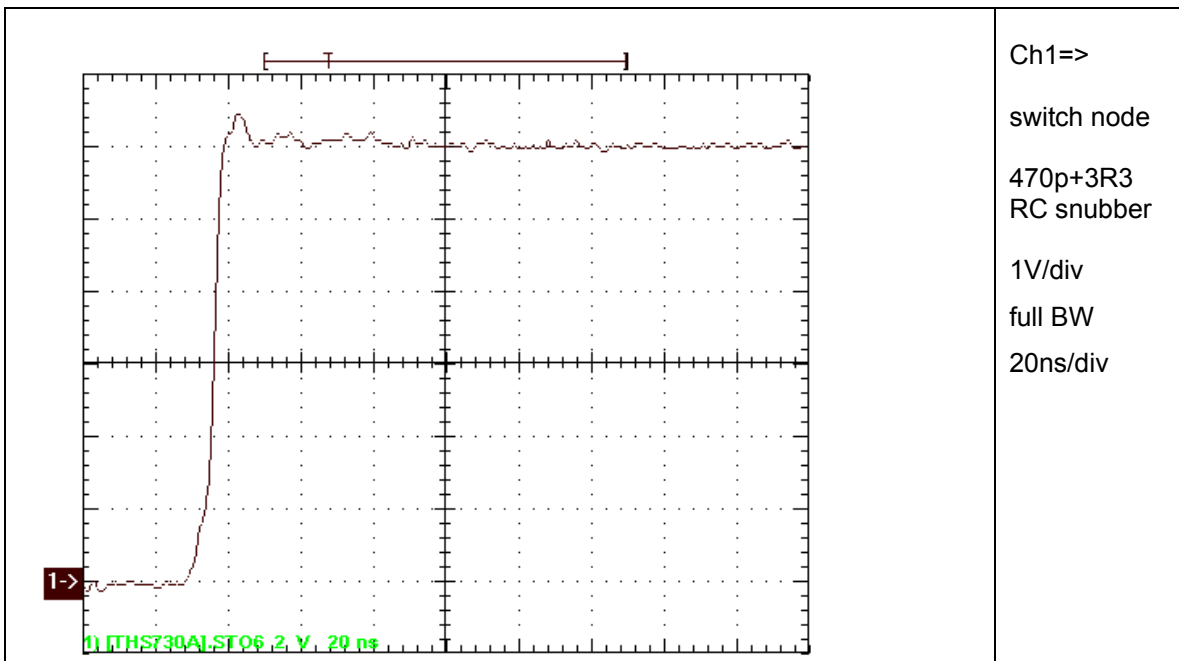
Figure 8

The overshoot of less than 3V is negligible. Maximum input voltage is 16V, Vds rating of FDC654P is -30V – enough margin. To fight the 149MHz ringing further (close to 2m band) a RC snubber circuit was implemented to demonstrate RF suppression:

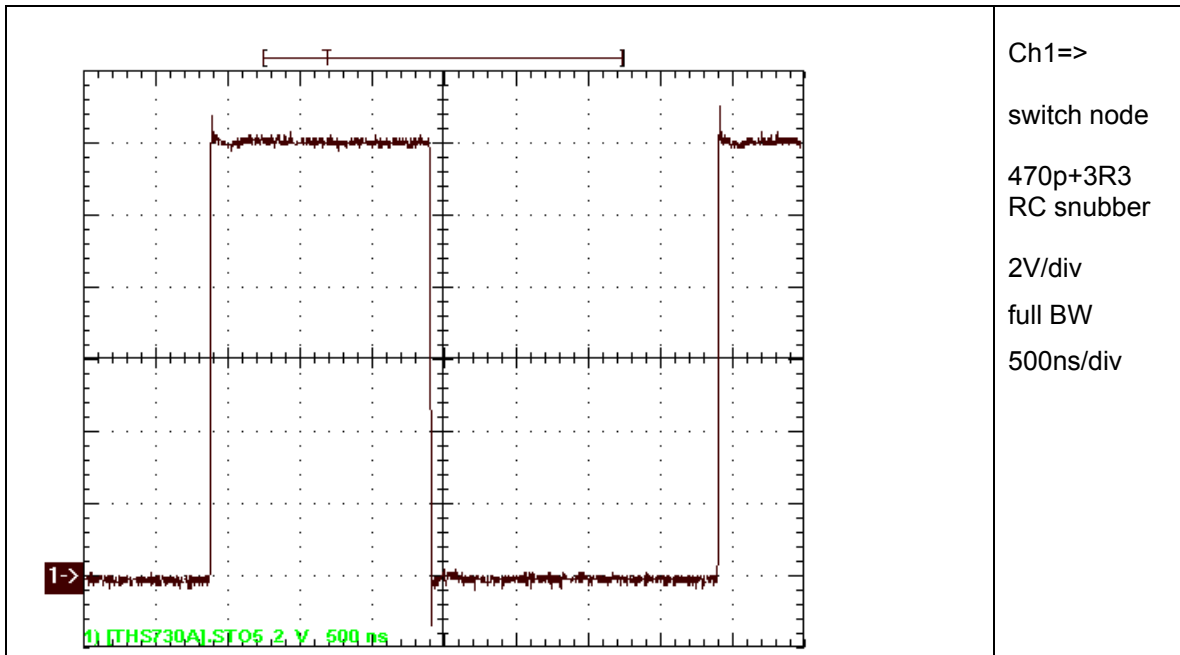
Measure ringing frequency at switch node w/ RF probe (no GND leads, use GND clip), here 148.8MHz – could cause trouble , radiated emissions:



- 1) **add capacitor from switch node to GND to achieve half of the prior frequency**, here 470pF resulted in 83MHz
- 2) **add resistor in series to achieve half of the prior overshoot**, here 3.3 Ohm reduced overshoot from 3V to 1.2V:



Clamping network 470pF / 3.3 Ohm reduces RF content at the switch node, less EMI !



It has to be stated that this hard clamping of the switch node causes a drop in efficiency of 0.5%, so roughly 25mW losses at the snubber resistor.

By experience could be said that a drop in efficiency from 0.2% to 0.5% is typically caused by adding the RC snubber circuit. For a low power design like PMP7154 geometry 0603 or 0805 might fit, but for high power designs be aware of losses up to 500mW:

- 0603 <100mW
- 0805 <150mW
- 1206 <200mW
- 1210 <250mW
- 1812 <500mW
- 2010 <750mW
- 2512 <1W

8.2 Gate-Source of MOS-FET

With input voltage set to 12V and 1A lout results in the waveform shown in Figure 8.

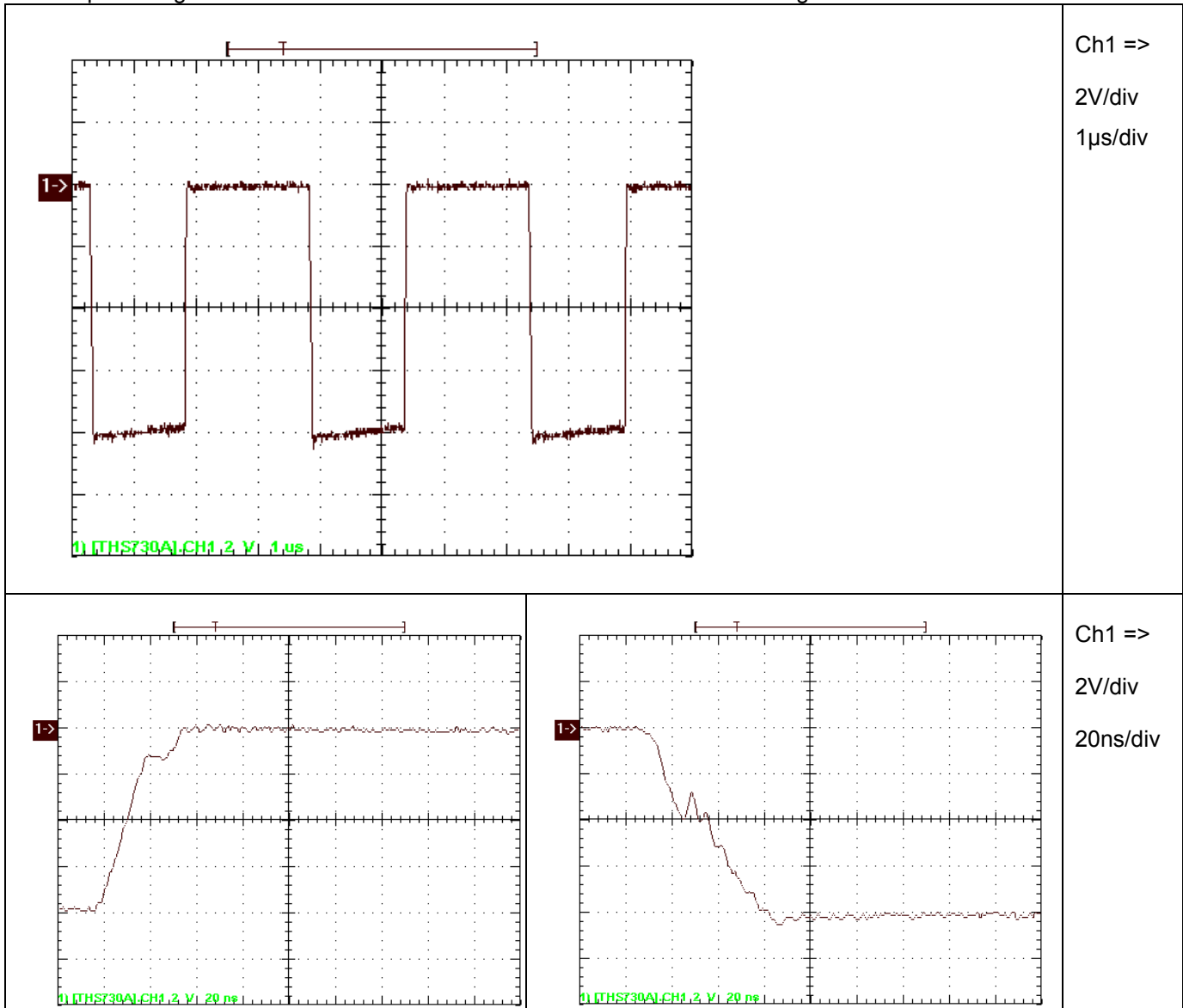
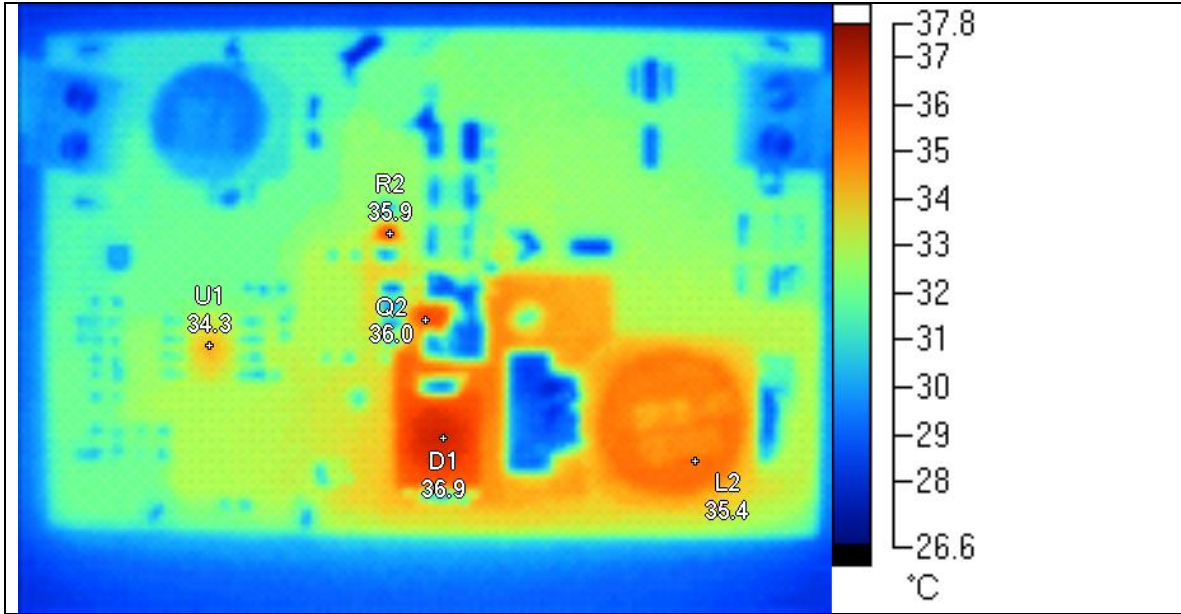


Figure 9

Right handed = SWITCH ON:

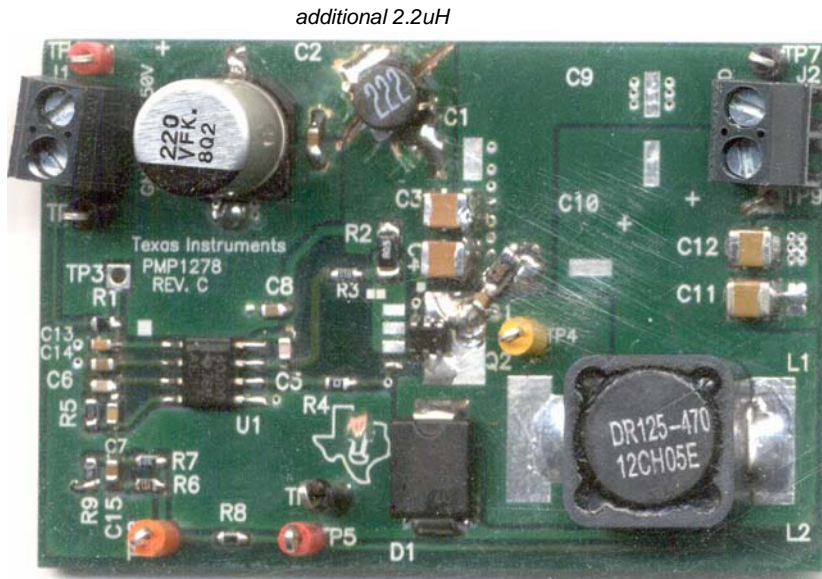
To reach the Miller plateau around 4V it needs around 20ns, switching the Miller capacitance C_{rss} from drain to source causes a drop of 1V. The 300mA driver fits only for very small FETs w/ lowest gate charge (<10nC). Passing the Miller plateau happens in less than 10ns – which could be seen at the drain-source voltage, too. Rise and fall time here around 10ns – this fast switching ensures low switching losses. Those switching losses are in the same region as the conducted losses at R_{dsON} 70milliOhm typ. So both types of losses are well balanced, the FET selection is excellent. Looking for lowest R_{dsON} only must not result in best efficiency !

Thermal image at 12V input and full load 1Amp after 1hour continuous operation [Rt = 23c]:



Name	Temperature
D1	36.9°C
Q2	36.0°C
L2	35.4°C
U1	34.3°C
R2	35.9°C

Temperature rise is below 15K, a proper design of the power stage with maximum efficiency results in relaxed thermal stress; this means higher reliability, best MTBF.



Filter inductor and RC snubber have been placed externally

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