PMP8629RevA Test Results

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Topology: Buck
Device: TPS40170 "deep impact"

The measurements are performed with VOUT≈32V (if not otherwise mentioned);
Setup w/:
HS FET = LS FET = CSD18534Q5A (10milliOhm for fast switching)
Inductor 15uH, 8.7milliOhm, 14Adc, 21Asat, WE 3013 series, # 744 363 1500

The SDM buck needs for optimum performance at 8Amps load and 16 Amp “double power pulse”:
HS = LS = 2x CSD18534 in parallel
WE 2212 series, 10uH, 3.4milliOhm, 21Adc, 26Asat, # 744 35 58 1000

Static:

- Fsw 392kHz, OK
- Max. duty PWM 31.36Vout/34.97Vin = 89.68%, OK
- ON 39.4V, OFF 34.1V OK

1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 40V, with 5A load at the output. (Power supply was switched on)

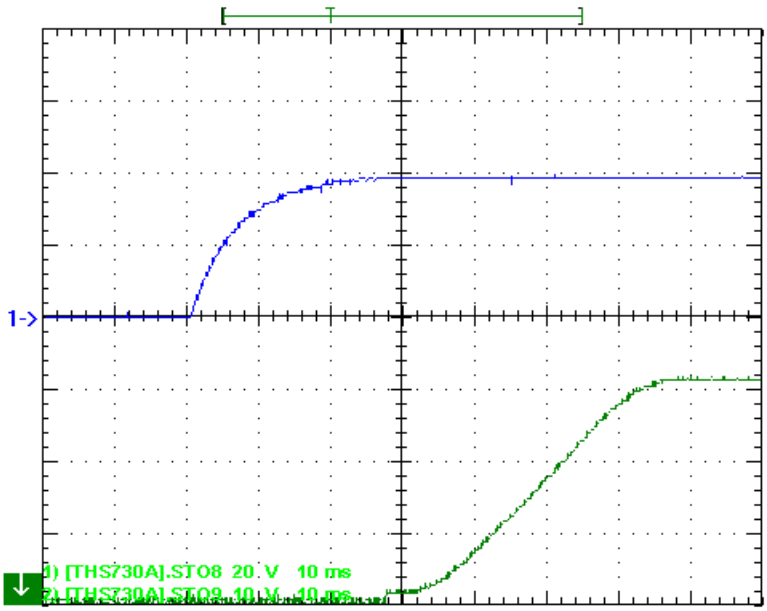


Figure 1

Ch1=> input voltage 20V/div

Ch2=> output voltage 10V/div

10ms/div

2 Shutdown

The shutdown waveform is shown in the Figure 2. The input voltage was set at 40V, with 5A load on the output. (Power supply was switched off)

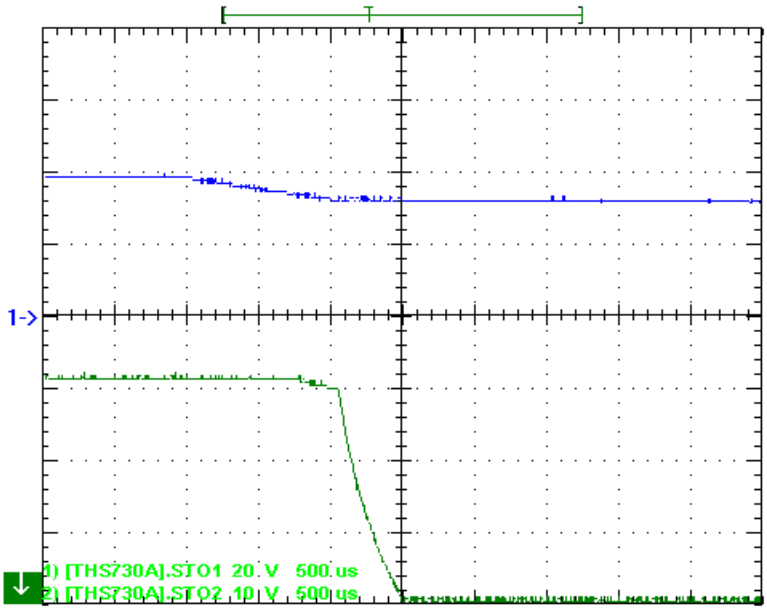


Figure 2

Ch1=> input voltage 20V/div

Ch2=> output voltage @ 10V/div

500µs/div

3 Efficiency

The efficiency is shown in the Figure 3 below. The input voltage was set to 40V;
Peak effcy at 70% load:

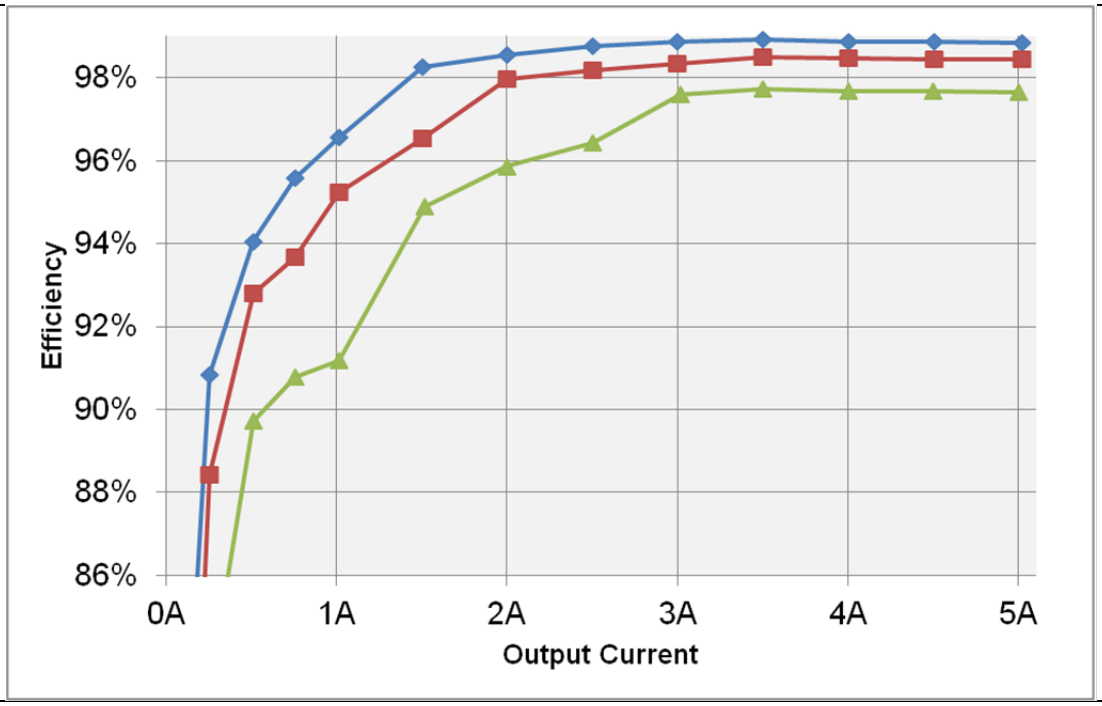


Figure 3

3.1 Measurement results

Used Equipment:
Voltage Source: GEN80-9.5
Load:6060B
Voltage Measurement:34401A
Current Measurement:MetrahitPro (Gossen)

3.1.1 VOUT 32V

VIN (V)	IIN(A)	VOUT(V)	IOUT(A)	PIN(W)	POUT(W)	Efficiency
40	0.0198	31.857	0	0.792		
40	0.0406	31.856	0.0283	1.624	0.902	55.51%
40	0.0931	31.846	0.0934	3.725	2.974	79.86%
40	0.2242	31.802	0.2562	8.969	8.148	90.84%
40	0.4348	31.754	0.5152	17.393	16.360	94.06%
40	0.6271	31.62	0.7582	25.085	23.974	95.57%
40	0.8305	31.579	1.016	33.226	32.084	96.56%
40	1.205	31.559	1.501	48.206	47.370	98.27%
40	1.6	31.522	2.001	64.003	63.076	98.55%
40	1.995	31.496	2.503	79.814	78.834	98.77%
40	2.391	31.511	3.001	95.650	94.565	98.87%
40	2.783	31.435	3.503	111.323	110.117	**98.92%**
40	3.183	31.453	4.003	127.339	125.906	98.87%
40	3.586	31.488	4.505	143.472	141.853	98.87%
40	4	31.504	5.02	160.012	158.150	**98.84%**

3.1.2 VOUT 24V

VIN (V)	IIN(A)	VOUT(V)	IOUT(A)	PIN(W)	POUT(W)	Efficiency
40	0.0207	24.046	0	0.828		
40	0.036	24.046	0.0275	1.440	0.661	45.92%
40	0.0754	24.045	0.0928	3.016	2.231	73.98%
40	0.1734	24.039	0.2551	6.936	6.132	88.41%
40	0.3324	23.976	0.5146	13.297	12.338	92.79%
40	0.4839	23.922	0.758	19.358	18.133	93.67%
40	0.6371	23.899	1.0156	25.488	24.272	95.23%
40	0.9269	23.848	1.501	37.080	35.796	96.54%
40	1.217	23.835	2.001	48.681	47.694	97.97%
40	1.516	23.798	2.502	60.649	59.543	98.18%
40	1.815	23.794	3.001	72.604	71.406	98.35%
40	2.112	23.758	3.503	84.495	83.224	**98.50%**
40	2.413	23.745	4.003	96.530	95.051	98.47%
40	2.718	23.766	4.504	108.739	107.042	98.44%
40	3.031	23.779	5.02	121.249	119.371	**98.45%**

3.1.3 VOUT 16V

VIN (V)	IIN(A)	VOUT(V)	IOUT(A)	PIN(W)	POUT(W)	Efficiency
40	0.0199	15.89	0	0.796		
40	0.0371	15.889	0.0445	1.484	0.707	47.64%
40	0.0561	15.889	0.0921	2.244	1.463	65.20%
40	0.1213	15.886	0.2544	4.853	4.041	83.28%
40	0.2268	15.854	0.5135	9.073	8.141	89.73%
40	0.3295	15.816	0.7566	13.181	11.966	90.78%
40	0.4395	15.807	1.0141	17.581	16.030	91.18%
40	0.6295	15.773	1.515	25.185	23.896	94.88%
40	0.8222	15.766	2	32.893	31.532	95.86%
40	1.0206	15.741	2.501	40.827	39.368	96.43%
40	1.216	15.739	3.017	48.649	47.485	97.61%
40	1.407	15.713	3.501	56.287	55.011	**97.73%**
40	1.608	15.705	4.001	64.323	62.836	97.69%
40	1.811	15.718	4.502	72.453	70.762	97.67%
40	2.014	15.726	5.003	80.568	78.677	**97.65%**

4 Load Regulation

The load regulation of the output is shown in the Figure 4, Figure 5 and Figure 6 below. The input voltage was set to 40V.

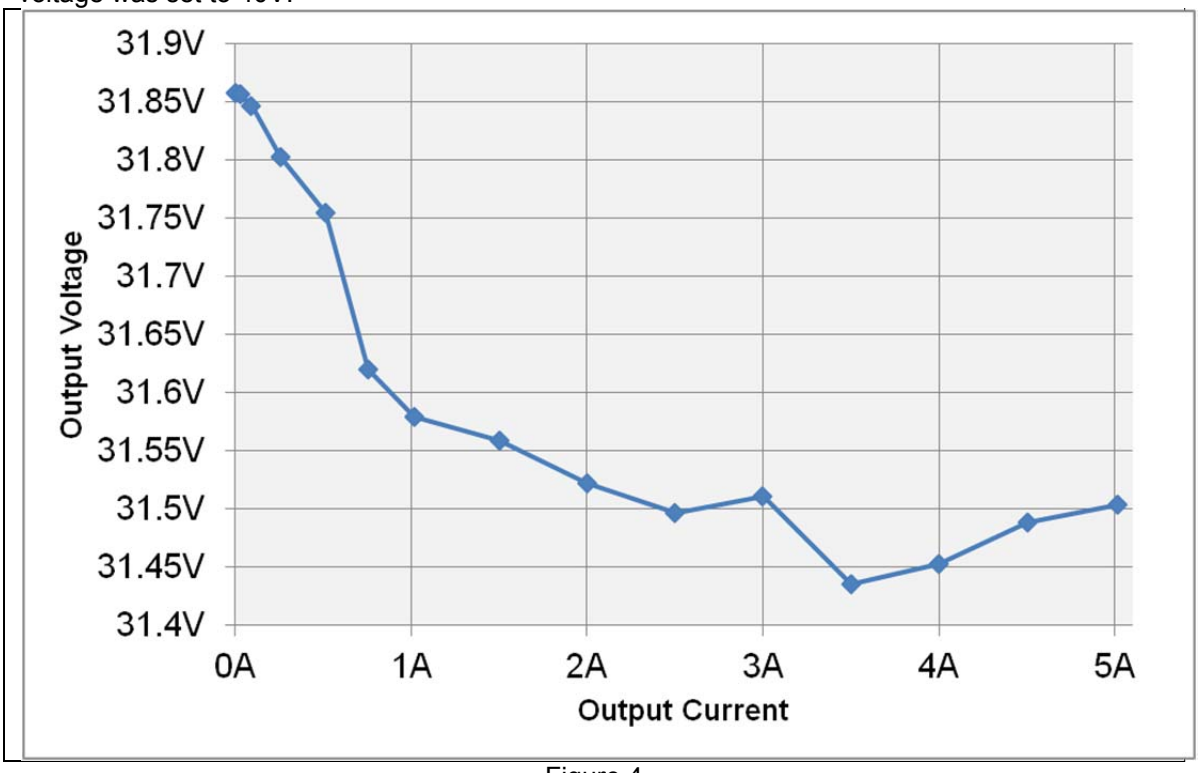


Figure 4

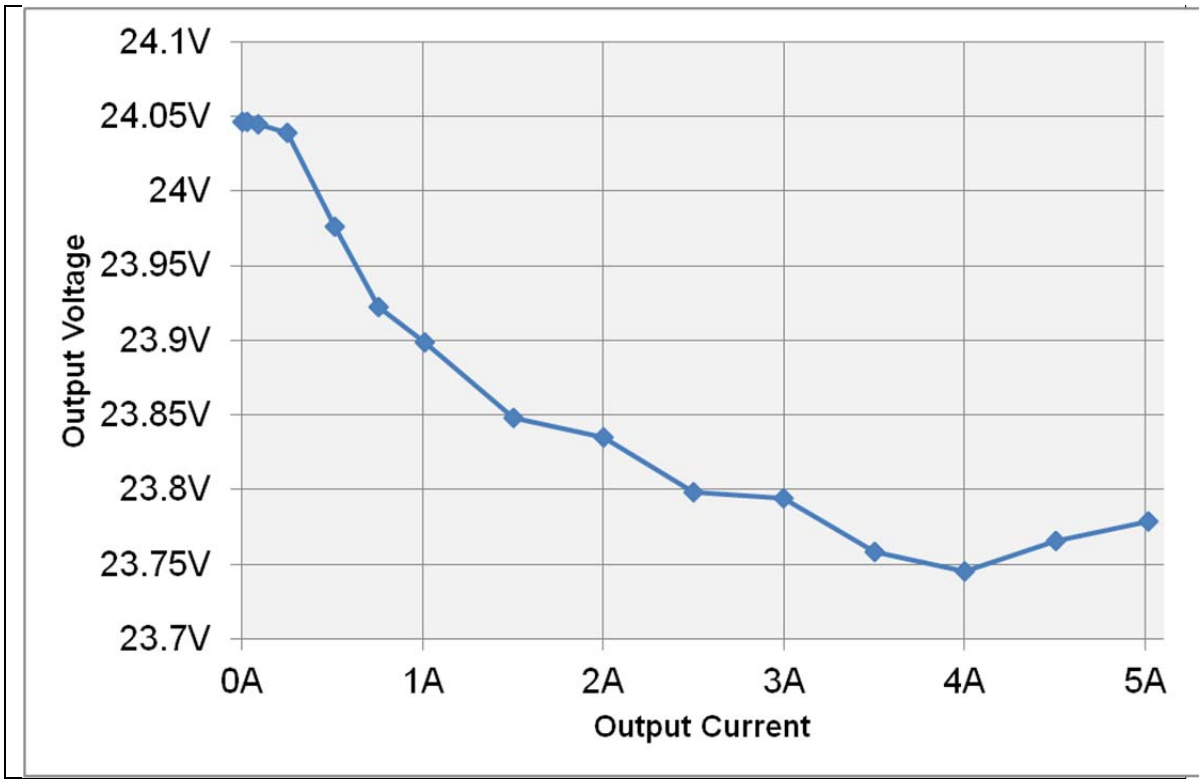


Figure 5

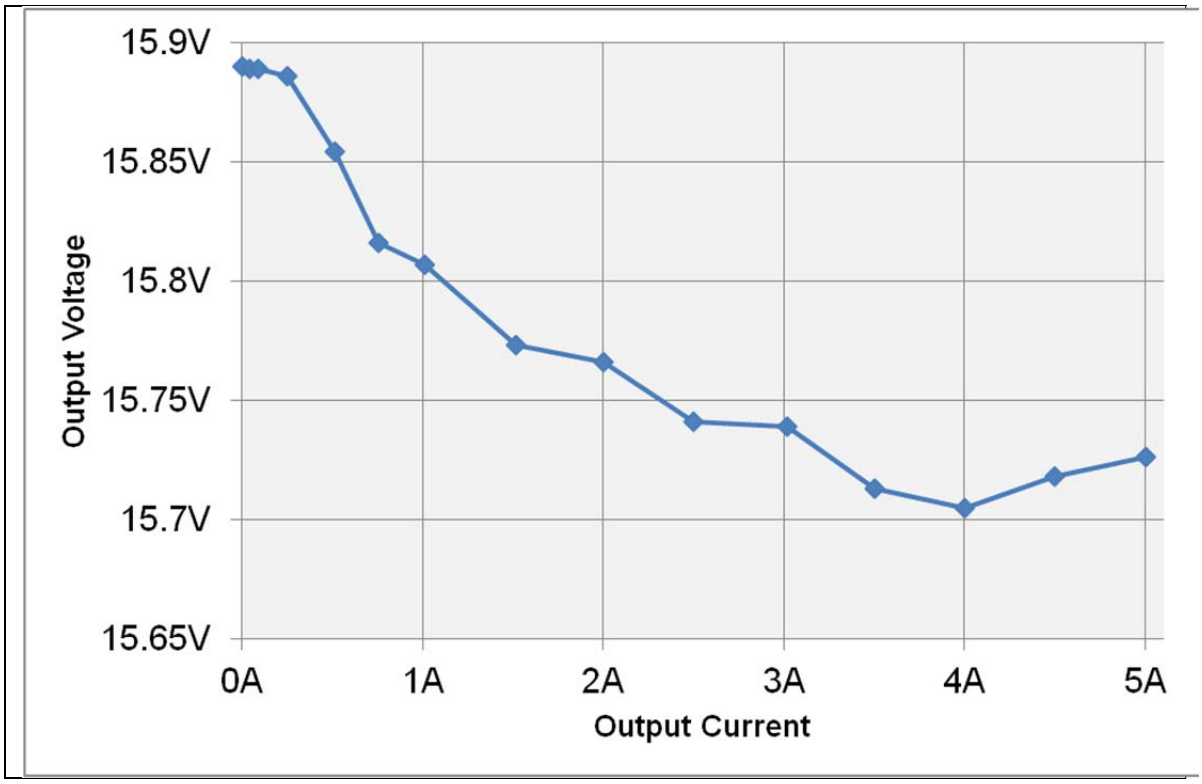


Figure 6

5 Ripple Voltage

The output ripple voltage is shown in Figure 7. The image was taken with a 5A load 40V at the input; due to MLCC only at the output du around 20mVpp, so less than 0.1%, fine for RF apps:

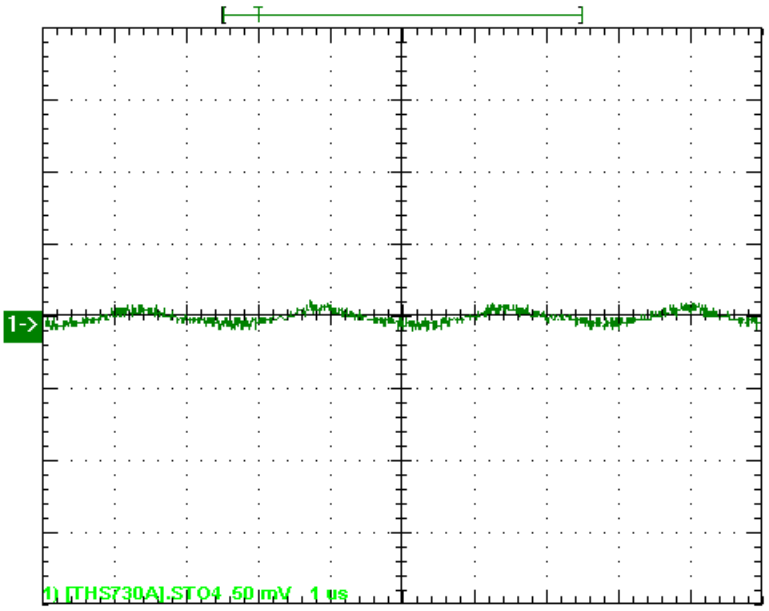


Figure 7

Ch1 => output voltage @ 40V input

50mV/div
AC coupled

20MHz bandwidth setting

1µs/div

The input ripple voltage is shown in Figure 8. The image was taken with a 5A load 40V at the input.

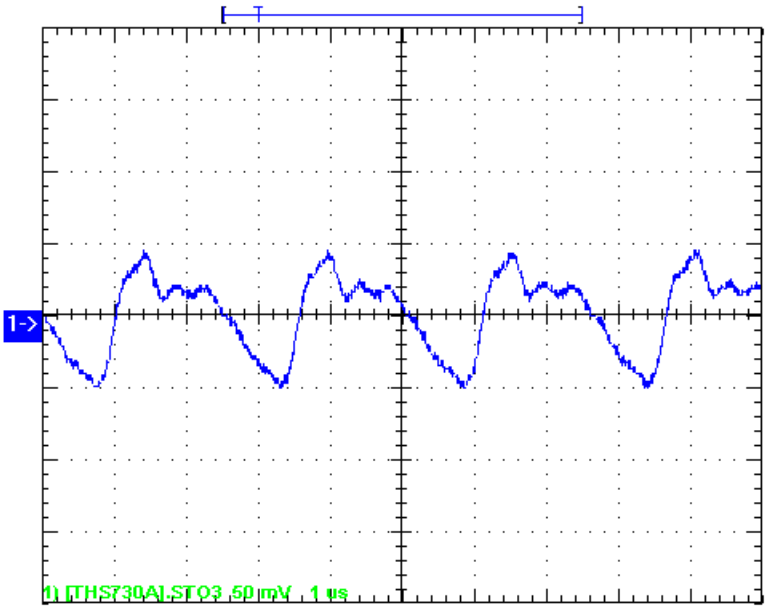


Figure 8

Ch1 => output voltage @ 40V input

50mV/div
AC coupled

20MHz bandwidth setting

1µs/div

6 Control Loop Frequency Response

Figure 9 shows the loop response with 5A load and 40V input.
Typically crossover frequency Fco is placed to 1/10 of switching frequency, so around 40kHz.
Increased bandwith a bit to get best transient response, here around 60kHz – phase margin PM still >60 degrees, gain margin GM less than -10dB:

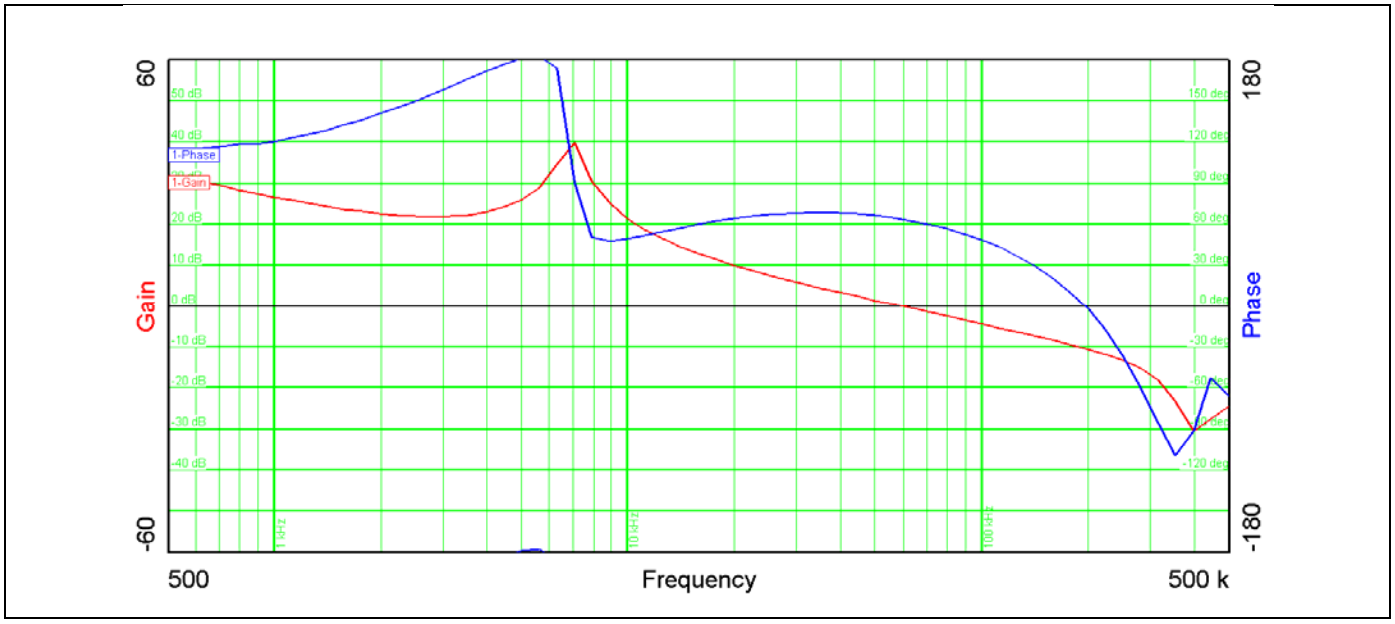


Figure 9

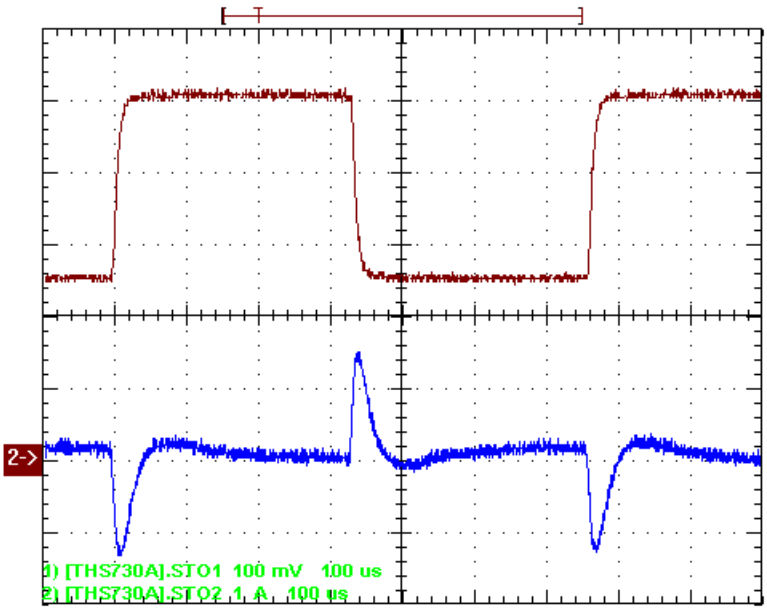
Table 1 summarizes the results from Figure 9

Bandwidth (kHz)	**59.4**
Phasemargin	**63.6°**
slope (20dB/decade)	-0.982
gain margin (dB)	**-10.4**
slope (20dB/decade)	-1.12
freq (kHz)	195

Table 1

7 Load Transients

The Figure 10 shows the response to load transients. The load is switching from 2.5A to 5A. The input voltage was set to 40V; voltage variation du is 150mVpk, so roughly 0.5% of Vout by an output capacitance of 10x 10uF MLCC, effective output capacitance 70uF w/ DC bias 32V:



Ch2 => output voltage 100mV/div

20MHz bandwidth setting

Ch1 => output current 1A/div

100µs/div

Figure 10

8 Miscellaneous Waveforms

8.1 Switch node (Low Side FET || D2)

With input voltage set to 40V and 5A Iout results in the waveform shown in Figure 11

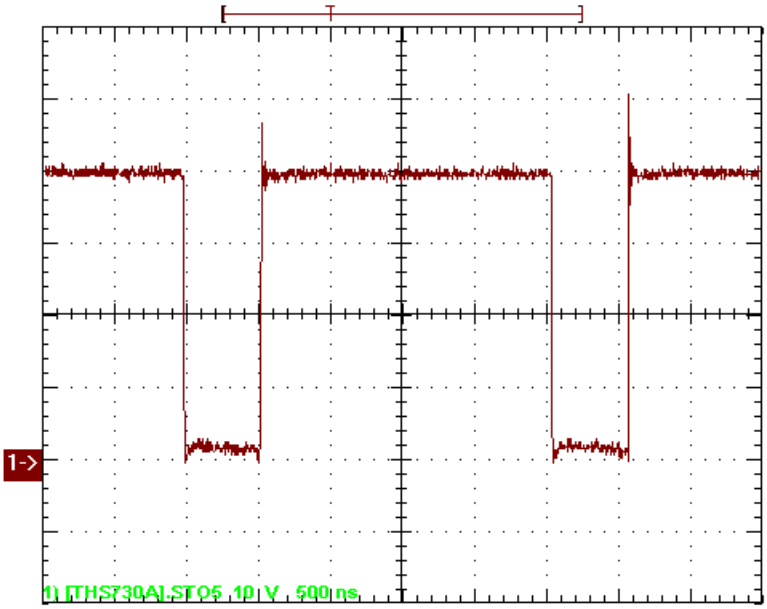
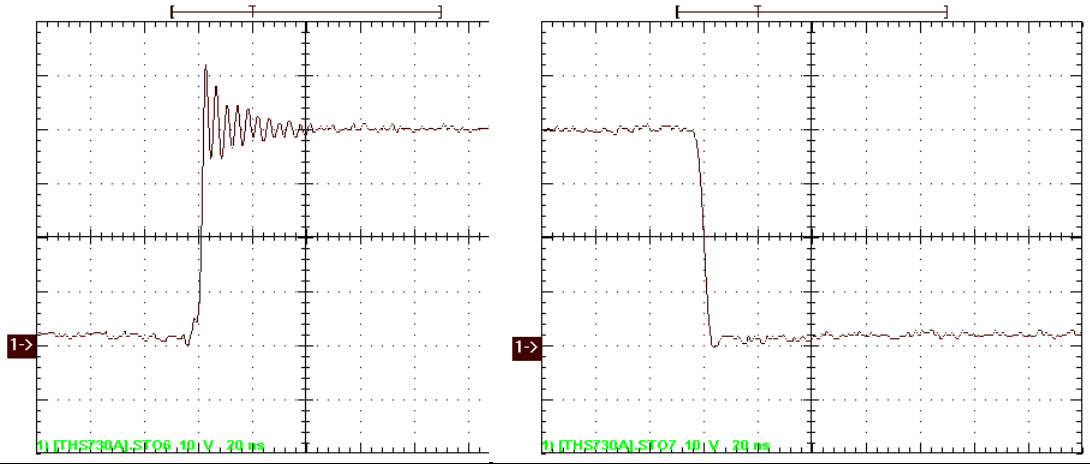
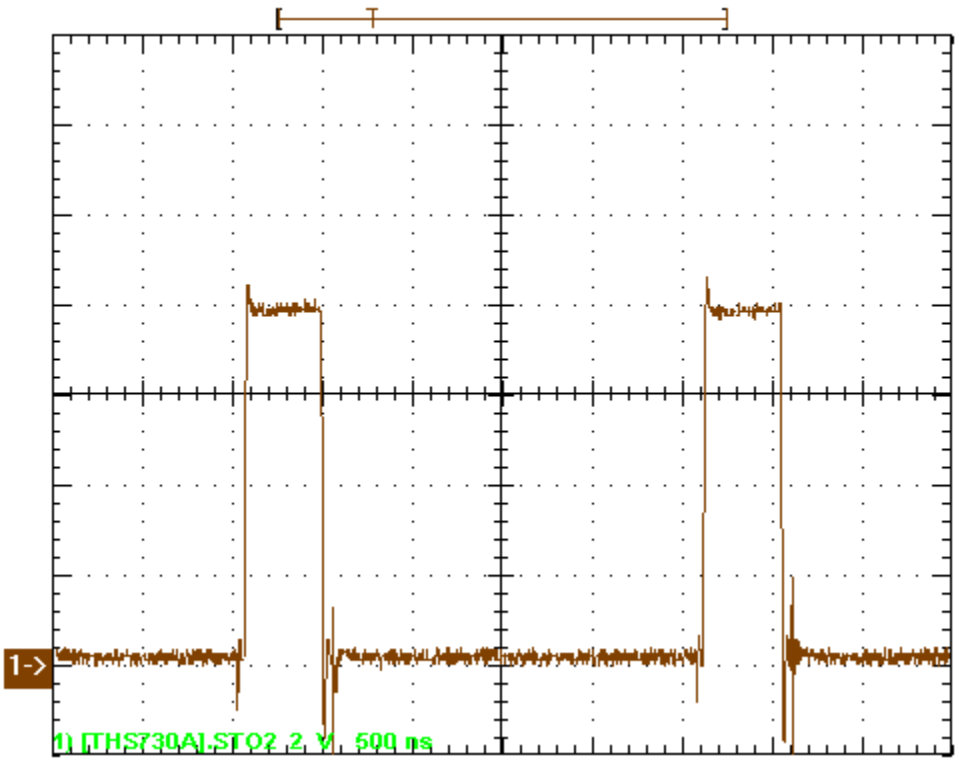
	Ch1 => 10V/div 500ns/div
	Ch1 => 10V/div 20ns/div

Figure 11

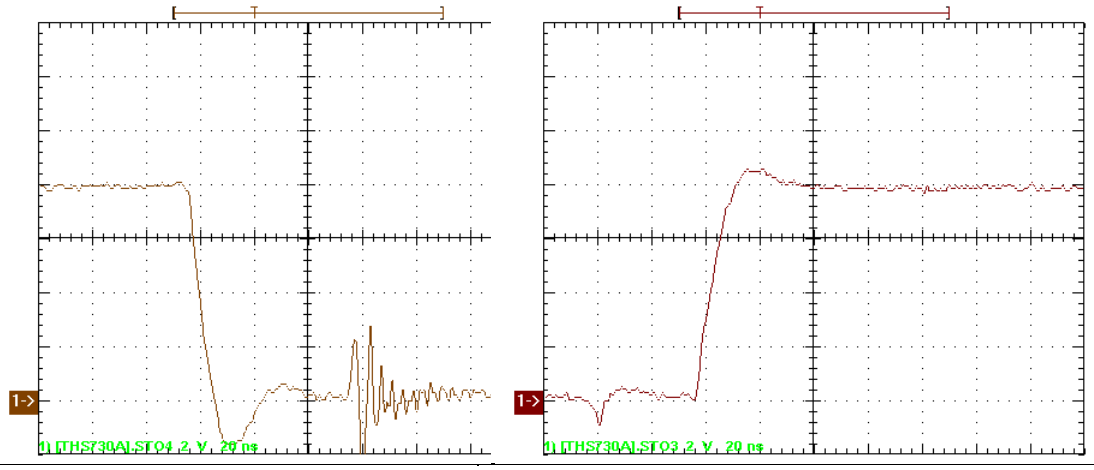
8.2 Gate of Low side MOS-FET

With input voltage set to 40V and 5A Iout results in the waveform shown in Figure 11.



Ch1 =>
2V/div

500ns/div



Ch1 =>
2V/div
20ns/div

Figure 12

8.3 Hi Side MOS FET

The waveform of the active clamp transistor is shown in **Figure 13**.(the same setup as above)

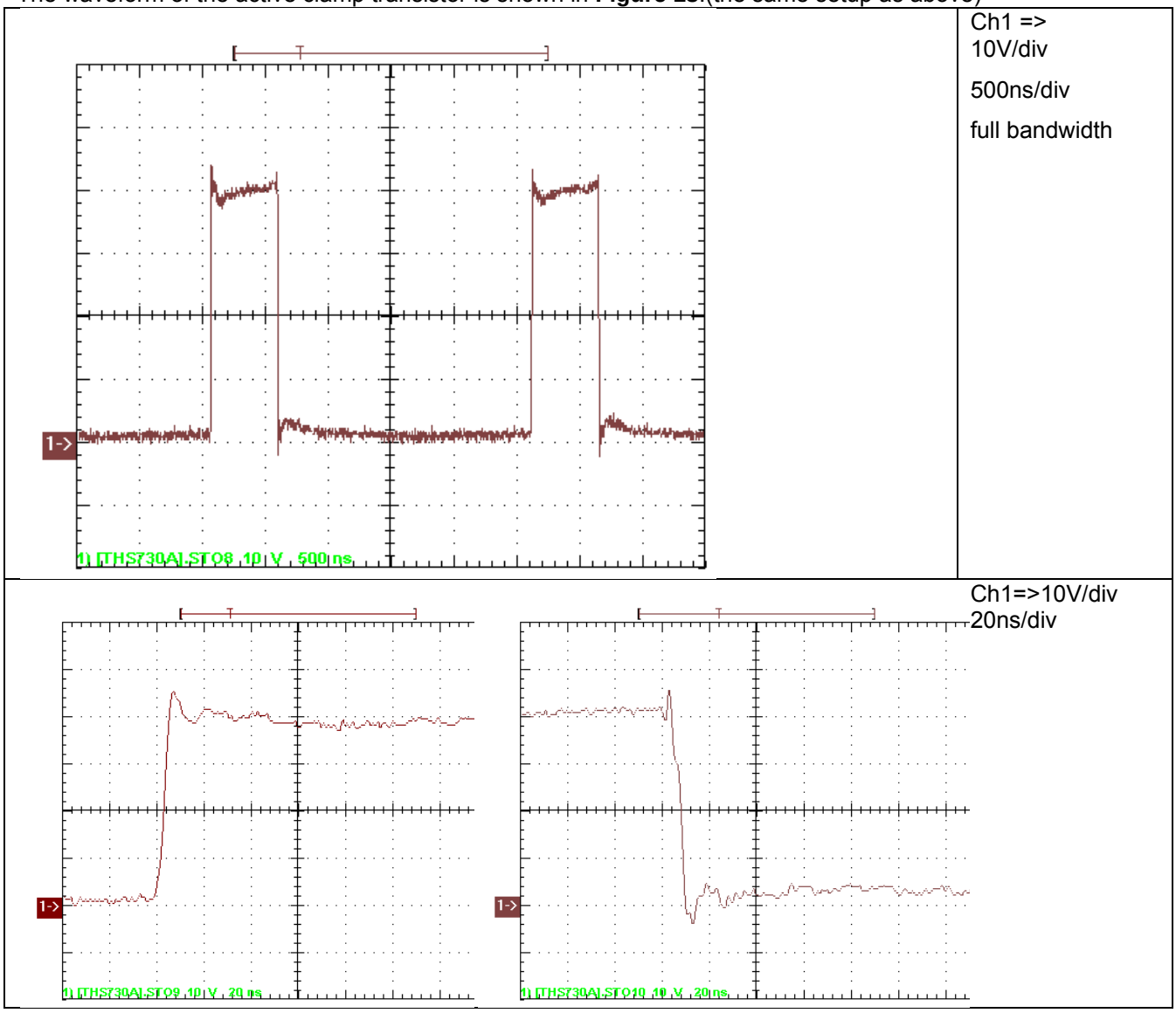
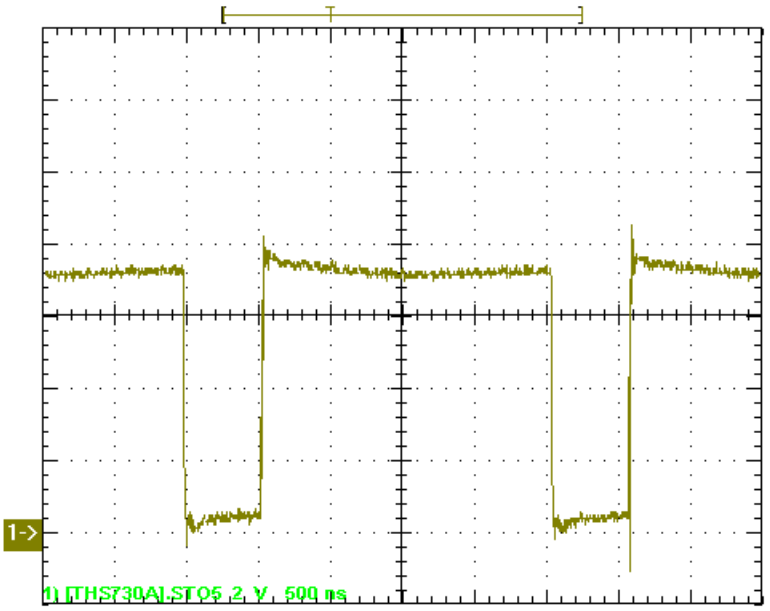


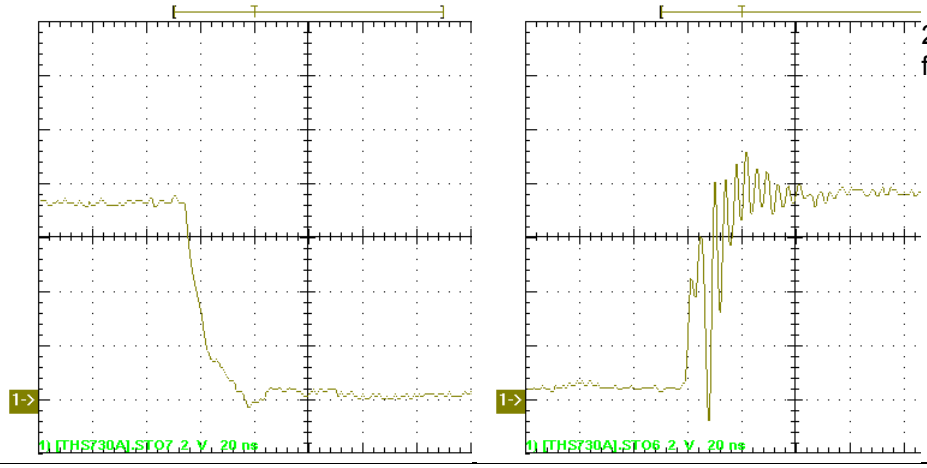
Figure 13

8.4 Hi Side MOS FET Gate

The waveform of the active clamp transistor is shown in Figure 14.



Ch1=>2V/div
500ns/div
full bandwidth



Ch1=>2V/div
20ns/div
full bandwidth

Figure 14

9 Thermal Image

Figure 15 shows the thermal image at 40V input and 5A output VOUT 32V, 160W output power:

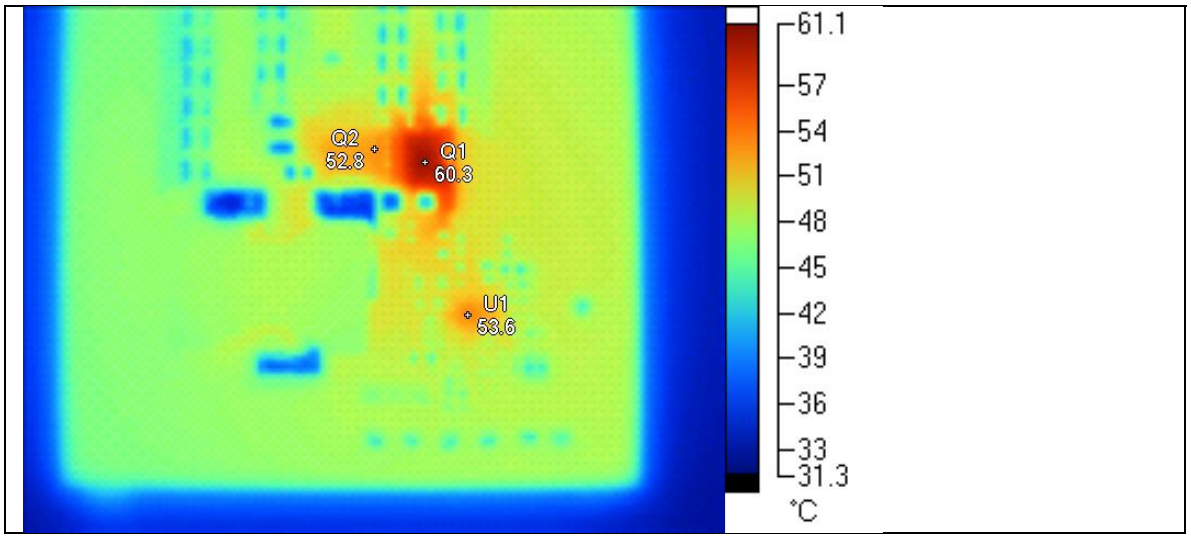


Figure 15

Name	Temperature
Q1	60.3°C
U1	53.6°C
Q2	52.8°C

Table 2, 80% duty cycle

Figure 16 shows the thermal image at 40V input and 5A output VOUT 24V, 120W output power:

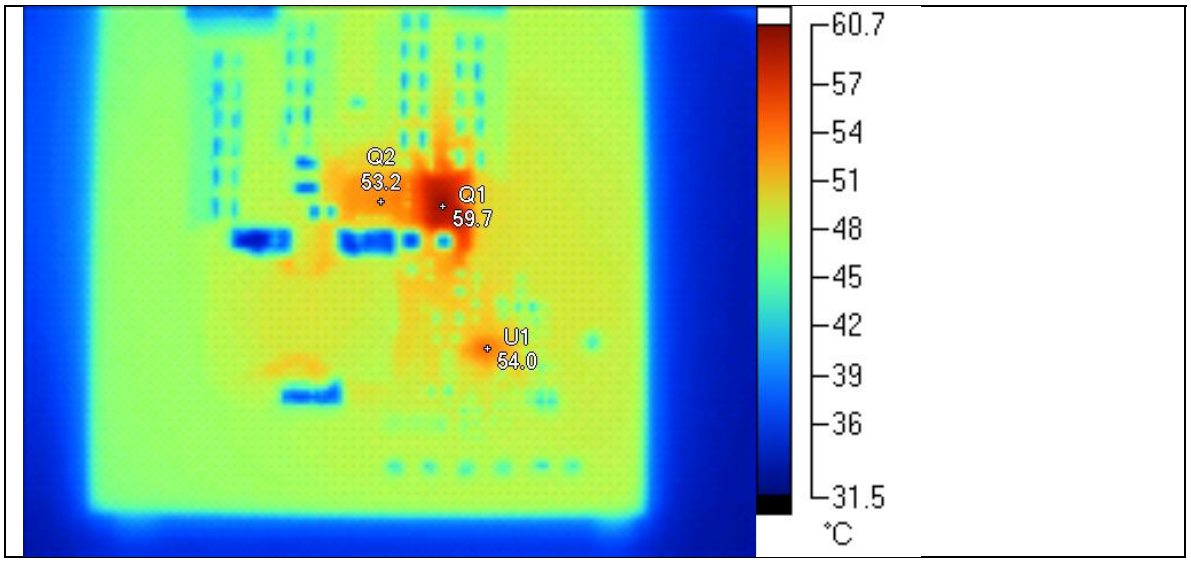


Figure 16

Name	Temperature
Q1	59.7°C
U1	54.0°C
Q2	53.2°C

Table 3, 60% duty cycle

Figure 15 shows the thermal image at 40V input and 5A output VOUT 16V, 80W output power:

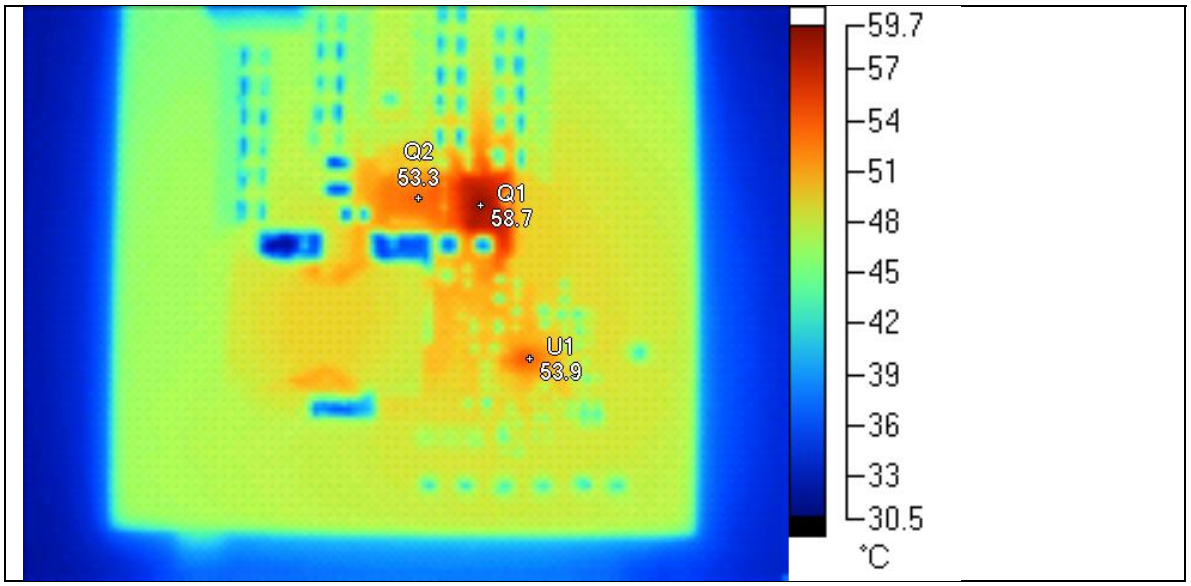


Figure 17

Name	Temperature
Q1	58.7°C
U1	53.9°C
Q2	53.3°C

Table 4, 40% duty cycle

Outstanding performance by the TI nexFETs chopping 40V input at switching frequency 400kHz !

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