TI Designs

Differential Pulse Train Output (PTO) Programmable Logic Controller (PLC) Module Reference Design

Description

The differential pulse train output (PTO) module TI Design illustrates the design of a differential high speed digital output module using RS-485 driver powered from the programmable logic controller (PLC) backplane using isolated fly-buck power converter. This TI Design is mainly used in positioning and motion control systems to allow simple distant high-speed motor control in noisy environments.

Resources

TIDA-00766	Design Folder
SN65LBC174A	Product Folder
TPS55010	Product Folder
ISO7140CC	Product Folder
TIDEP0027	Tools Folder
TIDA-00319	Tools Folder

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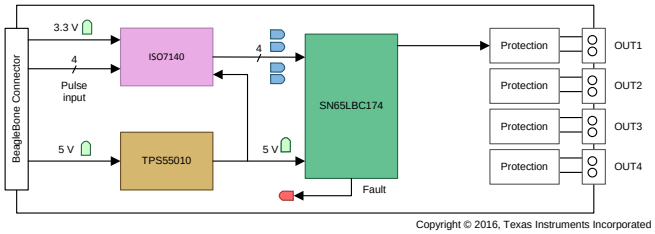
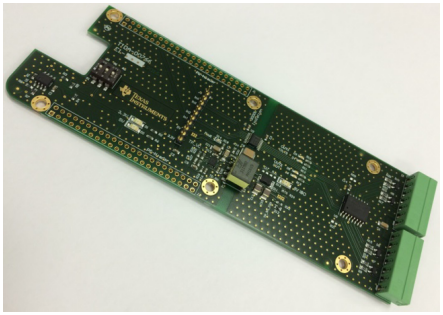
Features

- Four High-Speed Differential Digital Output Channels
- 1-MHz Pulse Frequency
- 25-mA Maximum Load Current Per Channel For 100-Ω Load
- 750-mW Total Power Consumption From Backplane Isolated Power Stage (150 mA)
- Parallel Control for Simple Microcontroller (MCU) Interface
- BeagleBone Black Cape Form Factor For Easy Evaluation Using TIDEP0027

Applications

- Factory Automation and Process Control
- Programmable Logic Controllers (PLC)
- Position Controller
- Servo Motor and Stepper Motor Driver





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1 System Overview

1.1 System Description

1.1.1 Introduction

The PLC digital outputs can be classified into low-speed outputs and high-speed outputs. High-speed outputs like Pulse Width Modulated (PWM) signals or PTO signals are mainly used in position controllers.

Each motor (constituting an axis of motion) is controlled through two signals, which typically represents speed and direction or equivalent quantities. PLC output module cards are available from one axis up to three axes required in 3D positioning.

Figure 1 and Figure 2 show a single axis position control PLC system in open loop scheme used for stepper motors and closed loop scheme used for servomotors. In both schemes, high-speed pulse train output module is used to run the motor driver with constant duty cycle variable frequency signal.

PTO signals might be speed and direction (forward, reverse) or speed in clockwise or counterclockwise directions.

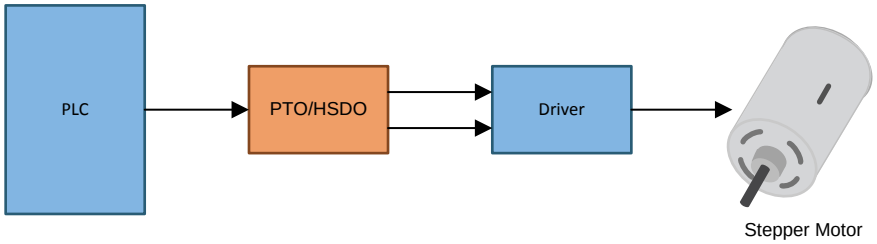

Figure 1. Open Loop Positioning Control

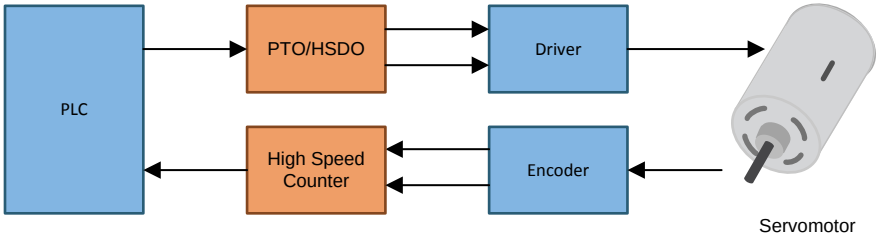

Figure 2. Closed Loop Positioning Control

1.1.2 Description

The PTO module core is a differential line driver. A voltage supply of 5 V is anticipated for this line driver. A digital isolator is required to connect the four digital pulse outputs from BeagleBone Black (BBB) programmable realtime unit (PRU) outputs or external inputs to the line driver input. For compatibility with BBB, 3.3 V is used as primary side isolator voltage while 5 V is chosen for the secondary side to simplify the power stage. The isolated power stage is used to provide the 5 V to the isolated side. The main power is driven from the 5-V pins of the BBB SYS_5V. The outputs are protected against surge and electro static discharge (ESD). Backplane power is preferred here due to low power requirements. Figure 3 shows conceptual block diagram of the target system.

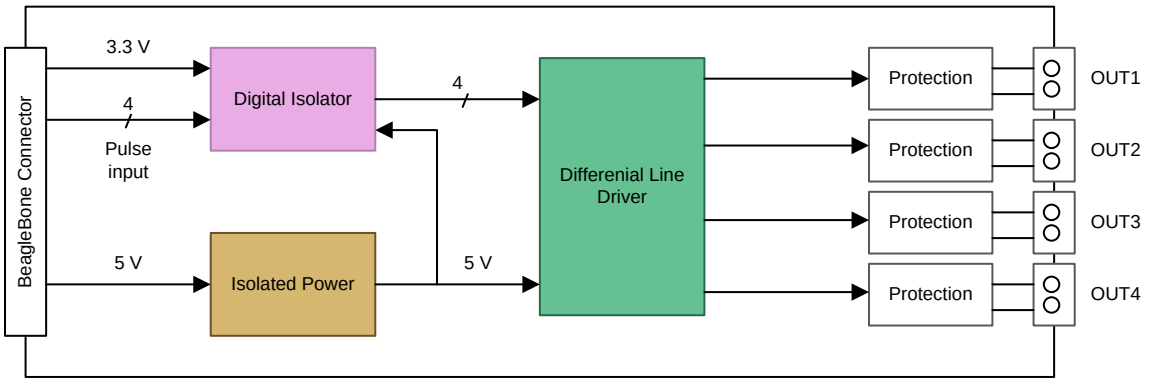

Figure 3. Four-Channel Differential PTO Module Block Diagram

1.2 Key System Specifications

Table 1 lists the target specifications for the PTO module. For this design, the differential output is targeted as it features higher speed and higher noise immunity. Please refer to the TIDA-00913 for counterpart single ended output implementation. To enable the module to work with the TIDEP0027, the design is made in BBB cape format.

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
Number of outputs	2 Channels (axes) , 4 differential outputs
Load type	ohmic, opto-coupler, differential inputs for step or servo amplifier
Load voltage	5-V internal
Rated output current	25-mA rated, 42-mA maximum over temperature range
Output signaling	RS485-compliant
Load impedance	100-Ω rated, 50-Ω minimum
Frequency	100 Hz to 1 MHz
Input duty cycle (mark/space ratio)	50% typical
Electrical Isolation	2 kV
Power source	5-V backplane power
Power consumption	1-W maximum
Temperature range	0 to 65 A°C
EMC protection	ESD: 12-kV IEC Contact: 15-kV HBM EFT: 4 kV Surge: 1 kV

1.3 Block Diagram

Figure 4 reflects the component selected Section 2 as well as the signage LED components added to monitor the availability of different power levels and input signals.

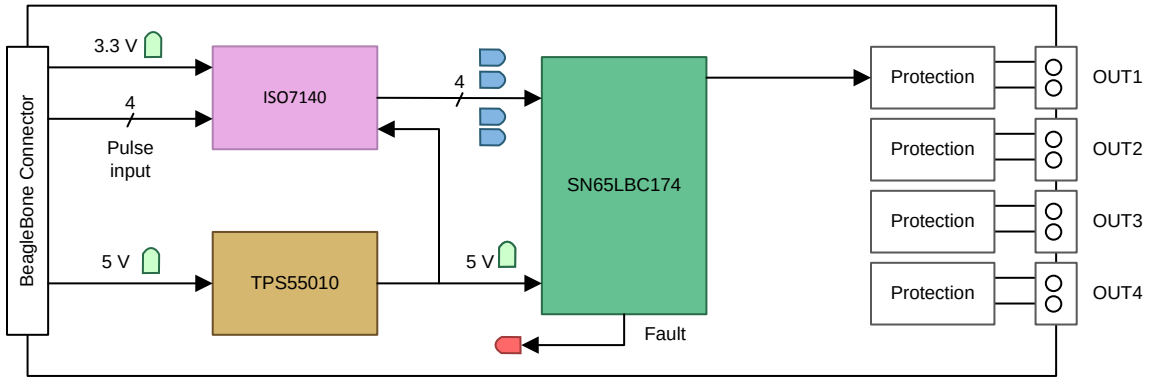

Figure 4. TIDA-00766 Block Diagram

2 Component Selection

2.1 Driver Selection

Selecting a suitable differential signaling scheme for 1 MHz is essential for this TI Design. Low-power, high-speed differential signaling that can drive a load over >10-m cable is required, thus, large common mode range is needed.

The RS-485 is one of the best and most versatile interfaces used for differential signaling in industrial environment. RS-485 signaling is used for multiple industrial standard interfaces including: ProfiBus, ModBus, Interbus, BACnet, CompoNet, and EnDat.

This popularity of RS-485 is due to several features including:

- Differential balanced interface less susceptible to noise
- Multipoint operation from single 5- or 3.3-V supply
- 7- to 12-V bus common mode range
- Ability to communicate over long distances (up to 1200 m)
- Fast communication rates (up to 50 Mbps)
- High receiver input resistance of 12 kΩ and high sensitivity of ±200 mV

Figure 5 shows the optimum range of signaling rate and the cable length where RS-485 is preferred.

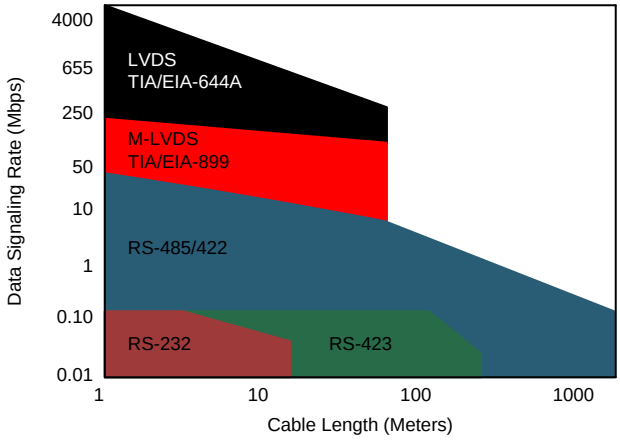

Figure 5. Comparison Between Common Differential Signaling Standards

For the TIDA-00766 target frequency of 1 MHz and cable length in the range of 10 to 100 m, the RS-485 seems to be the best fit. TI offers a wide range of RS-485 transmitters.

Taking the 5-V supply and four transmitter requirements into account, using the parametric search at least 13 products from TI that fulfills those criteria. The SN65LBC174A is one of the suitable drivers that can run up to 30 Mbps and features both low cost and low power.

2.2 Isolated Power

Isolated 5-V input to 5-V output power stage can be realized in multiple ways. Fly-buck architecture is used for simplicity due to low power requirement. The TPS55010 is an isolated DC-DC converter with output power up to 2 W. The TPS55010 is high efficiency with good regulation accuracy with primary side feedback that provides excellent line and load regulation. Using off-the-shelf transformer, this device can easily achieve 200 mA at 5-V output from 5-V input.

2.3 Digital Isolator

Digital isolator is selected based on the number of channels, direction, speed, power input and output levels, and isolation level requirement.

ISO7140 is selected as a four-channel digital isolator. The ISO714x family provides galvanic isolation at 2500 VRMS for 1 minute per UL or 4242 VPK per VDE. The selected isolators support up to 50 Mbps, which is well above the communication speed used in the design

3 Getting Started Hardware

3.1 Hardware

3.1.1 SN65LBC174 Driver

The SN65LBC174A is a quadruple differential line driver with 3-state outputs designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 applications. This device is optimized for balanced multipoint bus transmission at signaling rates up to 30 million bits per second with propagation delay less than 11 ns. Each driver features current limiting and thermal-shutdown circuitry making it suitable for high-speed multipoint applications in noisy environments. These devices are designed using LinBiCMOS, facilitating low power consumption and robustness. The SN65LBC174A is characterized for operation over the temperature range of –40°C to 85°C. The device can accept common mode range of -7 to 12 V. inputs can accept voltages in the range of -0.5 to Vcc+0.5 V. Supply voltage range is a bit tight (4.75 to 5.25 V) which means a stable power supply is required. Outputs are able to drive ±60-mA maximum current.

Output common mode is 2.4 V and differential output swing is 1.6-V single ended, that is, 3.2-V differential. Constant voltage swing means output current is a function of load or termination. In order to keep the total load current below 100 mA for all four channels, an output load of 120 Ω is selected. This load leads to 26-mA output current per channel at 25°C minimum load per channel is 50 Ω, which results in 60 mA.

Two series thick film 10-Ω resistors are placed at the differential outputs to help protect against short circuit and surges as well as improve signal integrity. These series resistors should be added to the termination or load resistors when calculating the output current.

Figure 6 shows the driver schematics including the output protection circuit for two outputs.

Device power consumption with no load is 38-mA typical, which means the whole driver requires less than 150 mA from the 5-V power supply (25 mA per channel for four channels plus 38 mA).

Enable signals are not used. The device is always enabled. Two resistors (R21 and R29) can be used for optional disable.

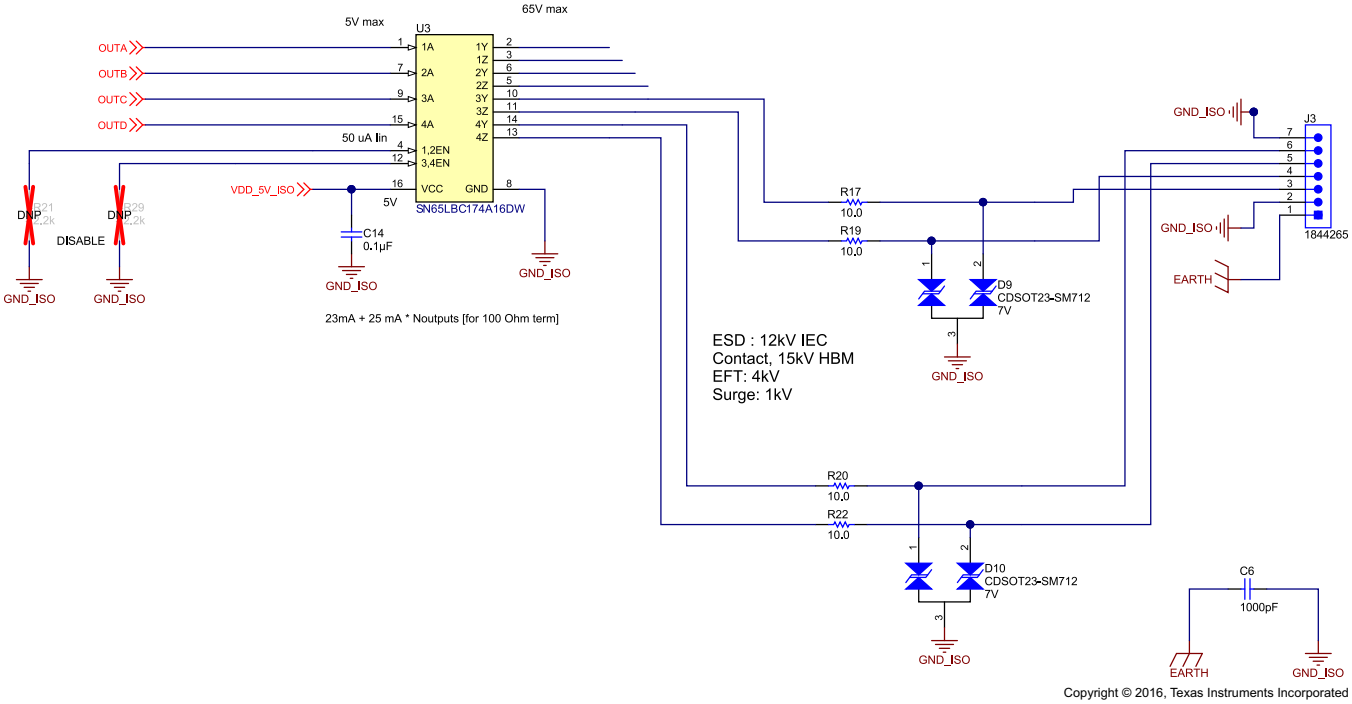

Figure 6. Figure 6: Driver Schematics for Two Outputs

3.1.2 Transient Protection

Industrial signal communication, like in the TIDA-00766, must operate reliably in harsh environments. Electrical over-stress transients caused by electrostatic discharge, switching of inductive loads, or lightning strikes will corrupt data transmission and damage bus transceivers unless effective measures are taken to diminish transient impact. Discussion here is limited to protecting the transmitter SN65LBC174A from permanent damage. The SN65LBC174A transmitter is able to withstand direct voltage on the bus in the range (-10 to 15 V). A parallel 7-V TVS diode with a series 10-Ω thick film resistor is used as a simple yet effective protection for RS-485 differential lines. The CDSOT23-SM712 has two diodes in a signal package, which protects the line pair and reduces the required board area.

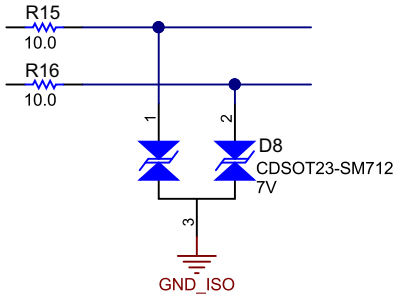

Figure 7. Output Protection Circuit

3.1.3 Data Isolation

In the case of signal transmission over long links or between equipments which have different power supply systems or within noisy environment including switches and motors different ground potential at different nodes can cause ground currents to flow through the ground or earth nodes. Isolating the link eliminates these issues. Using galvanic isolation allows for signal flow and prevents the ground current flow in case of different ground potential.

The ISO7140 is used as a four-channel digital isolator. The ISO7140 has two power supplies for both primary and isolated sides. The isolated side is powered by the 5-V isolated supply, and the primary side is powered by system 3.3-V supply provided by BBB or an external supply.

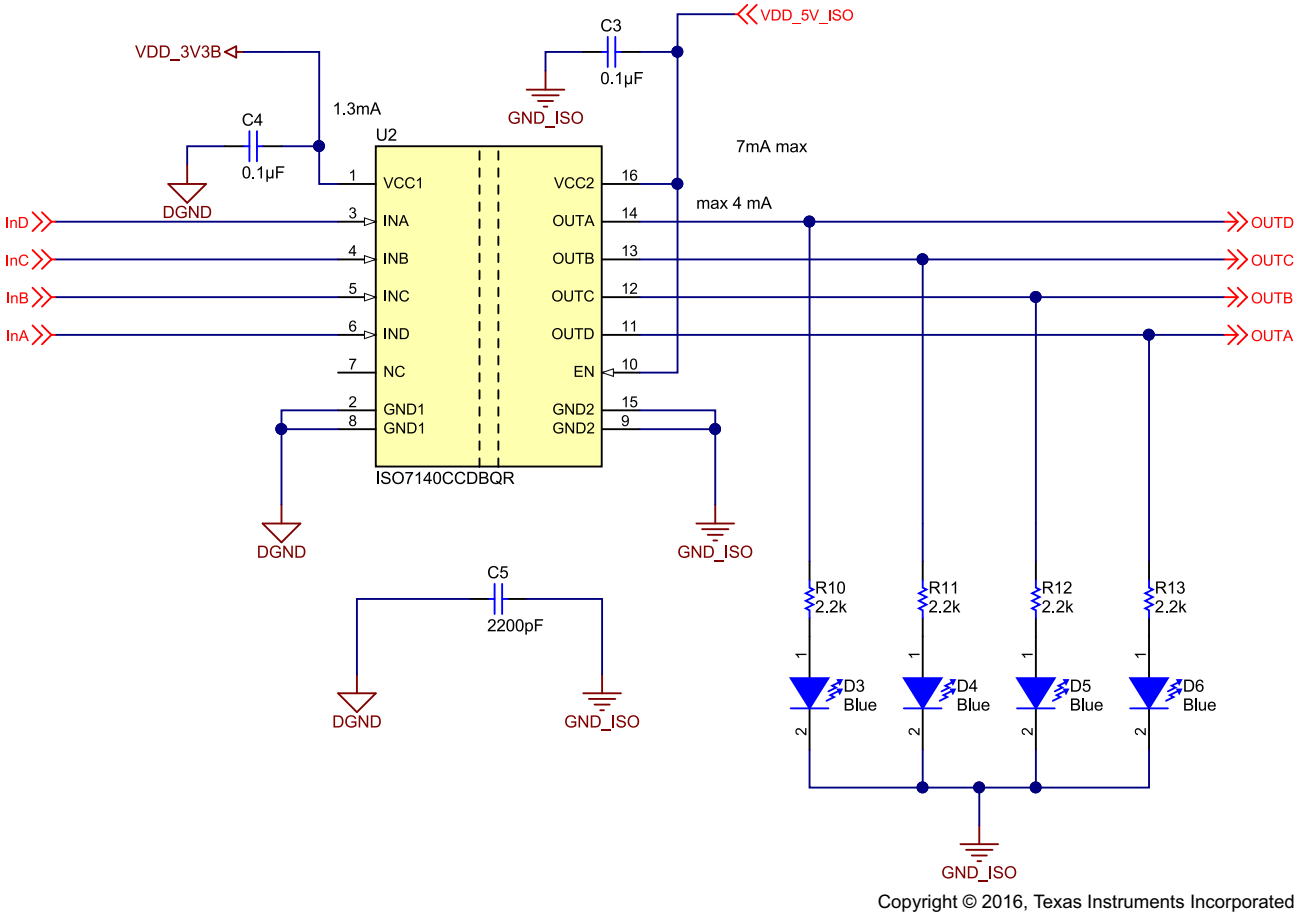

Figure 8. Isolator Schematics

3.1.4 Isolated Fly-Buck Design

In this section, detailed description of the design steps required to determine the fly-buck component values given the requirements of Vin = 5 V, Vout=5 V, and Iout=200 mA.

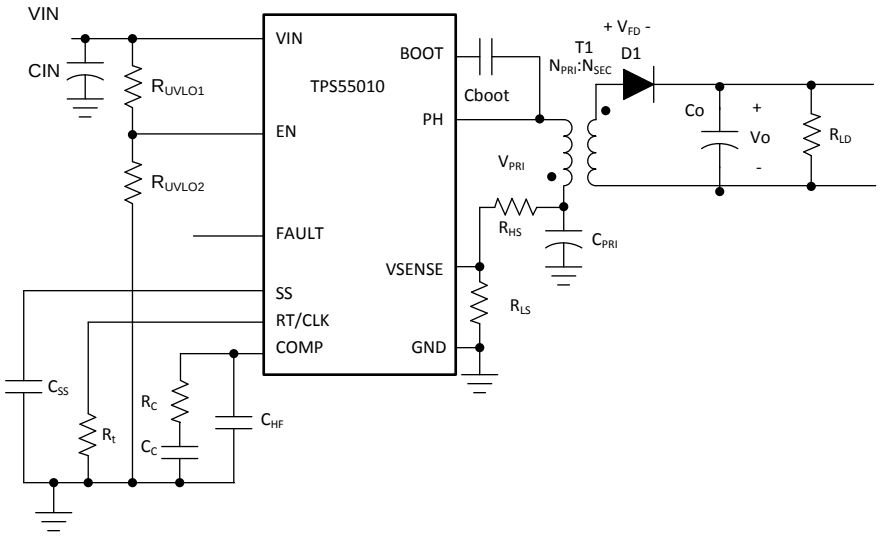

Figure 9. Fly-Buck Circuit Topology

3.1.4.1 Primary Voltage

Primary voltage is a function of duty cycle, like in the buck converter.

$$D = \frac{V_{PRI}}{V_{IN}}$$

In a fly-buck converter power is transferred to the secondary side in the rest of the cycle time (1-D), which means higher duty cycle values should be avoided to allow for sufficient time for power transfer.

Typically, for fly-buck topology a primary side voltage that is 50% of the input voltage is ideal to maximize output power. Assuming a minimum input voltage of 4.5 V, a primary side voltage of 2.2 V is selected, which leads to a duty cycle of about 45%.

3.1.4.2 Turns Ratio

The transformer turns ratio is calculated using the desired output voltage, diode voltage, and the primary voltage.

$$\frac{N_{SEC}}{N_{PRI}} = \frac{V_{OUT} + V_{FD}}{V_{PRI}}$$

Assuming a diode voltage drop of 0.5 V, a transformer turns ratio of 1:2.5 is required.

3.1.4.3 Feedback Network

The primary side voltage is set with a resistor divider from the primary side capacitor to the VSENSE pin where it is compared to the internal stable reference of 0.829 V. Feedback resistors are calculated using the equation.

$$R_{HS} = R_{LS} \times \left(\frac{V_{PRI} - 0.829\ V}{0.829\ V} \right)$$

An arbitrary value of R_LS =10 kΩ can be chosen to calculate R_HS = 16.5 kΩ. These resistors are chosen as 1% accurate resistors.

3.1.4.4 Switching Frequency and Primary Inductance

In isolated supplies, low-switching frequency improves efficiency by reducing gate drive losses and MOSFET and diode switching losses. However, a lower switching frequency operation requires a larger primary inductance, which will have more windings and higher DC resistance.

Primary inductance should be larger than L_(PRI(min)) to avoid peak switch current limit (taking minimum value of the current limit I_HSCL)

$$L_{PRI(min)} = \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{sw} \times \left(I_{HSCL} - I_{OUT} \times \frac{N_{SEC}}{N_{PRI}} \right)} = \frac{5 \times 0.44 \times 0.56}{2 \times f_{SW} \times (2 - 0.2 \times 2.5)} = \frac{0.41}{f_{SW}}$$

Primary inductance should also be less than L_(PRI(max))for zero voltage switching to improve efficiency

$$L_{PRI(max)} = \frac{V_{IN} \times D \times (1 - D)}{2 \times f_{SW} \times \left(I_{OUT} \times \frac{N_{SEC}}{N_{PRI}} \right)} = \frac{1.237}{f_{SW}}$$

It is important to maintain a magnetizing ripple current above 400 mA. This ripple current is part of the PWM control system and required for stable operation.

$$L_{PRI(max)} = \frac{(V_{IN} - V_{PRI}) \times D}{0.4 \times f_{SW}} = \frac{3.15}{f_{SW}}$$

It is clear that the first L_(PRI(max)) is lower and stricter. If f_SW = 350 kHz is chosen for switching frequency, a range of L between 1.17 and 3.5 µH is given. L_PRI = 2.5 µH is selected as primary magnetizing inductance value.

3.1.4.5 Transformer

The calculated the turns ratio is 1:2.5 and the primary inductance is 2.5 µH. The transformer WE-750311880 from Würth Elektronik is chosen, which is a recommended transformer for TPS55010. The transformer has less than 0.16 Ω of secondary DC resistance, a high saturation current of 12 A, and can withstand 2500 VAC for 1 minute.

3.1.4.6 Timing Resistor

Internal amplifier hold the RT/CLK pin at a fixed voltage (0.5 V) when using an external resistor to ground to set the switching frequency. Timing resistor is calculated using:

$$R_T\,(k\Omega) = \frac{156000}{f_{SW}\,(kHz)^{1.0793}}$$

The calculation leads to a resistor value of 280 kΩ . The resistor is selected as high accuracy 1% resistor.

3.1.4.7 Slow Start Capacitor

A capacitor on the SS pin to ground implements a slow start time to minimize inrush current and overshoot during startup. The TPS55010 has an internal pull-up current source of 2.2 µA, which charges the external slow start capacitor to an internal reference of 0.829 V. VSENSE voltage will follow the SS pin voltage with 35-mV offset up to 85% of the internal voltage reference then it enters the normal mode for a specified start time. The SS capacitor can be calculated using:

$$C_{SS}\,(nF) = \frac{T_{SS}\,(ms) \times I_{SS}\,(\mu A)}{V_{REF}\,(V)}$$

If 35 ms is chosen as slow start time, this results in a 0.1-µF slow start capacitor.

3.1.4.8 Primary and Secondary Side Capacitor

A primary side capacitor is selected to minimize the output voltage ripple. Details about calculating the primary side capacitor can be found in TPS55010 data sheet (SLVSAV0). A capacitor value of 47 µF is chosen to keep the size small, thus, a 6.3-V X5R capacitor is chosen.

Secondary side ripple should be below 1% of output voltage. As the converter is primary side is regulated, the output voltage may rise in light load conditions. This rise should be considered and a zener diode is used to prevent overvoltage at light or no load. Two 10-µF or 10-V load capacitors are used.

3.1.4.9 Secondary Side Diode

The diode should be selected to handle the voltage stress and the secondary side rms current. Typically, a low duty cycle or high turns ratio design will have a larger voltage stress on the diode. For detailed calculations for rms current and the voltage stress over the diode, check the TPS55010 data sheet (SLVSAV0). A B120 diode is used, which is rated for 20-V and 1-A rms current.

3.1.4.10 Input Capacitor

Input ripple should be less than 1% of input voltage. The TPS55010 requires a high-quality ceramic, type X5R or X7R input decoupling capacitor of at least 2.2 µF of effective capacitance or larger coupled to VIN and GND pins (and in some applications additional bulk capacitance). The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS55010. A 47-µF or 10-V X5R ceramic capacitor is used on the input. A 0.1-µF ceramic capacitor is placed as close to the VIN and GND pins as possible for a good bias supply.

3.1.4.11 Under Voltage Lockout Resistors

The TPS55010 is disabled when the VIN pin voltage falls below 2.6 V. The EN pin is pulled-up to the VIN level through a pull-up current source of 1.2 µA. Once the EN pin voltage exceeds 1.25 V, an additional 3.4 µA of hysteresis is added. When the EN pin is pulled below 1.18 V, the hysteresis current is removed.

In this design a higher stop voltage of 4 V is required, and a start voltage of 4.5 V is required.

Undervoltage lockout resistors are calculated using the following equations:

$$R_{UVLO1} = \frac{V_{START}\left(\frac{V_{ENfalling}}{V_{ENrising}}\right) - V_{STOP}}{I1 \times \left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_{HYS}}$$

$$I1 = 1.2\ \mu A;\ I_{HYS} = 3.4\ \mu A;\ V_{ENfalling} = 1.25\ V;\ V_{ENrising} = 1.18\ V$$

The other resistor is calculated using:

$$R_{UVLO2} = \frac{R_{UVLO1} \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R_{UVLO1}(I1 + I_{HYS})}$$

These equations lead to R_UVLO1 = 71 kΩ and R_UVLO2 = 26.7 kΩ.

4 Testing and Results

4.1 Test Setup

Figure 10 shows the test setup for one channel of the TIDA-00766 TI Design. An Agilent™ E3631A dual power supply is used to power the board with the needed 3.3- and 5-V supplies. An Agilent 33120A wave generator is used to feed the high speed input square wave signal using a T-junction, and the same input signal is fed to the scope for triggering. Output is connected to a load using a typical twisted pair cable. In addition to the cable capacitance of 30 pF/ft, a load capacitance is attached to the load to ground. A LeCroy™ Wavefurfer™ 454 scope is used to probe output node voltage. System power is directly monitored using the power supply.

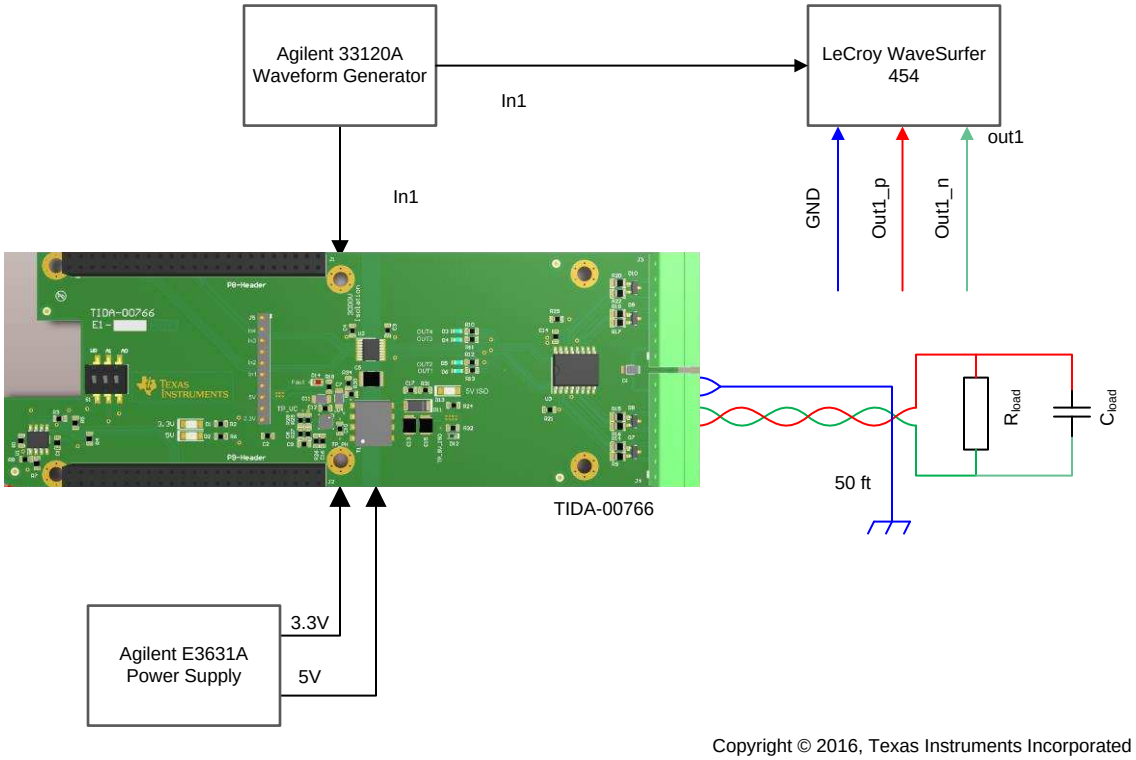

Figure 10. TIDA-00766 Test Setup

4.2 Test Procedure

The output waveform, rise and fall times, output delay, output high, output low, and system power are measured for target input frequencies.

4.3 Test Results

Figure 11 shows the output waveforms (single-ended each as well as differential signal) for the TIDA-00766 with 15 m (50 ft) of twisted pair cable attached, which has about 30 pF/ft parasitic capacitance and 1-nF load capacitance.

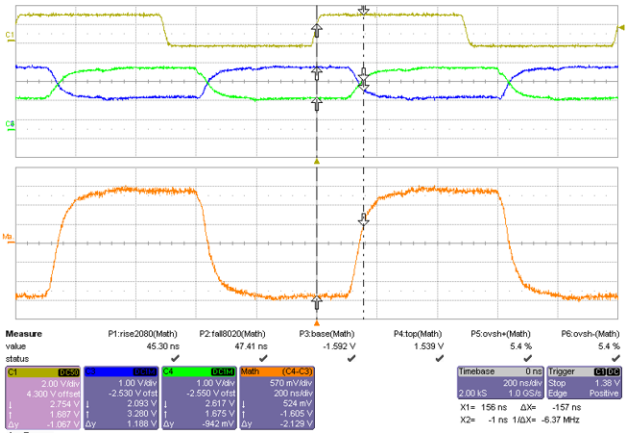

Figure 11. Output Waveform (SE, DIFF) of PTO module

Table 2 lists the test results of 1-MHz signal input. The cable effect on the signal waveform is shown in Table 2 as longer transition times. Very symmetric rise and fall times allows receivers to be sensitive to both edges. High and low levels are also pretty symmetric, and 3 Vpp is easily achieved. The power consumption when all channels are loaded with 100 Ω is close to 150 mA well above the limits of the fly-buck converter. The power consumption slightly increases with an increasing load capacitor and increasing frequency due to the dynamic power dissipation.

Table 2. Test Results With 15-m Cable at 1-MHz Output

Backplane power consumption	5 V: 43 mA + 25 mA × Nchannels 3.3 V: 8 mA
Rise time 20-80%	45 ns
Fall time 80-20%	47 ns
Output low level	-1.6 V
Output high level	1.54 V

Figure 12 shows the output waveforms with direct load without cable. A bit faster edges are observed. Output delay is also calculated to be about 70 ns. Figure 13 shows that the design can go further beyond 1-MHz limit. The waveforms shown are at 2-MHz input signal.

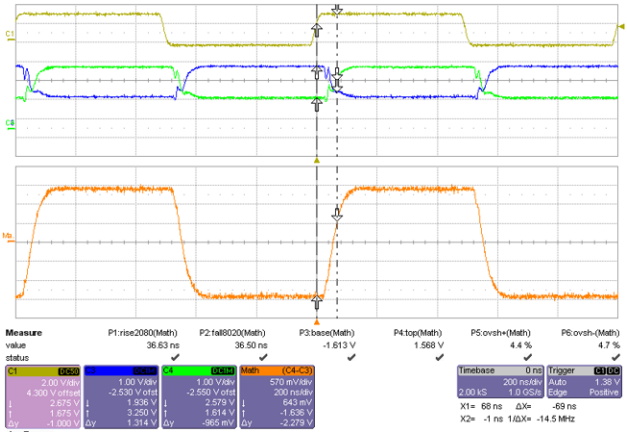

Figure 12. Output Waveform of TIDA-00766 With No Cable

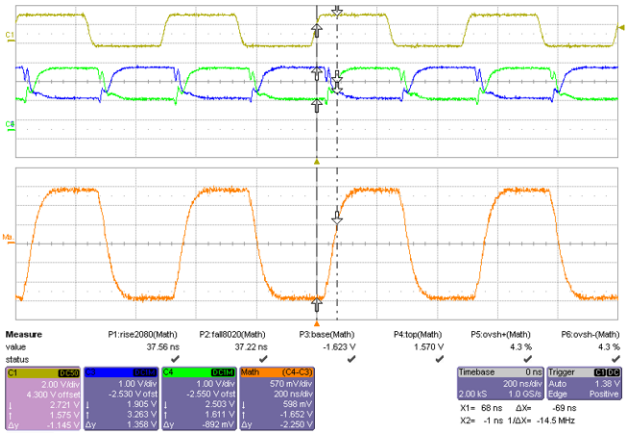

Figure 13. Output Waveforms of TIDA-00766 Module at 2 MHz Input

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00766.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00766.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00766.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00766.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00766.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00766.

6 Software Files

To download the software files, see the design files at TIDA-00766.

7 References

1. Texas Instruments, *High Performance Pulse Train Output (PTO) with PRU-ICSS for Industrial Applications Reference Design*, TIDEP0027 Tools Folder(TIDEP0027)
2. Texas Instruments, *TPS55010 2.95-V To 6-V Input, 2 W, Isolated DC/DC Converter with Integrated FETs*, TPS55010 Data Sheet (SLVSAV0).

8 About the Author

AHMED NOEMAN is a system engineer at Texas Instruments Germany developing reference design solutions for industrial applications. Ahmed has many years of experience in analog and RF design, AMS modeling, and verification as well as application and system engineering in a wide range of fields including RF transceivers, clocks and PLLs, memory systems, and more. Ahmed received his Bachelor of Science (BSC) and Master of Science in Electrical Engineering (MSEE) from Ain Shams University, Egypt.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2016) to A Revision	Page
• Changed from preview draft	1

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