TI Designs

Automotive 12- and 24-V Battery Input Protection Reference Design

Description

Automotive battery power supply lines are prone to transients while running the system. Typical protections required are overvoltage, overload, reverse polarity, and jump start. During the life of a car, the alternator may be replaced with a non-OEM part. The after-market alternator may have different or no load dump protection, which could lead to damaging the electronic control unit (ECU). This TI Design provides protection to handle these potential unsuppressed load dump pulses (12 V and 24 V) with hardware control. Class A operation may be attained during unsuppressed load dump pulses.

Resources

TIDA-01167	Design Folder
LM5060-Q1	Product Folder
TPS7A1650	Product Folder
LM2903-Q1	Product Folder

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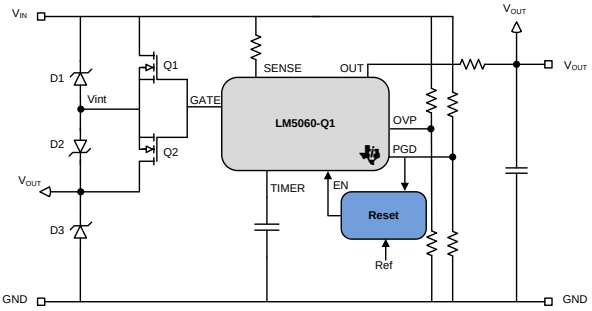
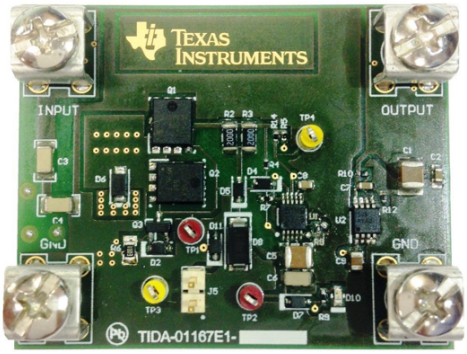
Features

- Overvoltage Protection
- Overload Protection
- Transient Suppression
- Reverse Polarity Protection
- Configurable Options to Support Class A Operation During Unsuppressed Load Dump Pulses
- Scalable to Multiple Battery Topologies (12 V, 24 V, 48 V)
- Improves System Efficiency With Very Low Quiescent Current
- Compliance to ISO 7637-2, ISO 16750-2

Applications

- Electronic Control Units
- Body Control Module
- Battery ORing Applications





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1 System Overview

1.1 System Description

Automotive 12-, 24-, and 48-V battery power supply lines are prone to transients while running the system. Typical protections required for such a system are overvoltage, overload, reverse polarity, and jump start. Electronic Circuits powered by direct battery lines needs to be protected from such transients. No or an improper protection circuit could lead to damages for components. Typically, DC-DC converters and system basis chips are directly operated on battery supply lines. Robust components and controllers are required to place on the battery power supply lines to suppress the transients. Typical protection requirements for 12- and 24-V batteries are considered for the TIDA-01167 reference design.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	MIN	TYP	MAX	UNIT
V_{INPUT}	DC input voltage	0	—	70 (1)	V
Output current	Q1, Q2 configurable	—	2.5	—	A
Gate voltage (turnon time)	12 V	—	527	—	µs
	24 V	—	570	—	µs
Gate voltage (turnoff time)	12 V	—	118	—	µs
	24 V	—	233	—	µs
Operating current	12 V, Jumper J5 closed	—	3.18	—	mA
	24 V, Jumper J5 closed	—	3.4	—	mA
Quiescent current	12 V, Jumper J5 open	—	53	—	µA
	24 V, Jumper J5 open	—	102	—	µA

(1) Based on requirement specification maximum operating voltage of the design can be changed.

1.3 Block Diagram

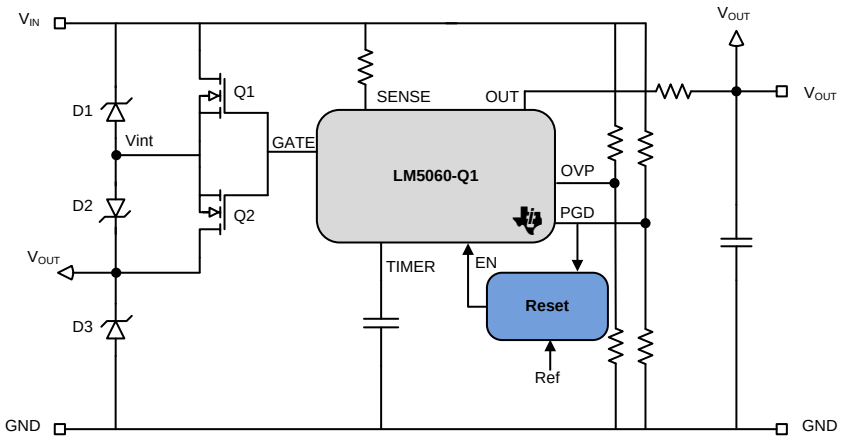


Figure 1. Block Diagram

1.4 Highlighted Products

1.4.1 LM5060-Q1

The LM5060 high-side protection controller provides intelligent control of a high-side N-channel MOSFET during normal on/off transitions and fault conditions. In-rush current is controlled by the nearly constant rise time of the output voltage. A Power Good output indicates when the output voltage reaches the input voltage and the MOSFET is fully on. Input UVLO (with hysteresis) is provided as well as programmable input overvoltage protection (OVP). An enable input provides remote on or off control. The programmable UVLO input can be used as second enable input for safety redundancy. A single capacitor programs the initial start-up V_{GS} fault detection delay time, the transition V_{DS} fault detection delay time, and the continuous overcurrent V_{DS} fault detection delay time. When a detected fault condition persists longer than the allowed fault delay time, the MOSFET is latched off until either the enable input or the UVLO input is toggled low and then high.

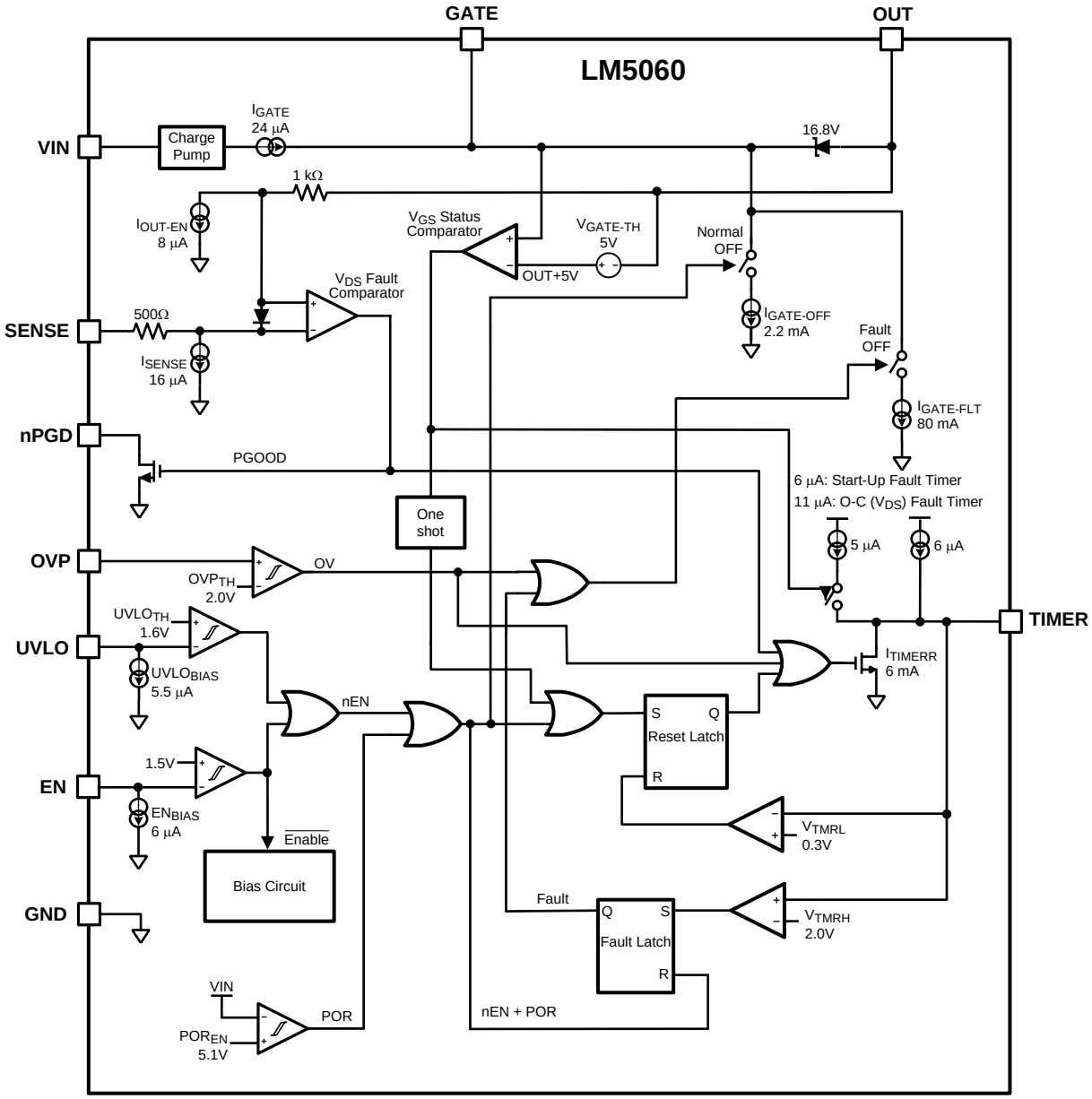


Figure 2. LM5060-Q1 Functional Block Diagram

Key features include:

- Available in automotive grade / AEC Q-100
- Wide operating input voltage range: 5.5 to 65 V
- Less than 15-μA quiescent current in disabled mode
- Controlled output rise time for safe connection of capacitive loads
- Charge pump gate driver for external N-channel MOSFET
- Adjustable undervoltage lockout (UVLO) with hysteresis
- Programmable fault detection delay time
- Adjustable input OVP
- Immediate restart after overvoltage shutdown

2 System Design Theory

2.1 Automotive Conducted Transients

In automotive environment batteries are connected to various electronic control units, loads, and sensor and load systems. Due to several parameters, conducted transients are seen on power lines for electronic control units. A short overview of such electrical transients are shown in Figure 3.

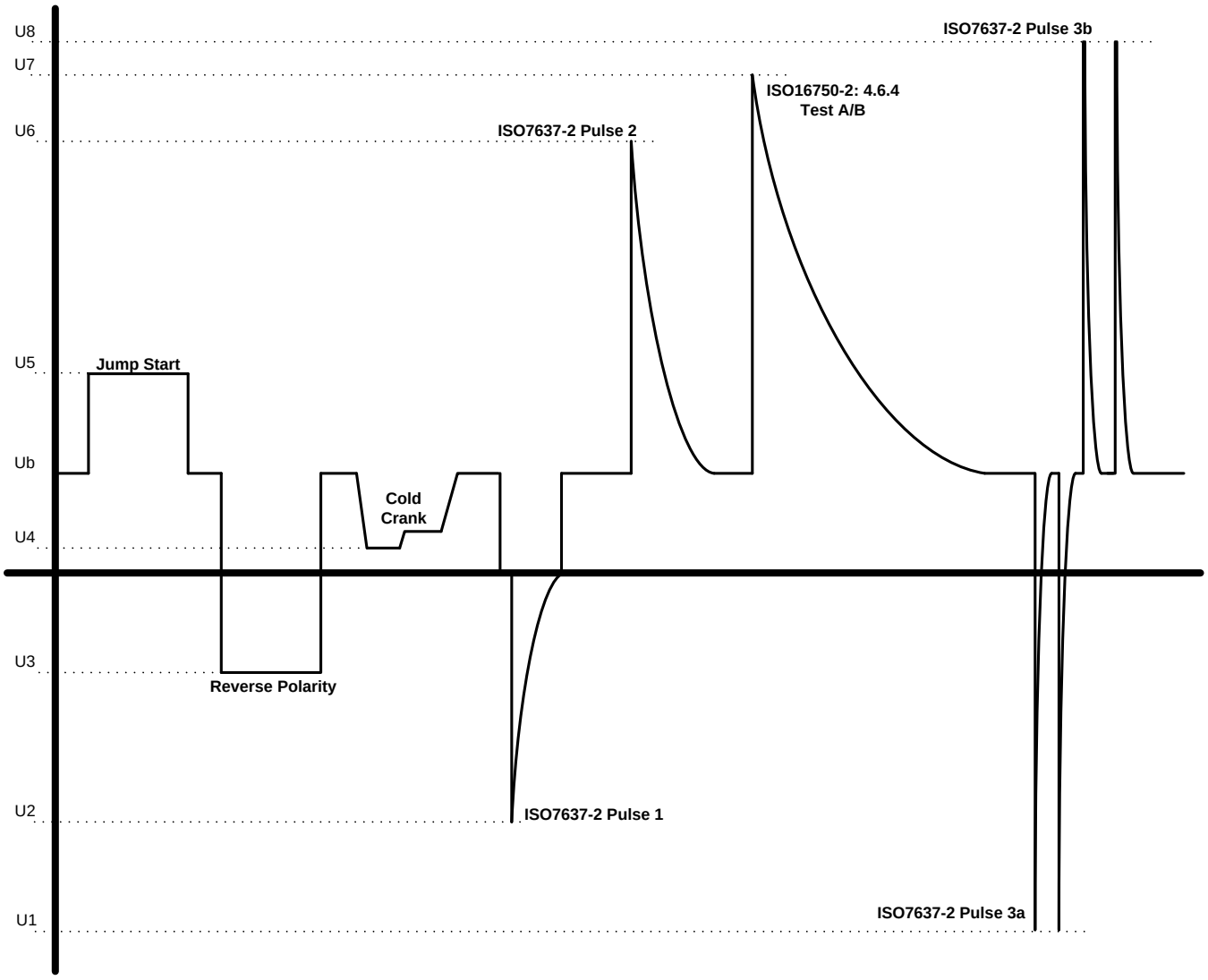


Figure 3. Overview of Transients

Table 2 provides the description, behavior, and impact of automotive power line electrical transients.

Table 2. List of Automotive Electrical Transients Standards

STANDARD OR SPECIFICATION	INSTITUTE OR COMPANY
ISO 7637-2	Road vehicles: Electrical disturbances from conduction and coupling
ISO 16750-2	Road vehicles: Environmental conditions and testing for electrical and electronic equipment
LV124	Group of OEMS (Audi, BMW, Porsche, VW, and so on)
SAEJ1113-11	USA Standard by the Society of Auto Engineers
JASO A-1	Japanese automobile standard

Specification of these standards are not limited to this list; auto manufacturers have their own internal standards. Although changes are typically only in a few parameters of different tests or limits, the essence of the requirements are the same.

ISO 7637 is titled *Road vehicles – Electrical disturbances from conduction and coupling*, and part 2 is specifically "Electrical transient conduction along supply lines only". The standard defines a test procedure, including the description of test pulses, to test the susceptibility of an electrical subsystem to transients, which could potentially be harmful to its operation. Each pulse is modeled to simulate a transient that could be created by a real event in the car. This design mainly focus for reverse polarity protection and ORing applications, which is predominantly placed next to battery.

ISO 16750 is titled *Road vehicles – Environmental conditions and testing for electrical and electronic equipment*, and part 2 is specifically "Electrical loads." An easy way to think of this standard is that it essentially defines a series of "supply voltage quality" events—variations of the battery supply voltage under various conditions. For the most part, these conditions are not harmful to the electrical subsystem, but can affect its state of operation. The tests in this standard are designed to see how the subsystem behaves before, during, and after these events.

2.1.1 ISO 7637-2 Pulse 1

This test is a simulation of transients due to supply disconnection from inductive loads. It is applicable to DUTs which, as used in the vehicle, remain connected directly in parallel with an inductive load.

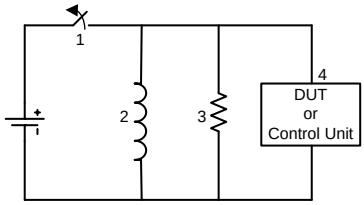


Figure 4. ISO 7637-2 Pulse 1

Key features include:

- Ignition switch and main relay or relevant
- Inductive load (relays, solenoids or motors, and so on)
- Load resistance (effective load on the power supply)
- Control unit or DUT (exposed to transients)
- Battery

Pulse 1 occurs when switch(1) is open. The pulse itself, simulating an inductive kick in a parallel system, is a high voltage, negative-going transient. The waveform and its parameters are given in Figure 5 and Table 3:

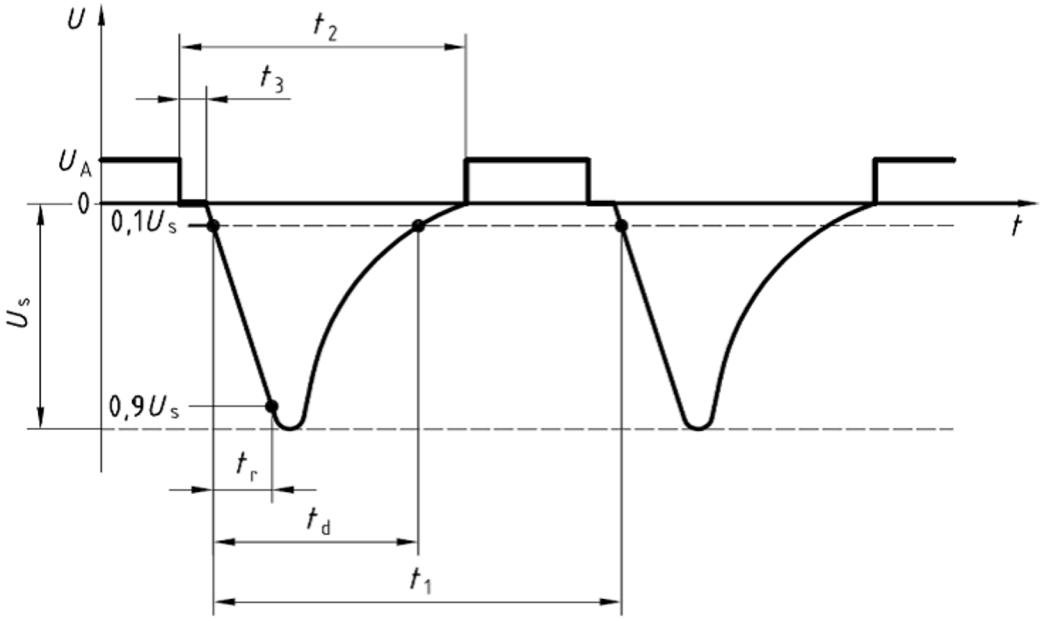


Figure 5. ISO 7637-2 Pulse 1 Waveform

Table 3. ISO 7637-2 Pulse 1 Parameters

PARAMETER	12-V SYSTEM	24-V SYSTEM
U_S	–75 to –100 V	–450 to –600 V
R_i	10 Ω	50 Ω
t_d	2 ms	1 ms
t_r	$\left(1^{\ 0}_{-0.5}\right)$ µs	$\left(3^{\ 0}_{-1.5}\right)$ µs
t_1 (1)	0.5 to 5 s	
t_2	200 ms	
t_3 (2)	< 100 µs	

(1) t1 must be chosen such that the DUT is correctly initialized before the application of the next pulse.
(2) t3 is the smallest possible time necessary between the disconnection of the supply source and the application of the pulse.

Pulse specification and parameters might vary based on OEM and vehicle configuration.

2.1.2 ISO 7637-2 Pulse 2a

Pulse 2a simulates transients due to sudden interruption of currents in a device connected in parallel with DUT due to inductance of the wiring harness.

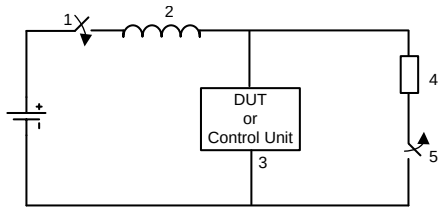


Figure 6. ISO 7637-2 Pulse 2a Simulation Picture

Key features include:

- Ignition switch and main relay or relevant
- Inductance (wiring harness)
- Control Unit or DUT (exposed to transients)
- Load resistance (effective load on the power supply)
- Load switch
- Battery

The pulse itself, simulating an inductive kick from the wiring harness, is a high-voltage, positive-going transient. The waveform and its parameters are given in Figure 7 and Table 4:

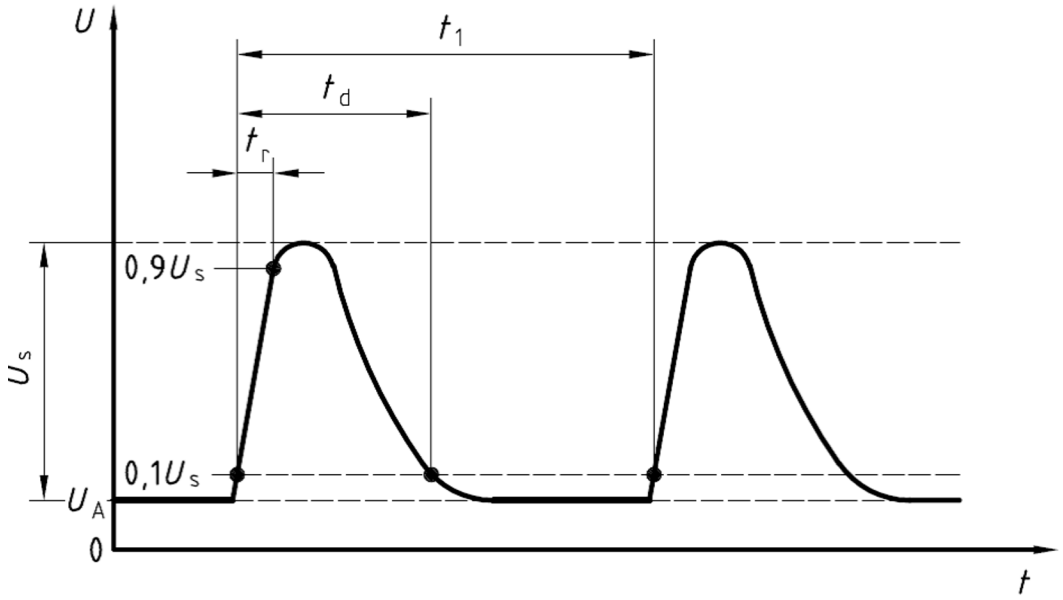


Figure 7. ISO 7637-2 Pulse 2a Waveform

Table 4. Pulse 2a Parameters

PARAMETER	12-V SYSTEM	24-V SYSTEM
U_S	37 to 50 V	
R_i	2 Ω	
t_d	0.05 ms	
t_r	$\left(1^{\ 0}_{-0.5}\right)\mu s$	
t_1 (1)	0.2 to 5 s	

(1) The repetition time t_1 can be short, depending on the switching. The use of a short repetition time reduces the test time.

Pulse specification and parameters might vary based on OEM and vehicle configuration.

2.1.3 ISO 7637-2 Pulses 3a and 3b

These test pulses are a simulation of transients, which occur as a result of the switching processes. The characteristics of these transients are influenced by distributed capacitance and inductance of the wiring harness.

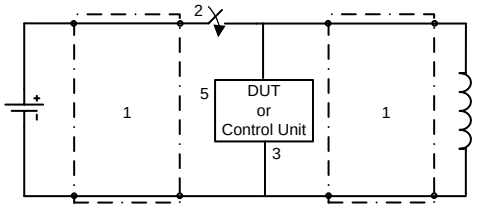


Figure 8. ISO 7637-2 Pulse 3a and 3b Simulation Picture

Key features include:

- Wiring harness with distributed inductance and capacitance
- Ignition switch and main relay or relevant
- Control Unit or DUT (exposed to transients)
- Inductive load (relays, solenoids or motors, and so on)
- Battery

Pulse 3a is seen in control unit or DUT when supply is turned ON or load is switched before the control unit. A burst of negative arching transients are seen due to relay on and off.

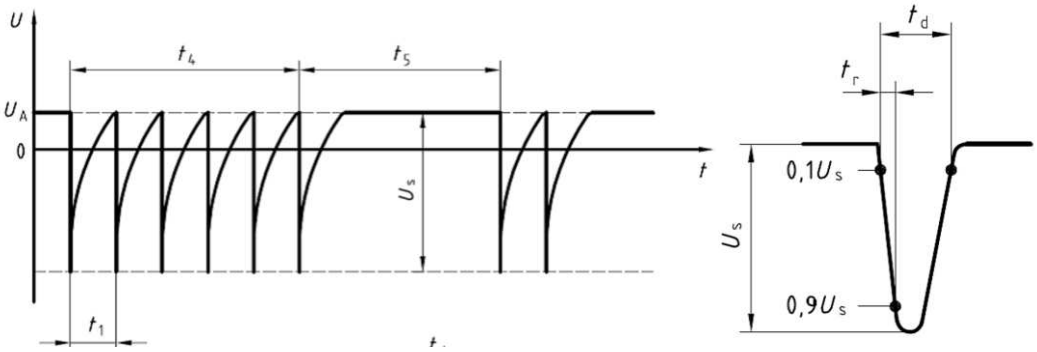


Figure 9. ISO 7637-2 Pulse 3a Waveform

Table 5. ISO 7637-2 Pulse 3a Parameters

PARAMETER	12-V SYSTEM	24-V SYSTEM
U_S	112 to 150 V	150 to 200 V
R_i	50 Ω	
t_d	$\left(0.1^{+0.1}_{0}\right)\mu s$	
t_r	5 ns ± 1.5 ns	
t_1	100 µs	
t_4	10 ms	
t_5	90 ms	

Pulse 3a is seen in control unit or DUT when load is switched after the control unit. A burst of positive arching transients are seen due to relay on and off.

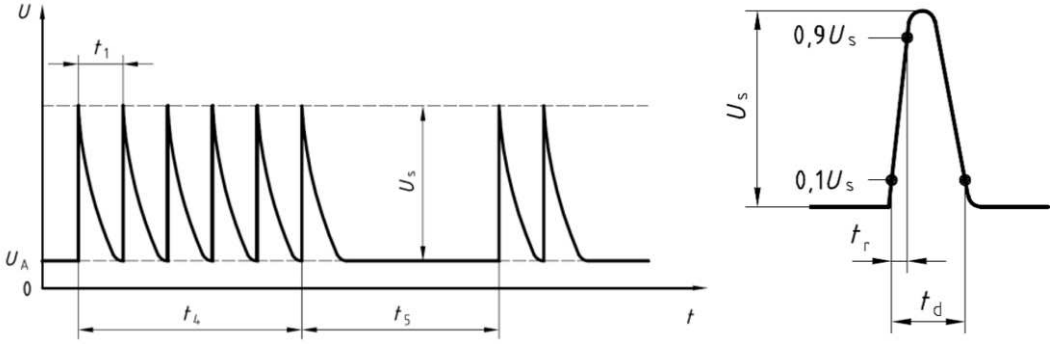


Figure 10. ISO 7637-2 Pulse 3b Waveform

Table 6. ISO 7637-2 Pulse 3b Parameters

PARAMETER	12-V SYSTEM	24-V SYSTEM
U_S	75 to 100 V	150 to 200 V
R_i	50 Ω	
t_d	$\left(0.1^{+0.1}_{0}\right)\mu s$	
t_r	5 ns ± 1.5 ns	
t_1	100 µs	
t_4	10 ms	
t_5	90 ms	

Pulse specification and parameters might vary based on OEM and vehicle configuration.

2.1.4 ISO 16750-2 4.6.4 Load Dump

This test is a simulation of load dump transient, occurring in the event of a discharged battery being disconnected while the alternator is generating charging current and with other loads remaining on the alternator circuit at this moment. Load dump may occur on account of a battery being disconnected as a result of cable corrosion, poor connection or of intentional disconnection with the engine running. This pulse was actually moved from ISO 7637 to ISO 16750.

The actual load dump event is extremely high energy and high voltage, which would be very difficult (and expensive) to protect against on every subsystem in the vehicle. Instead, every OEM installs a clamping circuit to the alternator, which limits the voltage to a more manageable level for the subsystem. This clamped voltage varies from OEM to OEM, but is typically in the range of 30 to 40 V.

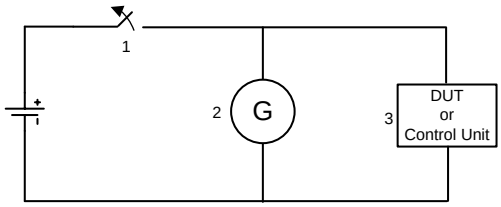


Figure 11. ISO 16750-2 Test A Simulation Picture

Key features include:

- Battery connection (loose contact or disconnection)
- Alternator with internal clamping
- Control Unit or DUT (exposed to transients)
- Battery

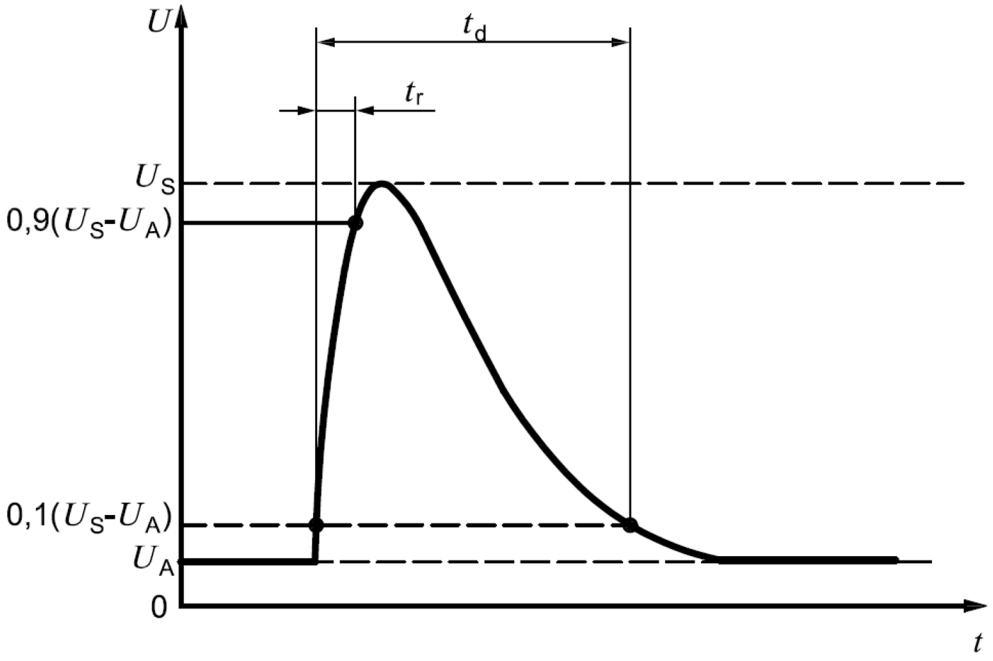


Figure 12. ISO16750-2 Test A Waveform (Without Centralized Load Dump)

Table 7. ISO16750-2 4.6.4.2.1 Test A Parameters

PARAMETER	TYPE OF SYSTEM	
	U_N = 12 V	U_N = 24 V
U_S (V)	$79 \le U_S \le 101$	$151 \le U_S \le 202$
R_i (Ω)	$0.5 \le R_i \le 4$	$1 \le R_i \le 8$
t_d (ms)	$40 \le t_d \le 400$	$100 \le t_d \le 350$
t_r (ms)	$10\left(\begin{smallmatrix}0\\-5\end{smallmatrix}\right)$	

Pulse specification and parameters might vary based on OEM and vehicle configuration.

2.1.5 ISO 16750-2 4.7 Reverse Voltage

This test checks the ability of a control unit to withstand against the connection of a reversed battery when using an auxiliary starting device. During the service or while repairing the car, there is a possible risk of mis wire or wrong connections of system wiring harness to battery. In such case electronic control units needs to have protection for reverse battery voltage.

In automotive systems, the alternator is directly connected to battery without any fuse. Rectifier diodes in the alternator can withstand the reverse voltage for 60 s. If the diodes in alternator are damaged, then there is a scope for damage of wires and possible fire inside the system. Once the fuses or alternator are replaced, the rest of the devices are expected to run with class A. So the control units are expected to withstand the reverse voltage for at least 60 s ± 6 s.

Table 8. ISO16750-2 Reverse Voltage Parameters

NOMINAL VOLTAGE U_N (V)	TEST VOLTAGE U_A (V)
12	14
24	28

Pulse specification and parameters might vary based on OEM and vehicle configuration.

3 Getting Started Hardware

3.1 Undervoltage (V_{IN} < 5 V)

When the battery voltage is less than 5 V, the LM5060-Q1 is in undervoltage mode, and the gate voltage will be pulled to ground. Q1 and Q2 will remain in OFF state. In an automotive environment, the UVLO state is not widely used as it is not included as feature of this design. The UVLO pin connected directly to the input pin. The LM5060-Q1 will start functioning once input voltage is above 1.6 V (UVLO threshold voltage).

In an automotive environment, typical batteries used for supply are 12 V, 24 V, and 48 V. In normal operation, the LM5060-Q1 will always remains in an ON state. Methods and mechanism to support cold crank conditions will be explained in Section 3.4.

3.2 Normal Operation (5 V ≤ V_{IN} ≤ 75 V)

If the enable pin is high and input voltage is less than the overvoltage threshold, then the gate of the LM5060-Q1 will turn on Q1 and Q2. Output voltage follows the input voltage with a voltage drop across Q1 and Q2 as shown in Figure 13.

$$V_{OUT} = V_{IN} - \left(R_{DS(on)\_Q1} + R_{DS(on)\_Q2}\right) \times I_{LOAD} \quad (1)$$

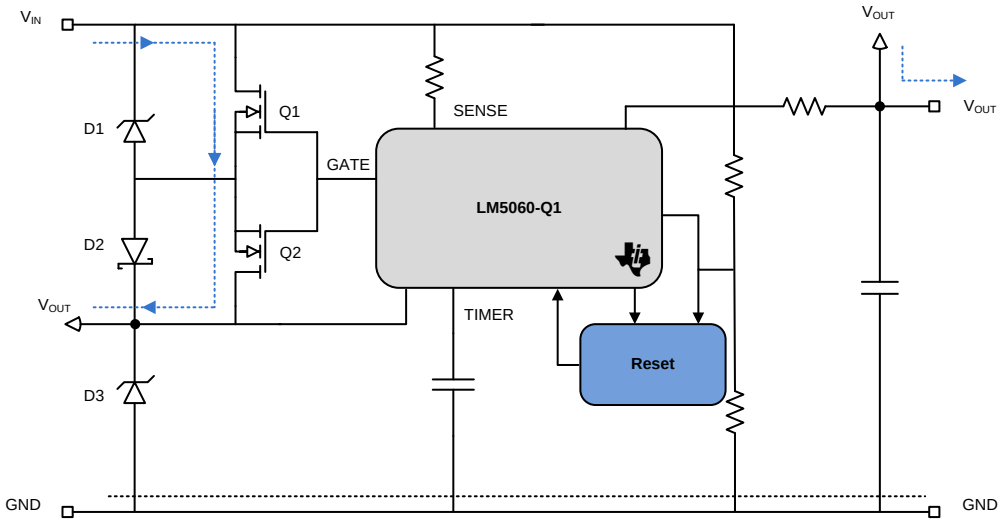


Figure 13. Normal Behavior

3.3 Transient Suppression

Transient suppression is a critical part for automotive input protection. As mentioned in Section 2.1, there are different types of transients that need to be handled at the battery input. There is a need to have a common topology to support various automotive input protection requirements. Load dump typically describes input protection. In most automotive cases, the load dump pulse is handled in the alternator. During the service or repairs, there is a scope and chance to replace the current alternator with a low-cost solution. Low-cost alternators might have different specification or no load dump protection, which might leads to damage of electronics.

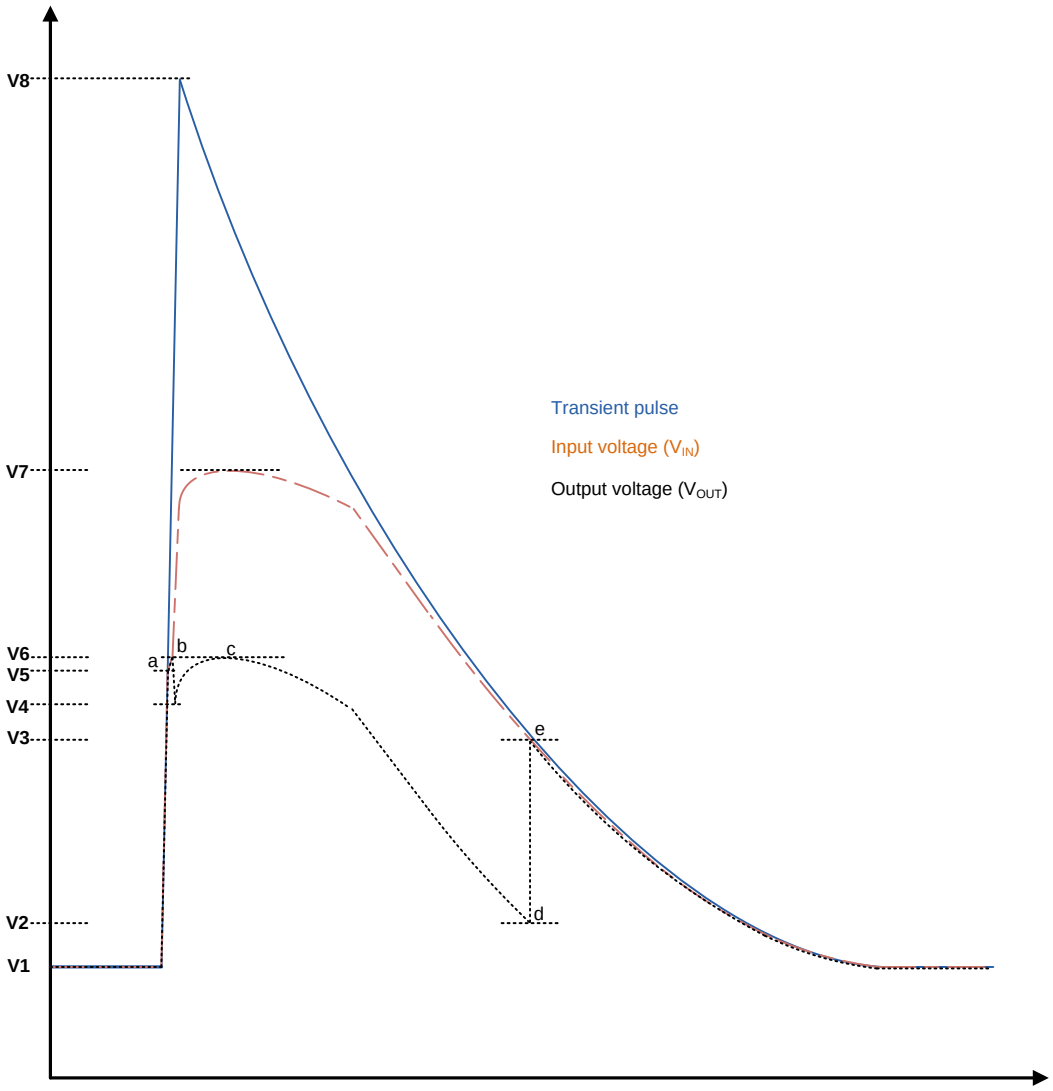


Figure 14. Input Protection Characteristics

Figure 14 represents the behavior of an input protection module during load dump pulses. Output voltage can be reduced to the voltage levels based on requirements and system design. V1 is the nominal battery input voltage applied to the system. During normal state, voltage at the output will be constant based on state of input voltage. As discussed in this case, circuit behavior is same as shown in Figure 13 (output voltage following the input voltage with Q1 and Q2). Since Q1 and Q2 are turned on, D3 is the TVS diode that will suppress the transients from input and output. Due to transients as shown in Figure 14, if the input voltage starts rising, output voltage will follow the input voltage until V5. V5 is the minimum break down voltage of D3.

$$V5 = V_{BV\_D3\_Min} \quad (2)$$

When D3 breaks down, input current will start rising and leading D3 to clamp the voltage. As per Figure 14, the transition between a to b represents the clamping behavior of D3.

$$I_{INPUT} = I_{LOAD} + \frac{\left(V_{IN} - V_{CV\_D3}\right)}{\left(R_{DS(on)\_Q1} + R_{DS(on)\_Q2}\right)} \quad (3)$$

As the input voltage rises, the input current (I_{INPUT}) will further increase. The LM5060-Q1 has overload detection, which will turn off Q1 and Q2 (and so on). If the input current is above the overcurrent threshold limit (I_{OCP_LM5060}), gate voltage will be pulled down with an 80-mA sink current. When the gate voltage is pulled down, Q1 and Q2 will be turned off. As shown in Figure 15, when Q1 and Q2 are turned off current will be flowing through D1, D2. Output voltage (V_{OUT}) will vary based on input voltage (V_{IN}), V_{BV_D1}, V_{BV_D3} (break down voltages), and load current (I_{LOAD}).

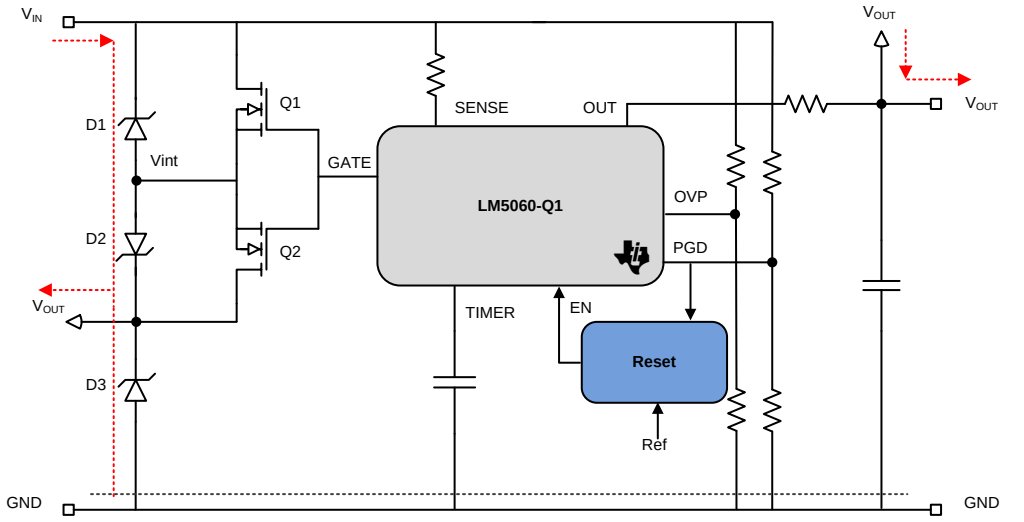


Figure 15. LM5060-Q1 OCP Latch During Transient

When OCP error is latched at the initial stage when $V_{IN} < (V_{BV\_D1\_min} + V_{BV\_D3\_min} + V_{FD\_D2})$

$$V_{OUT} = V4 = V_{IN} - V_{FD\_D2} - V_{BV\_D1\_min} \quad (4)$$

During the load dump, voltage will further rise, which leads to clamping of both D1 and D3. When $V_{TRANS} \geq (V_{BV\_D1\_min} + V_{BV\_D3\_min} + V_{FD\_D2})$

$$V_{IN\_max} = V7 = \left(V_{CV\_D1\_max} + V_{CV\_D3\_max} + V_{FD\_D2}\right) \quad (5)$$

$$V_{OUT\_max} = V6 = V_{CV\_D1\_max} \quad (6)$$

The load current of the system during the transients plays an important role for power dissipation and component selection. Peak power dissipation in the TVS diodes depends on the clamping voltage, peak transient voltage, and resistance of alternator. Selecting TVS diodes must be done based on energy dissipated in them during the peaks of transient.

Q1 and Q2 are turned off due to over current error. If the circuit design is not done properly, the LM5060-Q1 will turn OFF output voltage upon the completion of transient pulse. Input protection circuit must be implemented with appropriate circuit to remove the over current error. Take care when designing this circuit so that it will not clear all overcurrent errors. An overcurrent error that is produced due to transient (overvoltage) must be reset with an appropriate circuit. Selecting a reset voltage must be chosen appropriately to handle voltage drops and breakdown voltage of D1 ($V_{BV\_D1\_min}$).

If:

- V_{OUT_min} is the maximum voltage drop allowed
- V_{IN_RESET} is the LM5060-Q1 transient reset voltage
- R_i is the alternator input resistance

Then:

$$V_{IN\_RESET} > V_{OUT\_min} + V_{CV\_D1\_max} \quad (7)$$

$$V_{IN\_RESET} < V_{BV\_D3} + (I_{OCP\_LM5060}) \times (R_i) \quad (8)$$

If V_{IN_RESET} was set at very high voltages, there could be a chance of repeating the overcurrent error along with D3 breakdown voltage, which leads to output voltage latched off. So to avoid this incidence, reset voltage has to be set in such a way that overcurrent error will not be repeated.

If V_{IN_RESET} is set at low input voltage, then output voltage might fall too low. If the output voltage falls low, it could be inconvenient to the DC-DC converter and affect the selection of components. In such a case, place a better filter circuit at input to avoid the damage or overstress to DC-DC converter or relevant components.

3.4 Circuit Behavior

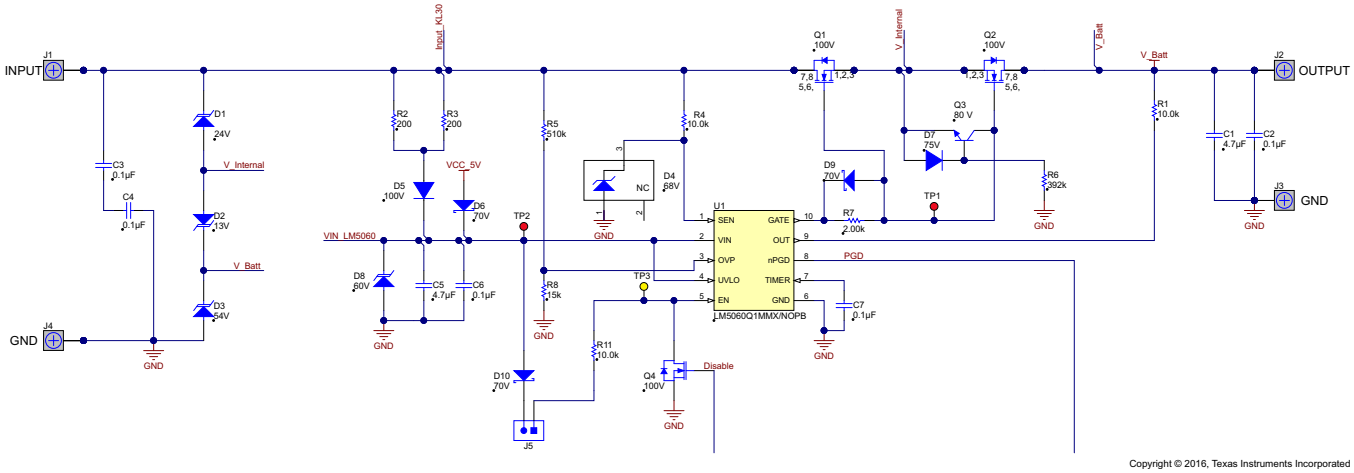


Figure 16. Input Protection Circuit

- R2, R3, D5, and D8 are used to protect the VIN pin of the LM5060 during the transients. R1, R2, and D8 can be changed accordingly to support transient peak voltages.
- Q1 is the main switch for overload and overvoltage errors for U1, whereas Q2 is to support the reverse polarity protection.
- There is no internal protection or detection of reverse polarity in the LM5060. Q3, D7, R6, and R7 are used to protect the design from reverse polarity. Q3 will turn on and reduce the gate to source voltages of Q1 and Q2. D7 is used to protect the Q3 whereas R6 to reduce the current consumption.
- R7 is used to control the turnon time of Q1 and Q2. It will also support in reducing the leakage current during the reverse polarity. During error state it is required to turn off the supply lines faster, so D9 is used to bypass R7 to turn off the Q1 and Q2.
- The undervoltage function is rarely used in automotive environment. It is not common for 12-V or 24-V systems. Design can be adapted for a 48-V system to set a defined voltage at the UVLO pin to save or reduce complexities of DC-DC converters.
- During cold crank conditions, input voltage will fall less than 5 V. The 5-V output of DC-DC converter can be connected through D6 to keep the LM5060 in active mode.
- D10 is used in the design to support external trigger input at test point along with J5 jumper pin. In end applications, D10 and J5 can be removed, and the external trigger input can be connected directly to R11.
- R1 and R4 are used to set the threshold for overload protection in the design. D4 will protect the sense pin during the peak transients. If unsuppressed load dump pulse is applied at input pin. Sense pin can withstand maximum 75V, D4 is used to protect the sense pin during high voltage transients.
- Due to inrush currents, high- or low-voltage transients, and noise, there could be OVP and overload errors set in the LM5060. An external timer capacitor C7 will be used to allow blanking period for these errors to differentiate noise and actual errors. Based on system requirement C7 is configurable. A fault will be latched when a 6-µA current flowing the C7 builds a voltage at timer, typically 2 V. When a fault is latched, Q1 and Q2 are turned off.

- R5, R8 potential divider to support OVP for LM5060. During an overvoltage, Q1 and Q2 are turned off when the input voltage falls less than the OVP threshold voltage; then output voltage resumes as Q1 and Q2 are turned ON.

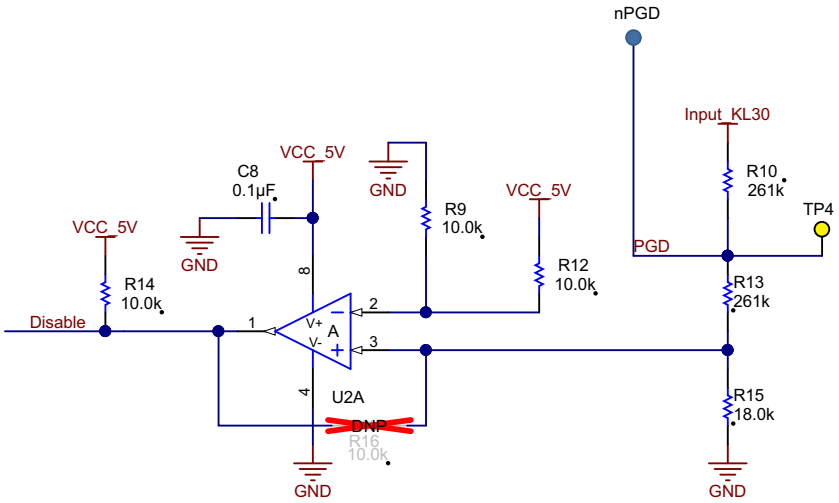


Figure 17. Comparator Reset Mechanism

- Comparator circuit is used to reset the LM5060. As discussed in Section 3.3, it is required to reset the LM5060 if the overload error is latched due to transient voltage. Do not reset overload errors if the input voltage is in normal range.
- In a normal state, if the nPGD pin of the LM5060 is pulled low, voltage at non-inverting pin of U2A also remains low. As a result, voltage in the disable net is pulled to low by a comparator as 2.5 V is present at the inverting pin due to R9 and R12.
- The nPGD pin of the LM5060 is floating when overvoltage or overload errors are detected. Voltage at R15 gives a fraction of battery voltage across potential dividers of R10, R13, and R15. R16 can be populated with a appropriate value to give the hysteresis for the module.
- R14 is the pullup resistance for the open drain connection of the comparator.
- As specified in Equation 8, V_{IN_RESET} must be less than sum of the breakdown voltage and overload current with internal resistance. OVP for the LM5060 must be chosen to support the application appropriately.

4 Testing and Results

Test setup for automotive polarity protection has been done as shown in Figure 18.

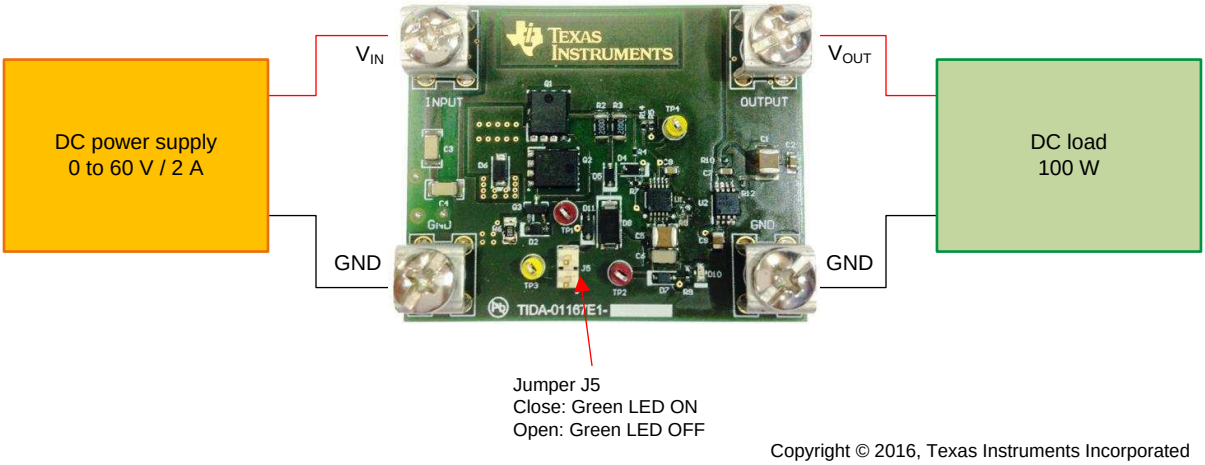
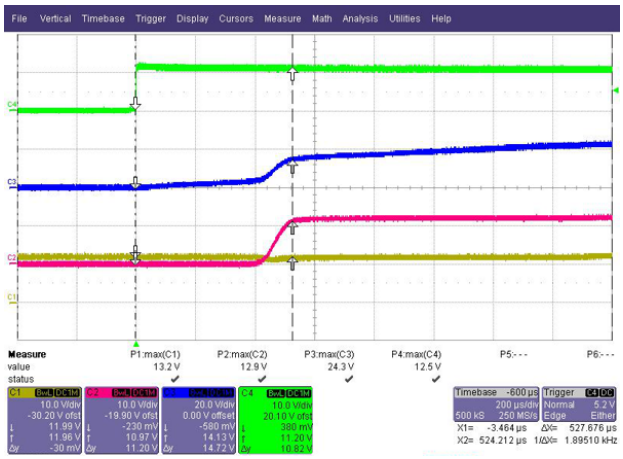


Figure 18. Test Setup

To check the performance of the LM5060-Q1, This TI Design has been tested for 12-V and 24-V applications.

4.1 Operational Tests

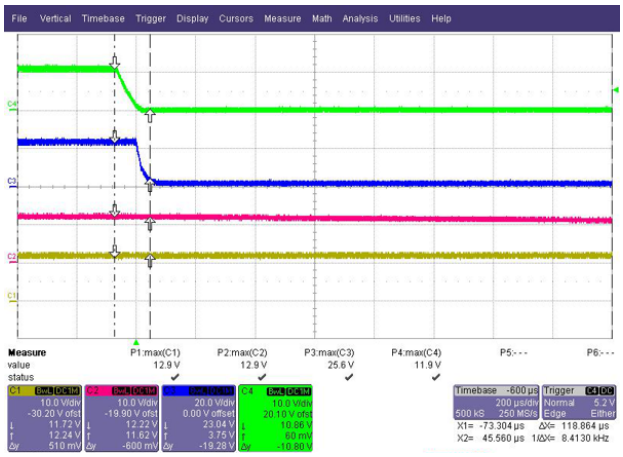


CH1: Input
CH2: Output
CH3: Gate
CH4: Enable

NOTE: Turnon behavior of the LM5060-Q1 has been checked.

Input = 12 V
Gate on-time ≈ 527 µs

Figure 19. Turnon Behavior at 12 V

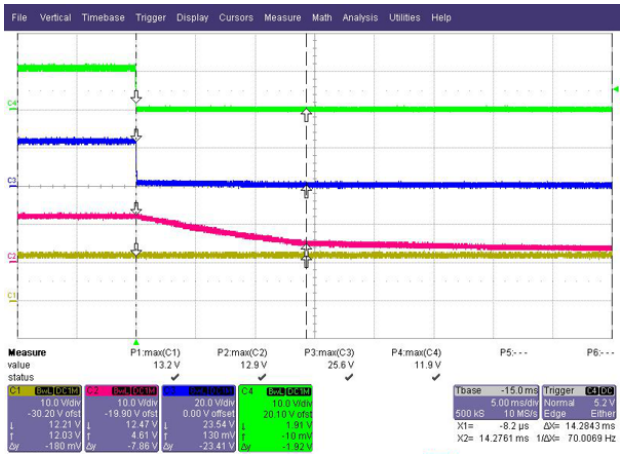


CH1: Input
CH2: Output
CH3: Gate
CH4: Enable

NOTE: Turnoff behavior of the LM5060-Q1 has been checked.

Input = 12 V
Gate off-time ≈ 118 µs

Figure 20. Gate Turnoff Behavior at 12 V

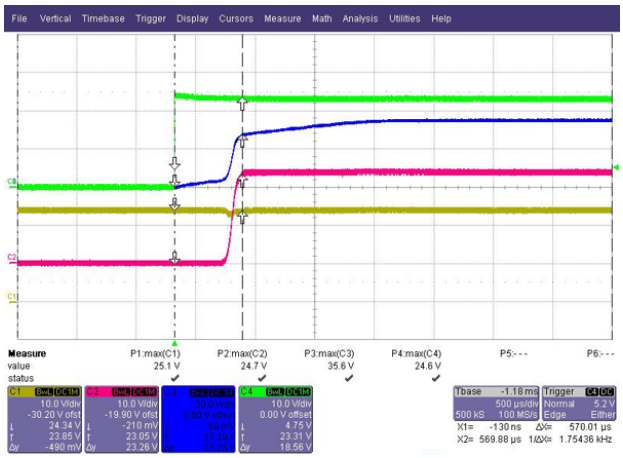


CH1: Input
CH2: Output
CH3: Gate
CH4: Enable

NOTE: Turnoff behavior of the LM5060-Q1 has been checked.

Input = 12 V
Output off-time ≈ 14.28 ms

Figure 21. Output Turnoff Behavior at 12 V

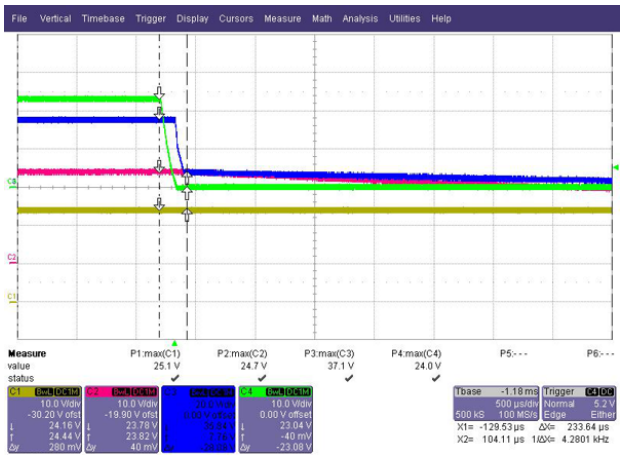


CH1: Input
CH2: Output
CH3: Gate
CH4: Enable

NOTE: Turnon behavior of the LM5060-Q1 has been checked.

Input = 24 V
Gate on-time ≈ 570 µs

Figure 22. Gate Turnon Behavior at 24 V

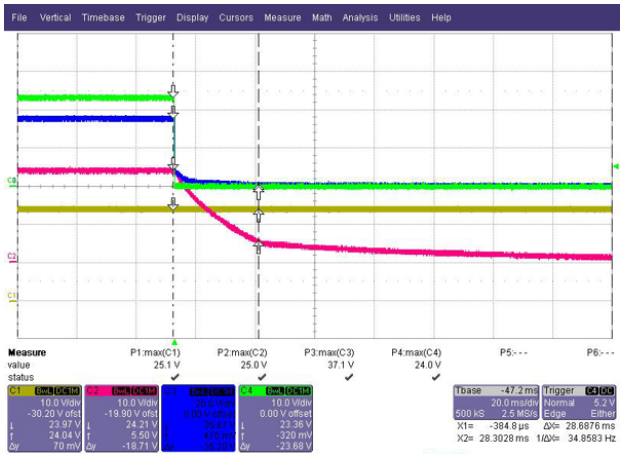


CH1: Input
CH2: Output
CH3: Gate
CH4: Enable

NOTE: Turnoff behavior of the LM5060-Q1 has been checked.

Input = 24 V
Gate off-time ≈ 233 µs

Figure 23. Gate Turnoff Behavior at 24 V



CH1: Input
CH2: Output
CH3: Gate
CH4: Enable

NOTE: Turnoff behavior of LM5060-Q1 has been checked

Input = 24 V
Output off-time ≈ 28 ms

Figure 24. Output Turnoff Behavior at 24 V

4.2 Transient Tests

Figure 25 shows the setup for transient testing.

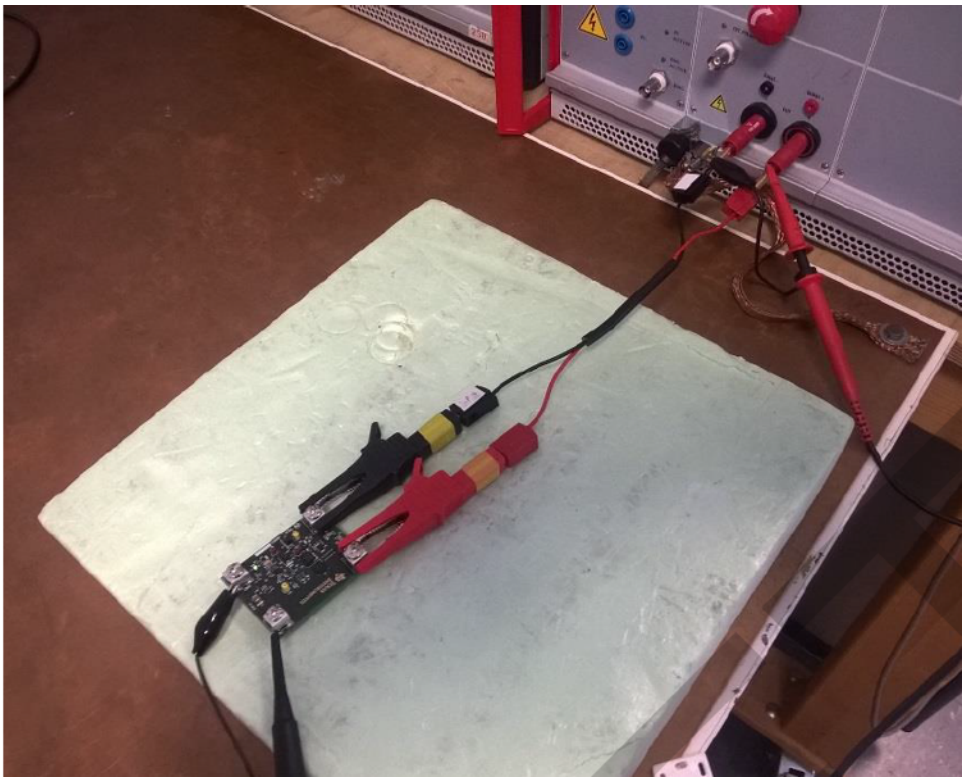
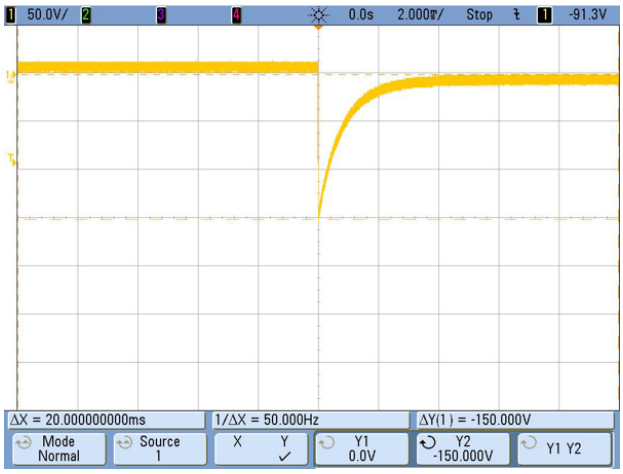


Figure 25. Setup for Transient Tests

The transient tests used the following equipment:

- Teseq PA5840 Power Amplifier and Battery Simulator
- Teseq NSG 5500 Automotive Transient Immunity Tests
- Agilent Technologies Oscilloscope

4.2.1 12-V Battery

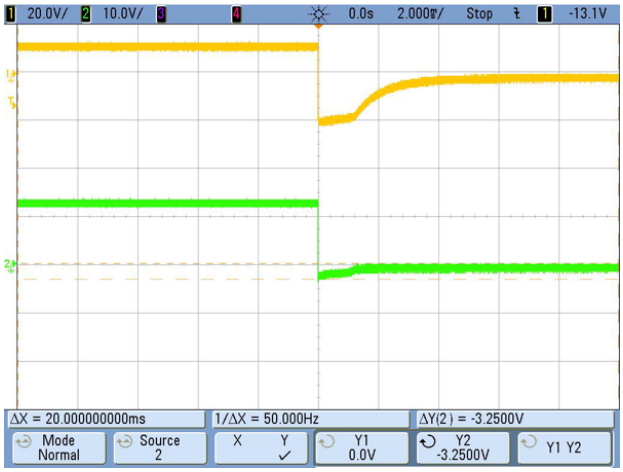


CH1: Generator source

NOTE: ISO7637-2 Pulse 1 from generator

ISO7637-2 Pulse 1
Level: 4
Number of pulses: 500
U_S: 150 V
t_r: 1 µs
t_d: 2 ms

Figure 26. ISO7637-2 Pulse 1

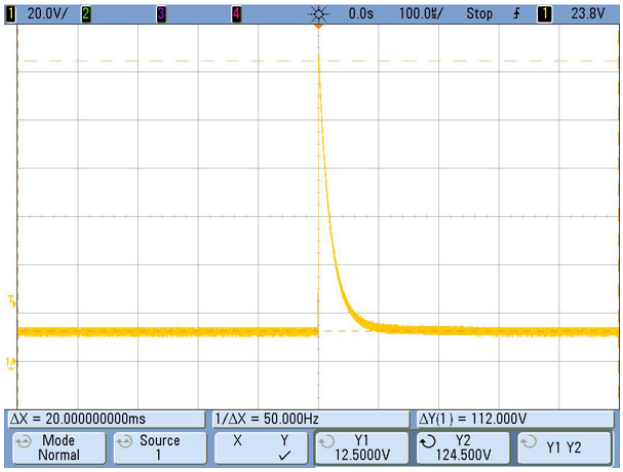


CH1: Input
CH2: Output

NOTE: Max negative output voltage is –3.25 V.

ISO7637-2 Pulse 1
Level: 4
Number of pulses: 500
U_S: 150 V

Figure 27. TIDA-01167 Pulse 1 Behavior at 12 V

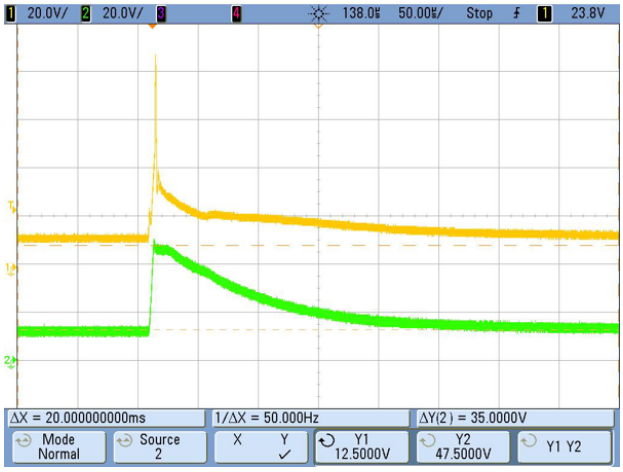


CH1: Generator source

NOTE: ISO7637-2 Pulse 1 from generator

ISO7637-2 Pulse 2a
Level: 4
Number of pulses: 500
U_S: 112 V
t_r: 1 µs
t_d: 0.05 ms

Figure 28. ISO7637-2 Pulse 2a

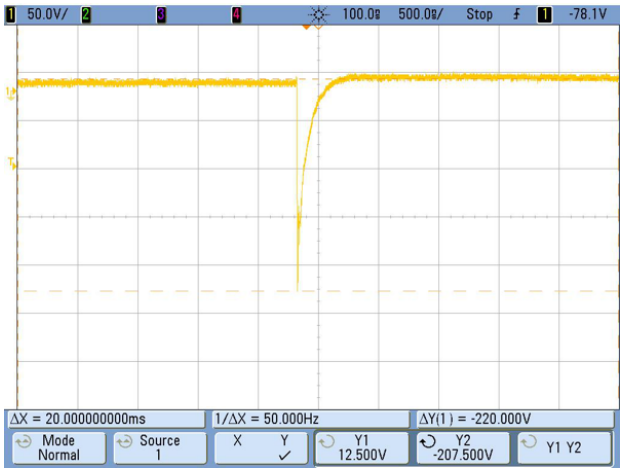


CH1: Input
CH2: Output

NOTE: Max transient voltage is 35 V.

ISO7637-2 Pulse 2a
Level: 4
Number of pulses: 500
U_S: 112 V

Figure 29. TIDA-01167 Pulse 2a Behavior at 12 V

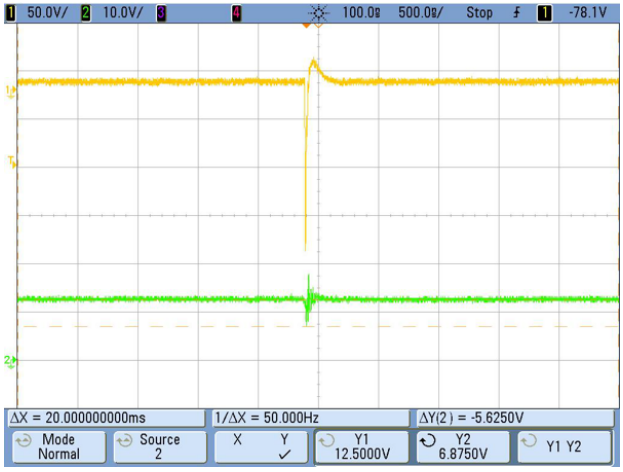


CH1: Generator source

NOTE: ISO7637-2 Pulse 1 from generator

ISO7637-2 Pulse 3a
Level: 4
Duration of pulses: 10 min
U_S: 220 V
t_r: 5 ns
t_d: 150 ns

Figure 30. ISO7637-2 Pulse 3a

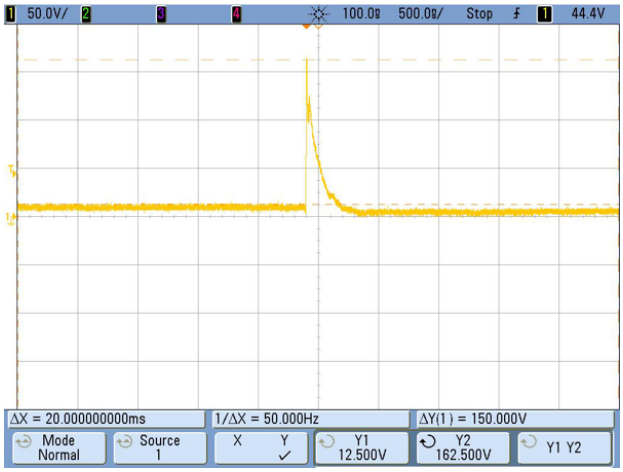


CH1: Input
CH2: Output

NOTE: Max transient voltage is 5.62 V.

ISO7637-2 Pulse 3a
Level: 4
Duration of pulses: 10 min
U_S: 220 V

Figure 31. TIDA-01167 Pulse 3a Behavior at 12 V

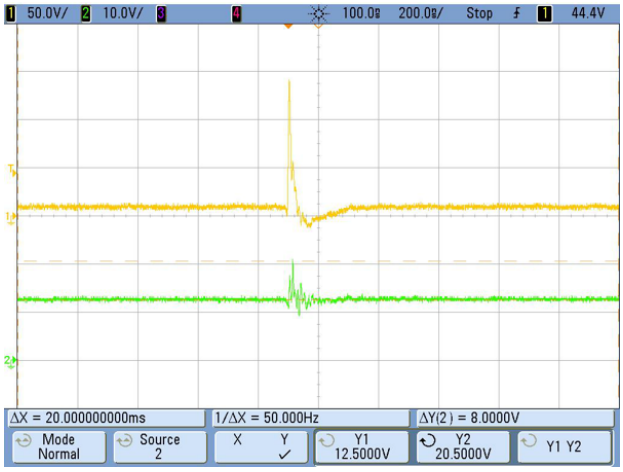


CH1: Generator source

NOTE: ISO7637-2 Pulse 1 from generator

ISO7637-2 Pulse 3b
Level: 4
Duration of pulses: 10 min
U_S: 150 V
t_r: 5 ns
t_d: 150 ns

Figure 32. ISO7637-2 Pulse 3b

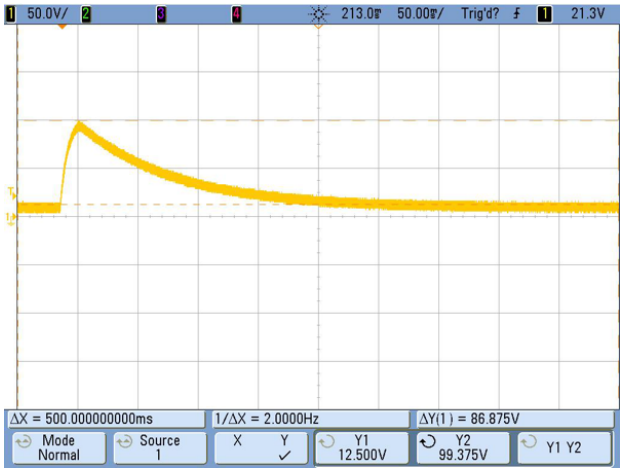


CH1: Input
CH2: Output

NOTE: Max transient voltage is 8 V.

ISO7637-2 Pulse 3b
Level: 4
Duration of pulses: 10 min
U_S: 150 V

Figure 33. TIDA-01167 Pulse 3b Behavior at 12 V

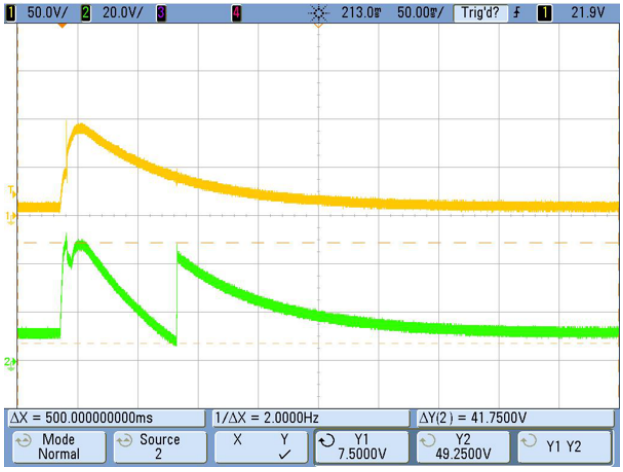


CH1: Generator source

NOTE: ISO16750-2 unsuppressed load dump from generator

ISO16750-2 unsuppressed load dump
U_S: 101 V (87+14)
R_i: 0.5 Ω
t_r: 10 ms
t_d: 200 ms

Figure 34. ISO16750-2 Pulse 3b



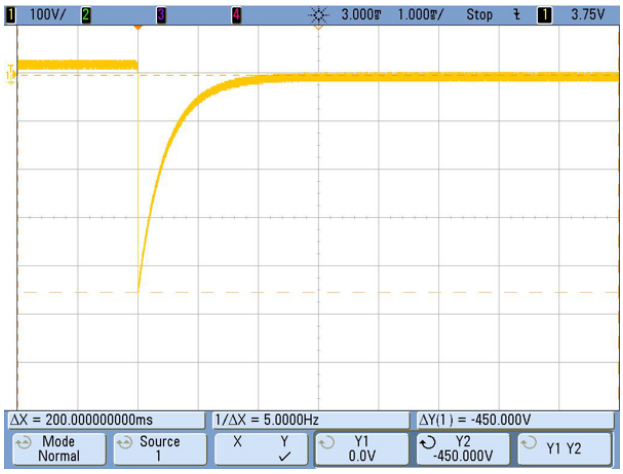
CH1: Input
CH2: Output

NOTE: Output max voltage is 41.75 V and min voltage is 7.5 V. Class A operation is possible as output voltage is in operating range for the 12-V system.

ISO16750-2 unsuppressed load dump
U_S: 101 V (87+14)
R_i: 0.5 Ω

Figure 35. TIDA-01167 Behavior 12-V Unsuppressed Load Dump

4.2.2 24-V Battery

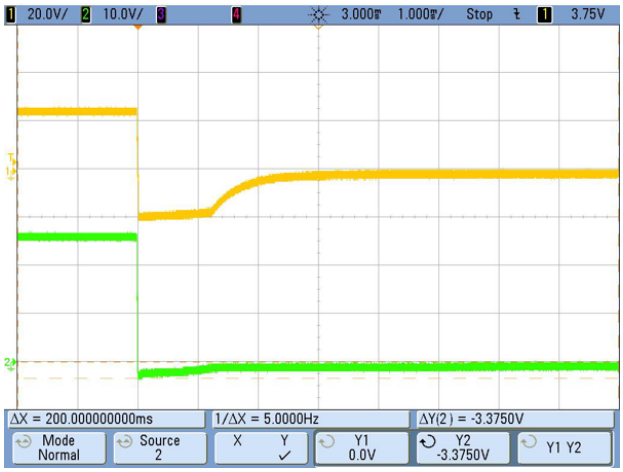


CH1: Generator source

NOTE: ISO7637-2 Pulse 1 from generator

ISO7637-2 Pulse 1
Level: 3
Number of pulses: 500
U_S: 450 V
t_r: 3 µs
t_d: 1 ms

Figure 36. ISO7637-2 Pulse 1

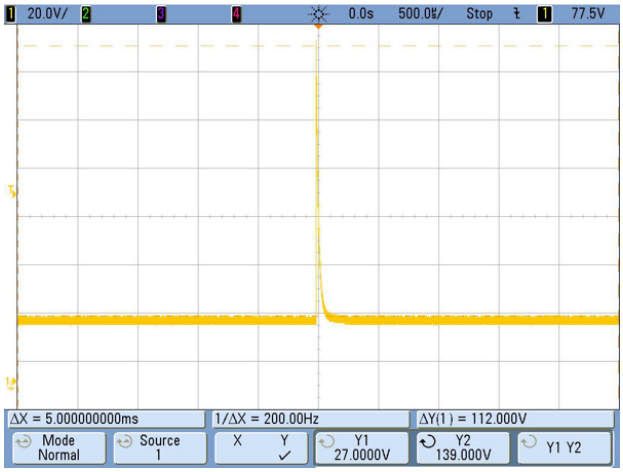


CH1: Input
CH2: Output

NOTE: Max negative output voltage is –3.37 V.

ISO7637-2 Pulse 1
Level: 3
Number of pulses: 500
U_S: 450 V

Figure 37. TIDA-01167 Pulse 1 Behavior at 24 V

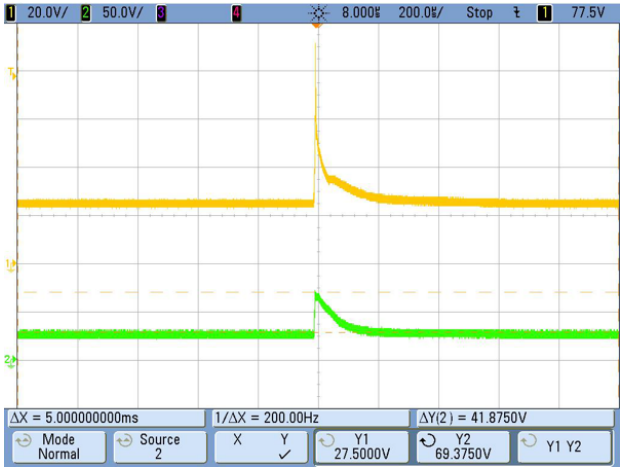


CH1: Generator source

NOTE: ISO7637-2 Pulse 1 from generator

ISO7637-2 Pulse 2a
Level: 4
Number of pulses: 500
U_S: 112 V
t_r: 1 µs
t_d: 0.05 ms

Figure 38. ISO7637-2 Pulse 2a

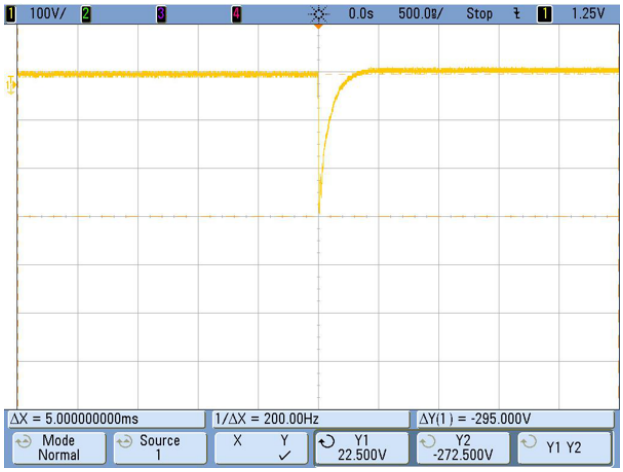


CH1: Input
CH2: Output

NOTE: Max transient voltage is 41.8 V.

ISO7637-2 Pulse 2a
Level: 4
Number of pulses: 500
U_S: 112 V

Figure 39. TIDA-01167 Pulse 2a Behavior at 24 V

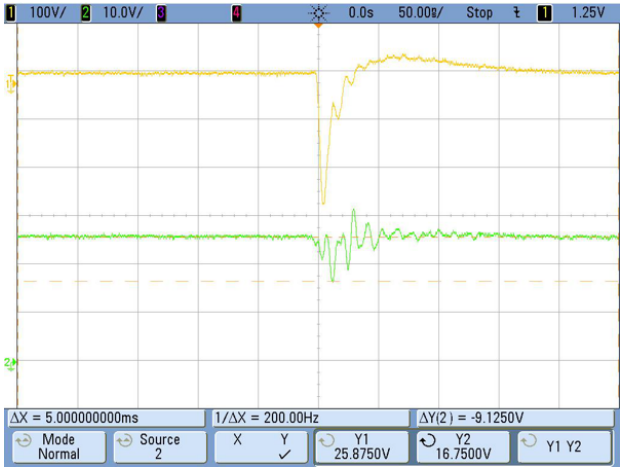


CH1: Generator source

NOTE: ISO7637-2 Pulse 1 from generator

ISO7637-2 Pulse 3a
Level: 4
Duration of pulses: 10 min
U_S: 300 V
t_r: 5 ns
t_d: 150 ns

Figure 40. ISO7637-2 Pulse 3a

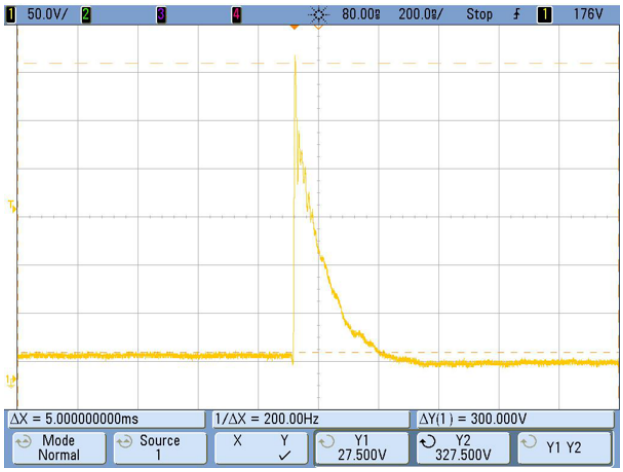


CH1: Input
CH2: Output

NOTE: Max voltage dip is 9.12 V.

ISO7637-2 Pulse 3a
Level: 4
Duration of pulses: 10 min
U_S: 300 V

Figure 41. TIDA-01167 Pulse 3a Behavior at 24 V

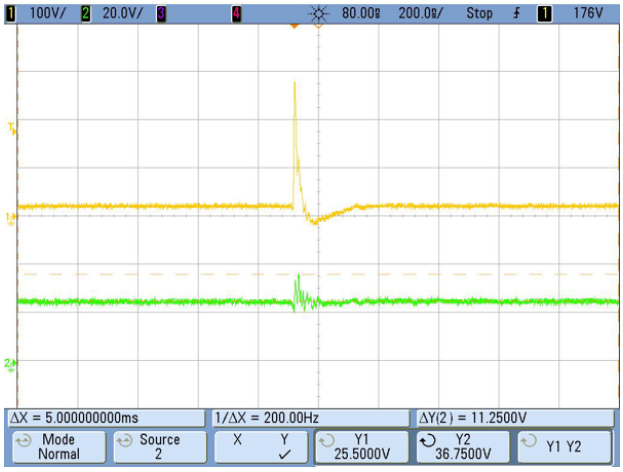


CH1: Generator source

NOTE: ISO7637-2 Pulse 1 from generator

ISO7637-2 Pulse 3b
Level: 4
Duration of pulses: 10 min
U_S: 300 V
t_r: 5 ns
t_d: 150 ns

Figure 42. ISO7637-2 Pulse 3b

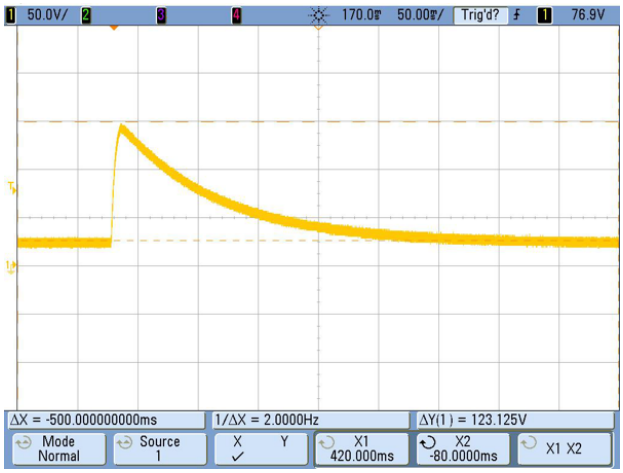


CH1: Input
CH2: Output

NOTE: Max transient voltage is 11.2 V.

ISO7637-2 Pulse 3b
Level: 4
Duration of pulses: 10 min
U_S: 300 V

Figure 43. TIDA-01167 Pulse 3b Behavior at 24 V

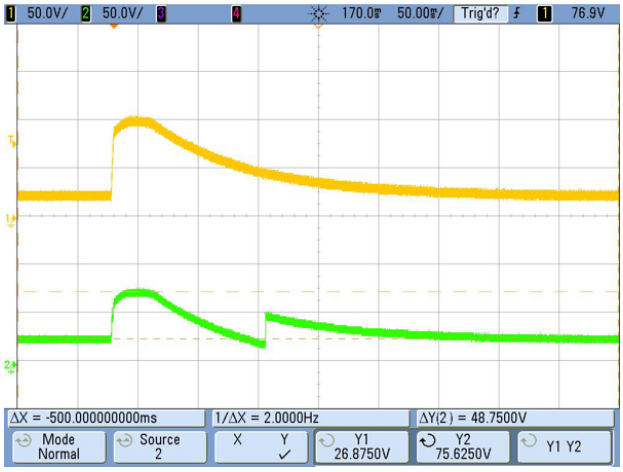


CH1: Generator source

NOTE: ISO16750-2 unsuppressed load dump from generator

ISO16750-2 unsuppressed load dump
U_S: 150 V (123.1+27)
R_i: 4 Ω
t_r: 10 ms
t_d: 200 ms

Figure 44. ISO16750-2 Unsuppressed Load Dump 24 V



CH1: Input
CH2: Output

NOTE: Output max voltage is 75 V and min voltage is 26.8 V. Class A operation is possible as output voltage is in operating range for the 24-V system.

Take care in the design for maximum operating voltage of devices.

ISO16750-2 unsuppressed load dump
U_S: 150 V (123.1+27)
R_i: 4 Ω
t_d: 200 ms

Figure 45. TIDA-01167 Unsuppressed Load Dump Behavior for 24 V

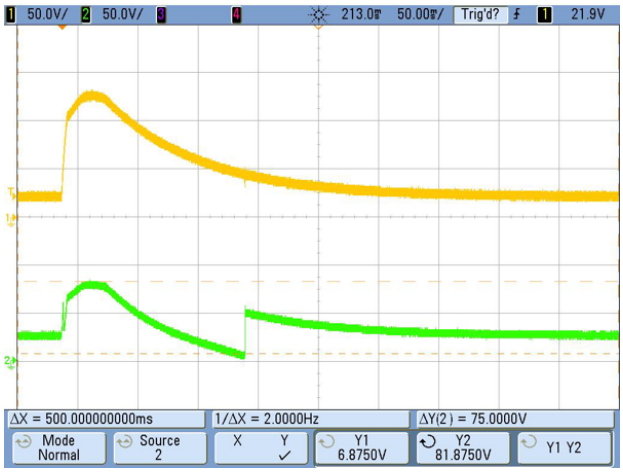


Figure 46. TIDA-01167 Unsuppressed Load Dump Behavior for 24 V

CH1: Input
CH2: Output

NOTE: Output max voltage is 81 V and min voltage is 6.8 V. Class B operation is possible.

Take care in the design for maximum operating voltage of devices.

ISO16750-2 unsuppressed load dump
U_S: 175 V (148+27)
R_i: 4 Ω
t_d: 200 ms

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01167.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01167.

5.3 PCB Layout Recommendations

PCB layout has to be done with appropriate measures to ensure the smooth operation of functionality for input protection:

1. Check the series path tracks for power dissipation, set the layer thickness and area appropriately
2. Place vias appropriately to handle the conduction currents.
3. Place C3 and C4 very close to the connector.
4. Place D1, D2, D3 very closely and appropriately near to the connector.

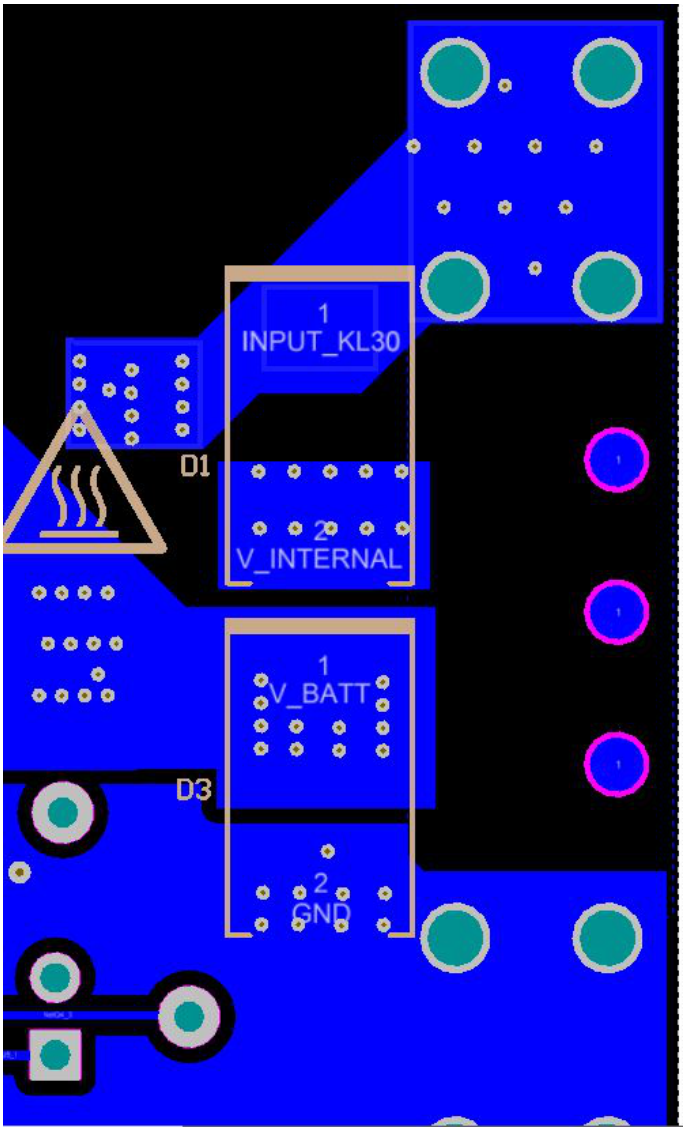


Figure 47. TVS Diodes Placement

5. Place decoupling capacitors near to ICs.
6. Place Q1 and Q2 close together.

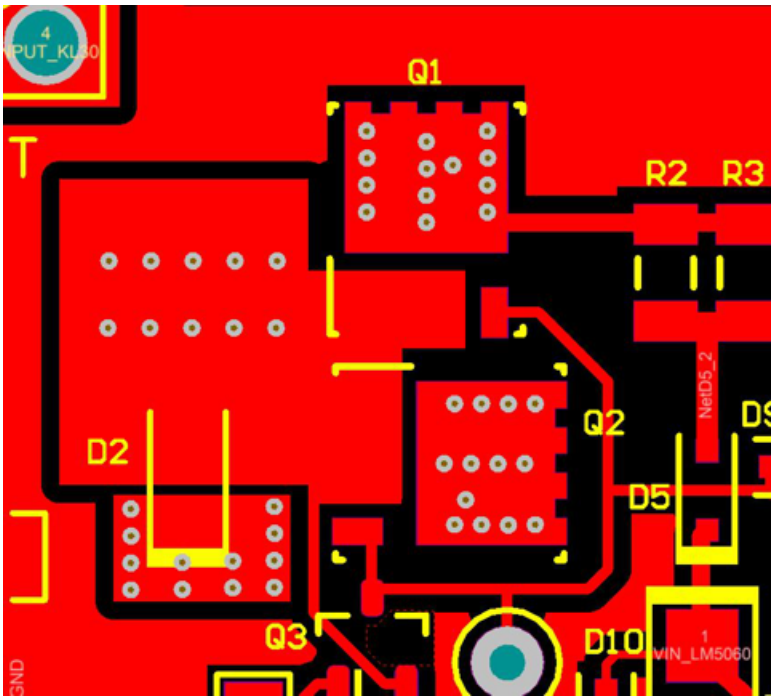


Figure 48. Q1,Q2 Placement

7. Connections from sense pin and output pins should be short and noise free.
8. Timer capacitor C7 should be near to U1 with low resistance to ground.
9. Place C5 and C6 near to U1, C9 and C10 near to U3 , C8 near to U2.
10. C1 and C2 should be placed close to the output pins.
11. Place the current sensing device and shunt on the same side of the PCB.
12. Follow layout guidelines for U1 and U3.

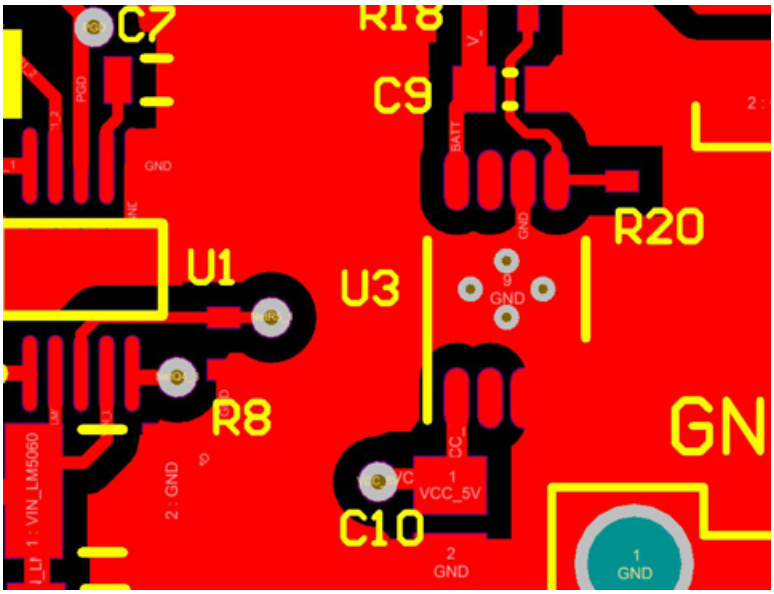


Figure 49. U1 and U3 Layout

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01167.

5.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01167.

5.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01167.

6 Related Documentation

1. Texas Instruments, LM5060-Q1 Hotswap Design Calculator (SLVC667)
2. Texas Instruments, *Hot Swap Calculator Tutorial: Steps 1 & 2 – Operating Conditions, Current Limit, & Circuit Breaker* (http://www.ti.com/general/docs/video/watch.tsp?entryid=4607940999001)
3. Texas Instruments, *Circuit protection overview*, TI Training (https://training.ti.com/circuit-protection-overview)

6.1 Trademarks

7 About the Author

RAMA KAMBHAM (Rama Chandra Reddy) is an automotive system engineer working in Texas Instruments Deutschland. Rama brings to this role his extensive experience in Battery Management Systems and Engine Management Systems in the automotive domain. Rama earned his bachelor of engineering degree from Osmania University Hyderabad, India.

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