Understanding Failure Modes in Isolators

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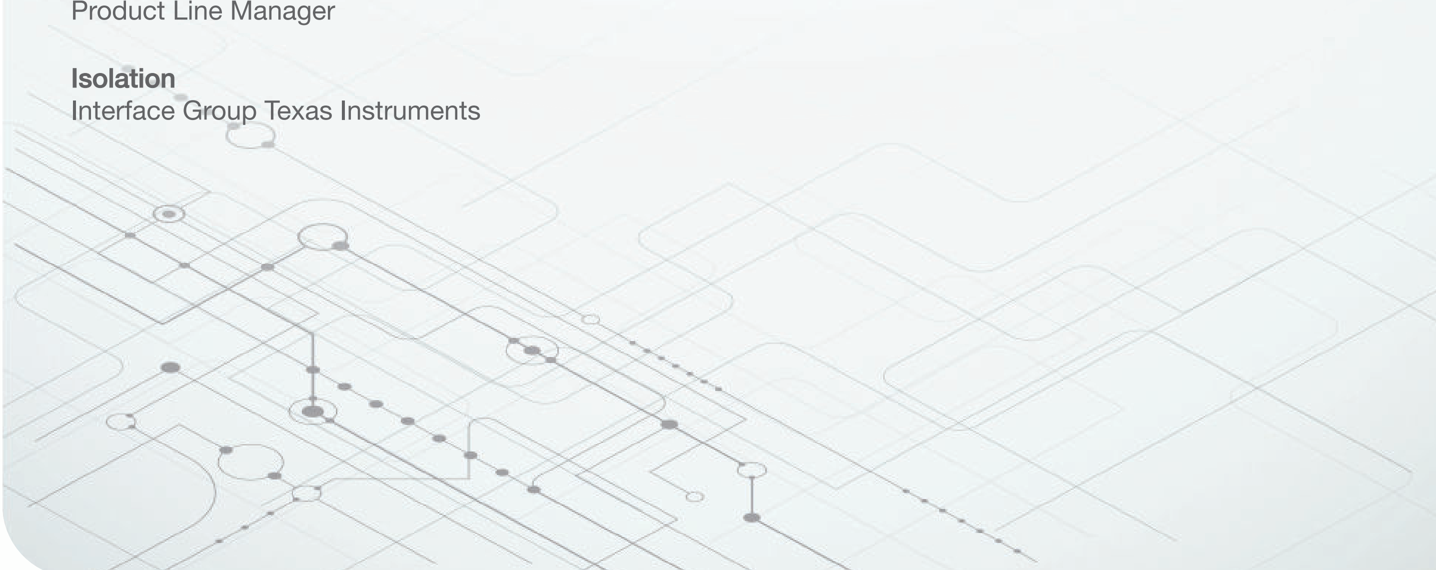

Analyzing how isolators fail under high voltage, high current stress fault conditions is important in order to determine if additional measures are required to prevent an electrical hazard.

Isolators are devices that minimize direct current (DC) and unwanted transient currents between two systems or circuits, while allowing data and power transmission between the two. In most applications, in addition to allowing the system to function properly, isolators also act as a barrier against high voltage. For example, in the motor drive system shown in **Figure 1**, the isolated insulated gate bipolar transistor (IGBT) gate drivers level shift low-voltage signals from the control module to IGBT gate-drive controls referenced to the inverter outputs. At the same time, they also form a protective barrier between the high voltage (DC bus, inverter outputs, and input power lines) and the control module, which may have human accessible connectors and interfaces.

In high-voltage applications, failure of the isolation barrier can result in a potential hazard to human operators, or cause damage to sensitive control circuitry leading to further system malfunction. Therefore, it is important to understand what may cause the isolator to fail, both under normal and fault conditions. You also need to know the nature of the failure in each case in order to check if additional measures are required to prevent an electrical hazard.

In this paper, we discuss two possible failure modes of isolators. The first is when the voltage across the isolation barrier exceeds the isolator's rated limits. The second is when circuits or components integrated in the isolator close to the isolation barrier are damaged by a combination of high voltage and high current. Potentially this can cause damage to the isolation barrier. In our analysis, we consider the latest reinforced isolation technology from TI and traditional optocouplers as examples. We show that while all isolators "fail short" for the first failure mode, TI isolators reduce the likelihood of failure because of higher isolation performance. We also show through analysis and test results that TI reinforced isolators "fail open" for the second failure mode.

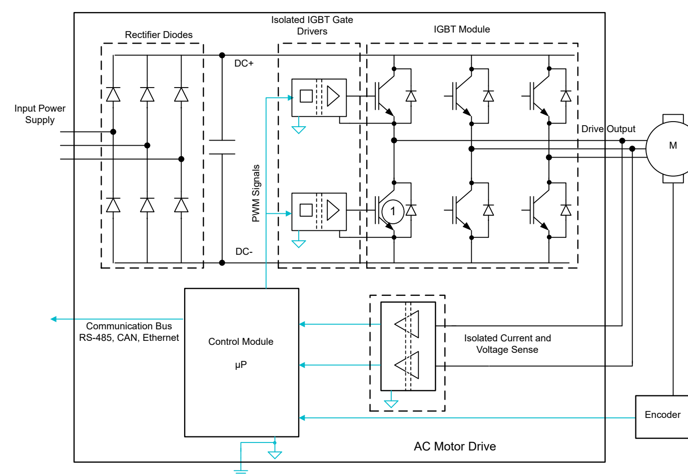

Figure 1. *Simplified block diagram of an AC motor drive.*

Failure mode 1: High voltage across the isolation barrier

An example of an isolator configuration is shown in **Figure 2**. The isolator has two sets of pins. One set is on side 1 and the other set is on side 2. In normal operation, the pins on side 1 are all low voltage with respect to GND1; and the pins on side 2 are all low voltage with respect to GND2. The power dissipated in the isolator depends on voltages and currents applied to the isolator's pins. In normal operation, power is maintained below the maximum limits specified in the isolator's data sheet. Very high voltage can exist between GND1 and GND2.This voltage appears across the isolator's internal isolation barrier.

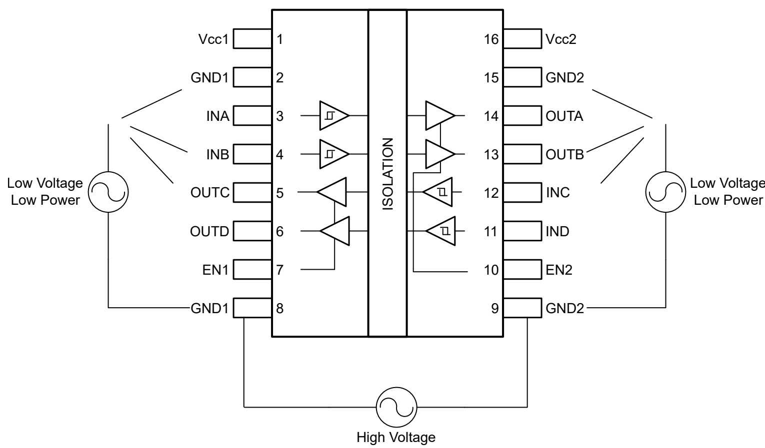

***Figure 2.** Example normal operating configuration of an isolator.*

Isolators are designed to withstand high voltage transient profiles of different magnitude and duration. Correspondingly, the isolation performance of the isolator is quantified by several parameters. The 60-second isolation withstand voltage (V_{ISO} and V_{IOTM}) indicates tolerance to short duration overvoltage caused on the system supply lines by switching loads or faults. Repetitive peak or working voltage (V_{IOWM} and V_{IORM}) is the voltage that the isolator can withstand on a continuous basis throughout its operating lifetime. Surge withstand voltage (V_{IOSM}) represents tolerance to a particular transient profile (1.2/50 μs – see IEC 61000-4-5) that represents voltages induced on the power supply lines during direct and indirect lightning strikes.

For each parameter, the limit is set by the voltage value that causes the isolation barrier to break, creating a short circuit from one side of the isolator to another. These parameters are indicated in the isolator's datasheet and reflect the ability of the isolator to handle high voltage without damage. A detailed discussion of these parameters is presented in reference [1]. At the system level, for example for the motor drive system shown in **Figure 1**, the incoming supply lines do experience the different over-voltage profiles mentioned above. With one end of the isolated gate-driver galvanically connected to the AC lines, and the other end referenced to earth, it is clear that the isolation barrier in the gate-driver directly faces these stresses.

Figure 3 and **Figure 4** depicts these high-voltage stresses appearing across the isolation barrier, for example, using an optocoupler and a series capacitor reinforced isolator from TI. As the stress voltage increases beyond the isolators' safety limiting values, the isolation barrier can degrade, creating a low resistance path between sides 1 and 2. In the case of optocouplers, the isolation barrier is a combination of silicone and insulating tape; whereas in the case of isolators from TI, it is a series combination of two high voltage SiO_2 capacitors. In each case, since the rated limits are obtained by failing the isolation barrier, by definition, both isolators "fail short."

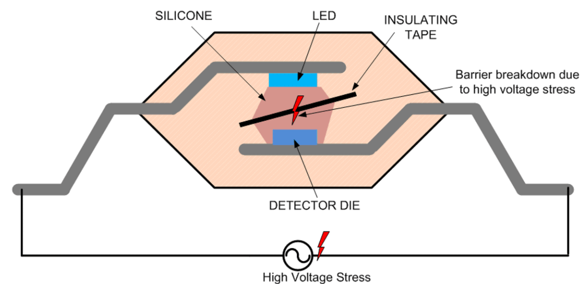

***Figure 3.** High-voltage stress across an optocoupler.*

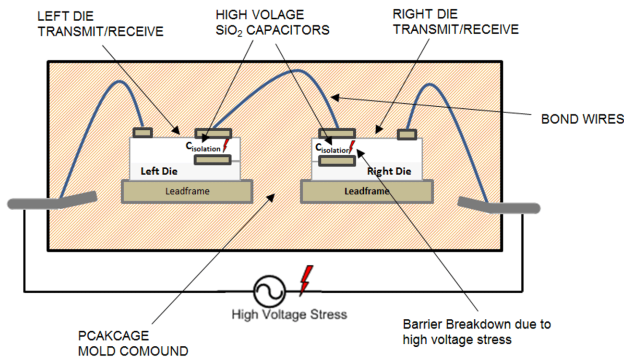

Figure 4. *High-voltage stress on a series-capacitor isolator.*

Depending on the application, end-equipment standards determine the specifications for isolators being used in the system. These standards ensure that isolators are stronger than the voltage stress levels they are likely to encounter across the isolation barrier in a realistic use case. For example, the IEC 61800-5-1 sets the requirements for isolators used in AC motor drive applications. Choosing an isolator that complies with the end-equipment standard minimizes the risk of breakdown of the isolation barrier through overvoltage during actual operation. However, if the isolator exceeds standard requirements, the risk can be reduced further.

Reinforced isolation devices from TI described in this paper use SiO_2 as the insulation material, which has a much higher breakdown strength (500 V/µm) than those used by competing solutions. For example, silicone and mold compound used in traditional optocouplers have breakdown strengths of 30 V/µm to 50 V/µm. TI reinforced isolators are also built using a precision semiconductor fabrication process, leading to a tight control on dimensions and spacing. Due to these two factors, TI devices have very high isolation performance for a given package. They effectively address temporary over voltages and surges as well as continuous high-voltage operation for many years. For example, TI Isolators in 16-SOIC packages have 50 percent higher working voltage than similar competing solutions. Further details regarding isolation performance of TI isolators can be found in the corresponding product data sheets, and in reference [1].

For a given application, TI reinforced isolation devices can provide crucial margin, even beyond the requirements mandated by the end equipment standards, which minimizes the likelihood of failure mode 1. A discussion of the IEC 61800-5-1 standard and a performance comparison of TI isolators against the requirements of this standard are provided in reference [2].

Failure mode 2: A combination of high voltage and high current close to the isolation barrier

Under abnormal or fault events, it is possible that the voltage or currents on one side of the isolator can be very high with respect to the ground on the same side (see Figure 5). One example of this is a short circuit event on a low-impedance output pin. Another example is a short circuit of any pin to a high-voltage DC bus line resulting in electrical breakdown. These are high-power events since high voltages and high currents are simultaneously present.

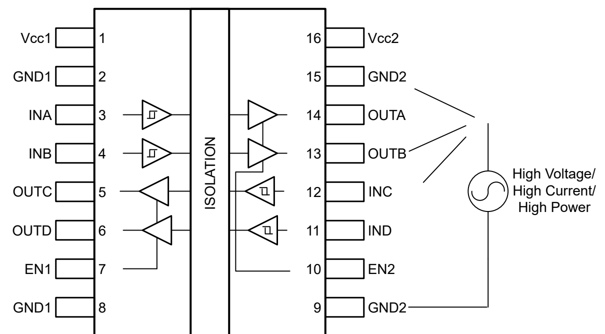

Figure 5. *High-power dissipation on one side of the isolator.*

When these events occur, electrical over stress (EOS) or internal heating can cause the isolation barrier to degrade. For example, if the optocoupler in Figure 6 has a high power event on side 2, it can cause heating or EOS on the detector die. This damage can easily extend into the insulation material, which can degrade isolation performance. It is fair to assume that the insulation is not completely destroyed, but at the same time it is difficult to quantify exactly how much insulation is left.

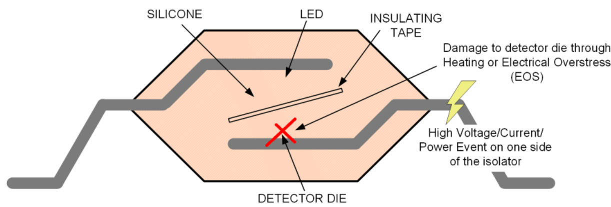

Figure 6. *High-power dissipation on one side of the isolator.*

Looking at **Figure 7** for a series capacitor-based isolator, a high-voltage/high-power event on side 2 could damage the right die, and along with it the isolation capacitor that is part of the right die. However, due to the interceding mold compound, the damage does not extend to the left die nor to the isolation capacitor placed on that die. This maintains isolation while preserving roughly half of the original insulation. For instance, if the original isolator is rated for reinforced isolation, after the high-power event, it can be expected to retain full isolation rating of one capacitor. Therefore, while the isolator "fails open," the "basic insulation" is still maintained.

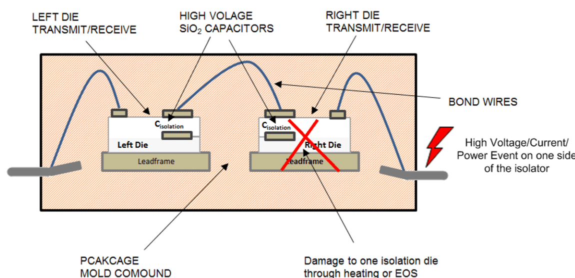

Figure 7. *High-power dissipation on one side of the isolator.*

One way to prevent failure mode 2 is to ensure through external means, for example through current limited power supplies, that even under fault events the heat dissipated inside the isolator is limited to a certain safe limit. This limit is specified through "safety limiting values" for current and power in isolator data sheets, below which the isolation performance remains intact.

However, such current limits are not always feasible to implement. Going back to **Figure 1**, if the IGBT (1) suffers from a collector to gate breakdown, the high voltage of the DC bus appears at the gate-driver output pin and causes electrical overstress on circuitry connected to that pin. There is no easy way to prevent this from happening at the system level. In such scenarios, the "fail open" behavior of

TI reinforced isolators greatly enhances the system's electrical safety.

Failure mode 2: Test results

To verify that TI reinforced isolation technology exhibits a "fail open" behavior for stress conditions where the safety-limiting current or power parameters are violated, several tests were performed. For experiments 1 and 2, **ISO5851**, a reinforced isolated gate-driver, and **ISO7841**, a reinforced quad-channel digital isolator were chosen.

In experiment 1, the isolator's output pins were short circuited, while raising the isolator's supply voltage until the isolator was no longer functional.

In experiment 2, using a surge generator, a repetitive high-voltage strikes (1 kV and 2 kV) was applied to one-side of the isolator. This was to simulate the impact of short circuits to high-voltage DC buses in motor drive, solar inverter, and other similar applications.

TI has also implemented a new "fail open" feature on the input die for products such as the **ISOM8710** Opto-emulator where the isolation is based on a 3-die solution as shown in **Figure 8**. This new feature ensures that the insulation barrier and output-die are protected under input-side EOS events. **Figure 9** provides a cross-sectional view of the 3-die opto-emulator with the input fail open IP.

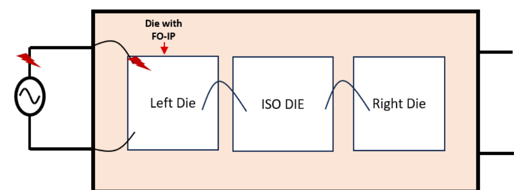

Figure 8. *High voltage stress applied on one side of the 3-die isolator. The left die designed with fail-open (FO) IP ensures integrity of ISO die and the right die under EOS events.*

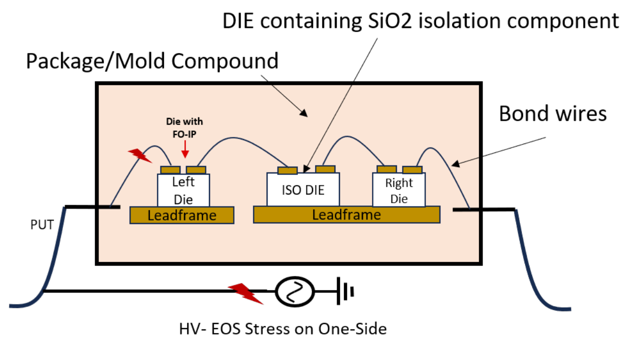

Figure 9. *Cross-sectional view of the 3-die opto-emulator with Fail-Open IP.*

To demonstrate the fail open feature, input die with three EOS types was stressed in experiments 3-5 and looked at isolation integrity post stress.

In experiment 3, EOS voltage was applied to the input-side (between Anode and Cathode) at room and high temperature using a DC supply through different source impedances for 10 minutes, which causes the input-die to fail-open. This emulates a DC-EOS event that can persist until system shutdown. Next, EOS was applied for 12 hours to ensure input-die remains fail-open even for prolonged EOS stress on the open device. Finally, ramp to breakdown test (RTB) was conducted on the insulation barrier to check isolation integrity post functional failure caused by EOS event on the left die. Figure 10 shows the RTB setup where we apply HV stress across isolation barrier.

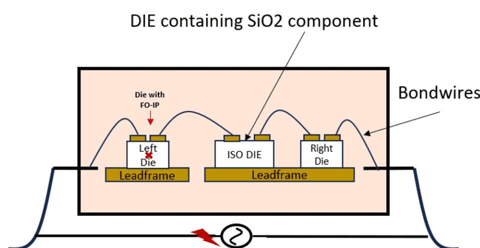

Figure 10. *HV Ramp-to-Breakdown (RTB) across Isolation.*

In experiment 4, the EOS-input is changed from experiment 3 with similar test procedure. We connected pre-charged capacitors to study the impact of capacitor discharge on the input side of the isolation.

In experiment 5, a current source was applied to the input side and ramped it up until fail open on the input side. Experiments 3 to 5 simulate DC-supply bus shorts to the input side in the above applications.

Fail-open feature is also implemented on the output-die pins (VDD, OUT1, and OUT2) in ISO-comparators such as AMC23C10 where the isolation is based on single die reinforced isolation capacitor approach as shown in Figure 6. Experiments 3-5 were also performed on these parts to ensure input die and isolation are both intact post functional failure of output die from EOS events. The results are summarized in Table 1.

Table 1 lists the results of these experiments. In all cases, after the high-power stress, all isolators maintained a high-impedance between side 1 and side 2. That is, they “fail open.” Additionally, ISO5851 and ISO7841 were further tested for basic isolation rating of 3 kVRMS for 60 seconds. All devices were able to withstand this voltage without breakdown. ISOM8710 were further tested in ramp-to-breakdown in oil post stress. In other words, basic isolation was preserved after the high-power test. As an extreme test, 50 2-kV surge impulses of both positive and negative polarity were applied to two units each of the gate driver and digital isolator. Even after such a severe stress, the isolators maintained high impedance between side 1 and side 2, maintained basic isolation, and “failed open.”

Experiment number	Device	Test description	Number of devices	Observation	Post-stress RIO	Post-stress VISO 60-s test, 3 kVRMS
1,2	ISO5851	Gate-driver output shorted to side-2 ground. Supply was raised to 50 V until device became damaged	5	Die 3 damaged	>1TΩ	Passed
		2kV surge on gate-driver output, 5 times each polarity (+ve and - ve)	5	Die 3 damaged	>1TΩ	Passed
		2kV surge on gate-driver output, 50 times each polarity (+ve and - ve)	2	Die 3 damaged	>1TΩ	Passed
1,2	ISO7841	All side-2 pins shorted to side-2 ground or supply, or were left floating. Supply was raised to 25 V until the device became damaged.	5	Die 2 damaged	>1TΩ	Passed
		1kV or 2kV surge on all side-2 pins, 5 times each polarity (+ve and - ve)	4	Die 2 damaged	>1TΩ	Passed
		2kV surge on all side-1 pins, 5 times each polarity (+ve and - ve)	2	Die 1 damaged	>1TΩ	Passed
		2kV surge on all side-1 pins, 50 times each polarity (+ve and - ve)	2	Die 1 damaged	>1TΩ	Passed
		2kV surge on all side-1 pins, 500 times each polarity (+ve and - ve)	1	Die 2 damaged	>1TΩ	Passed
3,4,5	ISOM8710	EOS applied to input side between pin-1 to ground with output side open. Different values of supply voltages up to 43 V and currents were tested until fail open on the input die. EOS was applied for 12 hours post fail and input die resistances were measured. Isolation integrity post stress was tested using RTB.	270	No isolation degradation, non-functional	>1TΩ	Passed
		Connect a pre-charged 2.2 mF cap (30 V, 3A) between pin1 to ground. If fail-short continue driving up to 3A until input die fail open. Isolation integrity post stress was tested using RTB.	5	No isolation degradation, non-functional	>1TΩ	Passed
		Apply graudally increasing current up to 3A to primary until input die fail open. In fail-short, continue feeding short until open. Isolation integrity post stress was tested using RTB.	5	No isolation degradation, non-functional	>1TΩ	Passed
3,4,5	AMC23C10	EOS applied to input side between pin-1 to ground with output side open. Different values of supply voltages up to 36 V and currents were tested until fail open on the input die. EOS was applied for 24 hours post fail and input die resistances were measured. Isolation integrity post stress was tested using RTB.	20 per pin 60 in total	No isolation degradation, non-functional	>1TΩ	Passed
		Connect a pre-charged 2.2 mF cap (30 V, 3A) between pin1 to ground. If fail-short continue driving up to 3A until input die fail open. Isolation integrity post stress was tested using RTB.	5	No isolation degradation, non-functional	>1TΩ	Passed
		Apply graudally increasing current up to 3A to primary until input die fail open. In fail-short, continue feeding short until open. Isolation integrity post stress was tested using RTB.	5	No isolation degradation, non-functional	>1TΩ	Passed

Table 1. *Summary of tests performed on TI reinforced isolators (gate drivers and isolated comparators) and TI opto-emulators to check if the devices experienced "fail open" post EOS stress.*

After the high-power stress was applied, some of these devices were de-capsulated and photographed to check the internal state of each (see **Figure 11** and **Figure 12**). The results are consistent with expectations from our failure analysis. While the die facing the high-power stress was substantially damaged, at least one-die with one isolation capacitor was completely preserved. This die was responsible for the "fail open" nature observed. In the case of ISO5851, being a three-die module, the damage was limited to the gate-driver die, and damage to the isolation barrier was minimal.

Other TI reinforced isolators

The analysis and results presented in this paper are equally applicable to other reinforced isolators from TI, including ISO77xx digital isolators, ISO1042 isolated CAN transceivers, UCC21520 and UCC53xx isolated gate-drivers, and AMC13xx isolated ΣΔ modulators and isolated amplifiers.

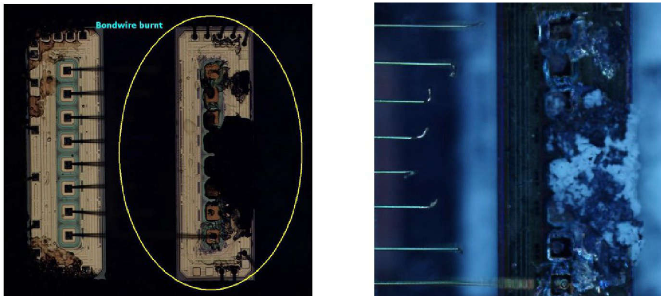

Figure 11. *EOS damage is limited to the die that suffers the high-power event (ISO7841).*

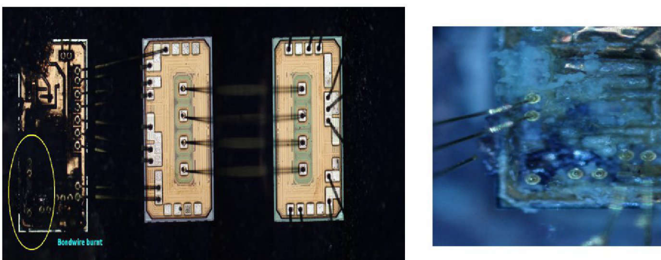

Figure 12. *EOS damage is limited to the driver-die that suffers the high-power event (ISO5841).*

Conclusion

In order to determine if additional precautions are needed to prevent electrical hazards at the system level, it is important to fully understand the failure modes of isolators used in high-voltage systems under both normal and fault conditions. Isolators, by definition, "fail short" when voltages across the isolation barrier exceed rated limits (**failure mode 1**). This failure mode can be avoided by choosing isolators that meet, preferably with margin, the specifications set forth by the relevant end equipment electrical safety standards. Because TI reinforced isolators offer the highest isolation performance available in the market today, they provide the highest margin against this type of failure mode. When the safety-limiting current or power limits of the isolators are violated (**failure mode 2**), the isolator's isolation barrier can potentially be compromised. For TI reinforced isolators that use series-capacitor isolation, the damage in this mode is limited to one capacitor. That leaves the other capacitor intact, causing these isolators to "fail open," preserving basic isolation."

References

1. Texas Instruments: Anant S Kamath, Kannan Soundarapandian. ***High-voltage reinforced isolation: Definitions and test methodologies***
2. Texas Instruments: Anant S Kamath, ***Isolation in AC Motor Drives: Understanding the IEC 61800-5-1 Safety Standard***
3. 61800-5-1 Ed. 2.0., Adjustable speed electrical power drive systems, safety requirements, electrical, thermal and energy, International Electrotechnical Commission (IEC), July 2007.
4. 60060-1:2010 Ed 3.0, High-voltage test techniques – Part 1: General definitions and test requirements. International Electrotechnical Commission (IEC), September 2010.
5. Download these data sheets: **ISO5851**, **ISO7841**.

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