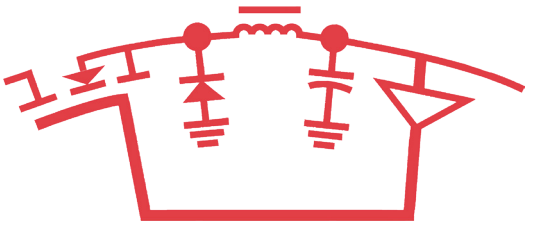

Power Supply Design Seminar

Power Factor Correction (PFC) Circuit Basics

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Power Factor Correction (PFC) Circuit Basics

Brent McDonald and Ben Lough

ABSTRACT

From laptop adapters to power tools, any end equipment powered from the AC grid represents a complex load where the input current is not always in phase with the instantaneous line voltage. As such, the end equipment consumes both real power as well as reactive power from the grid. The ratio between real, usable power (measured in watts) and the total real-plus-reactive power is known as the power factor. A power factor correction (PFC) circuit intentionally shapes the input current to be in phase with the instantaneous line voltage and minimizes the total apparent power consumed.

While this is advantageous to utility companies, a PFC circuit also provides benefits in end applications. This topic presents these benefits, how the PFC circuit can impact the AC-to-DC power-conversion architecture, common PFC circuit types, the benefits/disadvantages of different approaches and a PFC solution selection process based on end-equipment priorities.

I. Introduction

With the emergence of personal computing devices, such as laptops and smartphones, electronics have become essential components of everyday life. As the demand for smaller, more powerful electronics with longer battery life continues to grow, the need to charge or continuously power these devices continues to increase. This ever-growing demand for electrical power presents a unique challenge for AC power generation and distribution. To address this issue, many areas around the world have implemented voluntary programs, such as Energy Star, that require a minimum power factor (PF) for certain applications running at heavy loads. Other areas of the world have implemented even stricter mandatory requirements on the input current's total harmonic distortion (THD) in order to sell products within specific regions, such as the European Union. In order to meet these requirements, some products incorporate passive or active power factor correction (PFC) to minimize the total apparent power consumed by the electronic application. In this paper, the motivation of modern energy standards to mandate a high power factor is examined. Different active power factor correction approaches are examined and the characteristics of each power factor correction solution are analyzed regarding size, cost and performance.

II. Efficiency Standards and Power Factor Correction

The classical definition of power factor is defined as the ratio of real power measured in watts (W) consumed by a load divided by the total apparent power measured in volt-amperes (VA) circulating between the power source and load. For a DC input, the input current and input voltage are always in phase and, as such, maintains a power factor of 1. For an electronic application that is powered from the AC grid, the input current does not naturally follow the instantaneous AC line voltage.

To illustrate the importance of high power factor and input current harmonic distortion for meeting modern energy standards, examine the use case of an AC/DC laptop adapter requiring 60 W of input power. If the laptop adapter in this example is capable of maintaining an ideal power factor of 1, the shape of the input current perfectly follows the instantaneous line voltage with no phase delay, as shown in Figure 1.

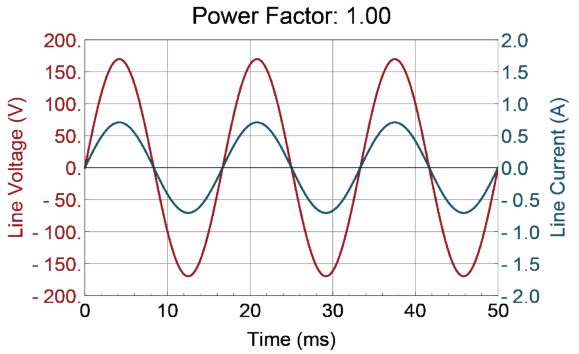

Figure 1 – Input voltage and current for PF=1.

For 60 W of input power at 115 V_{AC} input and PF=1.0, the RMS input current is equal to 521 mA. However, if a phase delay between the input current and input voltage is introduced to reduce the power factor to 0.4, more apparent power, and more circulating current, is required to deliver the same 60 W of real power, as shown in Figure 2.

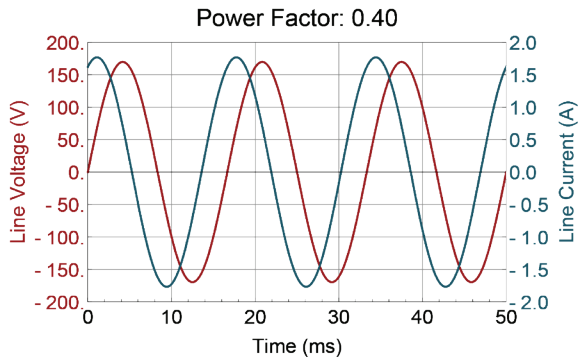

Figure 2 – Input voltage and current with PF=0.4 due to phase delay.

For the reduced power factor of 0.4, the RMS input current increases to 1.3 A. Regarding impacts to the electronic product, the laptop adapter with PF = 0.4 may require more expensive cabling to handle the increased circulating current, as illustrated in Figure 3.

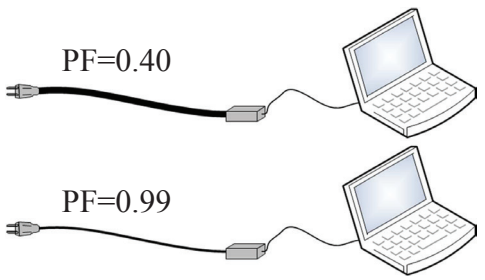

Figure 3 – Laptop cable comparison.

While an increase of 700 mA may seem insignificant for a single laptop adapter, consider the perspective of a US utility tasked with providing power at a national scale. For a power factor of 1, all the power generated by the utility is fully utilized by the load connected to the grid. For a power factor of 0.4, the generated power is not utilized effectively by the load and a significant portion of the generated power circulates in the system instead of being consumed by the load. The required amount of apparent power more than doubles in size due to the poor power utilization of the load. A common analogy is to compare power factor to a frothy glass of beer. The beer represents the power demand while the foam represents the unutilized power and the glass itself represents the generated power from the utility. In this analogy, power factor would represent the ratio between beer and foam. A high power factor would mean little to no foam in the glass and the generated power is well utilized. For a low power factor, a significant portion of the glass is filled with foam due to the poor power utilization. To obtain the same amount of beer as the high power factor scenario, a low power factor system would need a much taller glass to contain the extra foam. This analogy is meant to illustrate that a high power factor is advantageous for the utility as less generated power is needed to satisfy the same power demand.

As shown in the previous example, it is advantageous to maintain a high power factor in order to minimize the burden on the electrical grid. While this point is well understood, power factor and harmonic distortion requirements vary not only based on the classification of an electronic product but also differs from region to region.

While some requirements only define a minimum power factor at full load, other regulations pose requirements on input current harmonic distortion as these harmonic currents can cause voltage drops across the impedances of the power distribution network. To illustrate how loads can introduce harmonic currents into the AC grid, consider an AC to DC converter using a diode bridge to convert the AC line voltage to a rectified DC voltage , as illustrated in Figure 4. A capacitor is connected to the DC side of the

rectifier in order to limit the voltage ripple feeding the DC/DC converter. The diode bridge only conducts when the instantaneous line voltage exceeds the DC voltage on the capacitor plus the two diode drops of the bridge. This results in the diode bridge only conducting for a brief period of time over the line cycle.

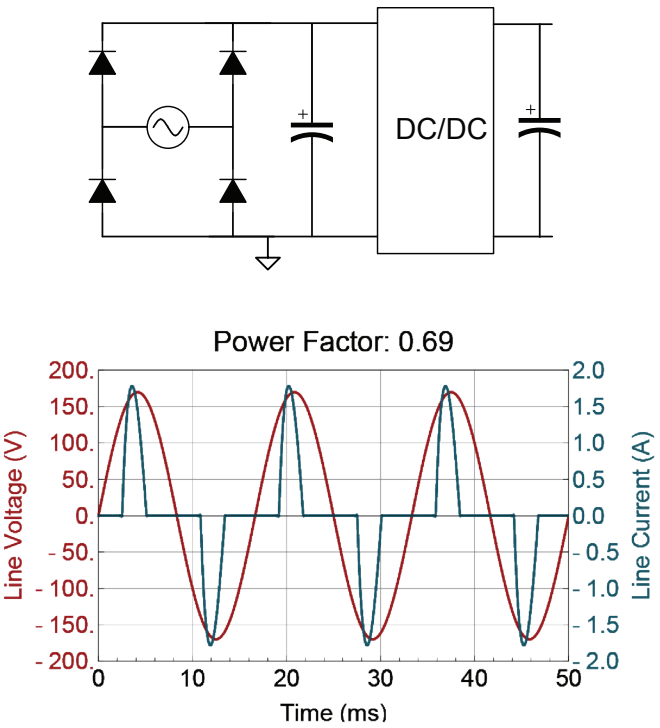

Figure 4 – AC/DC power supply input voltage and current.

This input current profile introduces a significant amount of harmonic content back into the AC line. Figure 5 shows a Fourier transform of the input current waveform as well as the IEC61000-3-2 Class D standard for harmonic limits of monitors, personal computers and televisions.

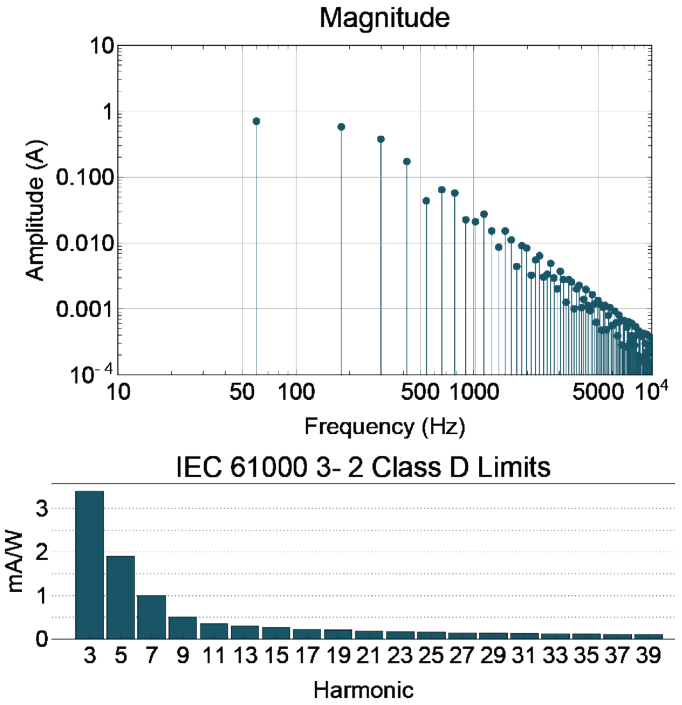

Figure 5 – Input current harmonic content and IEC61000-3-2 Class D limits.

Total harmonic distortion, often abbreviated as THD, is used to numerically describe the level of distortion to the AC line current. As shown in Equation (1), it is equal to the root mean square of the input current at each harmonic frequency divided by the RMS input current at the fundamental line frequency.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \qquad (1)$$

III. Power Factor Correction

To address the challenges of both phase delay as well as current distortion, a power factor correction stage can be introduced between the diode bridge and the DC/DC converter, as shown in Figure 6. It is possible to reduce this harmonic current content due to the relationship between power factor and harmonic distortion in Equation (2) below.

$$PF = \frac{cos(\varphi)}{\sqrt{1+THD}} \qquad (2)$$

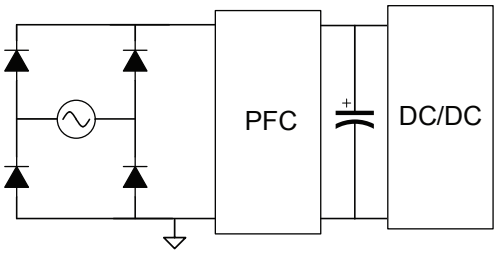

Figure 6 – Introduction of power factor correction stage.

This PFC function can be achieved through either passive or active means. Passive PFC can be implemented by placing inductance in between the diode bridge and the input capacitor to the isolated DC/DC stage. While this approach has minimal complexity and low cost, its effectiveness is limited and can be difficult to maintain good power factor correction performance over extended operating ranges, such as a universal AC input from 85 V_{RMS} to 265 V_{RMS}. An active power factor correction approach entails the use of a full power converter stage in between the diode bridge and the isolated DC/DC converter. While this approach is more complex, an active PFC offers superior power factor performance with little degradation over a wide operating range. While numerous converter topologies have been utilized over the years, each with their own advantages and disadvantages, the most common topology choice in use today for active power factor correction is the boost converter.

One of the primary reasons the boost converter has become the dominant PFC topology in use today is because the boost inductor is on the input side of the converter. This is advantageous because it means the input current does not experience high dI/dt, making the topology better equipped to achieve low input current distortion.

The current paths of the boost converter are show in Figure 7, while Figure 8 shows noteworthy waveforms in the boost power stage. Voltage is applied across the inductor and current in the inductor increases at a linear rate equal to V_{IN}/L. During the MOSFET on-time, charge that is stored in the output capacitance supplies current to the load. When the MOSFET is turned off, the energy stored in the inductance is delivered to the output and the inductor current decreases at a rate equal to $(V_{OUT} + V_f - V_{IN})/L$.

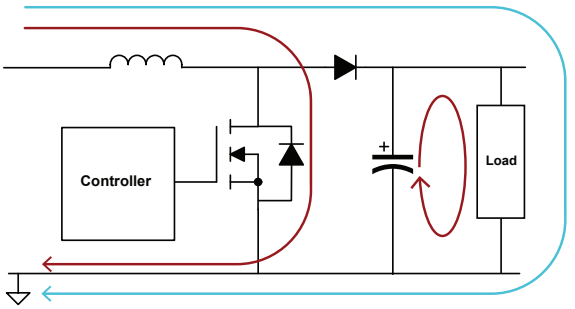

Figure 7 – Boost converter power paths.

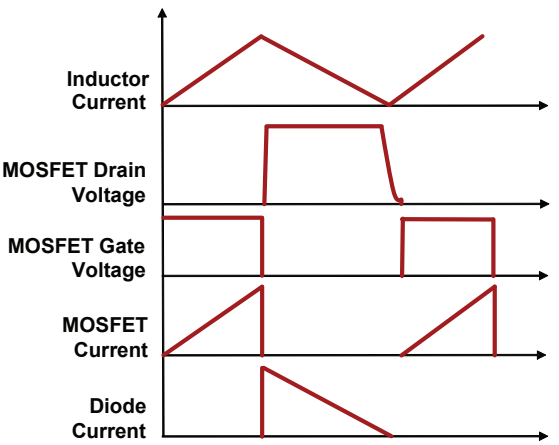

Figure 8 – Boost converter waveforms.

As a boost converter is only capable of stepping up its input voltage, the regulated output voltage of the PFC converter must be greater than the peak of the maximum AC input voltage. As such, most PFC designs fed from a single phase AC plug must have an output voltage greater than 380 V.

The high level block diagram first shown in Figure 6 can now be filled in with more detail and is shown in Figure 9. While the primary benefit of a PFC converter is a high power factor and low THD, there are secondary benefits that the overall AC/DC power supply enjoys due to the inclusion of active PFC. Due to the high output voltage of the PFC stage, a moderate amount of energy can be stored in the PFC output capacitance. This energy can be used by the product to ride through

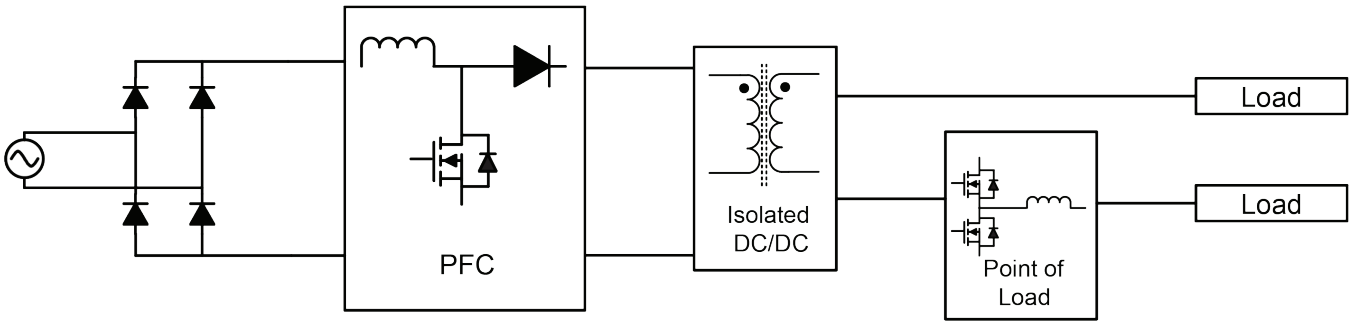

Figure 9 – AC/DC power supply block diagram.

brownout conditions where the AC line momentarily dips to a lower than expected voltage. This characteristic is especially useful if the electronic application needs time to store its last state into memory before completely shutting down. As the output voltage of the PFC is regulated, this greatly simplifies the design of the downstream isolated DC/DC converter, which can now be optimized for a narrow DC input.

IV. Critical Conduction Mode

Critical conduction mode (CrCM) PFC, sometimes referred to as transition mode (TM) PFC, is an extremely popular method of power factor correction due to a very simple control method that achieves reasonable power factor with a minimum number of components.

In its simplest form, the control mechanism works by generating an on-time (t_{ON}) which is constant over the entire line cycle. When the switch turns off, the next turn-on event is initiated when the inductor current reaches 0 A. This results in a high PF without the need of lossy and expensive current sensing or line voltage wave shaping circuits. In order to appreciate how this is done, examine the basic equation for the average current through an inductor over one switching cycle.

$$I_{L(AVG)}(t) = \frac{V_{IN}(t)}{2L} t_{ON} \qquad (3)$$

Notice that in the right hand side of the equation everything is constant over the switching cycle except $V_{IN}(t)$. Since $V_{IN}(t)$ varies slowly relative to the switching frequency, $I_{L(AVG)}(t)$ has the same shape as $V_{IN}(t)$. In other words, since $V_{IN}(t)$ is a sinewave so is $I_{L(AVG)}(t)$. This is the principle argument for the resulting good power factor.

Figure 10 shows how the switching cycle frequency varies over the course of a half line cycle for various RMS input voltages. Notice in particular for an input of 230 V the switching frequency becomes very high at the zero crossings. This results in significant losses as well as implementation challenges in the control. More on this will be discussed later.

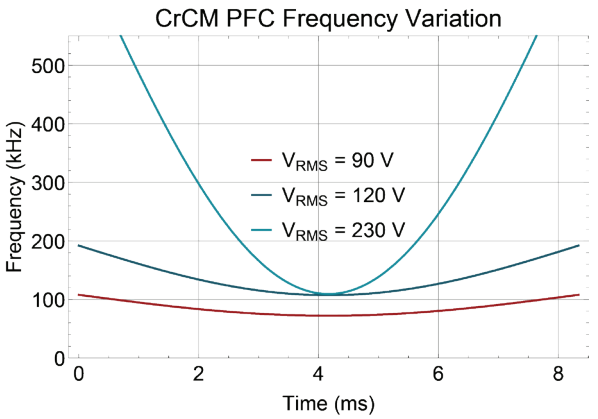

Figure 10 – F_{SW} variation over 1/2 line cycle.

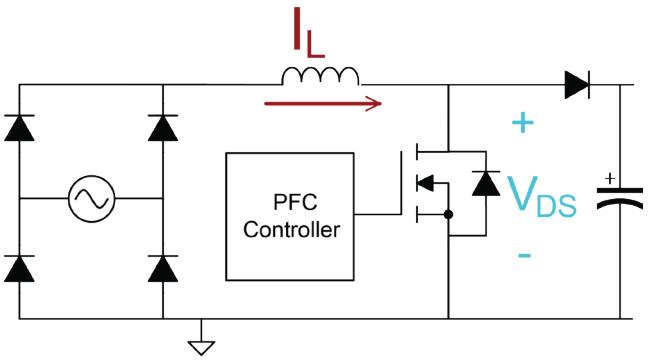

Figure 11 – Simplified boost PFC schematic.

Figure 11 shows the simplified boost PFC converter while Figure 12 illustrates what the cycle by cycle behavior looks like over a narrow time span relative to the line frequency.

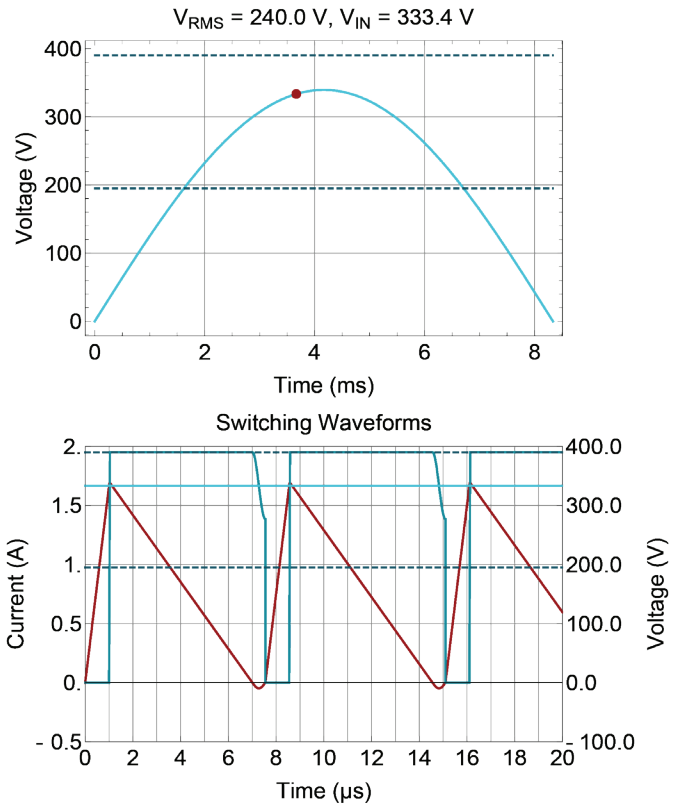

Figure 12 – CrCM near peak of AC line.

The top plot of Figure 12 shows the instantaneous variation of the line voltage over one half of the AC line cycle. The bottom plot shows the inductor current (red), the switch node voltage (solid blue), input voltage (solid blue flat line), output voltage (top dashed line) and 1/2 the output voltage (lower dashed line).

In this case, there are a few things worth noting. First, the drain voltage of the MOSFET does not reach zero before the switch turns on. Second, the switch did not turn on the first time the inductor current reaches 0 A. Instead, the MOSFET turned on the second time after the inductor current momentarily becomes negative. While the inductor current is negative, notice that the MOSFET drain voltage begins to "ring" downward. By turning on the MOSFET at the second zero crossing, this has the advantage of turning on the MOSFET when the drain voltage is at its lowest point, minimizing turn-on loss. It can be shown that the conditions under which the drain will actually ring all the way to 0 V are as shown in Equation (4).

$$V_{IN} < \frac{1}{2} V_{OUT} \tag{4}$$

Any time this inequality is met, zero voltage switching can result if turn-on is properly timed. If the inequality is not met, the MOSFET is valley switched.

As the inductor current drops to 0 A before the MOSFET is turned back on, the boost diode is zero current switched and will not experience reverse recovery, enabling the use of lower cost ultra-fast diodes. For CrCM, the inductor current ripple is always 200% of the average inductor current. For higher output power designs, this large ripple current would be challenging to design due to the high peak currents in the power stage.

Near the AC line zero crossing, the inductor does not have sufficient energy to turn on the output diode, resulting in no useful energy transfer. In addition, the cycle by cycle average current in the inductor is zero resulting in no current flow at the AC line zero crossings. This will result in significant distortion from the idealized equations.

While it is true the CrCM PFC does need to turn on when the inductor current hits zero, there are some practical reasons why this might not be ideal. As already discussed, there is a benefit to waiting for the valley of the drain voltage resonant ring to achieve a slightly softer switching event and minimize switching loss. Figure 13 illustrates three possible times to initiate the MOSFET switch turn-on.

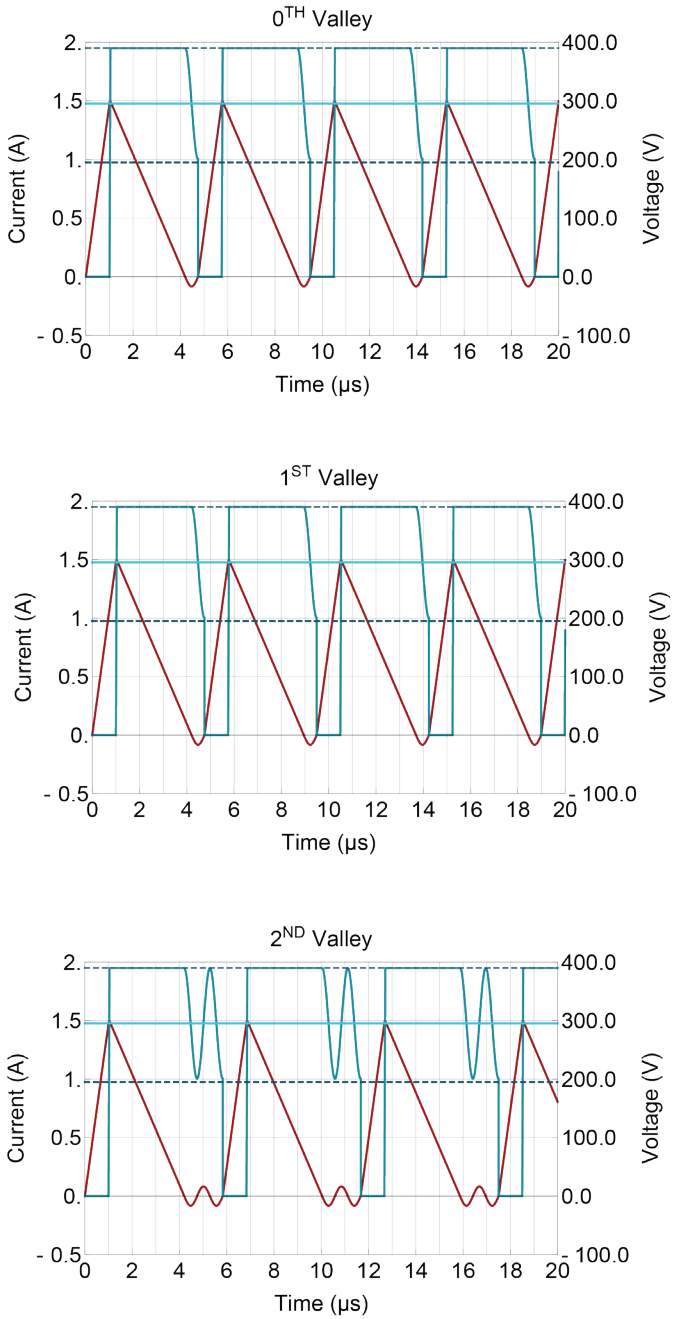

Figure 13 – Valley effect on inductor current.

For simplicity these events are going to be called 0^{TH}, 1^{ST} and 2^{ND} valley turn-on.

- 0^{TH} valley turn-on occurs as soon as the drain voltage hits zero. This method introduces some distortion but lends itself to being one of the simplest methods to implement when the drain voltage rings all the way to zero.
- 1^{ST} valley turn-on occurs when the MOSFET drain voltage rings to its minimum for the first time. For cases when $V_{IN} > \frac{1}{2}V_{OUT}$ this is relatively straightforward to implement. However, when $V_{IN} < \frac{1}{2}V_{OUT}$ it is more difficult since it requires that the 2^{ND} zero crossing of the inductor current be sensed. This is even more difficult due to the small signal being measured. This method can eliminate some of the distortion discussed in the previous bullet.
- 2^{ND} valley (or really N^{TH} valley) occurs at the second time the MOSFET drain voltage rings to zero. Doing nothing more than this solves the high frequency switching that would otherwise occur at the zero crossings, but it introduces significant distortion. An on-time modulation scheme is introduced to solve this issue.

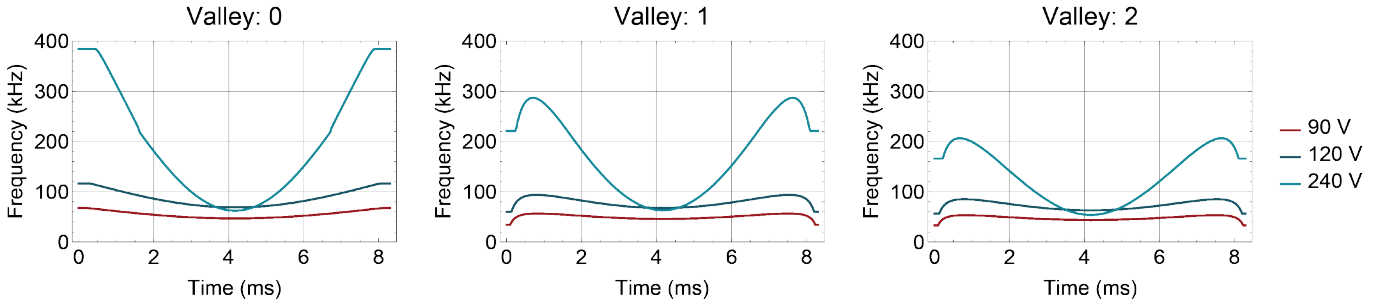

Figure 14 – Valley effect on F_{SW} profile.

Figure 14 shows how each of these three different on-time turn-on events impacts the associated switching frequency of the system.

Notice now that in all cases the high switching frequency at the zero crossing has been largely reduced. Much of this reduction is owing to the fact that the original on-time equation did not consider the switch C_{oss} capacitance. However, the 2^{ND} valley case intentionally increases the period in such a way to maintain zero voltage switching or at least near zero voltage switching and offers a substantial practical reduction in the switching frequency.

Figure 15 shows the power factor and THD performance for each of the three cases. 0^{TH} valley has the worst distortion due to the zero crossing distortion. This comes from the fact that the MOSFET turn-on is initiated when the inductor current is negative. In all other cases the MOSFET only turns on at 0 A. When the MOSFET turns on with a negative current and a constant on-time, the peak current at the end of that on-time is reduced and therefore there is a wider range of conditions under which no energy is transferred to the output. 1^{ST} valley and 2^{ND} valley both have similar results.

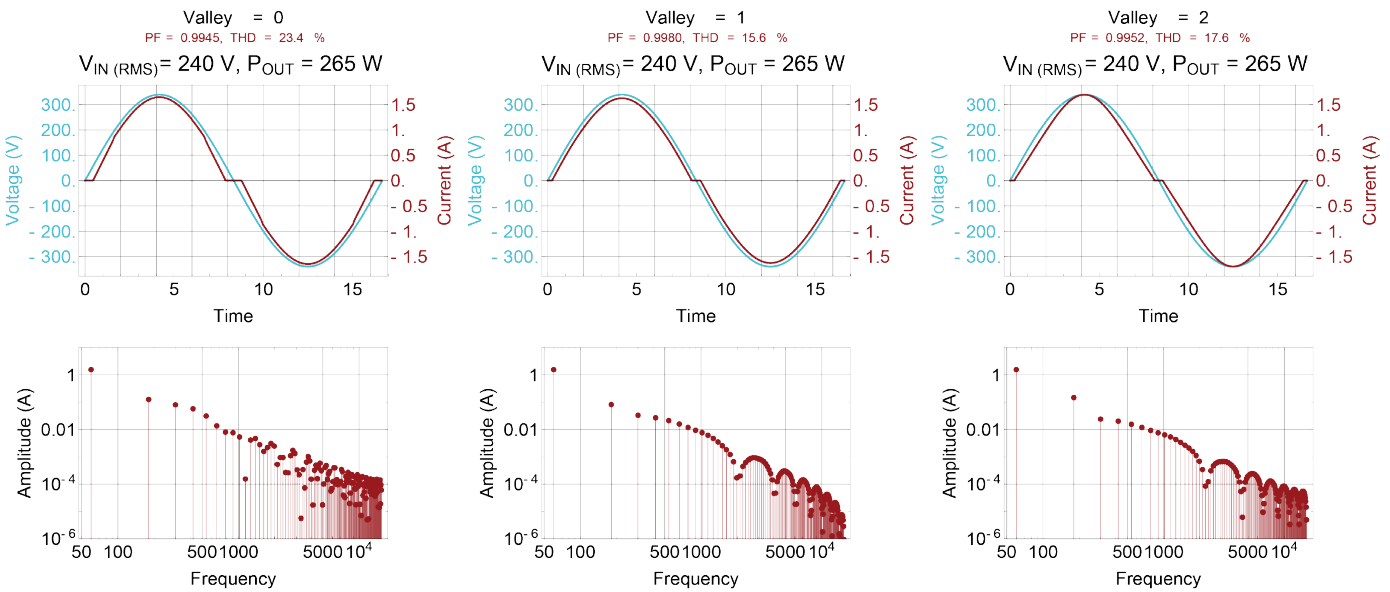

Figure 15 – THD comparison.

V. COMPENSATION

Since there is no current loop in the CrCM PFC, compensation is solely focused on the voltage loop. The first thing to keep in mind is that the voltage loop on the PFC supply needs to be slow. This comes from the fact that we want the input current (i.e., inductor current) to have the same smooth sinusoidal shape as the input voltage. This means that t_{ON} needs to be constant over the line cycle. Therefore, the compensator can't take any action that's faster than a line cycle. For most applications, the target bandwidth needs to be in the vicinity of 2 to 4 Hz. In addition, the gain at 2x the line frequency should be small. -20 to -40 dB is appropriate for most designs. Before showing an example bode plot there are a few more items to consider.

Conceptually it is often convenient to think of a CrCM PFC operating with constant on-time as a lossless resistor, $R_e(t)$, that draws current, $I_{AC}(t)$, from the line voltage according to Ohm's law. This input power, $P_{IN}(t) = I_{AC}(t)^2 \bullet R_e(t)$, is sent to the output load. Figure 16 shows a model for the CrCM PFC converter.

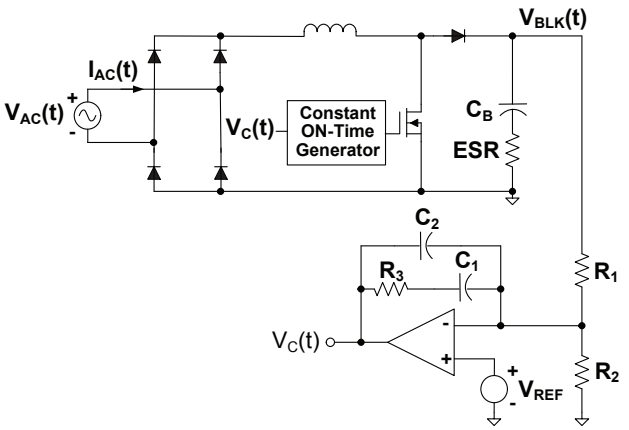

Figure 16 – PFC behavioral model and compensation.

The power drawn from the input can be expressed as in Equation (5).

$$P_D(t) = \frac{V_{AC(REC)}^2(t)}{R_e(t)} = \frac{2 \bullet V_{RMS}^2 \sin^2(\omega \bullet t)}{R_e(t)} \quad (5)$$

The output of the compensator will be modeled as a power command, as shown in Equation (6).

$$V_c(t) \bullet \frac{P_{MAX}}{V_{c(MAX)}} = \frac{k}{R_e(t)} \quad (6)$$

Rearranging this equation shows a substitution that can be made for $R_e(t)$. This is shown in Equation (7).

$$R_e(t) = \frac{k \bullet V_{c(MAX)}}{V_c(t) \bullet P_{MAX}} \quad (7)$$

Making this substitution yields Equation (8).

$$P_D(t) = 2 \bullet V_{RMS}^2 \bullet \sin^2(\omega \bullet t) \bullet \frac{V_c(t)}{V_{c(MAX)}} \bullet \frac{P_{MAX}}{k} \quad (8)$$

Simplifying gives us Equation (9).

$$P_D(t) = 2 \bullet \frac{V_{RMS}^2}{k} \bullet \sin^2(\omega \bullet t) \bullet V_c(t) \bullet \frac{P_{MAX}}{V_{c(MAX)}} \quad (9)$$

All that remains is to make a choice for the proportionality constant, k. If k is chosen to be equal to V^2_{RMS}, the relationship simplifies to Equation (10).

$$P_D(t) = 2 \bullet \sin^2(\omega \bullet t) \bullet V_c(t) \bullet \frac{P_{MAX}}{V_{c(MAX)}} \quad (10)$$

Using the trigonometric identity $\sin^2(\omega \bullet t) = \frac{1 - \cos(2 \bullet \omega \bullet t)}{2}$ and substituting yields Equation (11) below.

$$P_D(t) = \left(1 - \cos(2 \bullet \omega \bullet t)\right) \bullet V_c(t) \bullet \frac{P_{MAX}}{V_{c(MAX)}} \quad (11)$$

Essentially, $V_c(t)$ now commands a power delivery to the output. Notice $P_D(t)$ does not contain a V_{RMS} term. By using V^2_{RMS} as a proportionality constant, the delivered power to the load is independent of the input voltage. This method is called line voltage feedforward and is especially useful for PFC converters that must work over a wide input voltage range. The average power delivered can be calculated from Equation (12).

$$P_{D(AVG)}(t) = V_c(t) \bullet \frac{P_{MAX}}{V_{c(MAX)}} \tag{12}$$

The output of a PFC converter has output voltage ripple at twice the AC line frequency. This AC ripple can be calculated using Equation (13).

$$P_{D(AC)}(t) = -cos(2 \bullet \omega \bullet t) \bullet V_c(t) \bullet \frac{P_{MAX}}{V_{c(MAX)}} \tag{13}$$

By looking at $P_{D(AVG)}(t)$, the average nature of the power command $V_c(t)$ is readily apparent.

- $V_c(t)$ should be compensated such that $P_{D(AC)}(t)$ is dominated only by the cosine term.
- This means that $V_c(t)$ cannot do anything to reduce the output ripple voltage that results from the line frequency.

Next, consider the load that most PFC converters are driving. In most cases this load is another power supply. A power supply maintains a constant output voltage; therefore, it will seek to draw a constant amount of power from its input, in this case being the PFC output. This is shown in Equation (14).

$$I_{OUT}(t) \bullet V_{OUT}(t) = P_{OUT} \tag{14}$$

In order to use this to facilitate some intuition into the loop dynamics, this relationship can be perturbed using partial derivatives seen in Equation (15).

$$\frac{\partial I_{OUT}(t)}{\partial t} \bullet V_{OUT} + I_{OUT} \bullet \frac{\partial V_{OUT}(t)}{\partial t} = 0 \tag{15}$$

Where $Z_{OUT} = \dfrac{\dfrac{\partial V_{OUT}(t)}{\partial t}}{\dfrac{\partial I_{OUT}(t)}{\partial t}}$.

Solving for the effective impedance from these results yields Equation (16).

$$Z_{OUT} = \frac{V_{OUT}}{I_{OUT}} = -\frac{V_{OUT}^2}{P_{OUT}} \tag{16}$$

The remarkable thing to note here is the negative sign.

The following plot in Figure 17 is what a compensated system could look like.

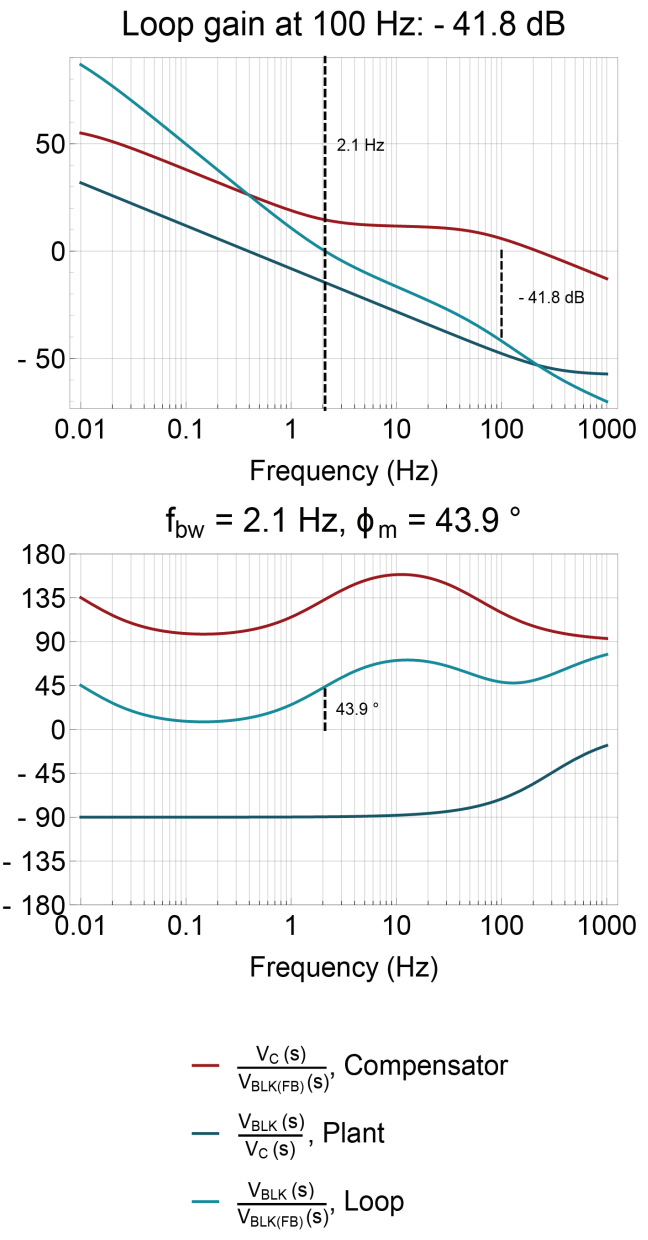

Figure 17 – PFC plant, compensator and closed loop gain and phase.

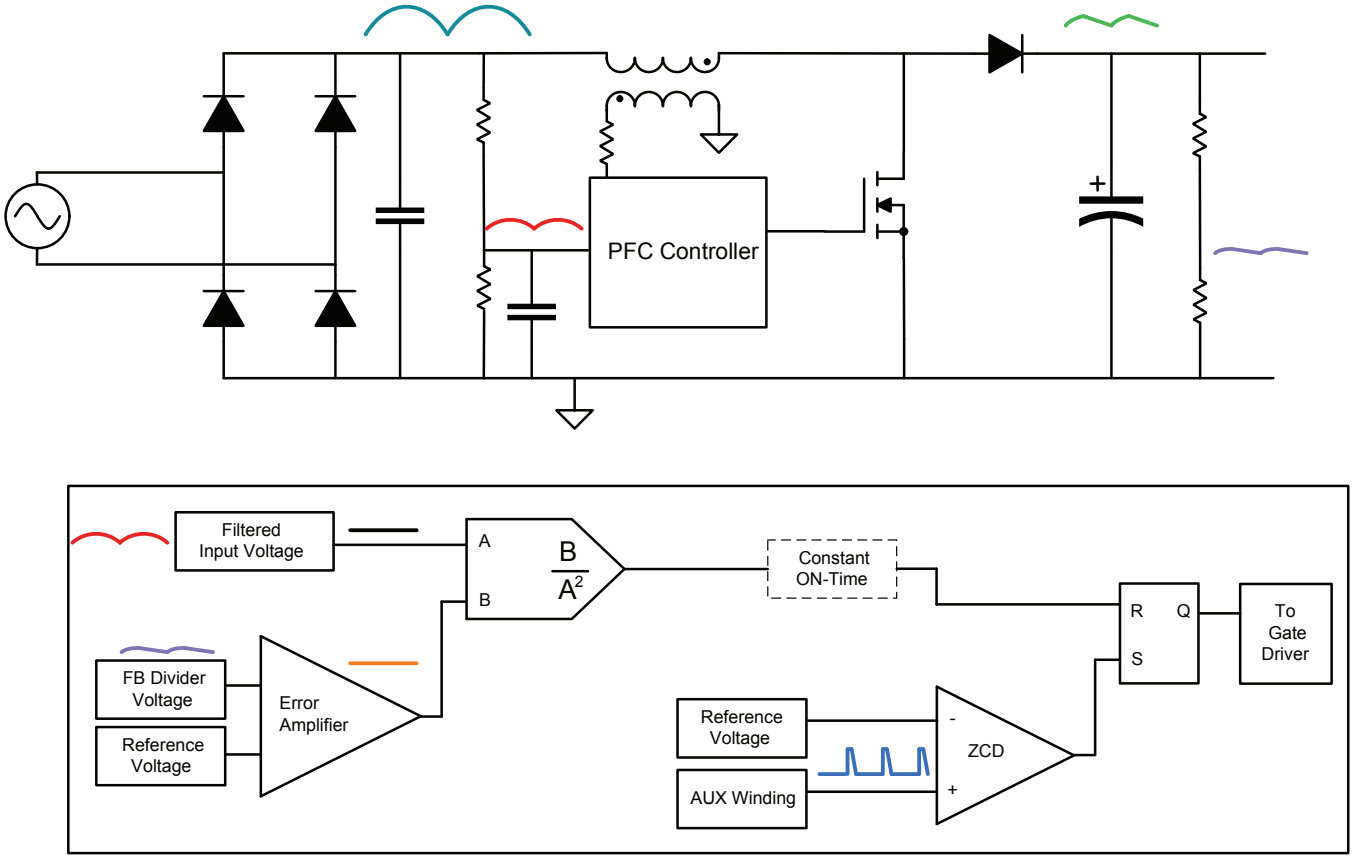

Figure 18 – CrCM PFC block diagram using constant on-time.

Notice that the plant has an integrator like behavior. This stems from the fact that the PFC is a constant power source driving a constant power load (negative impedance). These two goals end up in conflict and the result is a pole at DC. An integrator in the compensator is necessary to add to the control loop in order to achieve good DC accuracy. Stability demands that we get rid of one of these poles before getting to the cross over point. Shortly after zero-crossing another pole is added to achieve the gain margin discussed earlier.

Figure 18 shows the block diagram of a fully realized CrCM PFC converter using constant on-time. The output of the error amplifier and the sampled input voltage are fed to a multiplier to determine the on-time of the MOSFET. An auxiliary winding is used to sense when the inductor current has dropped to 0 A and turn the MOSFET back on.

In summary, the CrCM PFC is an inexpensive implementation that achieves lower switching losses due to valley switching and no reverse recovery on the boost diode. In practice, CrCM PFC is commonly used for <300 W designs due to the cost advantages and simple implementation. The reason CrCM PFC sees little use above 300 W is because the large peak currents become increasingly difficult to manage and the efficiency suffers due to the significant conduction losses.

VI. Continuous Conduction Mode

While continuous conduction mode shares similarities with its critical conduction mode counterpart, there are several fundamental differences. The primary goal of actively shaping the average input current to follow the instantaneous line voltage remains the same, but instead of using a fixed on-time with variable switching frequency, a fixed switching frequency is utilized and the duty cycle of the MOSFET is now a function of the instantaneous line voltage.

A high level block diagram of a CCM PFC implementation is shown in Figure 19. Intuitively, one may reason that the duty cycle simply increases

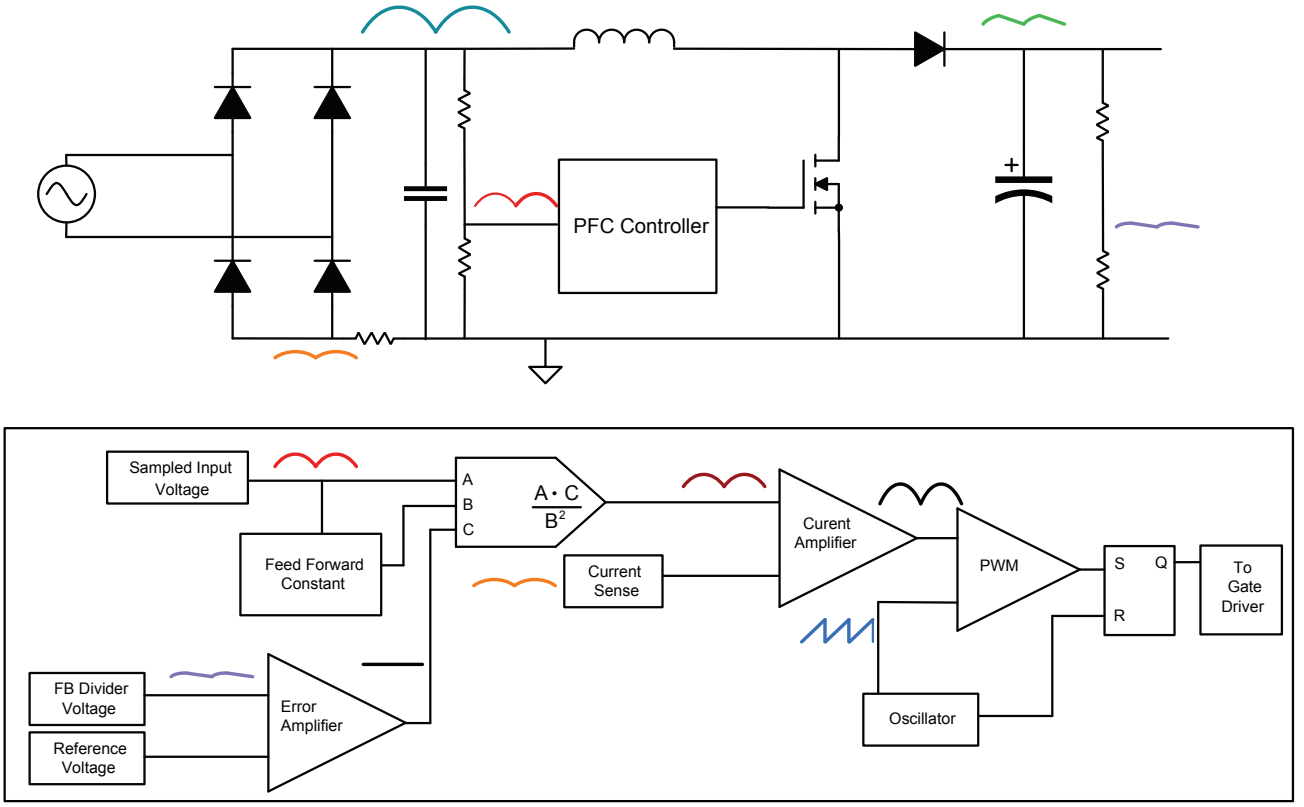

Figure 19 – CCM PFC block diagram using average current mode control.

with the instantaneous line voltage, but this would be an incorrect assumption as this would not account for the changing inductor current slope over the half AC line cycle. Instead, a common implementation is to use a current sense element to directly measure the input current and feed this current information to an error amplifier. The input of this current error amplifier is generated by a multiplier that combines 3 inputs.

- The output voltage of the PFC stage monitored through the output of the voltage error amplifier.
- The instantaneous input voltage measured from a resistor divider connected to the rectified AC line.
- A quantitized feedforward constant to compensate for different line voltages. Like the CrCM PFC, feedforward is a key component in allowing the PFC stage to handle the full range of international line voltages.

The output of the multiplier is used as a reference signal for the input current error amplifier. For most CCM PFC designs, a type I compensation network is needed in order to attenuate the current ripple, the goal being to make the output of the current amplifier a function of the average input current. The output of the current amplifier is compared against an internally generated fixed frequency ramp signal to generate the proper pulse width and duty cycle for the CCM boost.

Figure 20 illustrates the inductor current and MOSFET drain waveform over the half AC line cycle. Compared to the critical conduction mode PFC, the inductor current ripple is significantly lower with most designs targeting an inductor ripple current between 20% to 30% of the average input current. The lower peak currents in the power stage yield much lower conduction losses than critical conduction mode, making this control scheme attractive for higher output power designs greater than 300 W. The smaller peak currents also allow for smaller and cheaper core material to be used versus its critical conduction mode counterpart. As the inductor current does not fall to 0 A before the MOSFET is turned back on, the MOSFET drain sees the full output voltage at the

moment of turn-on. While the smaller ripple currents are beneficial for reducing conduction loss in the MOSFET, there is now higher turn-on switching loss in the MOSFET due to the hard switching. Due to the absence of zero current switching in the boost diode, the diode experiences hard commutation and reverse recovery. Excellent reverse recovery performance is essential to effectively manage the switching loss in the boost diode. As such, silicon carbide diodes which have greatly improved reverse recovery characteristics are more prevalent for CCM PFC designs.

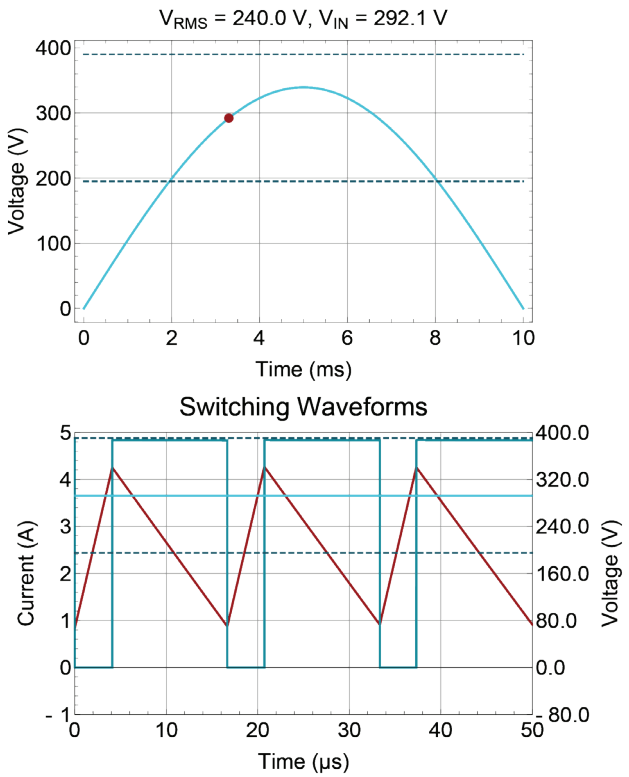

Figure 20 – Inductor current and MOSFET drain waveforms near peak of AC line.

When the instantaneous AC line voltage is near the zero crossing, there is insufficient current in the inductor to maintain CCM operation and the converter will drop into fixed frequency discontinuous conduction as shown in Figure 21.

Continuous conduction mode avoids some undesirable characteristics, such as the MOSFET C_{OSS} negative current that is present in critical conduction mode, and is able to achieve superior power factor and THD performance compared to the CrCM PFC. This improved performance does not come for free, however, as the power stage

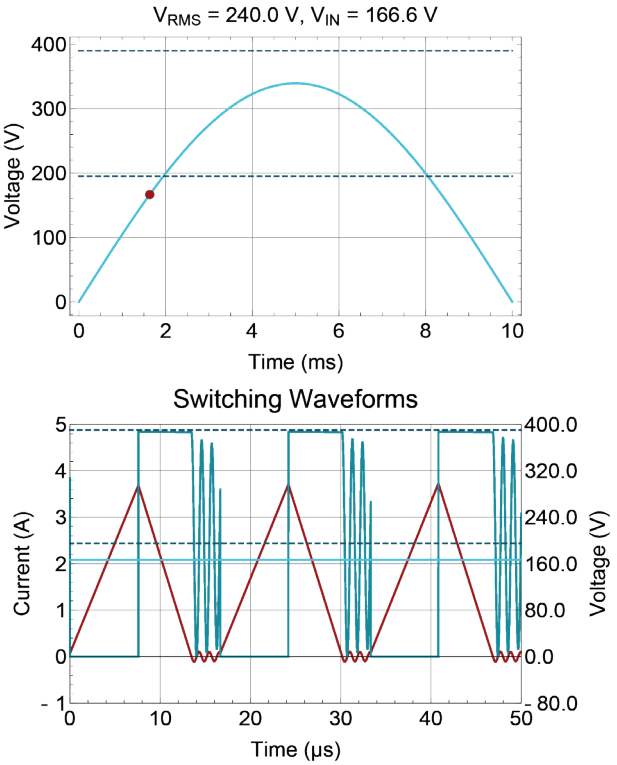

Figure 21 – Inductor current and MOSFET drain waveforms near AC zero crossing.

necessitates the need for more expensive power stage components that are able to accommodate the considerable increase in switching losses. The average current mode control used in CCM PFC is slightly more complex in implementation than the simple constant on-time approach used with CrCM PFC and requires compensation of a slow output voltage control loop as well as the fast input current control loop. While most of the burden for implementing average current mode control is taken care of by a PFC controller, this does result in slightly higher passive component count around the controller.

In practice, the CCM PFC sees frequent use in designs requiring >300 W to a few kW of output power while CrCM PFC is dominant in the <300 W space. The reason CrCM PFC sees little use above 300 W is the large peak currents become increasingly difficult to manage and the efficiency suffers due to the significant conduction losses. The better THD performance also makes CCM PFC an attractive option for designs requiring very low current distortion such as lighting applications.

VII. Interleaving

As highlighted in the previous sections, critical conduction mode and continuous conduction mode each have unique advantages and disadvantages. The CrCM PFC features low switching losses but high conduction loss due to the 200% inductor ripple current. In contrast, the CCM PFC is better equipped to manage the conduction losses more effectively at the expense of higher switching losses. An approach for increasing the practical power limit of CrCM is to use an interleaved approach where two boost power stages are operated 180° out of phase from each other as shown in Figure 22.

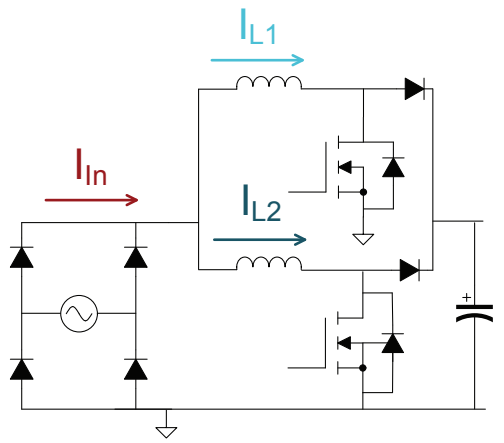

Figure 22 – Interleaved boost PFC.

This interleaving approach can be used to extend the practical power range of CrCM up to 700 W. In addition, the interleaving action results in some additional benefits to the PFC converter. While the ripple current in each individual inductor is still quite high, the total input current ripple is much smaller due to ripple cancellation as shown in Figure 23. The benefit of the input current ripple cancellation is a physically smaller EMI filter can be utilized.

For certain duty cycles, complete ripple current cancellation is achieved. For a two stage interleaved boost, this occurs when the rectified AC input voltage is equal to half of the output voltage as shown in Figure 24.

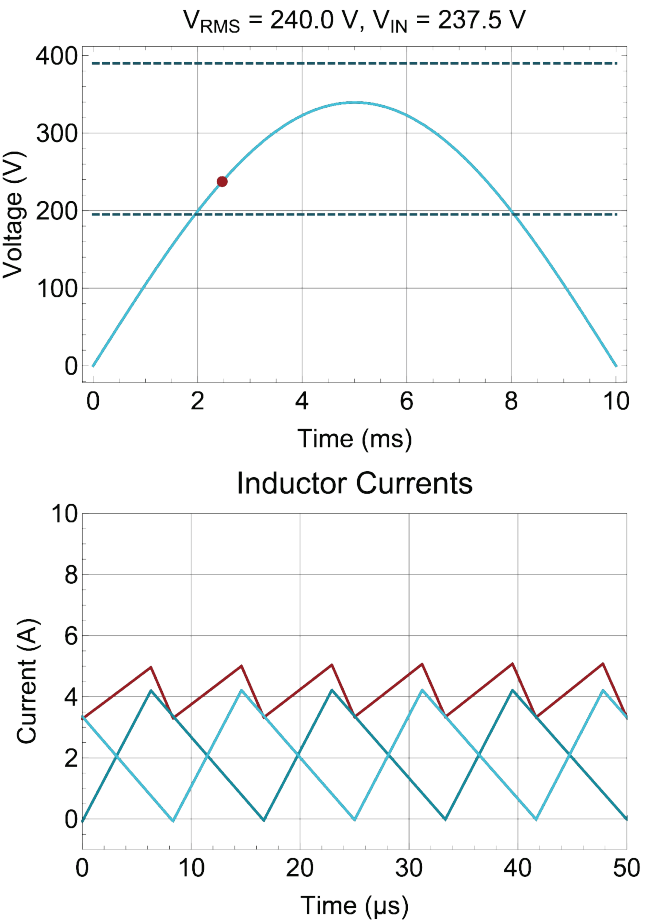

Figure 23 – Interleaved boost inductor currents and total input current ripple.

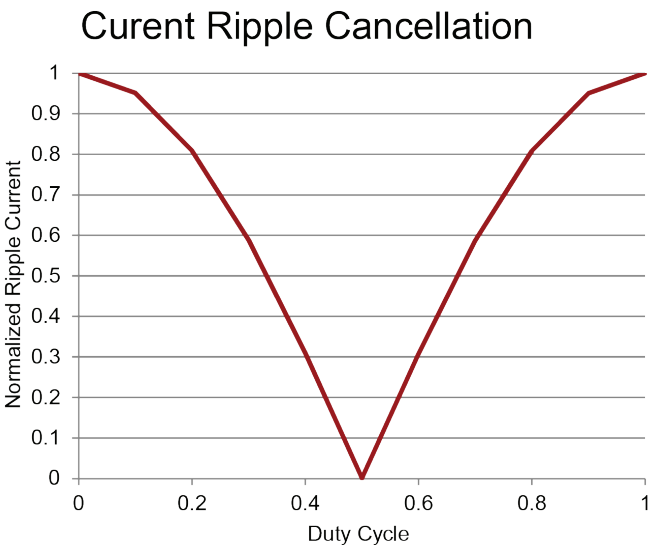

Figure 24 – Ripple current cancellation for two stage interleaved boost.

As the interleaved PFC distributes the loading equally between the two phases, the RMS currents in each boost stage are smaller compared to the single phase counterparts discussed in previous sections. The lower RMS currents allow for smaller, faster MOSFETs and diodes to be utilized. The size of each individual inductor can be minimized as well due to the lower per phase currents. The power losses are distributed over the two power stages, resulting in better thermal management than either single phase CrCM or single phase CCM. Note that this interleaving approach applies to the CCM as well and interleaved CCM PFC enjoys many of the same benefits such as higher output power capability, ripple current cancellation and smaller per phase RMS currents. The disadvantage of this interleaving approach is the requirement for two boost power stages resulting in an increase in cost and component count.

While interleaved CrCM and single phase CCM both tend to be utilized in the 300 W to 700 W output power range, interleaved CrCM is favored for designs requiring very small height and that are able to devote the necessary PCB board area for the two boost stages. Slim TV panel power is one such application. Interleaved CCM PFC enjoys use in the multi-kW output power range as it is better equipped to handle the larger output power than its single phase counterpart.

VIII. Bridgeless PFC

Bridgeless PFC sees significant interest because it attempts to eliminate the lossy diode bridge on the input. While in principle this is not that difficult, it becomes very challenging due to control complexity, component count and EMI. A logical first step would be to do something similar to Figure 25.

However, the additional noise introduced by this architecture creates a huge common mode noise problem that tends to offset any benefits realized from the elimination of the diode bridge.

In order to address this problem and still get the benefits of a bridgeless architecture, the following options shown in Figure 26 are considered.

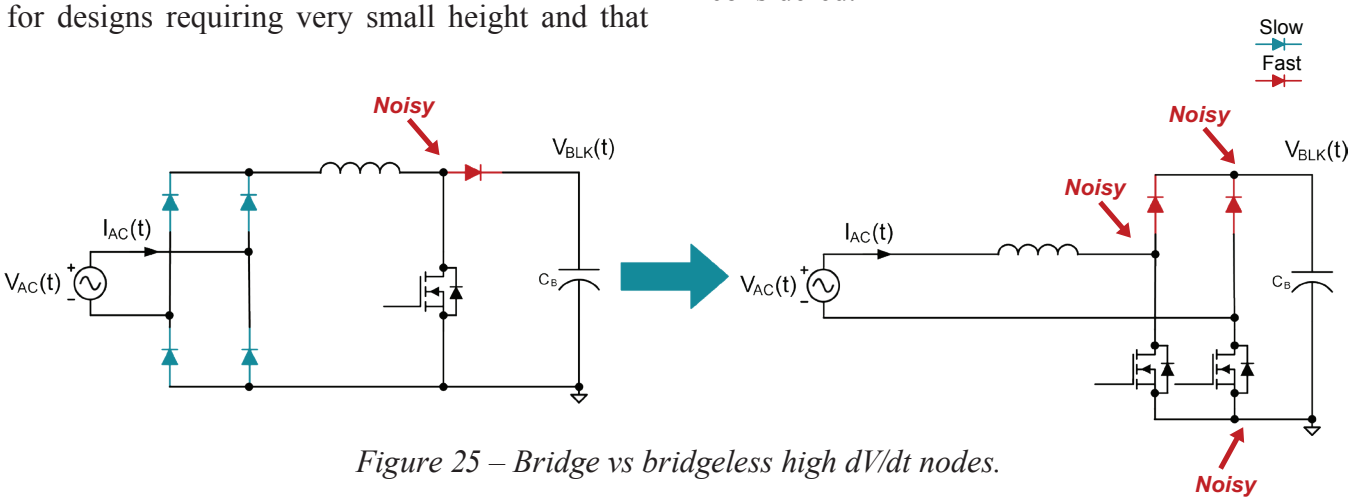

Figure 25 – Bridge vs bridgeless high dV/dt nodes.

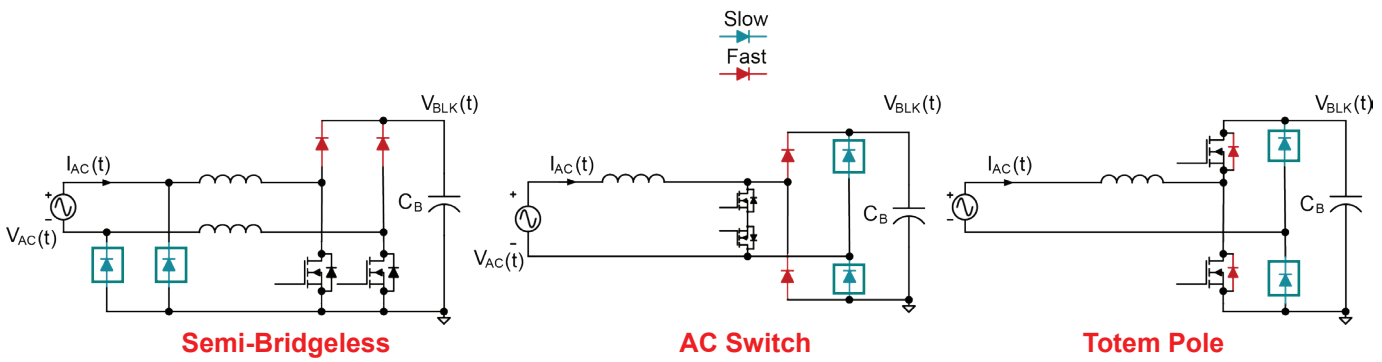

Figure 26 – Bridgeless PFC variations.

IX. Semi-Bridgeless

This topology operates by using a separate boost converter for each half line cycle. The slow diodes on the input are added to make sure that the common mode noise does not get out of control. It has ground referenced gate drivers but the resulting circuitry is quite large.

X. AC Switch

The AC switch offers a much more efficient utilization of the converter components. The bi-directional switch pair operates in the same way for both half cycles. It has the advantage of offering a balanced input impedance that can improve EMI. It does bring additional challenges associated with current sensing, isolated drive and the overall component count is still a little large.

XI. Totem Pole

This topology does the best job of minimizing components while at the same time eliminating the bridge and maximizing efficiency. However, it does so with the addition of significant control complexity. It has high side drive, MOSFET body diode reverse recovery challenges and complex current sensing. It also does not have quite the common mode performance of the AC switch or semi-bridgeless topologies.

The benefits and drawbacks of each bridgeless implementation are summarized in Table 1.

Semi-Bridgeless	AC Switch	Totem Pole
Advantages • Simple control • Ground referenced gate drive	**Advantages** • Lowest on-state conduction • Balanced EMI	**Advantages** • Minimum components • Good efficiency
Disadvantages • 2 power stages • 6 semiconductors • Poor core utilization	**Disadvantages** • Isolated drive • Current sense • 6 semiconductors	**Disadvantages** • Complex • High side drive • Current sense • Common mode • Reverse recovery

Table 1 – Bridgeless implementation considerations.

XII. PFC Selection Considerations

As mentioned in previous sections, single phase CrCM PFC tends to be limited to 300 W and below due to the challenges of managing the power stage peak currents at higher output power. To illustrate this, consider a universal AC input, 500 W output power design example using the UCC28056, a CrCM PFC controller. To determine an appropriate boost inductance, Equations (17) and (18) are used.

$$L_{Boost0} = \frac{V_{IN(RMS)\_min}^{2}}{110\% \bullet P_{OUT(max)}} \bullet \frac{T_{ON(max)\_0}}{2} \quad (17)$$

$$L_{Boost0} = \frac{85^2}{110\% \bullet 500\ W} \bullet \frac{12.8\mu s}{2} = 84\ \mu H \quad (18)$$

The peak input current at minimum AC input can be calculated using Equations (19) and (20).

$$I_{LPk0} = \frac{V_{IN(RMS)\_min} \bullet \sqrt{2} \bullet T_{ON(max)\_0}}{L_{BOOST}} \quad (19)$$

$$I_{LPk0} = \frac{85 \bullet \sqrt{2} \bullet 12.8\ \mu s}{84\ \mu H} = 18.31\ A \quad (20)$$

Even if the 10% margin in the inductance calculations is reduced to 5%, the peak current for CrCM PFC reduces only marginally to 17.49 A. Compare the same universal AC input, 500 W example for CCM PFC with the UCC28180. Efficiency is estimated to be 95%. To determine the peak input current, Equations (21) and (22) are used.

$$I_{IN(max)} = \sqrt{2} I_{IN(RMS)\_min} \frac{P_{OUT(max)}}{\eta \bullet V_{IN(RMS)\_min} \bullet PF} \quad (21)$$

$$I_{IN(max)} = \frac{500}{0.95 \bullet 85 \bullet 0.99} = 8.84\ A \quad (22)$$

For this example, a target ripple current of 25% and 100 kHz switching frequency are used. The ripple current can be calculated using Equation 23.

$$I_{RIPPLE(target)} = I_{IN(max)} \bullet 0.2 = 1.768\ A \quad (23)$$

The minimum boost inductance can be found using Equations (24) and (25) with the worst case duty cycle of 50%.

$$L_{BOOST(min)} > \frac{390 \bullet D \bullet (1-D)}{f_{SW} \bullet I_{ripple(target)}} \quad (24)$$

$$L_{BOOST(min)} > \frac{390 \bullet 0.5 \bullet (1-0.5)}{100\ kHz \bullet 1.768\ A} = 564\ \mu H \quad (25)$$

The absolute maximum peak current in the inductor can now be calculated using Equations (26) through (28).

$$I_{L(ripple)} = \frac{390 \bullet D \bullet (1-D)}{f_{SW} \bullet L_{BOOST}} \quad (26)$$

$$I_{L(ripple)} = \frac{390 \bullet 0.5 \bullet (1-0.5)}{100\ kHz \bullet 564\ A} = 1.73\ A \quad (27)$$

$$I_{L(peak)} = I_{IN(max)} + \frac{I_{L(ripple)}}{2} = 9.73\ A \quad (28)$$

For the same design inputs, the peak inductor current in the CCM PFC is nearly half of the peak inductor current in the CrCM PFC in this example. This is illustrated in Figure 27.

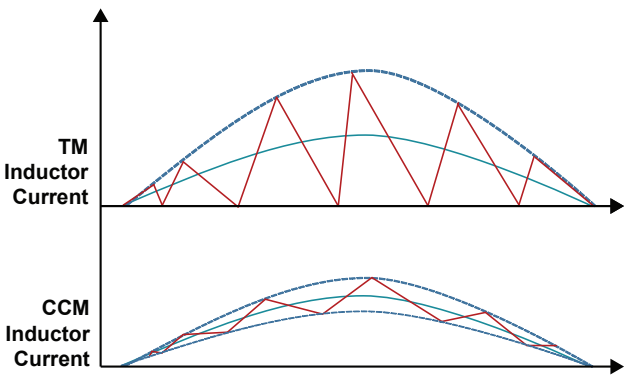

Figure 27 – CrCM/TM and CCM inductor ripple current comparison.

The larger peak inductor current not only affects the size of the inductor but also the current ratings for the boost diode and MOSFET. It is for this reason that transition mode is challenging to push to higher power levels without interleaving. The below graph, Figure 28, summarizes the typical output power ranges for the different PFC variations discussed in this paper.

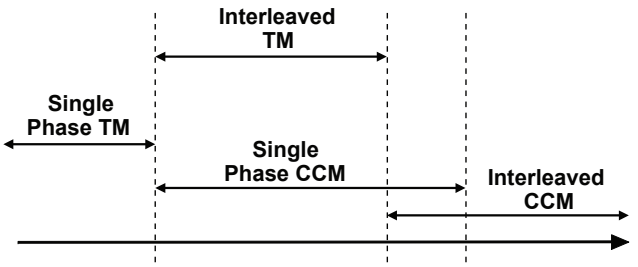

Figure 28 – Practical power ranges.

As interleaved TM/CrCM and single phase CCM PFC are both optimal choices for the 300 W to 700 W output power range, they differ in many characteristics. For interleaved TM, the conduction losses are split over two power stages and paired with the valley switching action, allowing for lower cost MOSFETs and diodes to be used in the power stage. While the power density is much greater for single phase CCM, the component stresses are greater, making more expensive components necessary such as the SiC diodes due to the reverse recovery.

The interleaved TM/CrCM is better equipped to handle the power dissipation as the generated heat is spread over a greater PCB board area. As interleaved TM requires two complete power stages, it is often a more expensive solution than single phase CCM. The tradeoffs between interleaved TM/CrCM and single phase CCM are summarized in Table 2.

Design Characteristics	Interleaved CrCM	Single Phase CCM
Component stress	Conduction loss split between two power stages, valley switched	Single power stage, hard switched
Power density	Lower	Higher
Height	Smaller overall component height	Single inductor, larger heatsinks
Thermal management	Power dissipation spread over greater X/Y space	More challenging
Complexity	High power stage component count	Single power stage
Cost	Higher	Lower

Table 2 – Interleaved CrCM/TM vs single phase CCM.

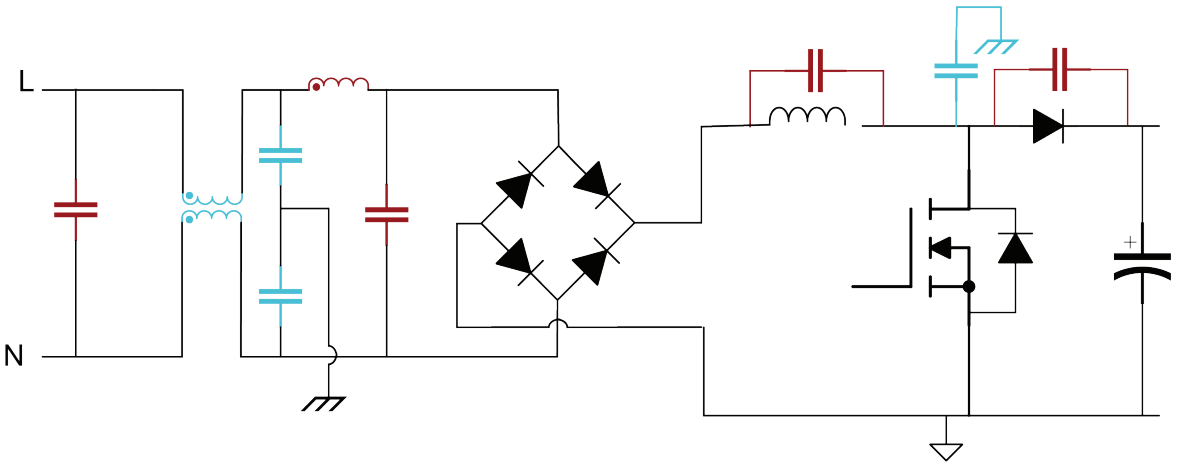

Figure 29 – Boost parasitics and EMI filtering.

For EMI, it is important to remember the parasitic elements in the boost topology that can potentially contribute to differential or common mode noise. Some of the primary parasitics to consider include the winding capacitance on the inductor and the parasitic capacitances on the switch node and across the boost diode. A boost with these parasitics as well as an example EMI filter is shown in Figure 29. To filter differential noise, a combination of a differential inductor and line to neutral capacitance is used. These capacitors connected from line to neutral are known as X capacitors. To filter common mode noise, a coupled inductor, commonly known as a common mode choke, is paired with capacitors connected from line to EARTH as well as neutral to EARTH. These capacitors are known as Y capacitors.

EMI performance is quite dependent on proper layout and parasitics associated with the surrounding PCB area. For example, if a grounded metal heatsink is attached to the MOSFET and diode to assist with thermal management, this contributes additional parasitic capacitance between the switch node drain and ground. While the finer details of EMI mitigation are outside the scope of this paper, characteristics of common PFC topologies that influence EMI performance and EMI filtering strategy are discussed.

The CrCM PFC 200% ripple current mandates the need for a physically larger input filter in front of the PFC power stage in order to effectively filter this ripple current from feeding back into the AC line. The variable switching frequency results in noise that is less concentrated in a singular frequency but spread over a frequency range similar to a dithering effect. The filter must account for the wide switching frequency range that the CrCM PFC will operate at over the AC line cycle, however.

The CCM PFC features greatly reduced ripple current and thus the input filter can be physically smaller. The fixed frequency can result in greater noise in the fundamental switching frequency and its respective harmonics. As the lower limit of most EMI standards, such as EN5022 or CISPR, is 150 kHz, a common strategy is to make the switching frequency of the CCM PFC less than this 150 kHz limit in order to take the fundamental frequency out of the range of concern. The interleaving ripple cancellation is beneficial for reducing the input current ripple in both interleaved CrCM and interleaved CCM, allowing for a physically smaller input filter. EMI filtering for bridgeless PFC is challenging for some variations, as high dV/dt switching nodes are no longer separated from the AC line by the bridge.

XIII. Summary

Power factor correction is essential to minimizing the total apparent power consumed from the grid. Regions around the world recognize this need and have implemented voluntary or mandatory requirements depending on the class of electronic equipment. There are many different methods for implementing power factor correction, each with their own benefits and drawbacks as this paper has discussed.

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