NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P12V" represents connection to the +12V power plane.
2. The netname "P3P3V" represents connection to the +3.3V power plane.
3. The netname "P1P8V" represents connection to the +1.8V digital power plane.
4. The netname "P1P1V" represents connection to the +1.1V power plane.
5. The netname "P1P8V_ITEA" represents connection to the +1.8V ITE6535 analog supply power plane.
6. The netname "F_VCCIO" represents connection to the +3V FPGA Vccio power plane.
7. The netname "P2P5V_FAUXPLL" represents connection to the +2.5V FPGA aux/pll power plane.
8. The netname "P1P8V_A" represents connection to the +1.8V controller analog supply power plane.
9. The netname "GND" represents connection to the ground plane.
10. A "Z" suffix on a signal name indicates an active low signal.
11. All components with designators "U*", "Q*", and "D*" are electrostatic discharge sensitive.

COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2137507: Initial Release	11/1/2013	NG
B	ECO 2140137: Updated to rev B	2/18/2014	NG
C	ECO 2141055: Updated to rev C	4/8/2014	NG
D	ECO 2142175: Updated to rev D	5/28/2014	NG
E	ECO 2144118: Updated to rev E	8/8/2014	NG

DLP®

TEXAS INSTRUMENTS

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		APVD L. Harvey 8/8/2014	TITLE: ESD, Dual DLPC900 Hi-Res Main Board Reference Design
		MFG xxxxxxxx	
2513535	0314PO	QA xxxxxxxx	
NEXT ASSY	USED ON		A3 DRAWING NO 2513534 REV E
APPLICATION		SW Cadence 16.5	SCALE SHEET 1 of 28

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DisplayPort EDID Page 6

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Master Controller Pixel Data

Slave Controller Pixel Data

Spare GPIOs

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LED driver Conn Page 26

128Mb Flash x 3 Page 14

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3.3V

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3.3V to 1.8V HDMI Rx Analog

3.3V to 2.5V FPGA Aux

12V to 3V FPGA IO

12V to 3.3V

3.3V to 1.8V Controller Analog

12V Monitor

12V to 1.1V Controller Core

12V to 1.8V

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1.1V Controller & FPGA Core
1.8V digital
1.8V Controller Analog
1.8V HDMI Rx Analog
2.5V FPGA Aux Pwr
3.0V FPGA VCCio
3.3V HDMI, IO power

TEXAS INSTRUMENTS	DWN A. Ng	DATE 8/8/2014	A3	DRAWING NO 2513534	REV E
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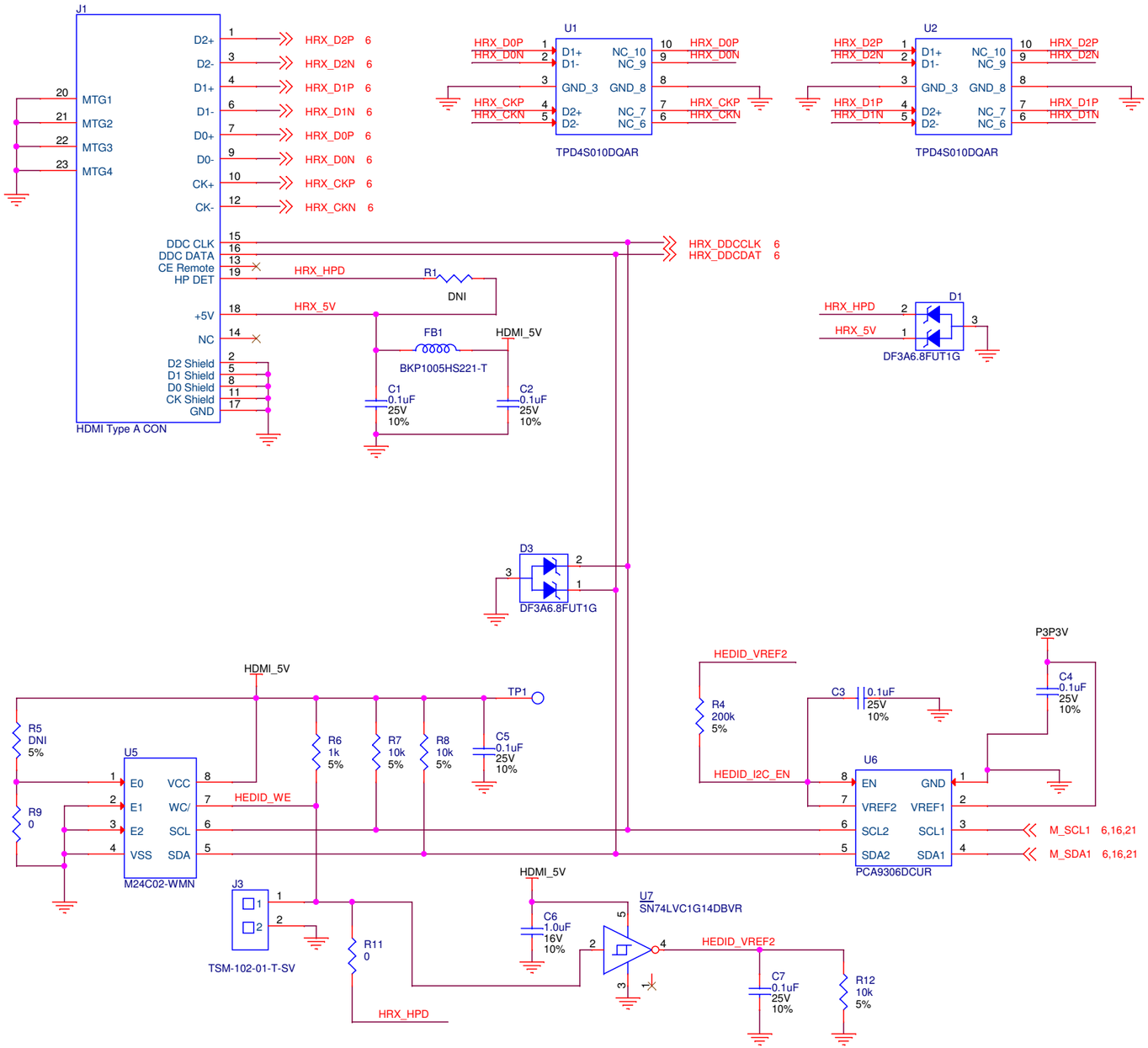

To program HDMI EDID
- install jumper to enable PROM write and disable hot plug detect
- connect HDMI cable to supply 5V
- use TI control program to update EDID

HDMI TypeA Rx Conn, ESD, and EDID

DisplayPort Rx Conn, ESD

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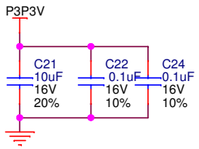
Apply a crystal input even audio function is not used per ITE recommandation

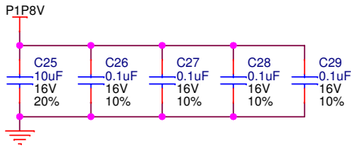
I2C address select
low = 0xB0
high = 0xB2

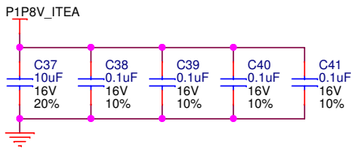
Must connect I2C and interrupt to controller for register setup

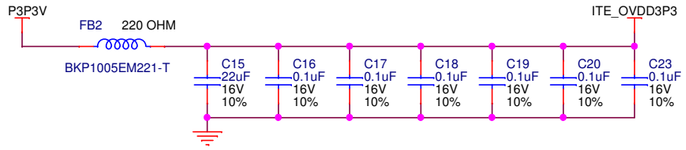
HDMI receiver input/output

TEXAS INSTRUMENTS	DWN A. Ng	DATE 8/8/2014	A3 DRAWING NO 2513534 REV E
	ISSUE DATE 8/82014		SCALE SHEET 6 OF 28

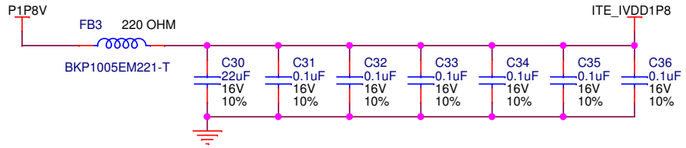




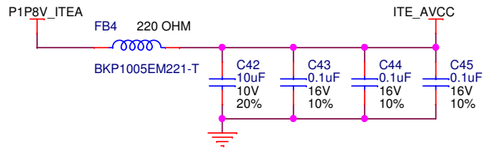




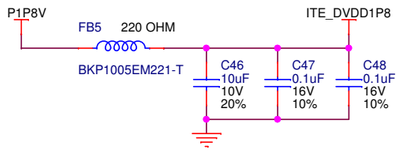
3.3V IO



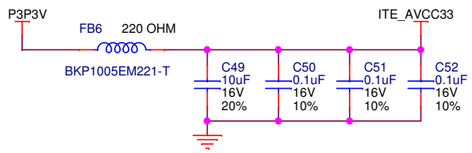
Digital logic core



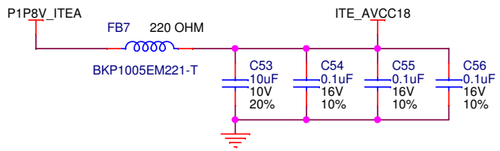
DP analog frontend



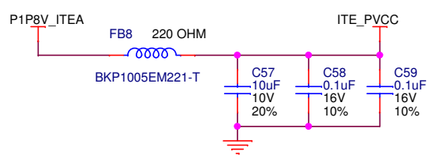
Logic power for analog frontend



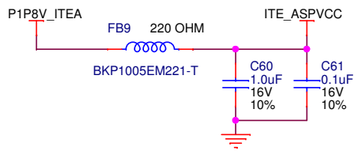
3.3V HDMI RX analog frontend



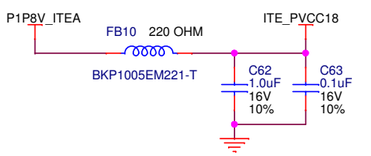
1.8V HDMI RX analog frontend



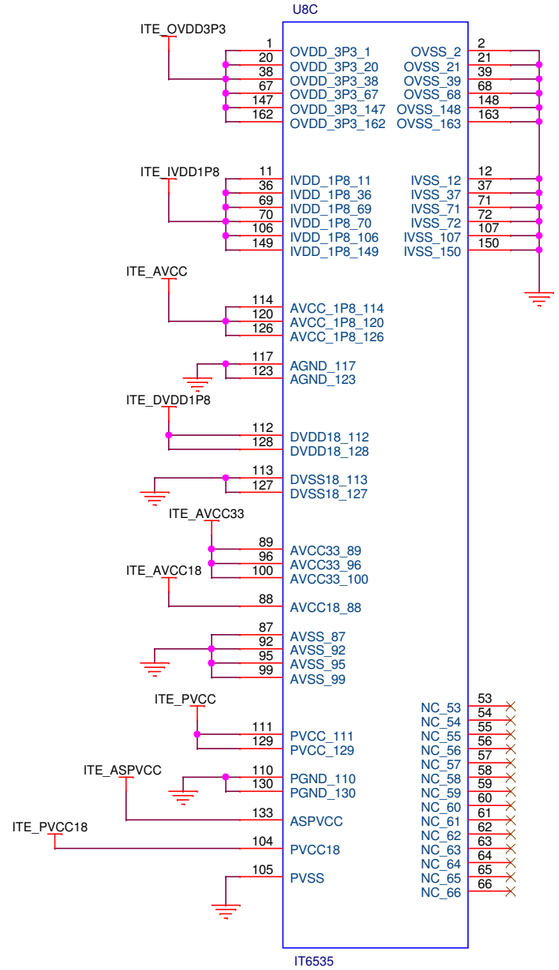
DP Rx PLL power



Crystal and audio PLL



HDMI Rx PLL power



HDMI receiver power/gnd bypass

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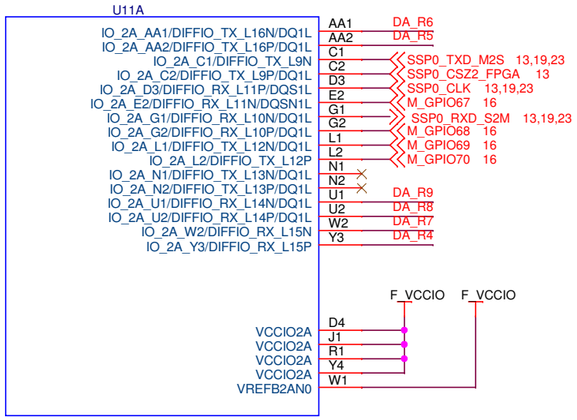

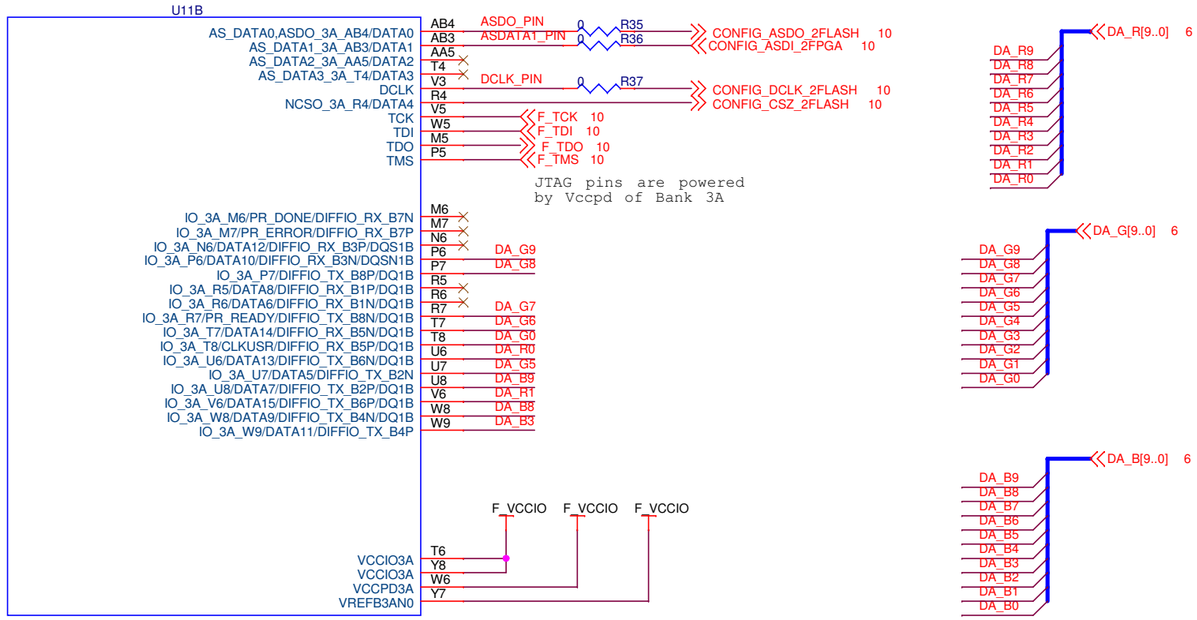

FPGA Bank 2A, 3A, 3B, 4A

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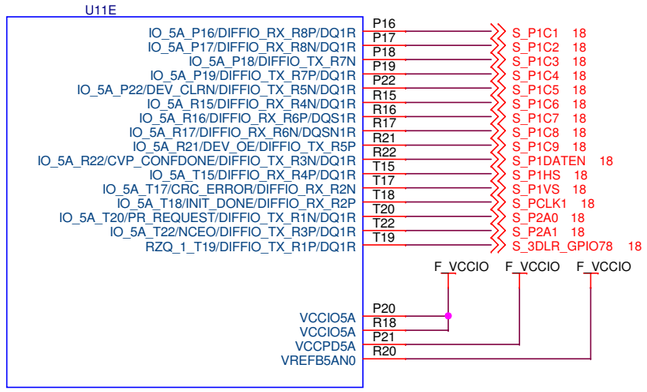

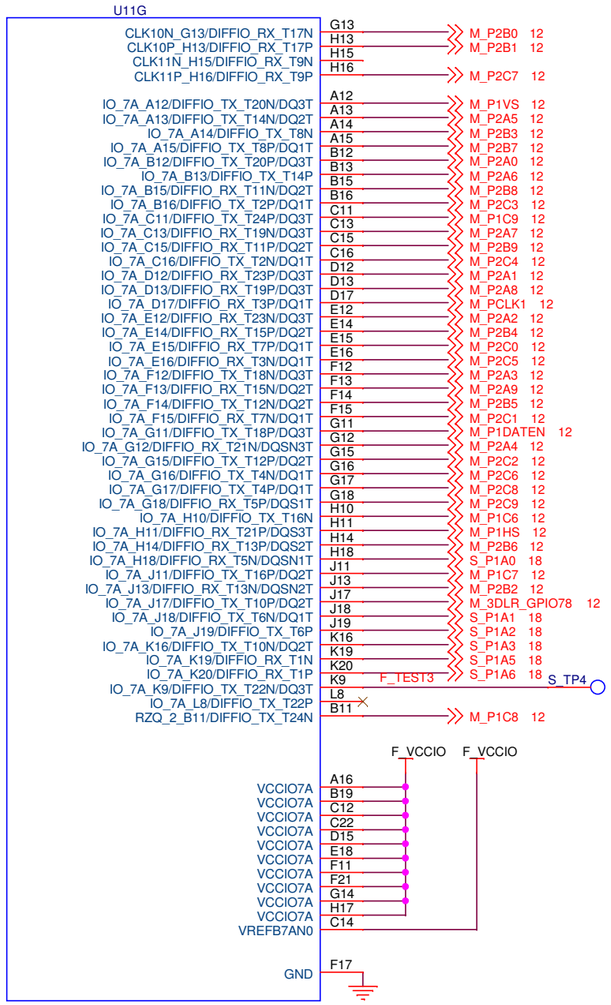

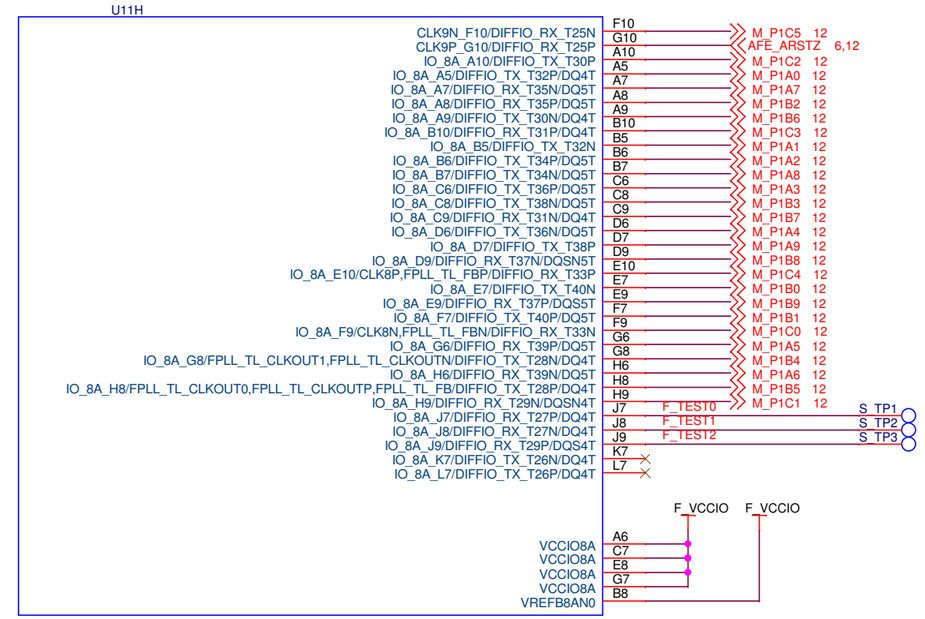

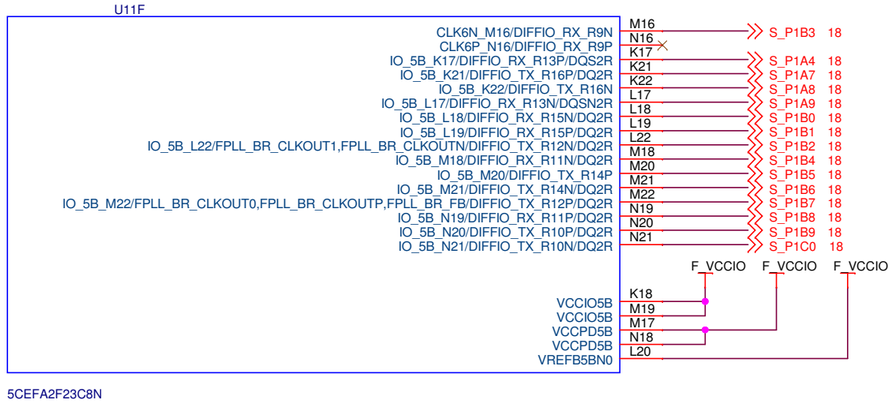

FPGA Bank 5A, 5B, 7A, 8A

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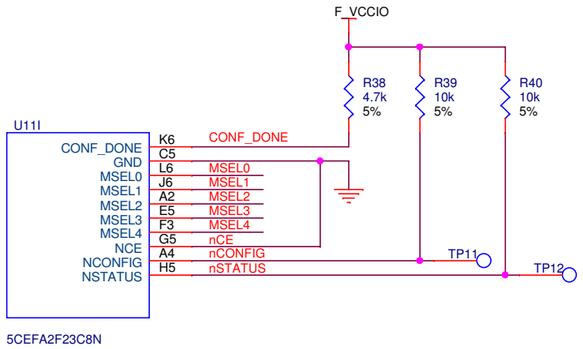
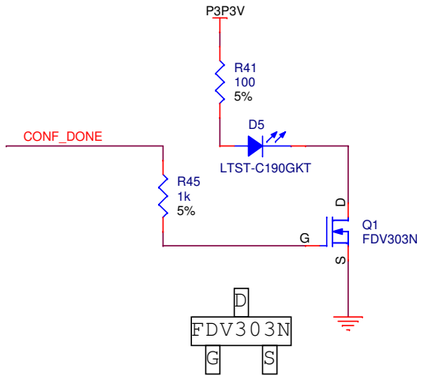
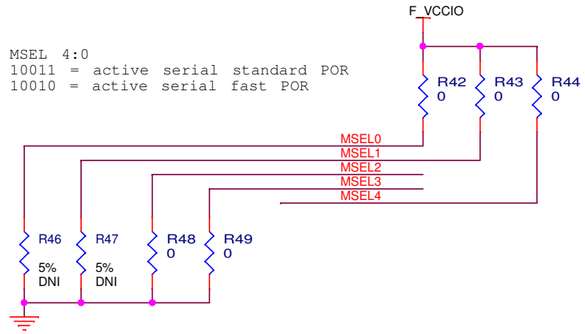
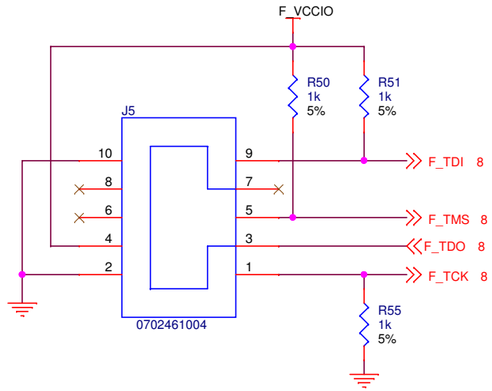
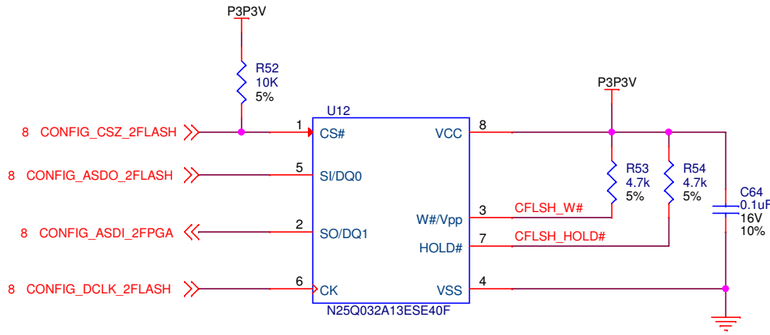








Altera's USB ByteBlaster Connector



Use Altera's "Serial loader" option to update flash
thru the FPGA JTAG port with Byteblaster cable

FPGA Configuration

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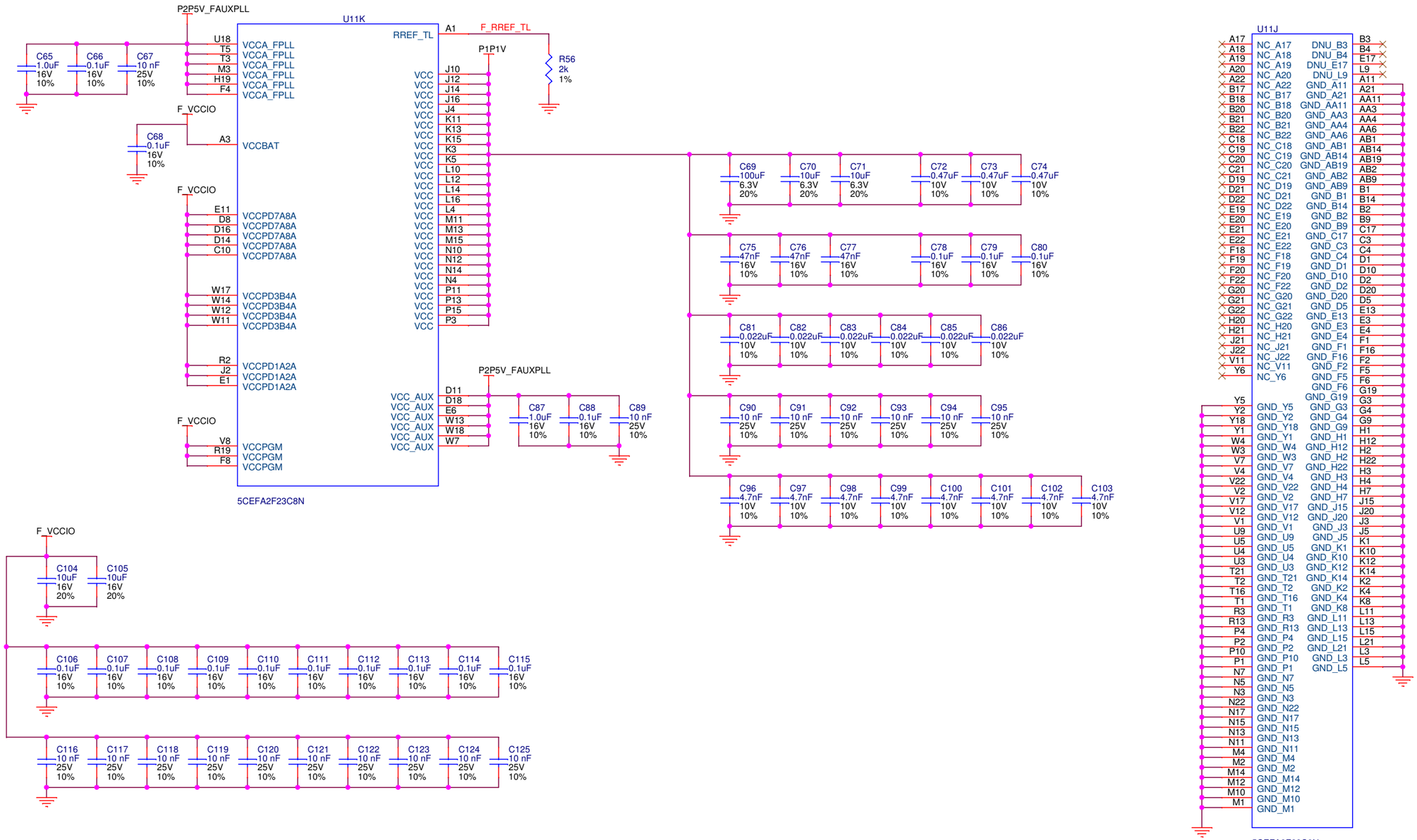

FPGA Pwr/Gnd

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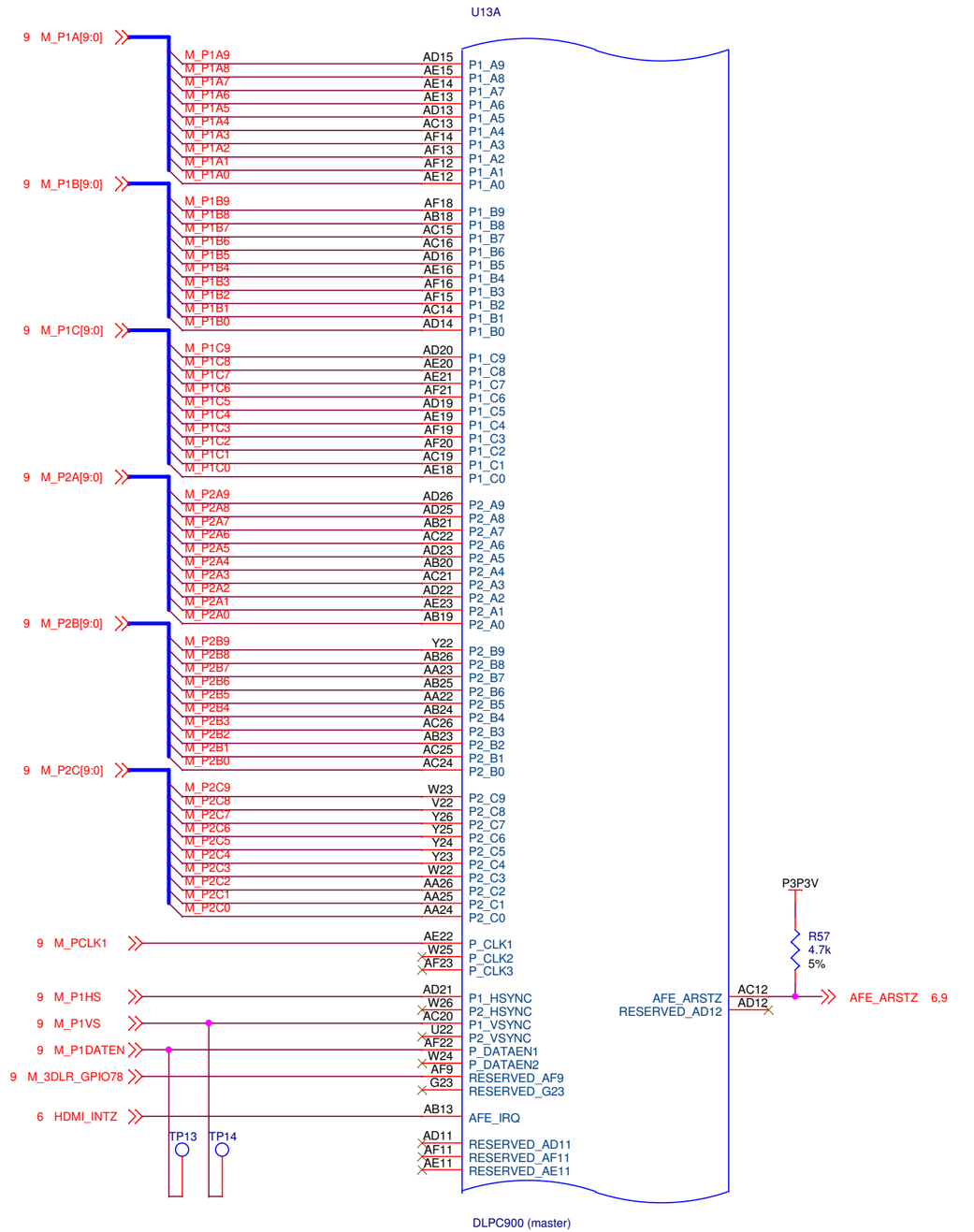

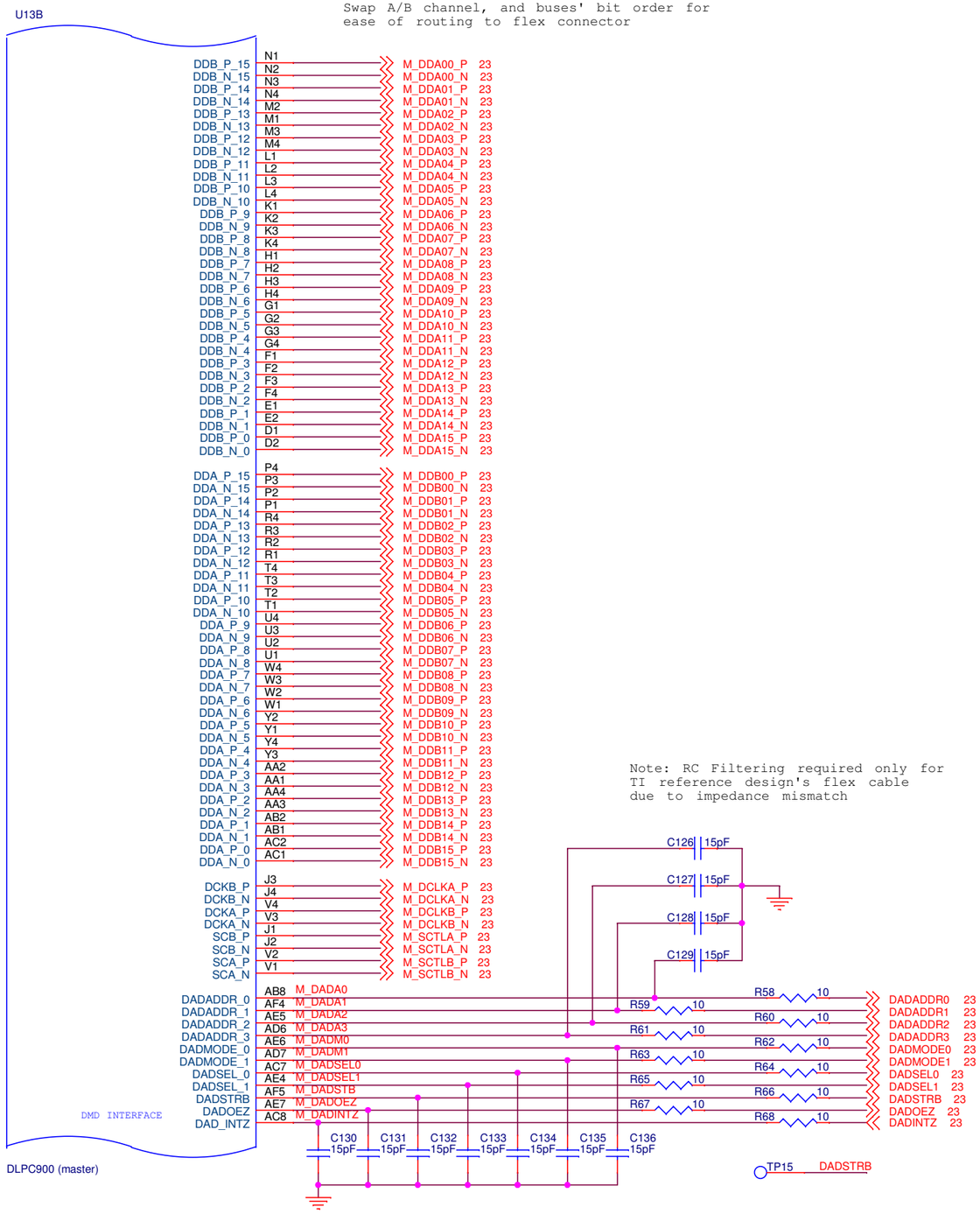

Master Video Input, DMD & DAD Output

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U13D

RESERVED_D26 — D26
RESERVED_E24 — E24
RESERVED_D25 — D25
RESERVED_F22 — F22
RESERVED_F23 — F23
RESERVED_F25 — F25

RESERVED_AE9 — AE9
RESERVED_AD9 — AD9
RESERVED_AB10 — AB10

DLPC900 (master)

UART debug message port,
not needed for production

DNI
J7
P3P3V
1 M_UART0_TXD
2 M_UART0_RXD
3 M_UART0_CTSZ
4 M_UART0_RTSZ
5
6
TMMH-103-01-L-DV
R71 10k 5%

U13E

27 M_OSC20M — M26 MOSCP
N26 MOSCN
P3P3V
R70 10k 5%
M_PMDINTZ — AE8 RESERVED_AE8
19,26 TRIGGER_IN1 — AF7 TRIG_IN_1
15,27 POWERGOOD — T26 PWRGOOD
14,27 M_POSENSE — P22 POSENSE

RESERVED_AD8 — AD8 M_CW_PWM TP16
OCLKA — AF6 M_OCLKA_PIN
R69 33 5%
OCLKA 1 J6 1 2 2
TSM-102-01-T-SV
RESERVED_B23 — B23
RESERVED_C22 — C22
EXT_RSTZ — T24 M_EXT_RSTZ 23
CTRL_ARSTZ — T25
R72 P3P3V 4.7k 5%

DLPC900 (master)

P3P3V
R73 4.7k 5%
R74 4.7k 5%
R75 4.7k 5%
R76 1k 5%

U13H

SSP0_CLK — AD4 — M_SSP0_CLK — R77 33 — SSP0_CLK 8,19,23
SSP0_TXD — AB7 — M_SSP0_TXD — R78 33 — SSP0_TXD_M2S 8,19,23
SSP0_RXD — AD5 — SSP0_RXD_S2M 8,19,23
RESERVED_AB4 — AB4
SSP0_CSZ_2 — AC3 — M_SSP0_CSZ2 — R79 33 — SSP0_CSZ2_FPGA 8
SSP0_CSZ_1 — AB6 — M_SSP0_CSZ1 — R80 33 — SSP0_CSZ1_DMD 23
SSP0_CSZ_0 — AC5 — M_SSP0_CSZ0 — R81 33 — SSP0_CSZ0_DAD1 23

DLPC900 (master)

P3P3V
C137 0.1uF 16V 10%

Buffer to prevent host from detecting
the USB slave before ARM finishes
initialization

U14
SN74AHC1G125DBVR
R82 10k 5%
USB_SENSE — TP17
M_USB_ENZ 16
R83 P3P3V 4.7K 5%
R84 1.5K 5%

M_UART0_TXD — AB3 UART0_TXD
M_UART0_RXD — AD1 UART0_RXD
M_UART0_CTSZ — AE2 UART0_CTSZ
M_UART0_RTSZ — AD2 UART0_RTSZ

J8
1 USB_VBUS
2 USB_DAT_N
3 USB_DAT_P
4
USB Type B Rcpt

R85 22 1% 3/4W — M_USB_N — C5 USB_DAT_N
R86 22 1% 3/4W — M_USB_P — D6 USB_DAT_P

U15
1 NC1
2 GND2
3 NC3
A 6
GND5 5
B 4
SN65220DBVT

Master Controller SSP0, UART0, USB, Reset, OSC

TEXAS INSTRUMENTS	DWN A. Ng	DATE 8/8/2014	A3	DRAWING NO 2513534	REV E
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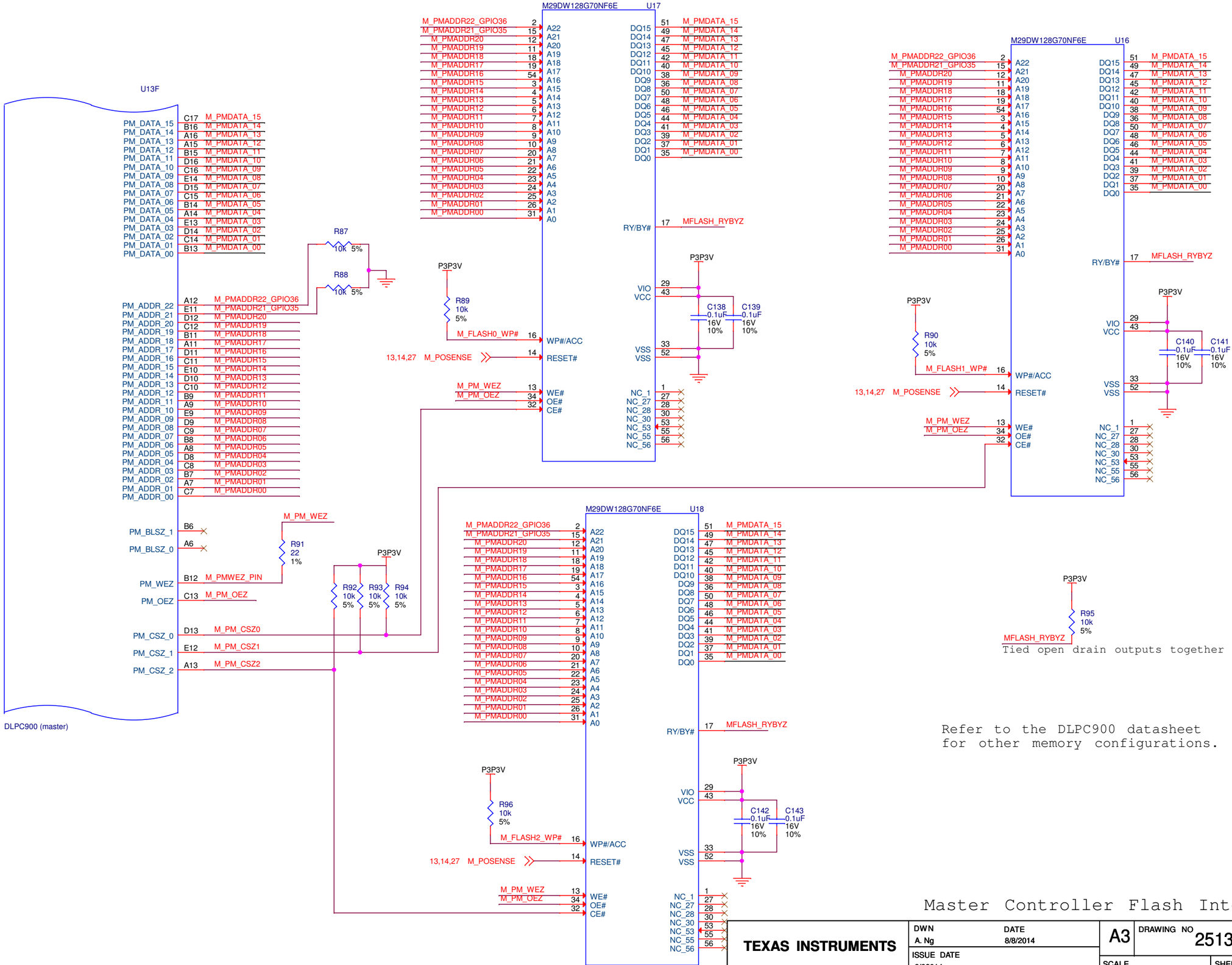
U13F
PM_DATA_15
PM_DATA_14
PM_DATA_13
PM_DATA_12
PM_DATA_11
PM_DATA_10
PM_DATA_09
PM_DATA_08
PM_DATA_07
PM_DATA_06
PM_DATA_05
PM_DATA_04
PM_DATA_03
PM_DATA_02
PM_DATA_01
PM_DATA_00
C17 M_PMDATA_15
B16 M_PMDATA_14
A16 M_PMDATA_13
A15 M_PMDATA_12
B15 M_PMDATA_11
D16 M_PMDATA_10
C16 M_PMDATA_09
E14 M_PMDATA_08
D15 M_PMDATA_07
C15 M_PMDATA_06
B14 M_PMDATA_05
A14 M_PMDATA_04
E13 M_PMDATA_03
D14 M_PMDATA_02
C14 M_PMDATA_01
B13 M_PMDATA_00
R87
10k 5%
R88
10k 5%
A12 M_PMADDR22_GPIO36
E11 M_PMADDR21_GPIO35
D12 M_PMADDR20
C12 M_PMADDR19
B11 M_PMADDR18
A11 M_PMADDR17
D11 M_PMADDR16
C11 M_PMADDR15
E10 M_PMADDR14
D10 M_PMADDR13
C10 M_PMADDR12
B9 M_PMADDR11
A9 M_PMADDR10
E9 M_PMADDR09
D9 M_PMADDR08
C9 M_PMADDR07
B8 M_PMADDR06
A8 M_PMADDR05
D8 M_PMADDR04
C8 M_PMADDR03
B7 M_PMADDR02
A7 M_PMADDR01
C7 M_PMADDR00
M_PM_WEZ
PM_BLSZ_1 B6
PM_BLSZ_0 A6
R91
22
1%
PM_WEZ B12 M_PMWEZ_PIN
PM_OEZ C13 M_PM_OEZ
P3P3V
R92 10k 5%
R93 10k 5%
R94 10k 5%
PM_CSZ_0 D13 M_PM_CSZ0
PM_CSZ_1 E12 M_PM_CSZ1
PM_CSZ_2 A13 M_PM_CSZ2
DLPC900 (master)
M29DW128G70NF6E U17
M_PMADDR22_GPIO36 2
M_PMADDR21_GPIO35 15
M_PMADDR20 12
M_PMADDR19 11
M_PMADDR18 18
M_PMADDR17 19
M_PMADDR16 54
M_PMADDR15 3
M_PMADDR14 4
M_PMADDR13 5
M_PMADDR12 6
M_PMADDR11 7
M_PMADDR10 8
M_PMADDR09 9
M_PMADDR08 10
M_PMADDR07 20
M_PMADDR06 21
M_PMADDR05 22
M_PMADDR04 23
M_PMADDR03 24
M_PMADDR02 25
M_PMADDR01 26
M_PMADDR00 31
A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
DQ15 51 M_PMDATA_15
DQ14 49 M_PMDATA_14
DQ13 47 M_PMDATA_13
DQ12 45 M_PMDATA_12
DQ11 42 M_PMDATA_11
DQ10 40 M_PMDATA_10
DQ9 38 M_PMDATA_09
DQ8 36 M_PMDATA_08
DQ7 50 M_PMDATA_07
DQ6 48 M_PMDATA_06
DQ5 46 M_PMDATA_05
DQ4 44 M_PMDATA_04
DQ3 41 M_PMDATA_03
DQ2 39 M_PMDATA_02
DQ1 37 M_PMDATA_01
DQ0 35 M_PMDATA_00
RY/BY# 17 MFLASH_RYBYZ
P3P3V
R89
10k
5%
M_FLASH0_WP# 16 WP#/ACC
13,14,27 M_POSENSE 14 RESET#
VIO 29
VCC 43
C138 0.1uF 16V 10%
C139 0.1uF 16V 10%
VSS 33
VSS 52
M_PM_WEZ 13 WE#
M_PM_OEZ 34 OE#
32 CE#
NC_1 1
NC_27 27
NC_28 28
NC_30 30
NC_53 53
NC_55 55
NC_56 56
M29DW128G70NF6E U16
M_PMADDR22_GPIO36 2
M_PMADDR21_GPIO35 15
M_PMADDR20 12
M_PMADDR19 11
M_PMADDR18 18
M_PMADDR17 19
M_PMADDR16 54
M_PMADDR15 3
M_PMADDR14 4
M_PMADDR13 5
M_PMADDR12 6
M_PMADDR11 7
M_PMADDR10 8
M_PMADDR09 9
M_PMADDR08 10
M_PMADDR07 20
M_PMADDR06 21
M_PMADDR05 22
M_PMADDR04 23
M_PMADDR03 24
M_PMADDR02 25
M_PMADDR01 26
M_PMADDR00 31
A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
DQ15 51 M_PMDATA_15
DQ14 49 M_PMDATA_14
DQ13 47 M_PMDATA_13
DQ12 45 M_PMDATA_12
DQ11 42 M_PMDATA_11
DQ10 40 M_PMDATA_10
DQ9 38 M_PMDATA_09
DQ8 36 M_PMDATA_08
DQ7 50 M_PMDATA_07
DQ6 48 M_PMDATA_06
DQ5 46 M_PMDATA_05
DQ4 44 M_PMDATA_04
DQ3 41 M_PMDATA_03
DQ2 39 M_PMDATA_02
DQ1 37 M_PMDATA_01
DQ0 35 M_PMDATA_00
RY/BY# 17 MFLASH_RYBYZ
P3P3V
R90
10k
5%
M_FLASH1_WP# 16 WP#/ACC
13,14,27 M_POSENSE 14 RESET#
VIO 29
VCC 43
C140 0.1uF 16V 10%
C141 0.1uF 16V 10%
VSS 33
VSS 52
M_PM_WEZ 13 WE#
M_PM_OEZ 34 OE#
32 CE#
NC_1 1
NC_27 27
NC_28 28
NC_30 30
NC_53 53
NC_55 55
NC_56 56
M29DW128G70NF6E U18
M_PMADDR22_GPIO36 2
M_PMADDR21_GPIO35 15
M_PMADDR20 12
M_PMADDR19 11
M_PMADDR18 18
M_PMADDR17 19
M_PMADDR16 54
M_PMADDR15 3
M_PMADDR14 4
M_PMADDR13 5
M_PMADDR12 6
M_PMADDR11 7
M_PMADDR10 8
M_PMADDR09 9
M_PMADDR08 10
M_PMADDR07 20
M_PMADDR06 21
M_PMADDR05 22
M_PMADDR04 23
M_PMADDR03 24
M_PMADDR02 25
M_PMADDR01 26
M_PMADDR00 31
A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
DQ15 51 M_PMDATA_15
DQ14 49 M_PMDATA_14
DQ13 47 M_PMDATA_13
DQ12 45 M_PMDATA_12
DQ11 42 M_PMDATA_11
DQ10 40 M_PMDATA_10
DQ9 38 M_PMDATA_09
DQ8 36 M_PMDATA_08
DQ7 50 M_PMDATA_07
DQ6 48 M_PMDATA_06
DQ5 46 M_PMDATA_05
DQ4 44 M_PMDATA_04
DQ3 41 M_PMDATA_03
DQ2 39 M_PMDATA_02
DQ1 37 M_PMDATA_01
DQ0 35 M_PMDATA_00
RY/BY# 17 MFLASH_RYBYZ
P3P3V
R96
10k
5%
M_FLASH2_WP# 16 WP#/ACC
13,14,27 M_POSENSE 14 RESET#
VIO 29
VCC 43
C142 0.1uF 16V 10%
C143 0.1uF 16V 10%
VSS 33
VSS 52
M_PM_WEZ 13 WE#
M_PM_OEZ 34 OE#
32 CE#
NC_1 1
NC_27 27
NC_28 28
NC_30 30
NC_53 53
NC_55 55
NC_56 56
P3P3V
R95
10k
5%
MFLASH_RYBYZ
Tied open drain outputs together
Refer to the DLPC900 datasheet
for other memory configurations.
Master Controller Flash Interface
TEXAS INSTRUMENTS
DWN A. Ng
DATE 8/8/2014
ISSUE DATE 8/82014
A3
DRAWING NO 2513534
REV E
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ARM Multi-ICE debug port

P3P3V

J9
5103308-5

C145 0.1uF 16V 10%

R98 10k 5%
R99 10k 5%
R100 10k 5%
R101 10k 5%
R102 5% DNI

TRSTZ_IN
TDI
TMS2 15,19
RTCK
TDO2
SRSTZ
TCK 15,19

C144 0.1uF 16V 10%
U19 SN74AHC1G125DBVR
R97 4.7k 5%
TRSTZ 15,19
R103 10K 5%
R104 10K 5%

C146 0.1uF 16V 10%
U20 TPS3838K33
VDD MR RESET CT GND
R105 4.7k 5%
BUTTON_RSTZ
SW1 TL1105F100Q
J10 TSM-102-01-T-SV

Install jumper to hold controllers in reset

19 S_RTCK
M_RTCK
R106 DNI
R107 0
RTCK

Install R106 only if slave controller is not populated for single controller operation

19 S_TDO2
M_TDO2
R109 DNI
R110 0
TDO2

Install R109 only if slave controller is not populated for single controller operation

19 S_TDO1
M_TDO1
R111 DNI
R112 0
TDO1

Install R111 only if slave controller is not populated for single controller operation

R108 10k 5%

C147 0.1uF 16V 10%
U21 SN74LVC1G07DBVR
POWERGOOD 13,27

Pullup on open-drain signal POWERGOOD found on page 27

J11
1 TRSTZ
2 TDI
3 TMS1 19
4 TDO1
5 TCK 15,19
6

JTAG Boundary scan port may be used to download flash image using USB-to-JTAG FTDI adapter board

R117 0
R118 DNI
19 S_TDI

Install R118 if using the JTAG boundary scan port to program the external flash memory with TI GUI's flash downloader. R117 is installed only if using the ARM Realview ICE debugger HW.

R119 4.7K 5%

U13G DLPC900 (master)

M_TDO2 N22 TDO2
M_TDO1 N23 TDO1
15,19 TMS2 P26 TMS2
TMS1 P25 TMS1
TDI N25 TDI
15,19 TCK N24 TCK
15,19 TRSTZ M23 TRSTZ
M24 ICTSEN
M25 HW_TEST_EN

RESERVED_E8 E8 M_TSTPT7 TP18
RESERVED_B4 B4 M_TSTPT6 TP19
RESERVED_C4 C4 M_TSTPT5 TP20
RESERVED_E7 E7 M_TSTPT4 TP21
RESERVED_E7 D5 M_TSTPT3
RESERVED_D5 E6 M_TSTPT2
RESERVED_E6 D3 M_TSTPT1
RESERVED_D3 C2 M_TSTPT0
RESERVED_C2

R113 R114 R115 R116 5% DNI
TP22 TP23 TP24 TP25

RESERVED_A4 A4 M_PIPESTAT2 TP26
RESERVED_B5 B5 M_PIPESTAT1 TP27
RESERVED_C6 C6 M_PIPESTAT0 TP28
RESERVED_A5 A5 M_TRACESYNC TP29
RESERVED_D7 D7 M_TRACECLK TP30
RTCK E4 M_RTCK_PIN
R120 33 5% M_RTCK

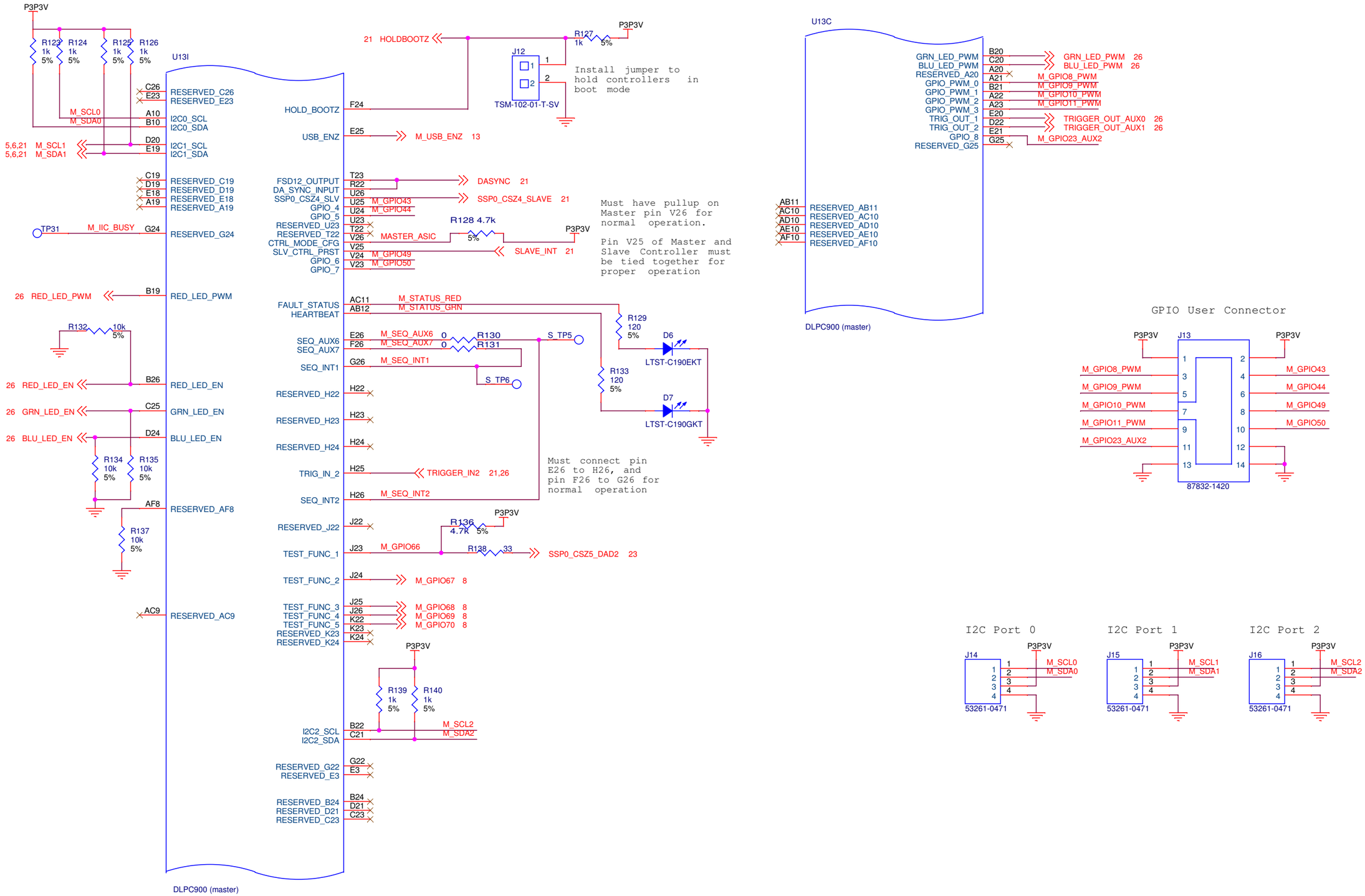
SEQ_SYNC AB9 M_SEQSYNC_PIN
R122 33 5%
R121 10k 5%
SEQ_SYNC 19

SEQ_SYNC used to synchronize PWM sequences in multi-controller system

VPGM AC6

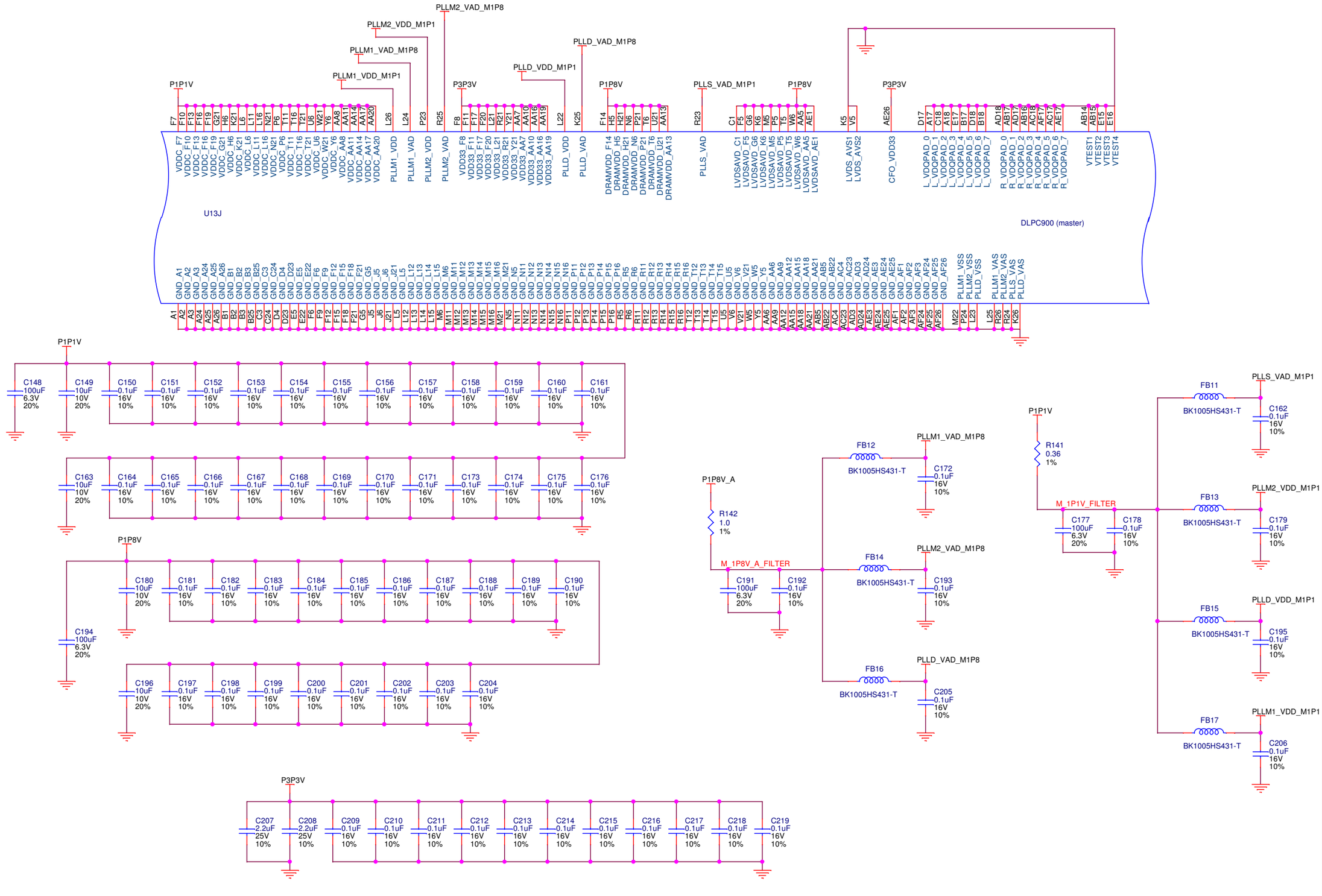
Master Controller Multi-ICE Port

TEXAS INSTRUMENTS	DWN A. Ng	DATE 8/8/2014	A3	DRAWING NO 2513534 REV E
	ISSUE DATE 8/82014		SCALE	SHEET 15 OF 28



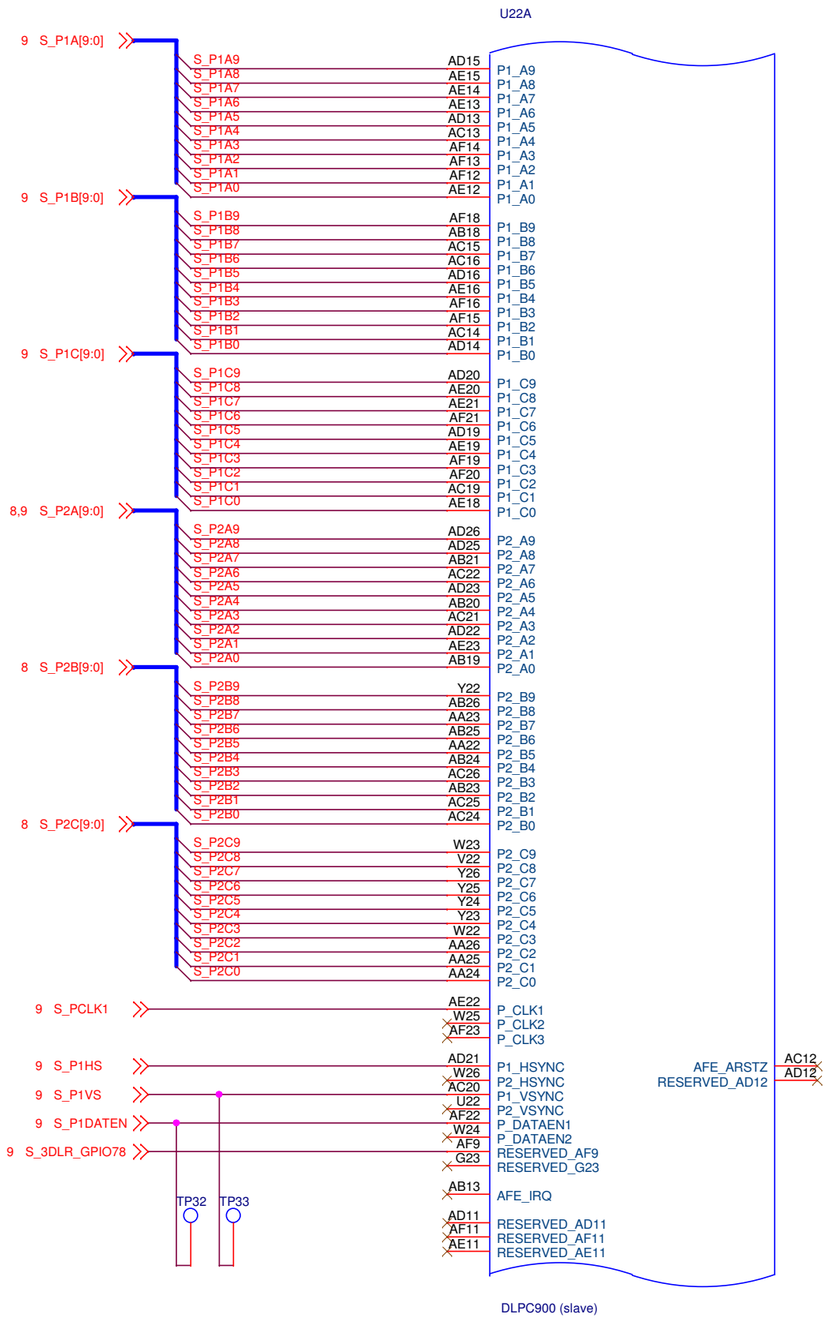
Master I2C, LED driver interface, In/Out Triggers and GPIOs

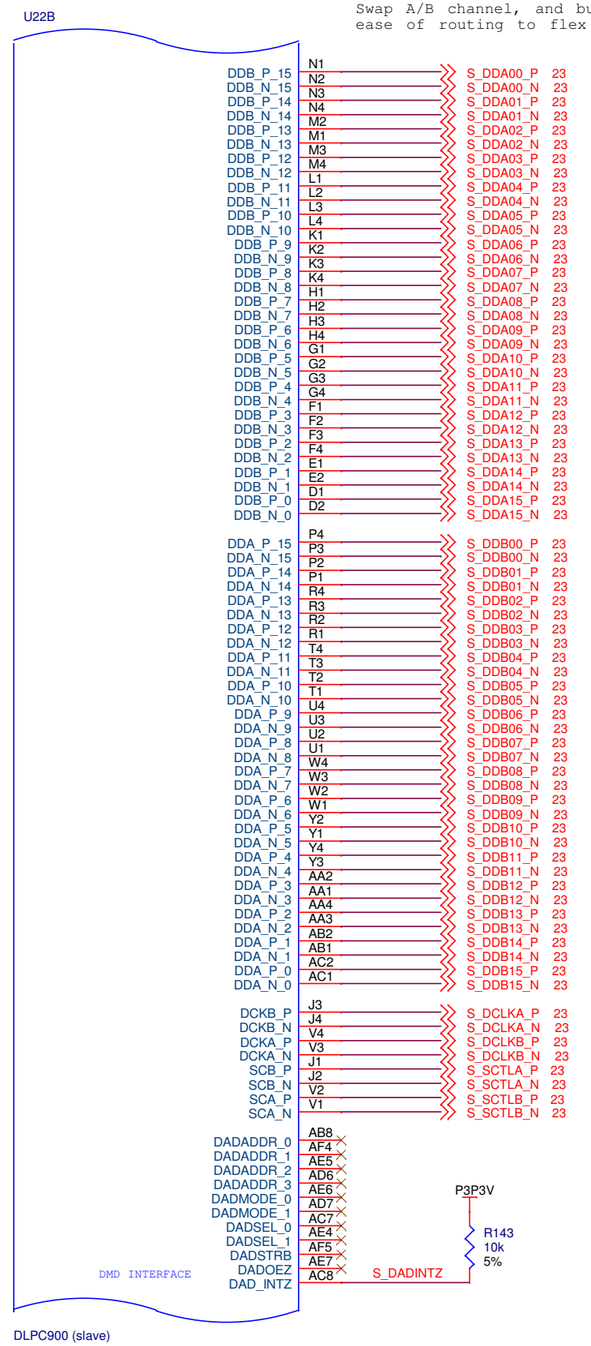
TEXAS INSTRUMENTS	DWN A. Ng	DATE 8/8/2014	A3	DRAWING NO 2513534	REV E
	ISSUE DATE 8/82014			SCALE	SHEET 16 OF 28



Master Controller Pwr Gnd

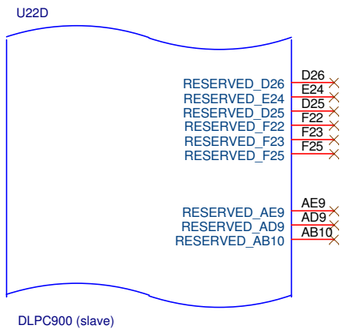
TEXAS INSTRUMENTS	DWN A. Ng	DATE 8/8/2014	A3	DRAWING NO 2513534 REV E
	ISSUE DATE 8/82014		SCALE	SHEET 17 OF 28

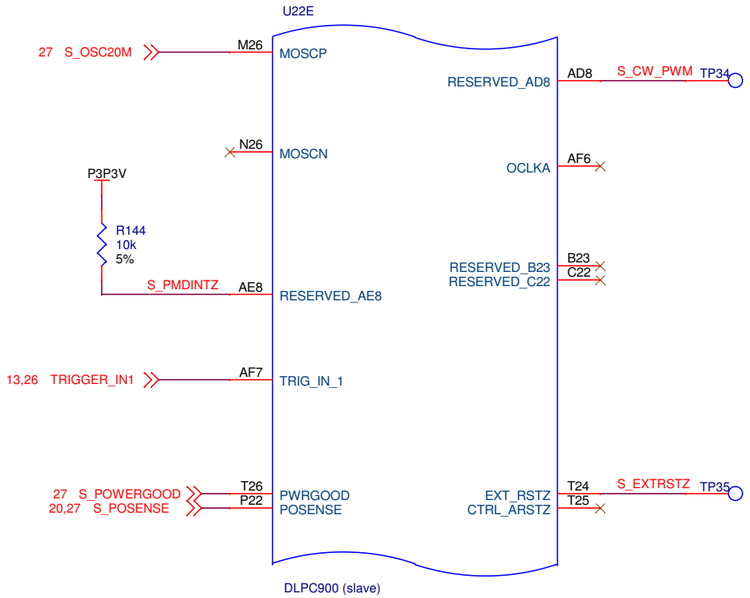


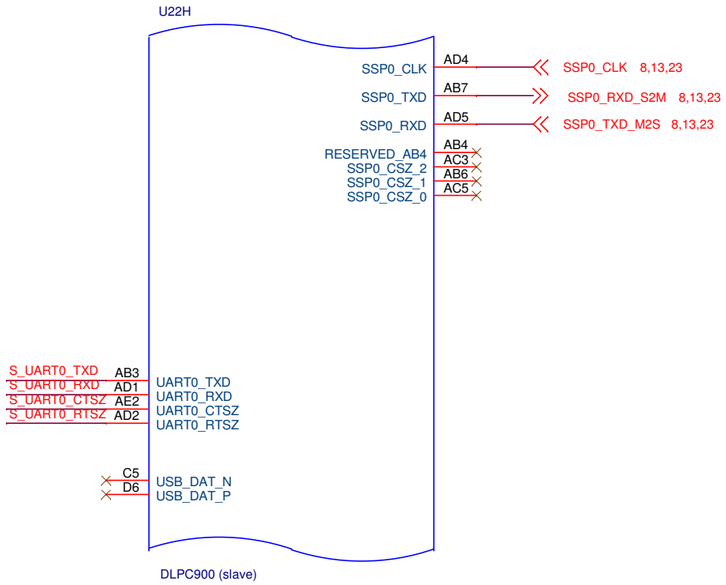


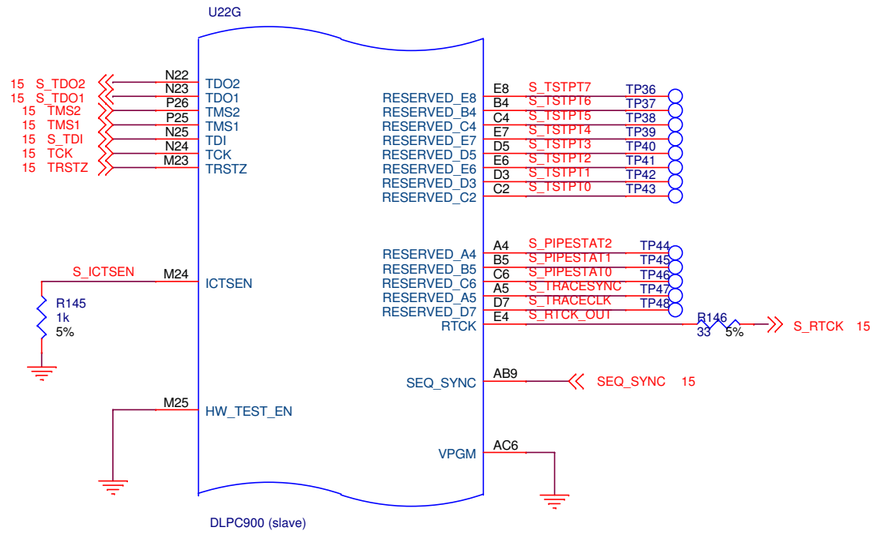
Slave Video Input, DMD Output

TEXAS INSTRUMENTS	DWN A. Ng	DATE 8/8/2014	A3	DRAWING NO 2513534 REV E
	ISSUE DATE 8/82014		SCALE	SHEET 18 OF 28



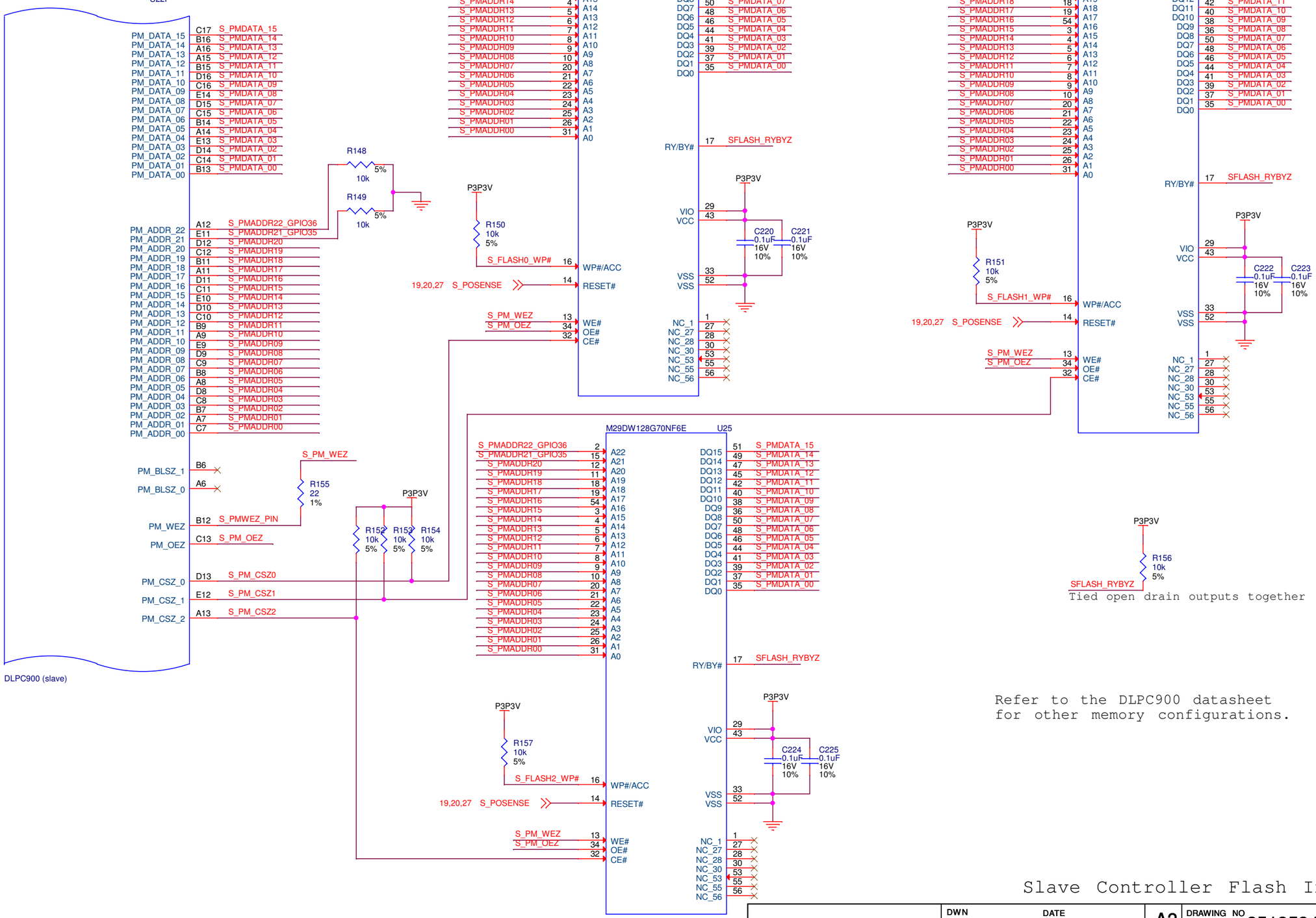






Slave Controller Reset, OSC, JTAG, UART0, SSP Port

TEXAS INSTRUMENTS	DWN A. Ng	DATE 8/8/2014	A3	DRAWING NO 2513534 REV E
	ISSUE DATE 8/82014		SCALE	SHEET 19 OF 28


U22F
PM_DATA_15
PM_DATA_14
PM_DATA_13
PM_DATA_12
PM_DATA_11
PM_DATA_10
PM_DATA_09
PM_DATA_08
PM_DATA_07
PM_DATA_06
PM_DATA_05
PM_DATA_04
PM_DATA_03
PM_DATA_02
PM_DATA_01
PM_DATA_00
C17 S_PMDATA_15
B16 S_PMDATA_14
A16 S_PMDATA_13
A15 S_PMDATA_12
B15 S_PMDATA_11
D16 S_PMDATA_10
C16 S_PMDATA_09
E14 S_PMDATA_08
D15 S_PMDATA_07
C15 S_PMDATA_06
B14 S_PMDATA_05
A14 S_PMDATA_04
E13 S_PMDATA_03
D14 S_PMDATA_02
C14 S_PMDATA_01
B13 S_PMDATA_00
R148 10k 5%
R149 10k 5%
PM_ADDR_22
PM_ADDR_21
PM_ADDR_20
PM_ADDR_19
PM_ADDR_18
PM_ADDR_17
PM_ADDR_16
PM_ADDR_15
PM_ADDR_14
PM_ADDR_13
PM_ADDR_12
PM_ADDR_11
PM_ADDR_10
PM_ADDR_09
PM_ADDR_08
PM_ADDR_07
PM_ADDR_06
PM_ADDR_05
PM_ADDR_04
PM_ADDR_03
PM_ADDR_02
PM_ADDR_01
PM_ADDR_00
A12 S_PMADDR22_GPIO36
E11 S_PMADDR21_GPIO35
D12 S_PMADDR20
C12 S_PMADDR19
B11 S_PMADDR18
A11 S_PMADDR17
D11 S_PMADDR16
C11 S_PMADDR15
E10 S_PMADDR14
D10 S_PMADDR13
C10 S_PMADDR12
B9 S_PMADDR11
A9 S_PMADDR10
E9 S_PMADDR09
D9 S_PMADDR08
C9 S_PMADDR07
B8 S_PMADDR06
A8 S_PMADDR05
D8 S_PMADDR04
C8 S_PMADDR03
B7 S_PMADDR02
A7 S_PMADDR01
C7 S_PMADDR00
PM_BLSZ_1
PM_BLSZ_0
B6
A6
S_PM_WEZ
R155 22 1%
PM_WEZ
B12 S_PMWEZ_PIN
PM_OEZ
C13 S_PM_OEZ
PM_CSZ_0
PM_CSZ_1
PM_CSZ_2
D13 S_PM_CSZ0
E12 S_PM_CSZ1
A13 S_PM_CSZ2
DLPC900 (slave)
M29DW128G70NF6E U23
S_PMADDR22_GPIO36 2 A22
S_PMADDR21_GPIO35 15 A21
S_PMADDR20 12 A20
S_PMADDR19 11 A19
S_PMADDR18 18 A18
S_PMADDR17 19 A17
S_PMADDR16 54 A16
S_PMADDR15 3 A15
S_PMADDR14 4 A14
S_PMADDR13 5 A13
S_PMADDR12 6 A12
S_PMADDR11 7 A11
S_PMADDR10 8 A10
S_PMADDR09 9 A9
S_PMADDR08 10 A8
S_PMADDR07 20 A7
S_PMADDR06 21 A6
S_PMADDR05 22 A5
S_PMADDR04 23 A4
S_PMADDR03 24 A3
S_PMADDR02 25 A2
S_PMADDR01 26 A1
S_PMADDR00 31 A0
DQ15 51 S_PMDATA_15
DQ14 49 S_PMDATA_14
DQ13 47 S_PMDATA_13
DQ12 45 S_PMDATA_12
DQ11 42 S_PMDATA_11
DQ10 40 S_PMDATA_10
DQ9 38 S_PMDATA_09
DQ8 36 S_PMDATA_08
DQ7 50 S_PMDATA_07
DQ6 48 S_PMDATA_06
DQ5 46 S_PMDATA_05
DQ4 44 S_PMDATA_04
DQ3 41 S_PMDATA_03
DQ2 39 S_PMDATA_02
DQ1 37 S_PMDATA_01
DQ0 35 S_PMDATA_00
RY/BY# 17 SFLASH_RYBYZ
P3P3V
VIO 29
VCC 43
C220 0.1uF 16V 10%
C221 0.1uF 16V 10%
VSS 33
VSS 52
NC_1 1
NC_27 28
NC_28 30
NC_30 53
NC_53 55
NC_55 56
R150 10k 5%
S_FLASH0_WP# 16 WP#/ACC
19,20,27 S_POSENSE 14 RESET#
S_PM_WEZ 13 WE#
S_PM_OEZ 34 OE#
32 CE#
M29DW128G70NF6E U24
S_PMADDR22_GPIO36 2 A22
S_PMADDR21_GPIO35 15 A21
S_PMADDR20 12 A20
S_PMADDR19 11 A19
S_PMADDR18 18 A18
S_PMADDR17 19 A17
S_PMADDR16 54 A16
S_PMADDR15 3 A15
S_PMADDR14 4 A14
S_PMADDR13 5 A13
S_PMADDR12 6 A12
S_PMADDR11 7 A11
S_PMADDR10 8 A10
S_PMADDR09 9 A9
S_PMADDR08 10 A8
S_PMADDR07 20 A7
S_PMADDR06 21 A6
S_PMADDR05 22 A5
S_PMADDR04 23 A4
S_PMADDR03 24 A3
S_PMADDR02 25 A2
S_PMADDR01 26 A1
S_PMADDR00 31 A0
DQ15 51 S_PMDATA_15
DQ14 49 S_PMDATA_14
DQ13 47 S_PMDATA_13
DQ12 42 S_PMDATA_12
DQ11 40 S_PMDATA_11
DQ10 38 S_PMDATA_10
DQ9 36 S_PMDATA_09
DQ8 50 S_PMDATA_08
DQ7 48 S_PMDATA_07
DQ6 46 S_PMDATA_06
DQ5 44 S_PMDATA_05
DQ4 41 S_PMDATA_04
DQ3 39 S_PMDATA_03
DQ2 37 S_PMDATA_02
DQ1 35 S_PMDATA_01
DQ0 35 S_PMDATA_00
RY/BY# 17 SFLASH_RYBYZ
P3P3V
VIO 29
VCC 43
C222 0.1uF 16V 10%
C223 0.1uF 16V 10%
VSS 33
VSS 52
NC_1 1
NC_27 28
NC_28 30
NC_30 53
NC_53 55
NC_55 56
R151 10k 5%
S_FLASH1_WP# 16 WP#/ACC
19,20,27 S_POSENSE 14 RESET#
S_PM_WEZ 13 WE#
S_PM_OEZ 34 OE#
32 CE#
M29DW128G70NF6E U25
S_PMADDR22_GPIO36 2 A22
S_PMADDR21_GPIO35 15 A21
S_PMADDR20 12 A20
S_PMADDR19 11 A19
S_PMADDR18 18 A18
S_PMADDR17 19 A17
S_PMADDR16 54 A16
S_PMADDR15 3 A15
S_PMADDR14 4 A14
S_PMADDR13 5 A13
S_PMADDR12 6 A12
S_PMADDR11 7 A11
S_PMADDR10 8 A10
S_PMADDR09 9 A9
S_PMADDR08 10 A8
S_PMADDR07 20 A7
S_PMADDR06 21 A6
S_PMADDR05 22 A5
S_PMADDR04 23 A4
S_PMADDR03 24 A3
S_PMADDR02 25 A2
S_PMADDR01 26 A1
S_PMADDR00 31 A0
DQ15 51 S_PMDATA_15
DQ14 49 S_PMDATA_14
DQ13 47 S_PMDATA_13
DQ12 42 S_PMDATA_12
DQ11 40 S_PMDATA_11
DQ10 38 S_PMDATA_10
DQ9 36 S_PMDATA_09
DQ8 50 S_PMDATA_08
DQ7 48 S_PMDATA_07
DQ6 46 S_PMDATA_06
DQ5 44 S_PMDATA_05
DQ4 41 S_PMDATA_04
DQ3 39 S_PMDATA_03
DQ2 37 S_PMDATA_02
DQ1 35 S_PMDATA_01
DQ0 35 S_PMDATA_00
RY/BY# 17 SFLASH_RYBYZ
P3P3V
VIO 29
VCC 43
C224 0.1uF 16V 10%
C225 0.1uF 16V 10%
VSS 33
VSS 52
NC_1 1
NC_27 28
NC_28 30
NC_30 53
NC_53 55
NC_55 56
R152 10k 5%
R153 10k 5%
R154 10k 5%
R157 10k 5%
S_FLASH2_WP# 16 WP#/ACC
19,20,27 S_POSENSE 14 RESET#
S_PM_WEZ 13 WE#
S_PM_OEZ 34 OE#
32 CE#
P3P3V
R156 10k 5%
SFLASH_RYBYZ
Tied open drain outputs together
Refer to the DLPC900 datasheet
for other memory configurations.
Slave Controller Flash Interface
TEXAS INSTRUMENTS
DWN A. Ng
DATE 8/8/2014
ISSUE DATE 8/82014
A3
DRAWING NO 2513534
REV E
SCALE
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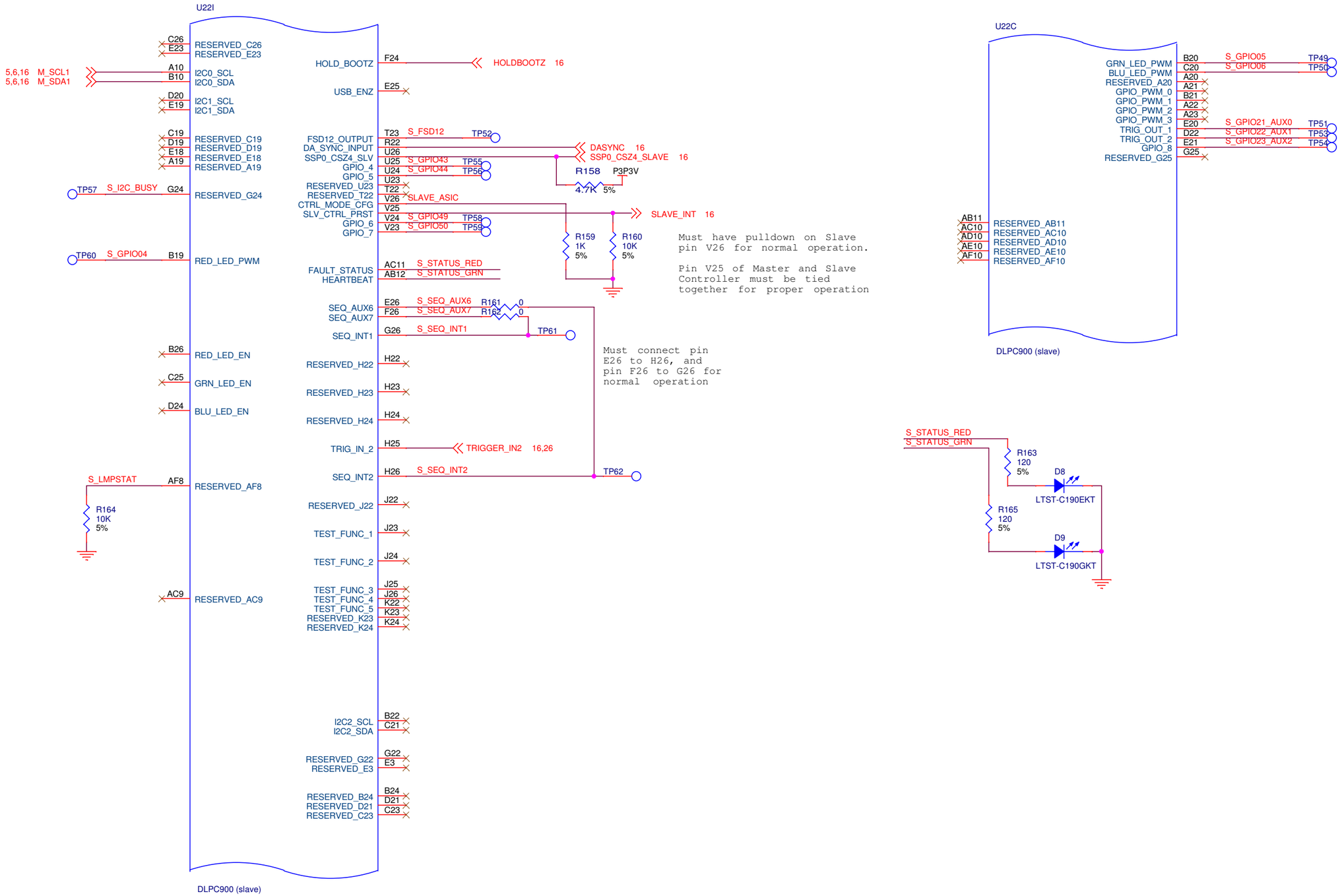

Must connect pin E26 to H26, and pin F26 to G26 for normal operation

Slave Controller I2C, GPIOs

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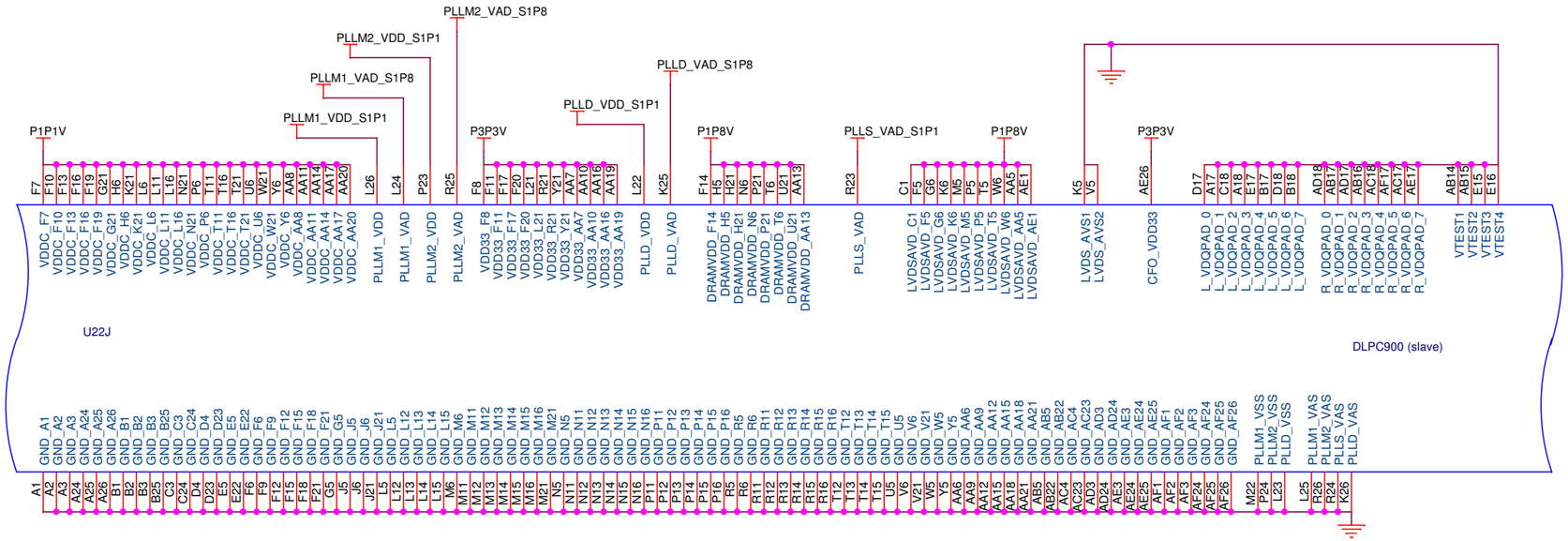

Slave Controller Pwr Gnd

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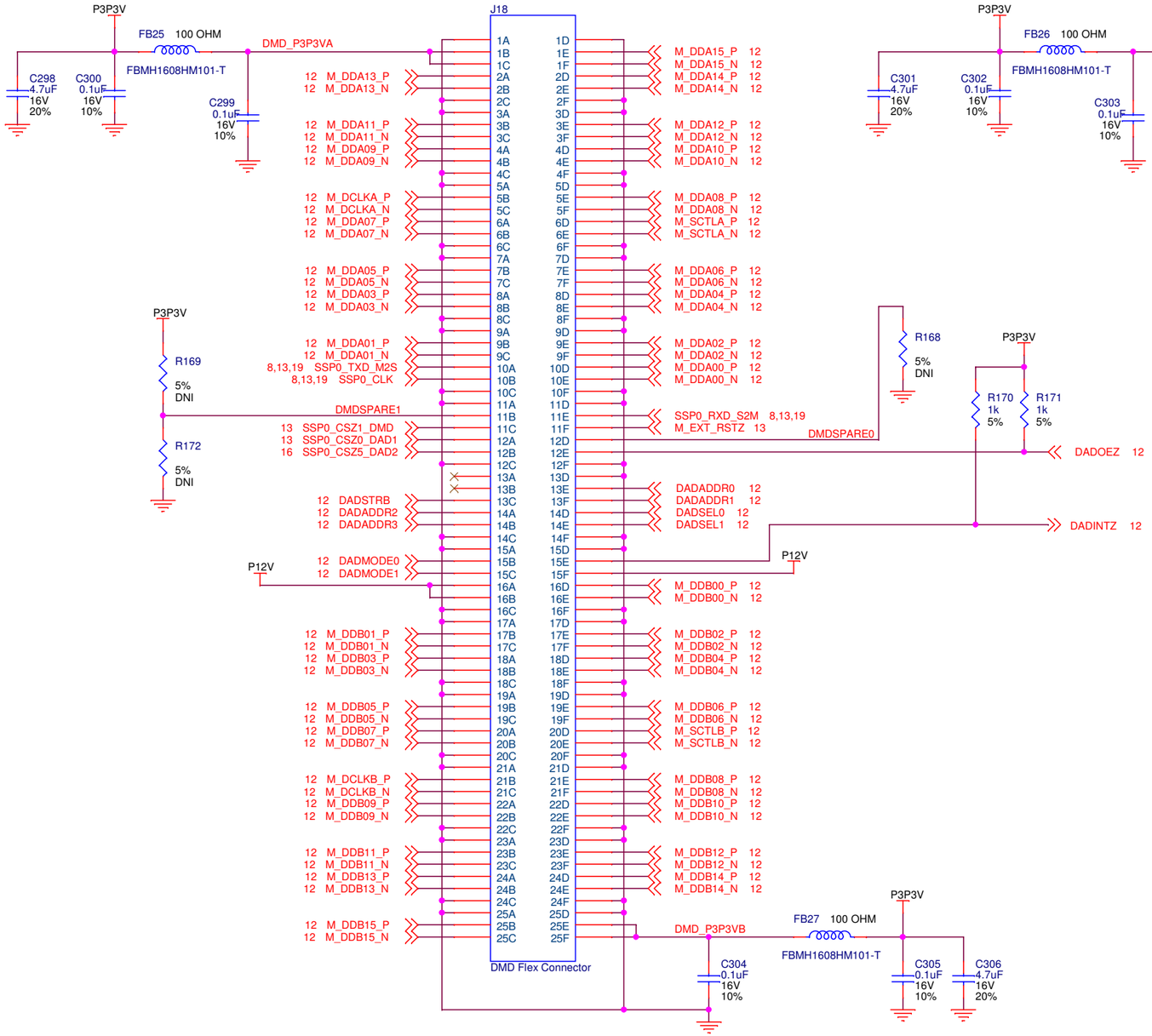
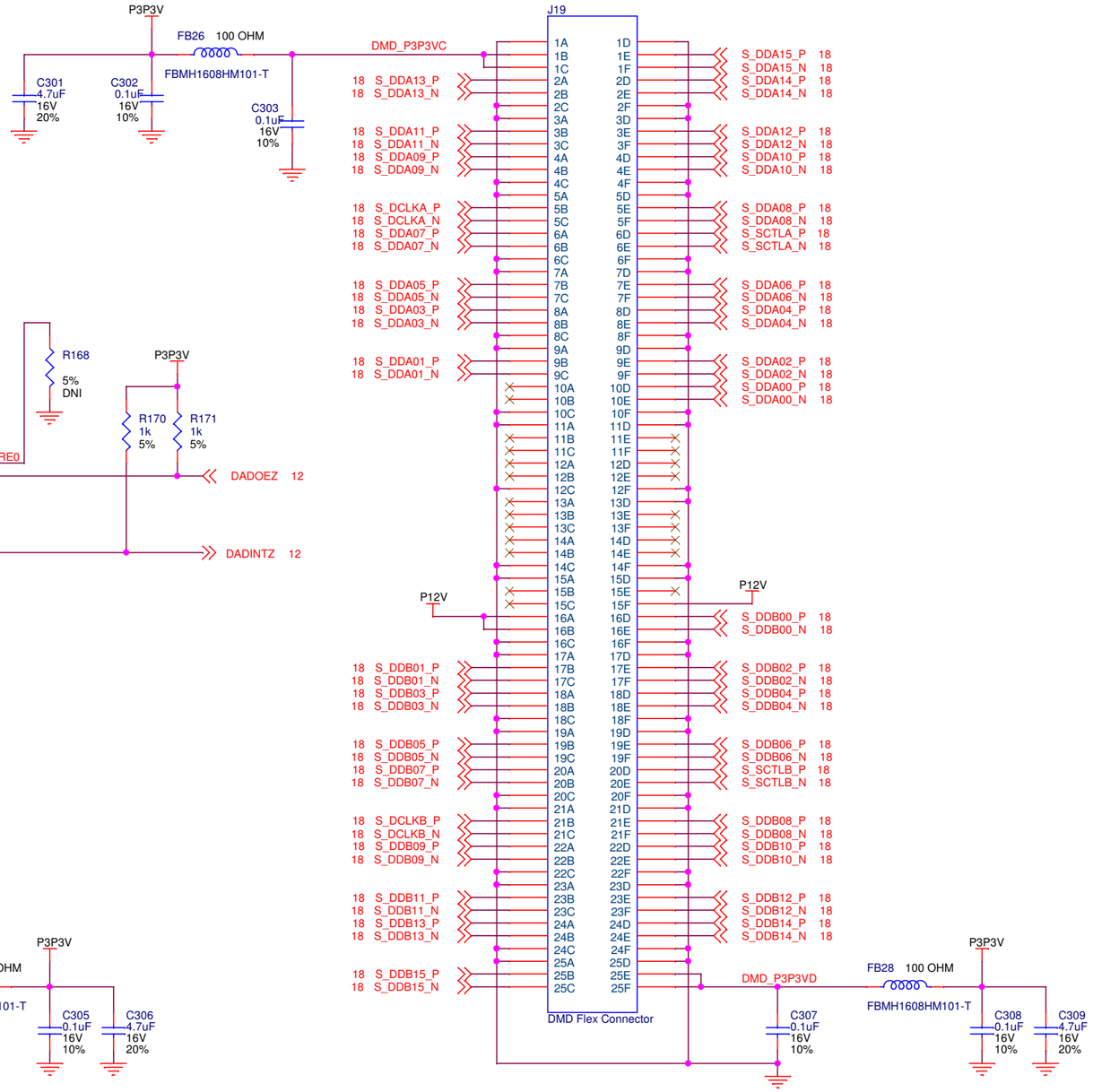
TI's EVM reference design has flex's electrical contact located on the PCB's top (component) side

Master DMD Flex



Slave DMD Flex



DMD Master/Slave Flex Connector

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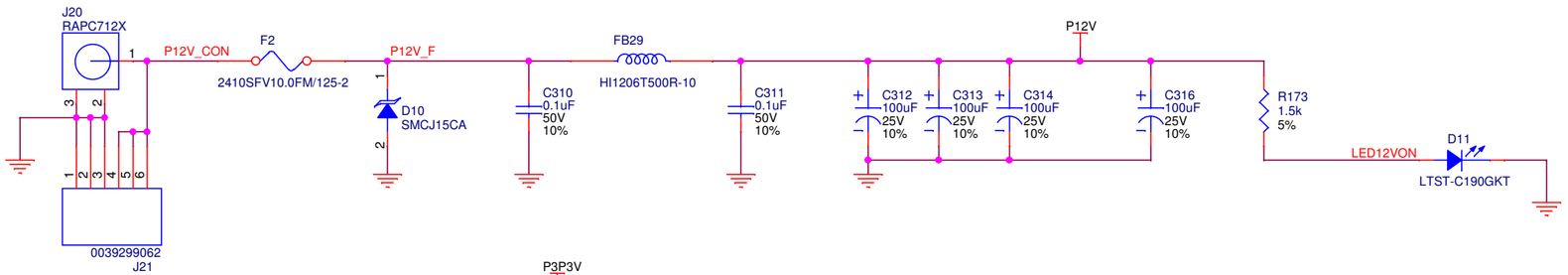
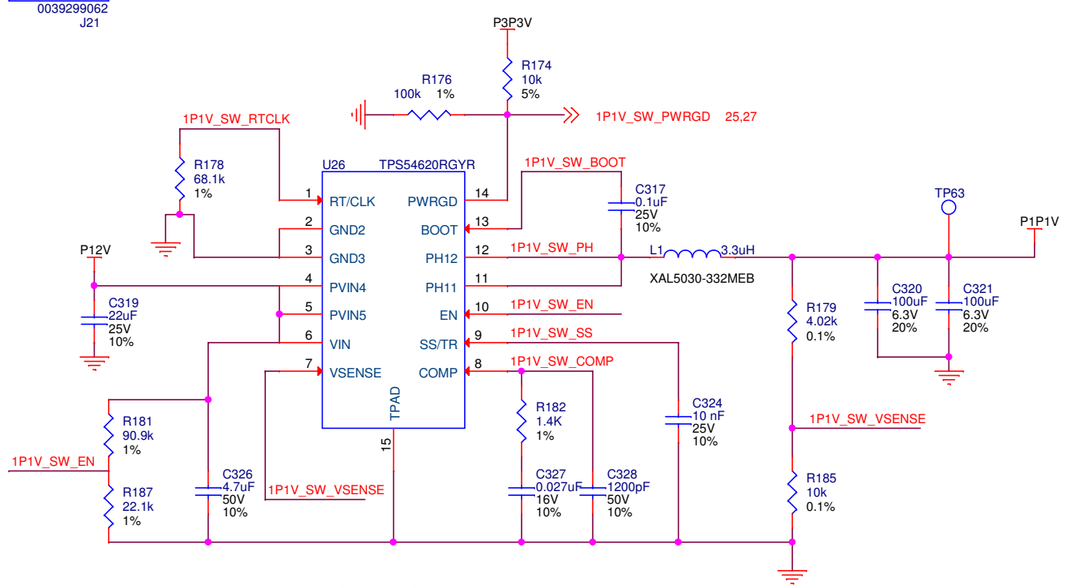
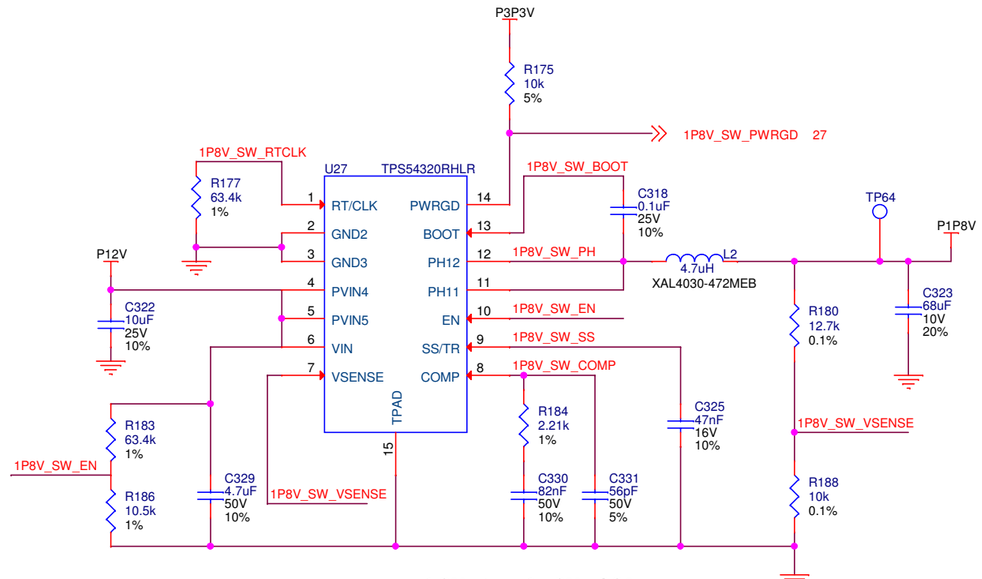
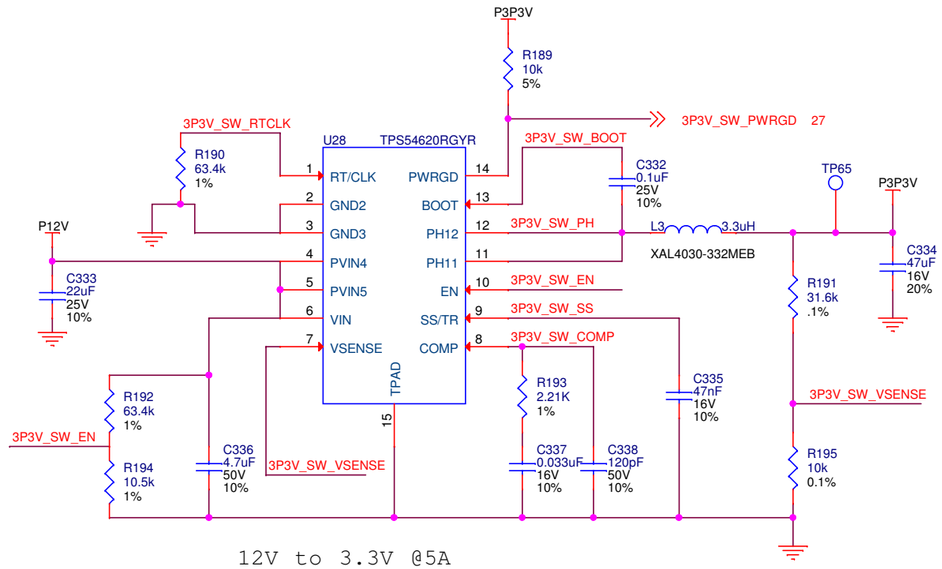




12V to 1.12V @6A
Switching Freq ~ 700KHz
Vstart/stop ~ 6.08V/5.57V
SS ~ 3.5ms



12V to 1.8V @3A
Switching Freq ~ 750KHz
Vstart/stop ~ 8.44V/7.95V
SS ~ 15ms



12V to 3.3V @5A
Switching Freq ~ 750KHz
Vstart/stop ~ 8.44V/7.95V
SS ~ 15ms

Power Generation 1.1V, 1.8V and 3.3V

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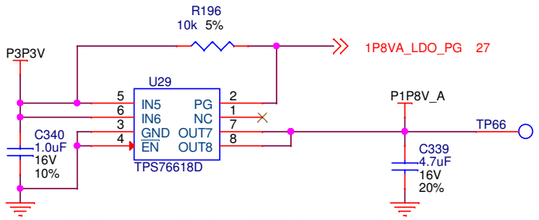
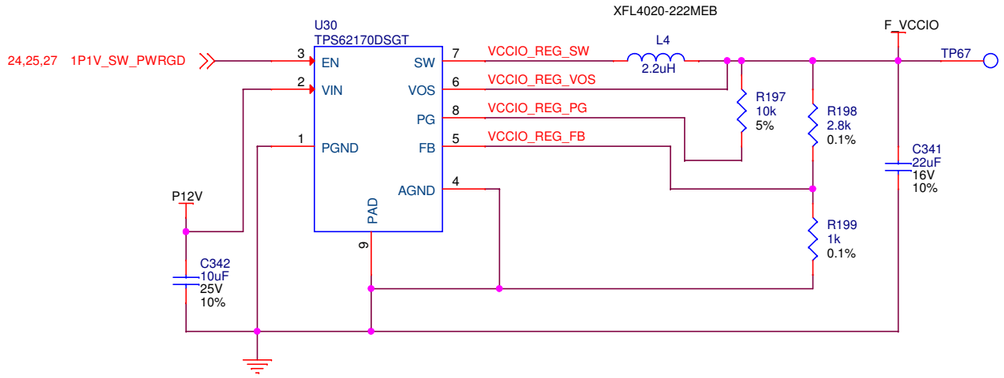
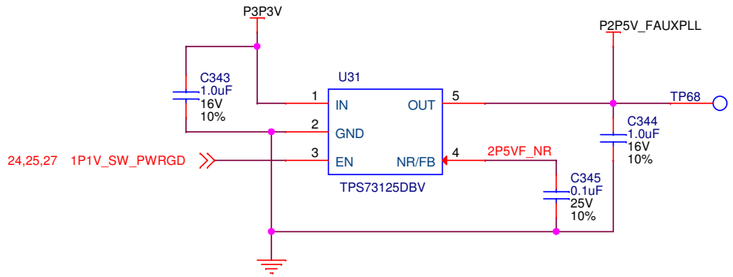


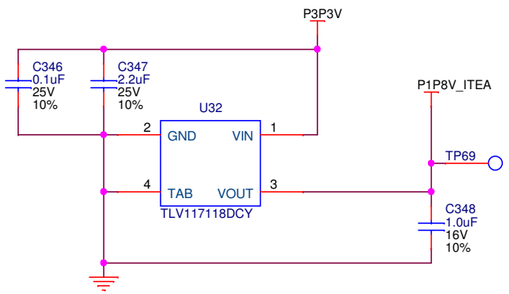
3.3V to 1.8V @250mA LDO
for controller 1.8V analog



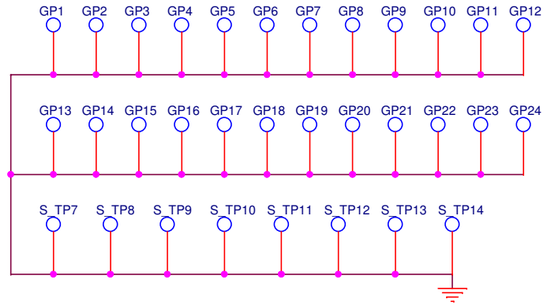
12V to 3V @500mA
for FPGA Vccio



3.3V to 2.5V @150mA LDO
for FPGA 2.5V AUX/PLL power



3.3V to 1.8V @1A LDO
for HDMI Rx 1.8V analog



Distribute ground vias around PCB

Power Generation FPGA's VCCIO, 1.8V & 2.5V LDOs

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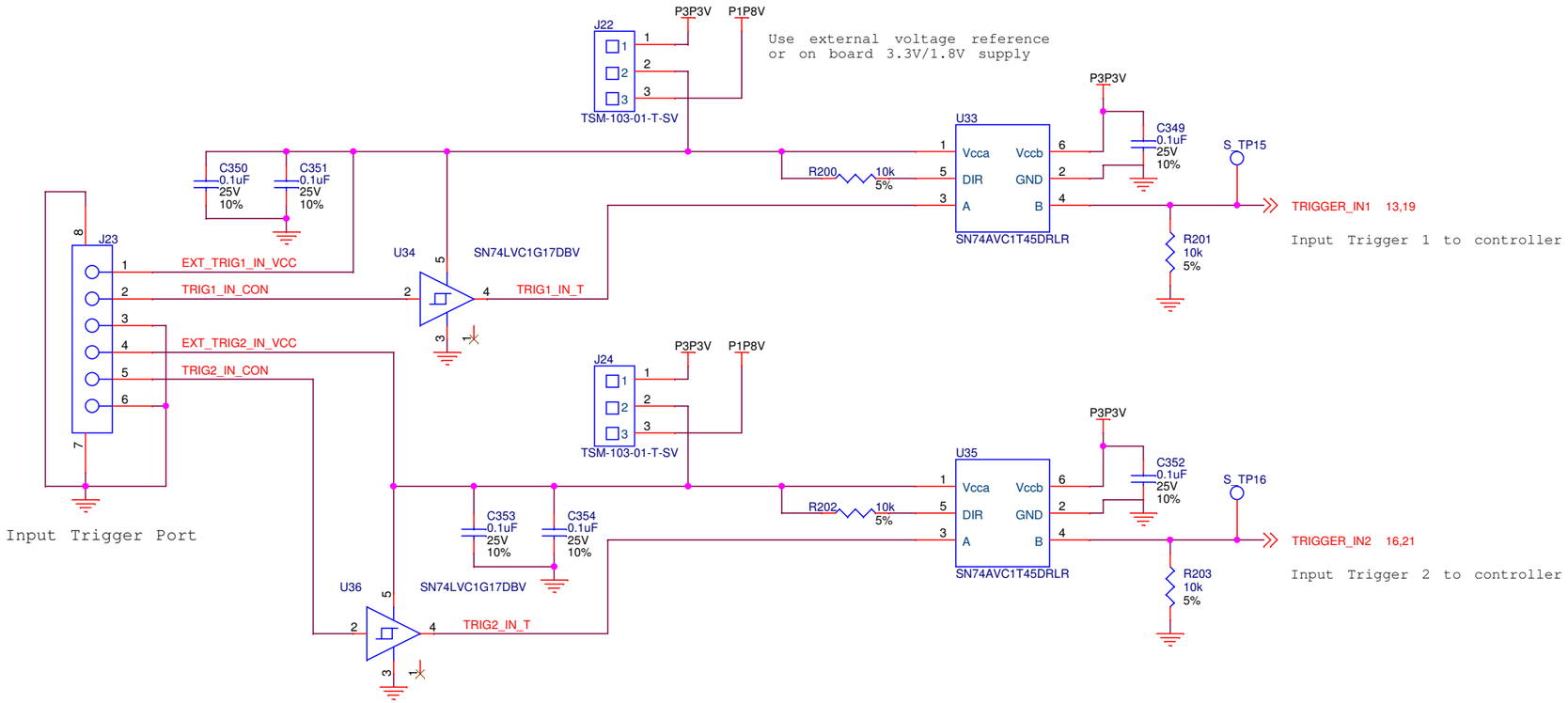

Input/Output Trigger and LED Driver Interface

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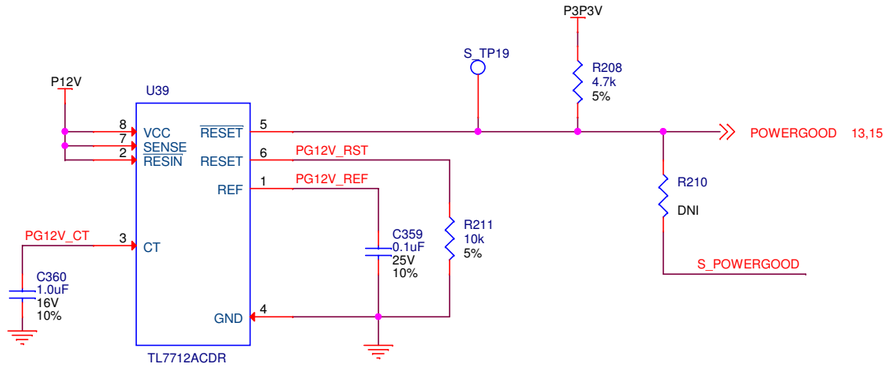
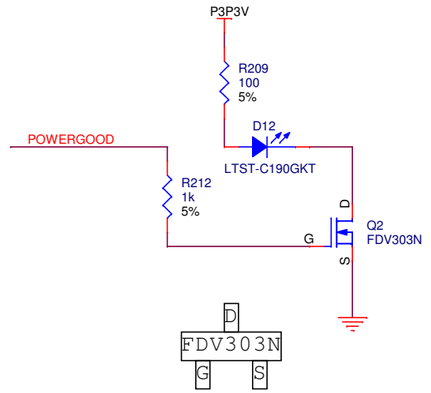
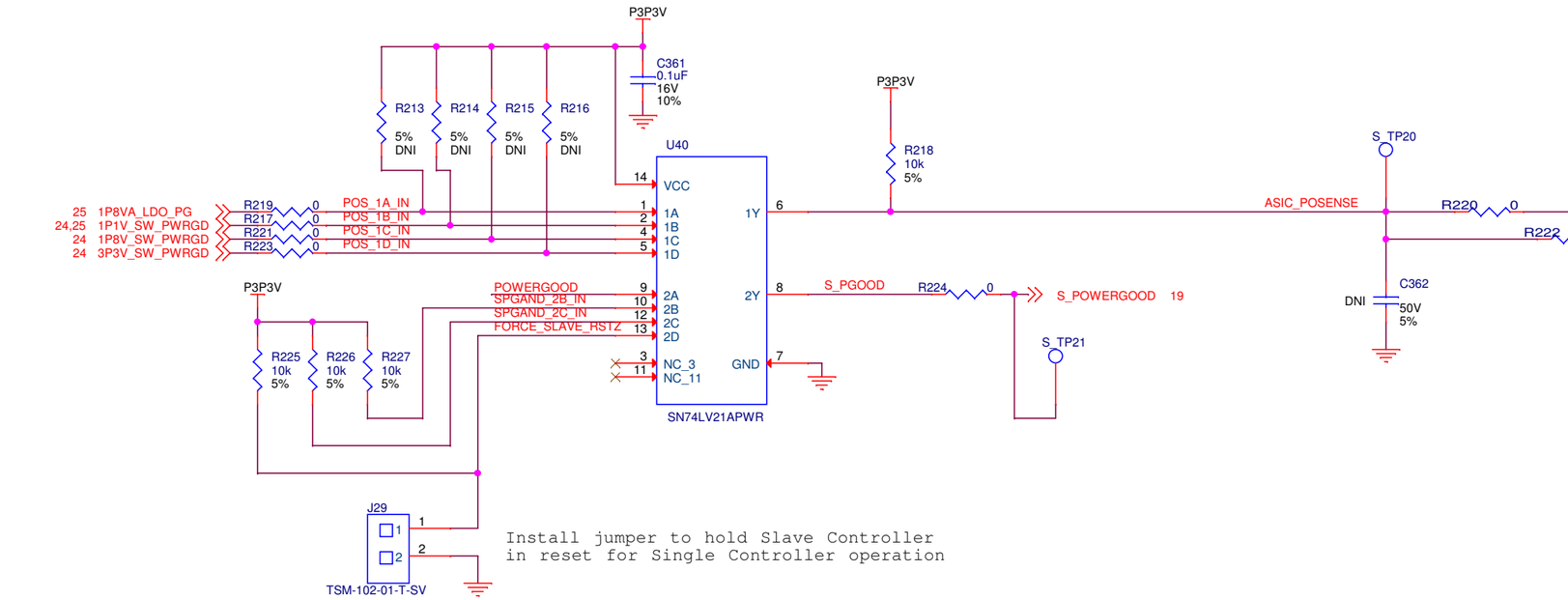
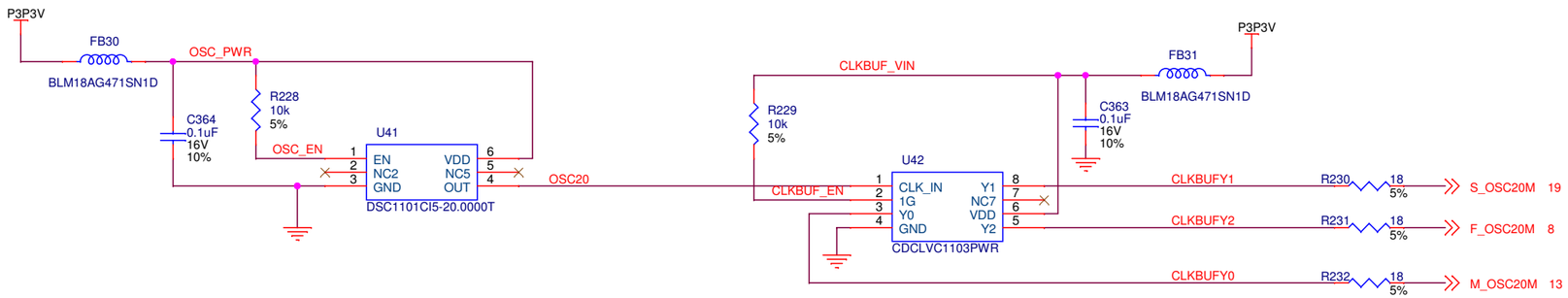
Per controller spec (Fig. 3), POWERGOOD has no impact on operation for 60ms after rising edge of POSENSE. In other words, during power up, controller will ignore the state of PG until the internal PLL is locked (require up to 60ms). Controller will then sample the PG input to begin normal operation.

During power down, POSENSE has to remain valid high for at least 500us after PG is deasserted to allow controller to complete the DMD parking procedure. The 500+ uF input caps on 12V would ensure the power monitor to trip at ~11V to deassert PG while keeping regulators operational to maintain POSENSE for > 500us.









Generate Powergood, POSENSE, Clocks

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REVISION HISTORY

Rev A

PAGES - ALL

- initial rev

Rev B

PAGE 27

- new part for C360

PAGE 26

- relocated S_TP17 and S_TP18

PAGE 24

- new part for R179
- removed C315, bulk cap not needed

PAGE 25

- new part for L4

PAGE 10

- new part for U12

Rev C

PAGES for U13 & U22

- update pin name to match datasheet

PAGE 15

- add comments for usage of R117 & R118

Rev D

Remove references to DLPC910

Rev E

Updated U7

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