NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "DMD_P3P3V" represents connection to the +3.3V digital power plane.
2. The symbol ⏚ represents connection to the digital ground plane.
3. A "Z" suffix on a signal name indicates an active low signal.
4. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
5. All resistor values are in ohms, 1/16W and 5% unless otherwise specified.

HIGHEST REFERENCE DESIGNATORS USED						
C90	D5	J3	L5	R33	TP43	U2
Q9						

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REVISIONS

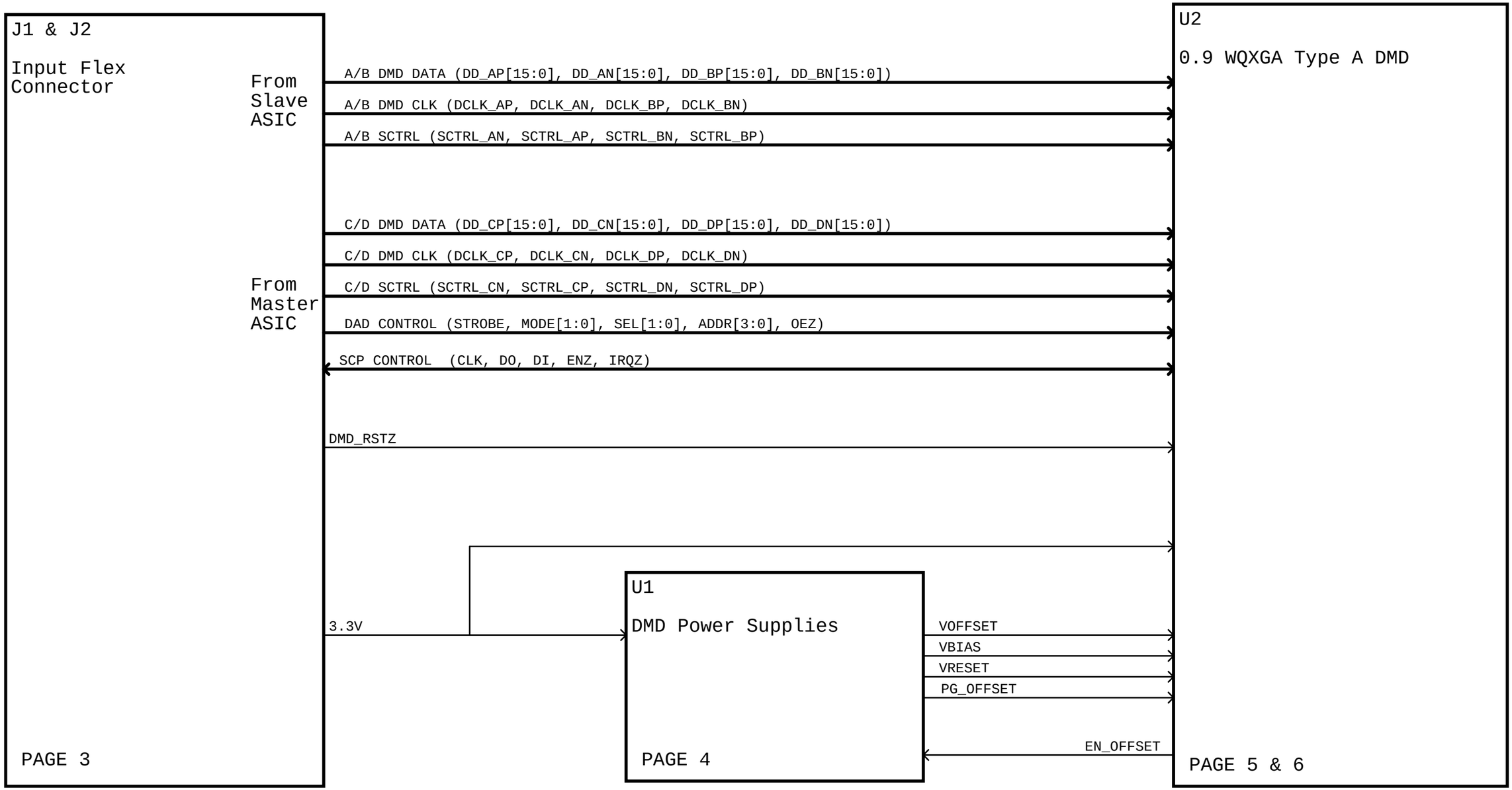
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2120805: Initial Release	01/04/2013	DH

DLP®

TEXAS INSTRUMENTS

TI Information - Selective Disclosure

		DWN A. Ng 01/02/2013	TEXAS INSTRUMENTS
		ENGR A. Ng 01/02/2013	(C) COPYRIGHT 2012 TEXAS INSTRUMENTS ALL RIGHTS RESERVED
		APVD Nathan Buettner 01/02/2013	TITLE: ESD, .9 WQXGA Type A DMD Board
		MFG	
2512147	0314SS	QA Richard Gall 01/03/2013	
NEXT ASSY	USED ON		D — DRAWING NO 2512146 — REV A
APPLICATION		SW Cadence CIS 16.3	SCALE — SHEET 1 of 6



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TEXAS INSTRUMENTS	DWN A. NG	DATE 1/15/2012	D	DRAWING NO 2512146	REV A
	ISSUE DATE			SCALE	SHEET 2 OF 6

Master LVDS

DMD_P3P3V
P3P3V1
L1 2A
220 OHM @ 100MHz
C2 0.1uF
C3 0.001uF

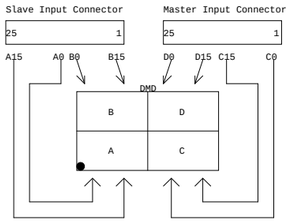
J1

DD_CN1 DD_CP1 DD_CN3 DD_CP3 DD_CN5 DD_CP5 DD_CN7 DD_CP7 SCTRL_CN SCTRL_CP DD_CN9 DD_CP9 DD_CN11 DD_CP11 DD_CN13 DD_CP13 DD_CN15 DD_CP15

DD_CN0 DD_CP0 DD_CN2 DD_CP2 DD_CN4 DD_CP4 DD_CN6 DD_CP6 DCLK_CN DCLK_CP DD_CN8 DD_CP8 DD_CN10 DD_CP10 DD_CN12 DD_CP12 DD_CN14 DD_CP14

Note: The C-Bus has been bit-order swapped (15:0 -> 0:15) from the standard connector pin-out configuration for routing purposes.

PCB Top View



Note: Do not install R3 if there is a pull-up on the SCP_DMD_CSZ signal on the Main board.

DMD_P3P3V

Note: Only install one 1K Ohm pull-up resistor on DAD_OEZ. If DAD_OEZ pull-up is installed on Main board side, do not install R1.

R1 1k
R2 10k

12V is not used on pins 10D, 10E, 11B

R3 DNI

P5 DADIRQZ
P5 DADSEL_1
P5 DADSEL_0

DAD_ADDR_3 R4 470
DAD_ADDR_2 R5 470
DAD_ADDR_0 R6 470

DADMODE_1 P5
DADMODE_0 P5
DADADDR_3 P5
DADADDR_2 P5
DADADDR_0 P5
DADSTRB P5

P5 DADADDR_1 R7 470
P5 DADOEZ R8 470
DAD_ADDR_1
DAD_OEZ

C5 2700pF 50V,10%

P5 DMD_RSTZ R9 470
DMDRSTZ

SCP_DMD_CSZ P5

P5 SCP_DI
SCP_CLK P5
SCP_DO P5

Note: R8 and C5 are specific values selected to delay ASIC driven DAD_OEZ to allow the DMD enough time to park properly. Recommend installing values as shown.

DD_DN15 DD_DP15 DD_DN13 DD_DP13 DD_DN11 DD_DP11 DD_DN9 DD_DP9 SCTRL_DN SCTRL_DP DD_DN7 DD_DP7 DD_DN5 DD_DP5 DD_DN3 DD_DP3 DD_DN1 DD_DP1 DD_DN0 DD_DP0

DD_DN14 DD_DP14 DD_DN12 DD_DP12 DD_DN10 DD_DP10 DD_DN8 DD_DP8 DCLK_DN DCLK_DP DD_DN6 DD_DP6 DD_DN4 DD_DP4 DD_DN2 DD_DP2

DMD_FLEX_CONNECTOR

J1MT1 J1MT2

P3P3V3 DMD_P3P3V TP1 TP2

L3 2A
220 OHM @ 100MHz
C6 0.001uF
C7 0.1uF

Note: 470 Ohm resistors R4 thru R9 protect the system when/if the wrong DMD is installed on-board.

Slave LVDS

DD_DP0 DD_DP1 DD_DP2 DD_DP3 DD_DP4 DD_DP5 DD_DP6 DD_DP7 DD_DP8 DD_DP9 DD_DP10 DD_DP11 DD_DP12 DD_DP13 DD_DP14 DD_DP15

DD_DP[15:0] P5

DD_DN0 DD_DN1 DD_DN2 DD_DN3 DD_DN4 DD_DN5 DD_DN6 DD_DN7 DD_DN8 DD_DN9 DD_DN10 DD_DN11 DD_DN12 DD_DN13 DD_DN14 DD_DN15

DD_DN[15:0] P5

DCLK_DP DCLK_DN
DCLK_DP P5
DCLK_DN P5

SCTRL_DP SCTRL_DN
SCTRL_DP P5
SCTRL_DN P5

DD_CP0 DD_CP1 DD_CP2 DD_CP3 DD_CP4 DD_CP5 DD_CP6 DD_CP7 DD_CP8 DD_CP9 DD_CP10 DD_CP11 DD_CP12 DD_CP13 DD_CP14 DD_CP15

DD_CP[15:0] P5

DD_CN0 DD_CN1 DD_CN2 DD_CN3 DD_CN4 DD_CN5 DD_CN6 DD_CN7 DD_CN8 DD_CN9 DD_CN10 DD_CN11 DD_CN12 DD_CN13 DD_CN14 DD_CN15

DD_CN[15:0] P5

DCLK_CP DCLK_CN
DCLK_CP P5
DCLK_CN P5

SCTRL_CP SCTRL_CN
SCTRL_CP P5
SCTRL_CN P5

DMD_P3P3V
P3P3V2
L2 2A
220 OHM @ 100MHz
C1 0.1uF
C4 0.001uF

J2

DD_BN14 DD_BP14 DD_BN12 DD_BP12 DD_BN10 DD_BP10 DD_BN8 DD_BP8 SCTRL_BN SCTRL_BP DD_BN6 DD_BP6 DD_BN4 DD_BP4 DD_BN2 DD_BP2 DD_BN0 DD_BP0

DD_BN15 DD_BP15 DD_BN13 DD_BP13 DD_BN11 DD_BP11 DD_BN9 DD_BP9 DCLK_BN DCLK_BP DD_BN7 DD_BP7 DD_BN5 DD_BP5 DD_BN3 DD_BP3 DD_BN1 DD_BP1

Pin 14B "SINGLE_ASIC_EN" is not needed WQXGA allows only dual ASIC

DD_AN0 DD_AP0 DD_AN2 DD_AP2 DD_AN4 DD_AP4 DD_AN6 DD_AP6 SCTRL_AN SCTRL_AP DD_AN8 DD_AP8 DD_AN10 DD_AP10 DD_AN12 DD_AP12 DD_AN14 DD_AP14 DD_AN15 DD_AP15

DD_AN1 DD_AP1 DD_AN3 DD_AP3 DD_AN5 DD_AP5 DD_AN7 DD_AP7 DCLK_AN DCLK_AP DD_AN9 DD_AP9 DD_AN11 DD_AP11 DD_AN13 DD_AP13

DMD_FLEX_CONNECTOR

J2MT1 J2MT2

P3P3V4 DMD_P3P3V

L4 2A
220 OHM @ 100MHz
C8 0.001uF
C9 0.1uF

DD_BP0 DD_BP1 DD_BP2 DD_BP3 DD_BP4 DD_BP5 DD_BP6 DD_BP7 DD_BP8 DD_BP9 DD_BP10 DD_BP11 DD_BP12 DD_BP13 DD_BP14 DD_BP15

DD_BP[15:0] P5

DD_BN0 DD_BN1 DD_BN2 DD_BN3 DD_BN4 DD_BN5 DD_BN6 DD_BN7 DD_BN8 DD_BN9 DD_BN10 DD_BN11 DD_BN12 DD_BN13 DD_BN14 DD_BN15

DD_BN[15:0] P5

DCLK_BP
DCLK_BP P5

DCLK_BN
DCLK_BN P5

SCTRL_BP
SCTRL_BP P5

SCTRL_BN
SCTRL_BN P5

DD_AP0 DD_AP1 DD_AP2 DD_AP3 DD_AP4 DD_AP5 DD_AP6 DD_AP7 DD_AP8 DD_AP9 DD_AP10 DD_AP11 DD_AP12 DD_AP13 DD_AP14 DD_AP15

DD_AP[15:0] P5

DD_AN0 DD_AN1 DD_AN2 DD_AN3 DD_AN4 DD_AN5 DD_AN6 DD_AN7 DD_AN8 DD_AN9 DD_AN10 DD_AN11 DD_AN12 DD_AN13 DD_AN14 DD_AN15

DD_AN[15:0] P5

DCLK_AP
DCLK_AP P5

DCLK_AN
DCLK_AN P5

SCTRL_AP
SCTRL_AP P5

SCTRL_AN
SCTRL_AN P5

INPUT CONNECTOR

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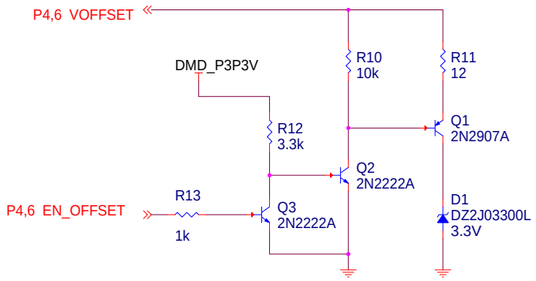
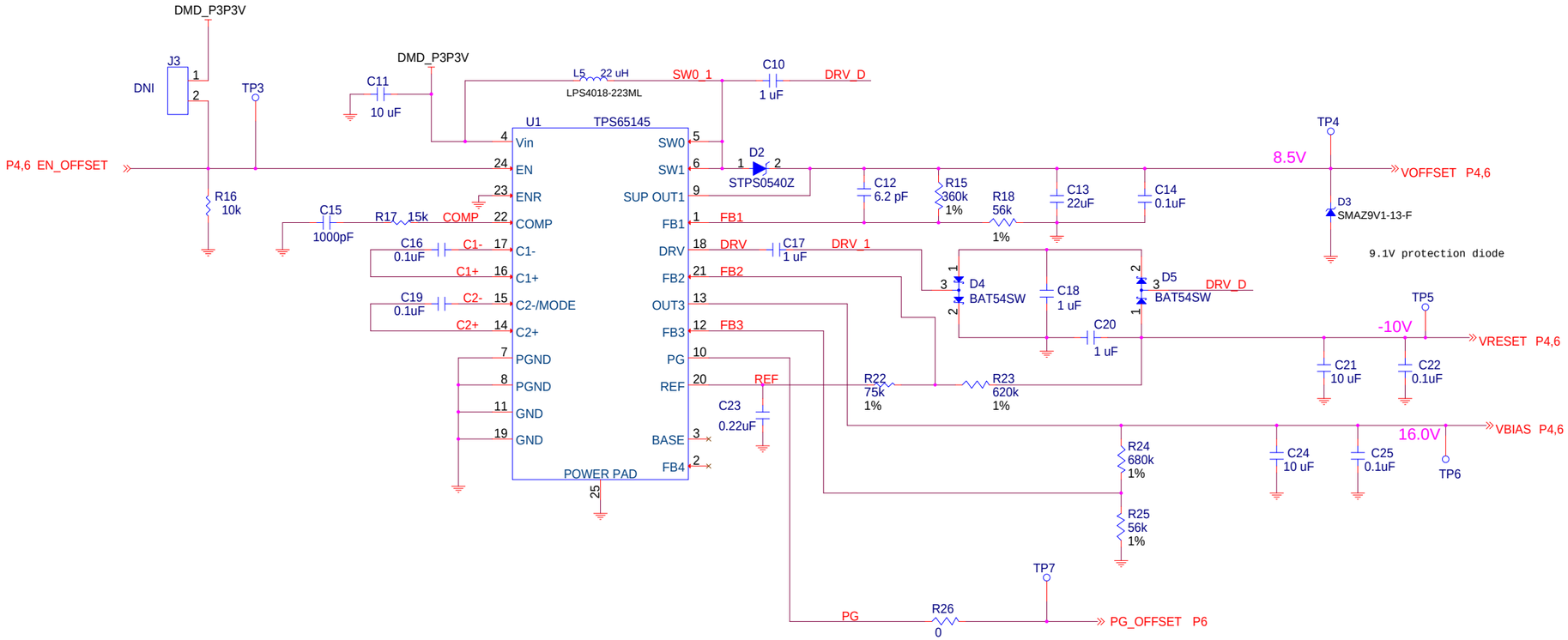
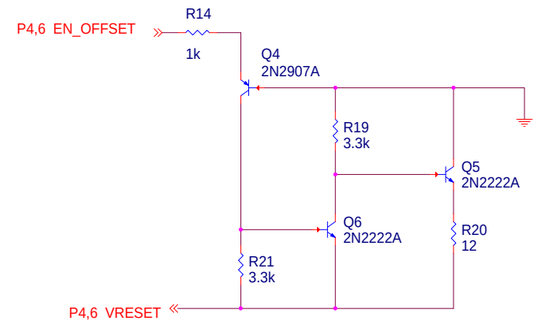
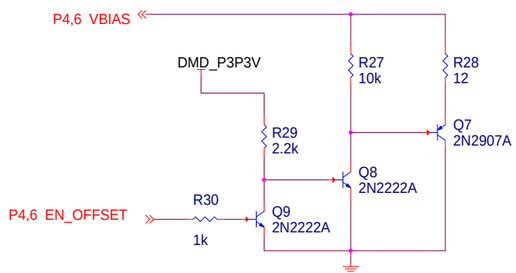
TEXAS INSTRUMENTS	DWN A. NG	DATE 1/15/2012	D
	ISSUE DATE		DRAWING NO 2512146
	SCALE		REV A
			SHEET 3 OF 6

Power Down Circuitry









DMD Power Supplies

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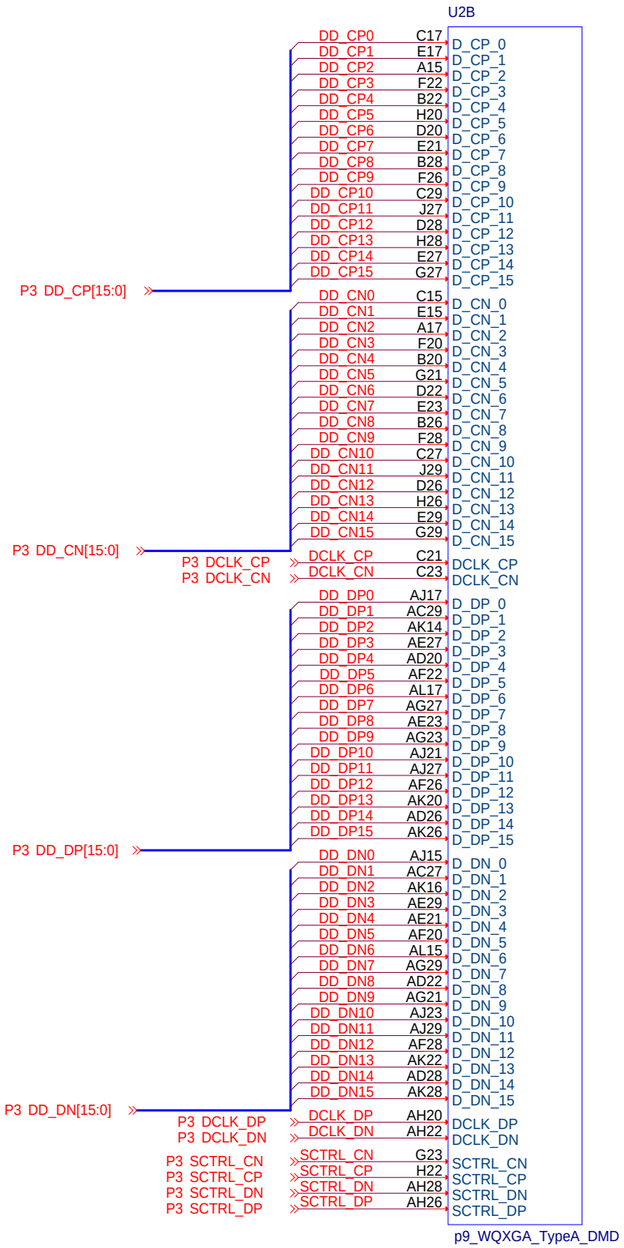
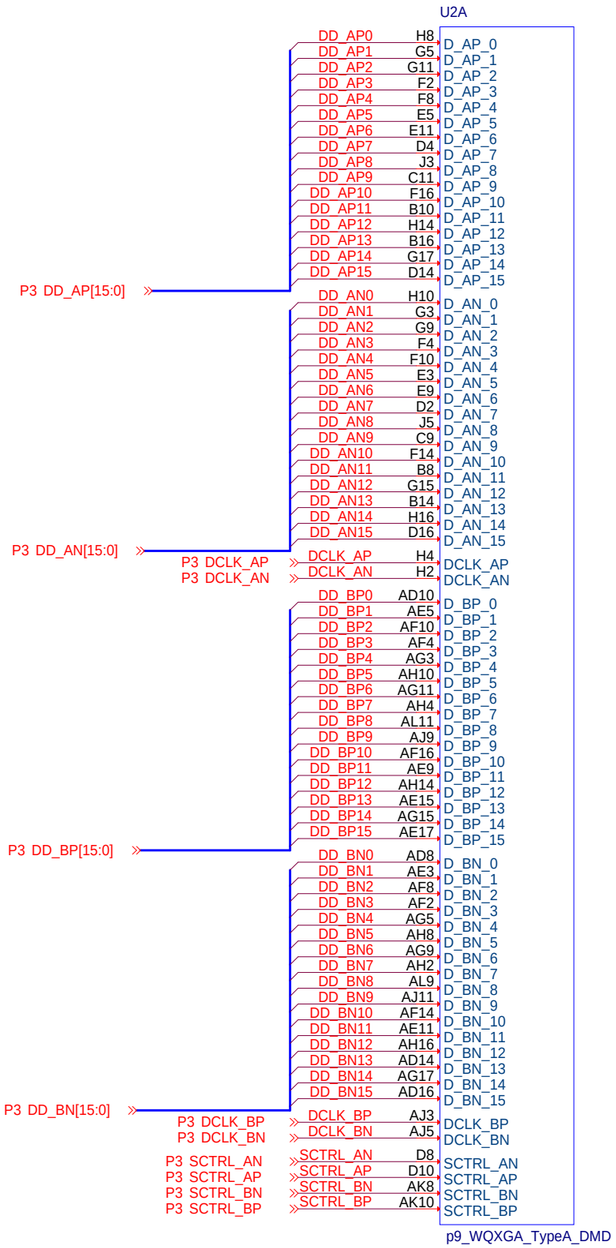
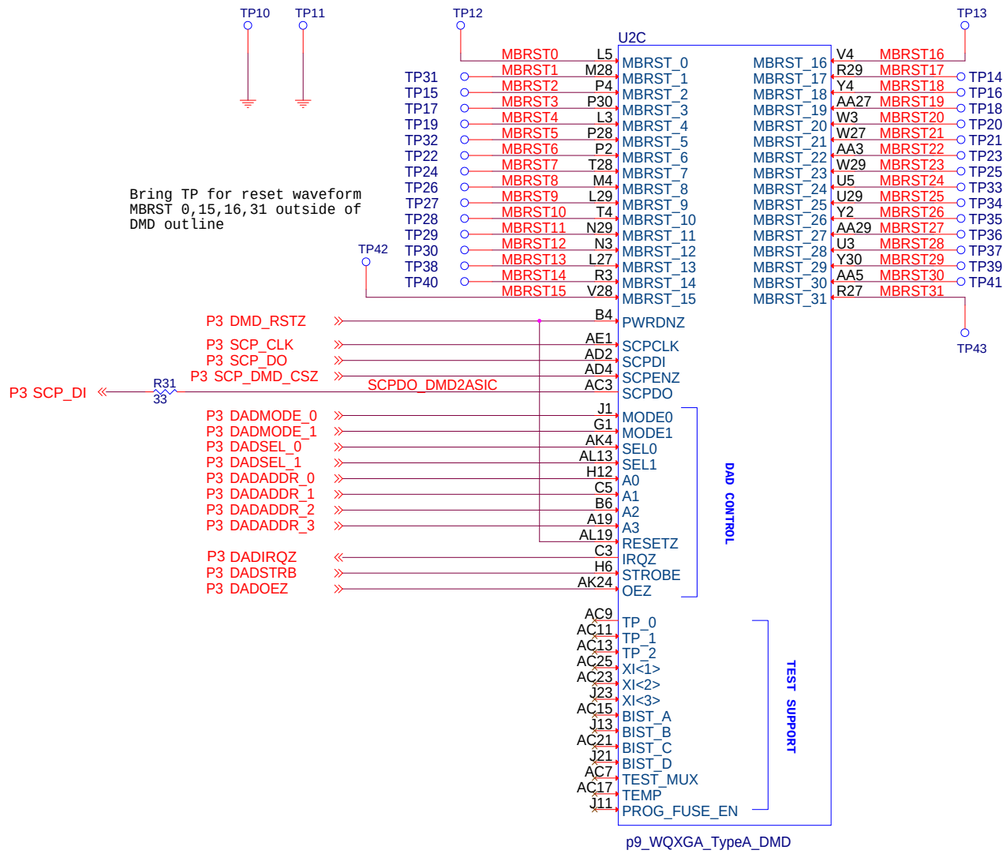
	ISSUE DATE			SCALE	SHEET 4 OF 6







DMD Data/Control

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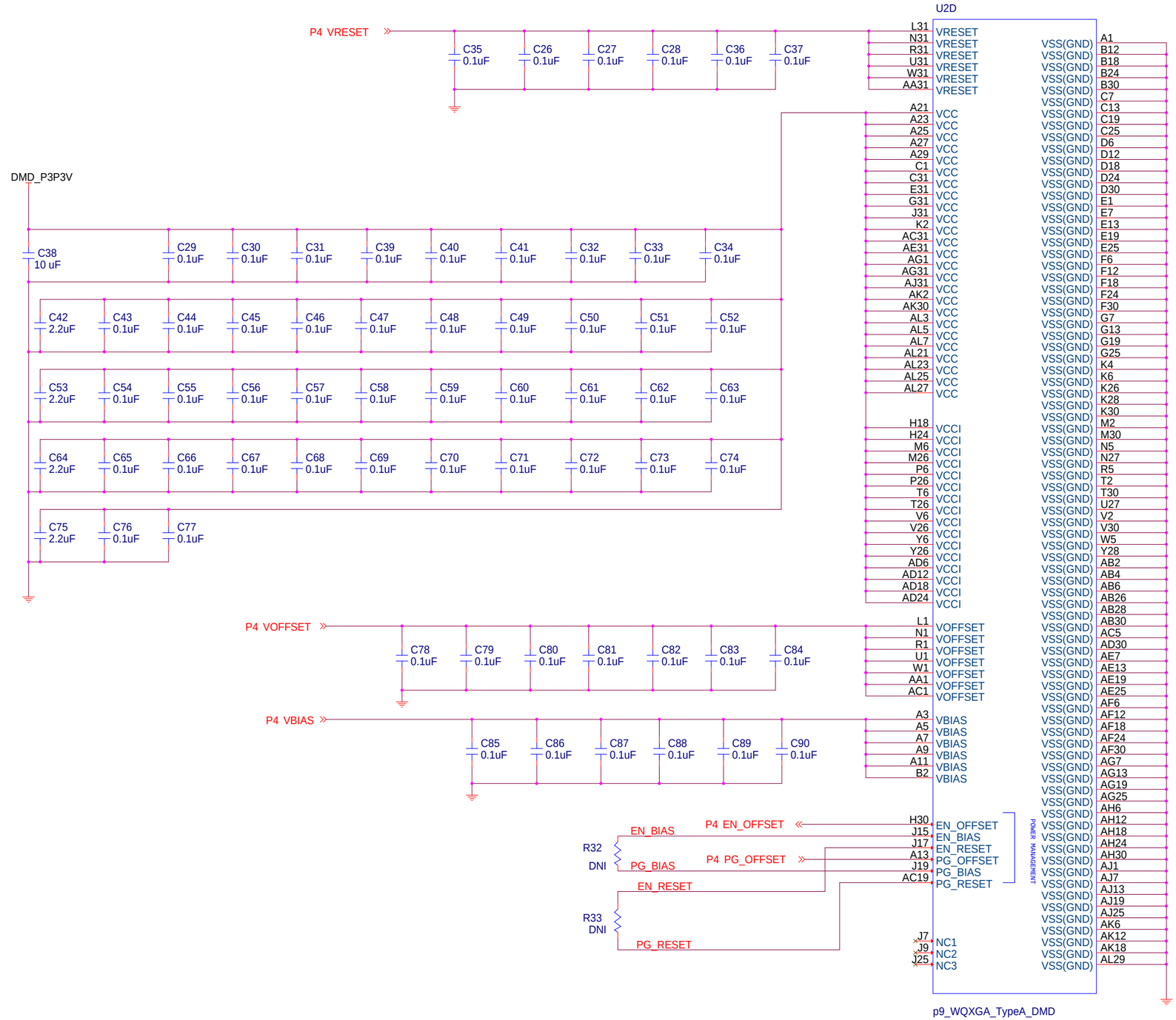
	ISSUE DATE		SCALE	SHEET 5 OF 6	



DMD Power/Gnd

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