

**NOTES, UNLESS OTHERWISE SPECIFIED:**

1. The netname "P3P3V" represents connection to the +3.3V digital power plane.
2. The netname "P1P8V" represents connection to the +1.8V digital power plane.
3. The netname "P1P1V" represents connection to the +1.1V digital power plane.
4. The symbol  $\oplus$  represents connection to the digital ground plane.
5. A "Z" suffix on a signal name indicates an active low signal.
6. A "\_S" suffix on a signal name indicates a trace that is between a driver and a series termination resistor.
7. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
8. The letters DNI near a part mean "do not install".

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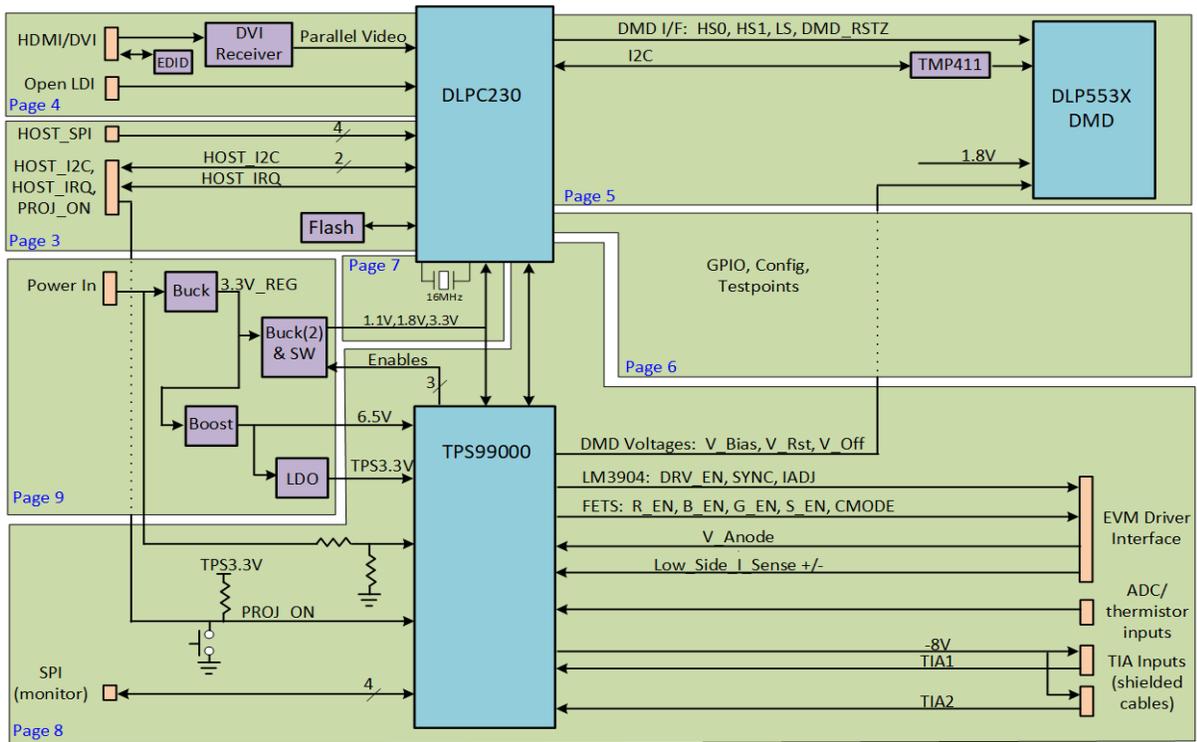
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	Initial Release		
B	Corrected 1.1V and 1.8V enables to regulator		

Z PCB1

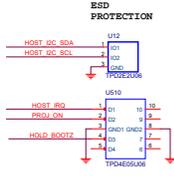
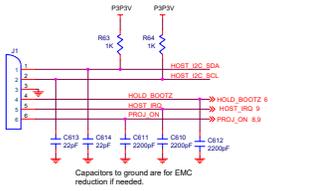
PCB: DLP553X Controller  
DLP033B



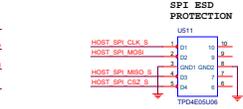
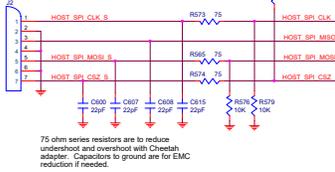
OWN	George Pawlowski	DATE	4/12/2019	<b>TEXAS INSTRUMENTS</b> © COPYRIGHT 2017 TEXAS INSTRUMENTS ALL RIGHTS RESERVED	
ENGR					
ENVT				TITLE	
PRV				DLP553x EVM Controller	
NEXT ASSY	USED ON	D	DRAWING NO	DLP033	REV
					B
APPLICATION	REV	Cadence Capture 16.6	SCALE		SHEET 1 of 9



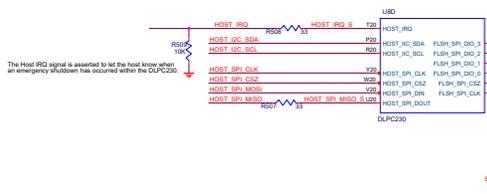
**HOST I2C, PROJ\_ON, IRQ, HOLD\_BOOT CONNECTOR**



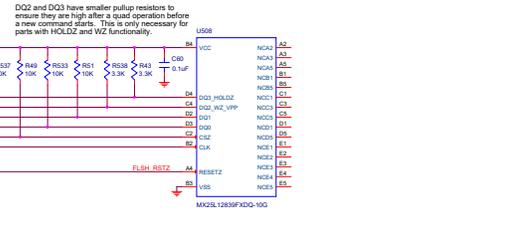
**HOST SPI CONNECTOR**



**DLP230 HOST INTERFACE**

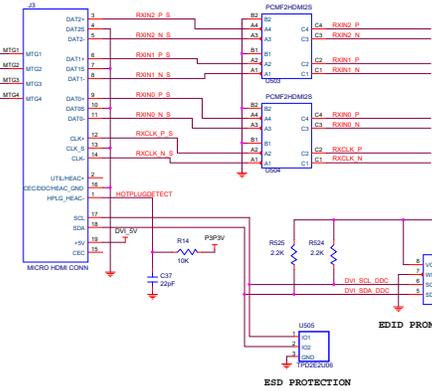


**DLP230 CONFIGURATION FLASH**



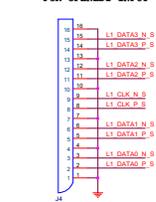
HDMI CONNECTOR FOR HDMI INPUT

HDMI EMI FILTERING AND ESD PROTECTION

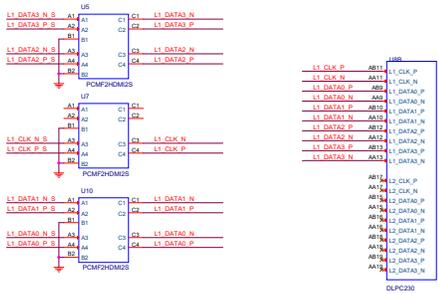


DLP7230 OPEN LDI VIDEO INTERFACE

FLEX CONNECTOR FOR OPENLDI INPUT

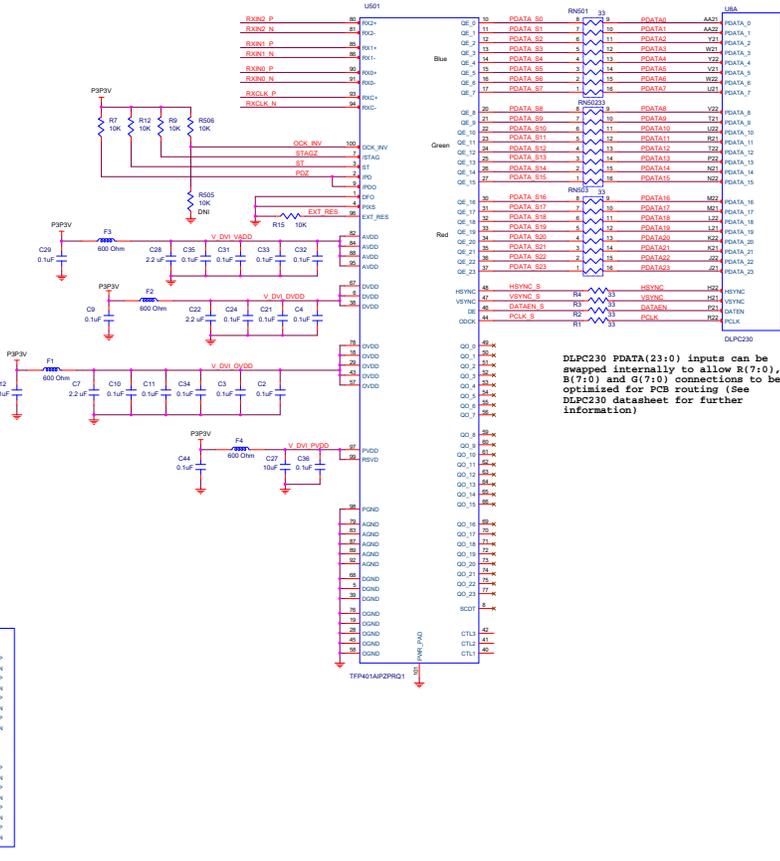


EMI FILTERING AND ESD PROTECTION

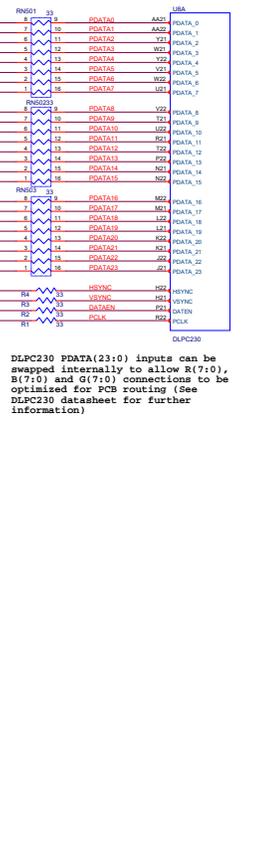


DVI VIDEO CIRCUIT

DVI RECEIVER



DLP7230 PARALLEL VIDEO INTERFACE

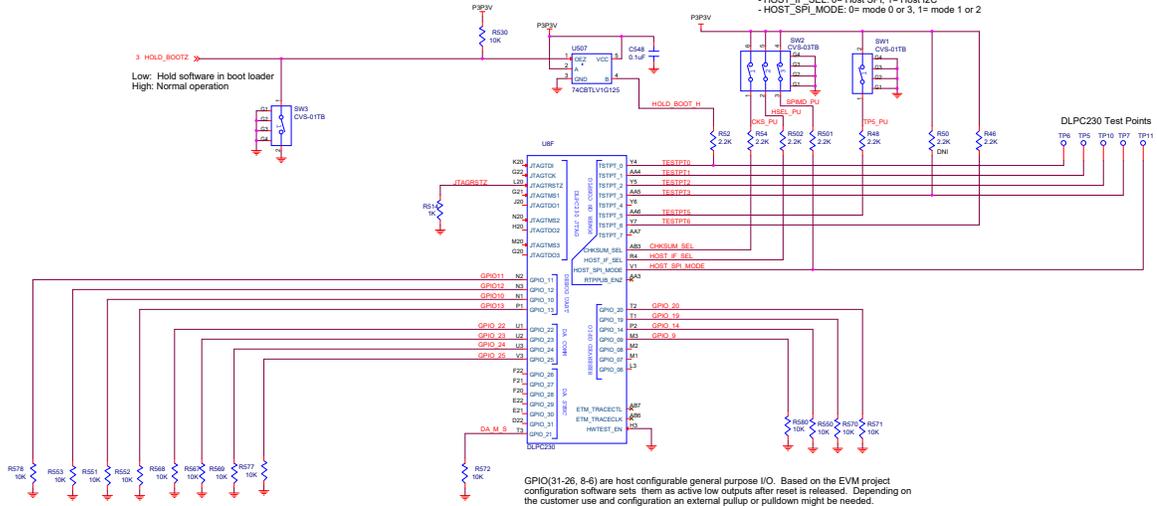




- TS1PT(7:0), CHKSUM\_SEL, HOST\_IF\_SEL, HOST\_SPI\_SEL are inputs when RESETZ is low and have internal weak pull-down resistors. The states of the inputs are sampled after reset transitions from low to high to determine configuration options. Pins are then set as outputs.

**CONFIGURATION OPTIONS**

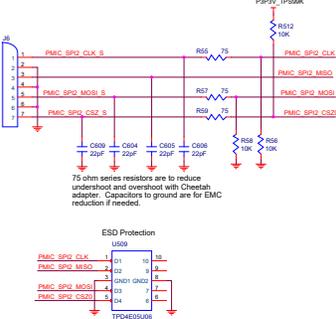
- TS1PT0 (STAY-IN-BOOT): 0= load main app, 1= stay in boot app
- TS1PT1 (EXT-BOOT-EN): 0= internal boot (must be low)
- TS1PT2 (I2C-ADDR-SEL): 0=0x36 (must be low)
- TS1PT3 (ALT-MADR-SEL): 0= load main app 1, 1= load main app 2
- TS1PT4 (BOOT-SPI-MASTER-EN): 0= disabled (must be low)
- TS1PT5 (Spread Spectrum Enable): 0= disabled, 1= enabled
- TS1PT6 (Crystal Frequency): 0= reserved, 1= 16MHz (must be high)
- CHKSUM\_SEL: 0= 8 bit CRC, 1= 8 bit checksum
- HOST\_IF\_SEL: 0= Host SPI, 1= Host I2C
- HOST\_SPI\_MODE: 0= mode 0 or 3, 1= mode 1 or 2



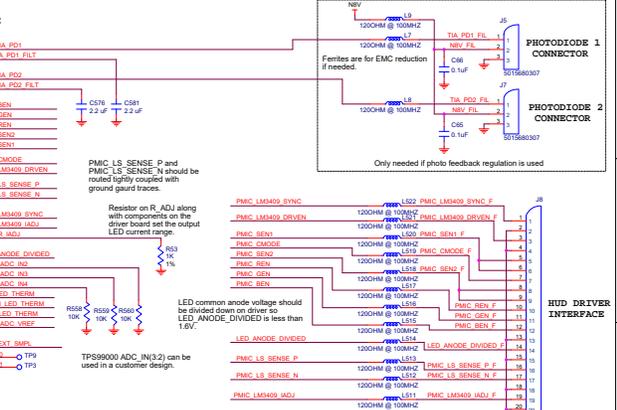
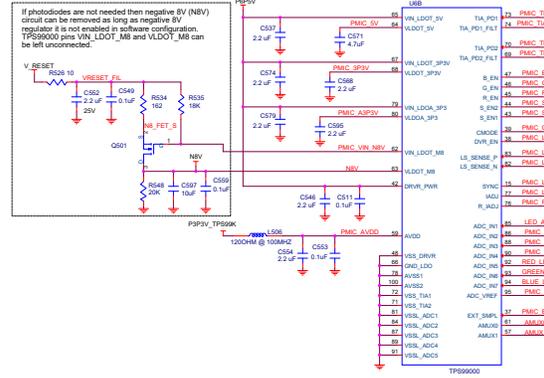
GPIO(31:26, 8-6) are host configurable general purpose I/O. Based on the EVM project configuration software sets them as active low outputs after reset is released. Depending on the customer use and configuration an external pullup or pull-down might be needed.



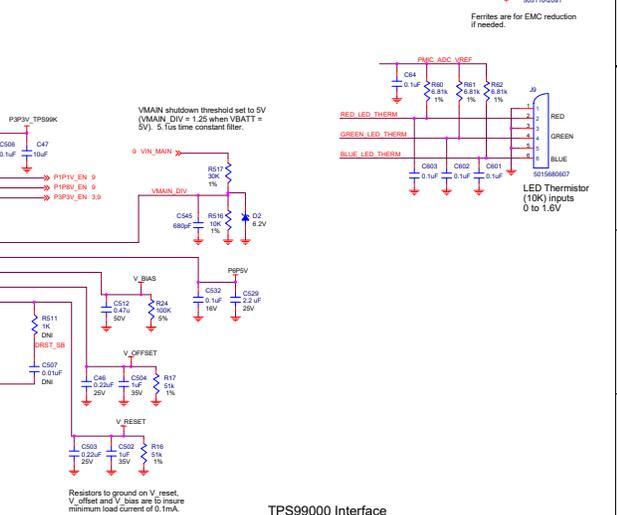
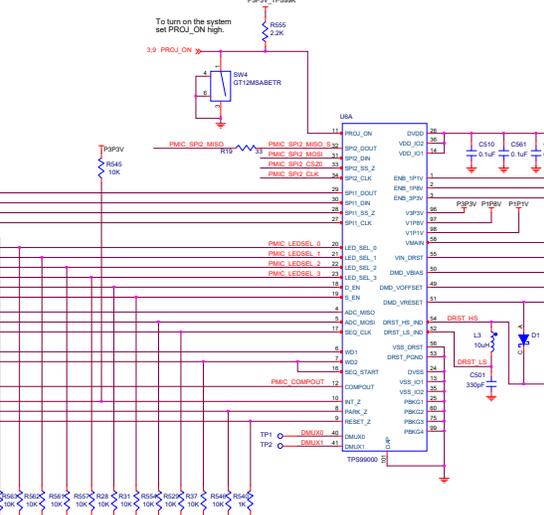
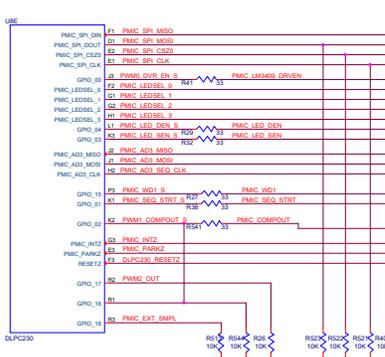
**TPS99000 SPI DEBUG CONNECTOR**



**TPS99000 ANALOG INTERFACE**

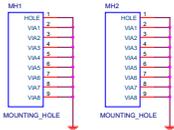
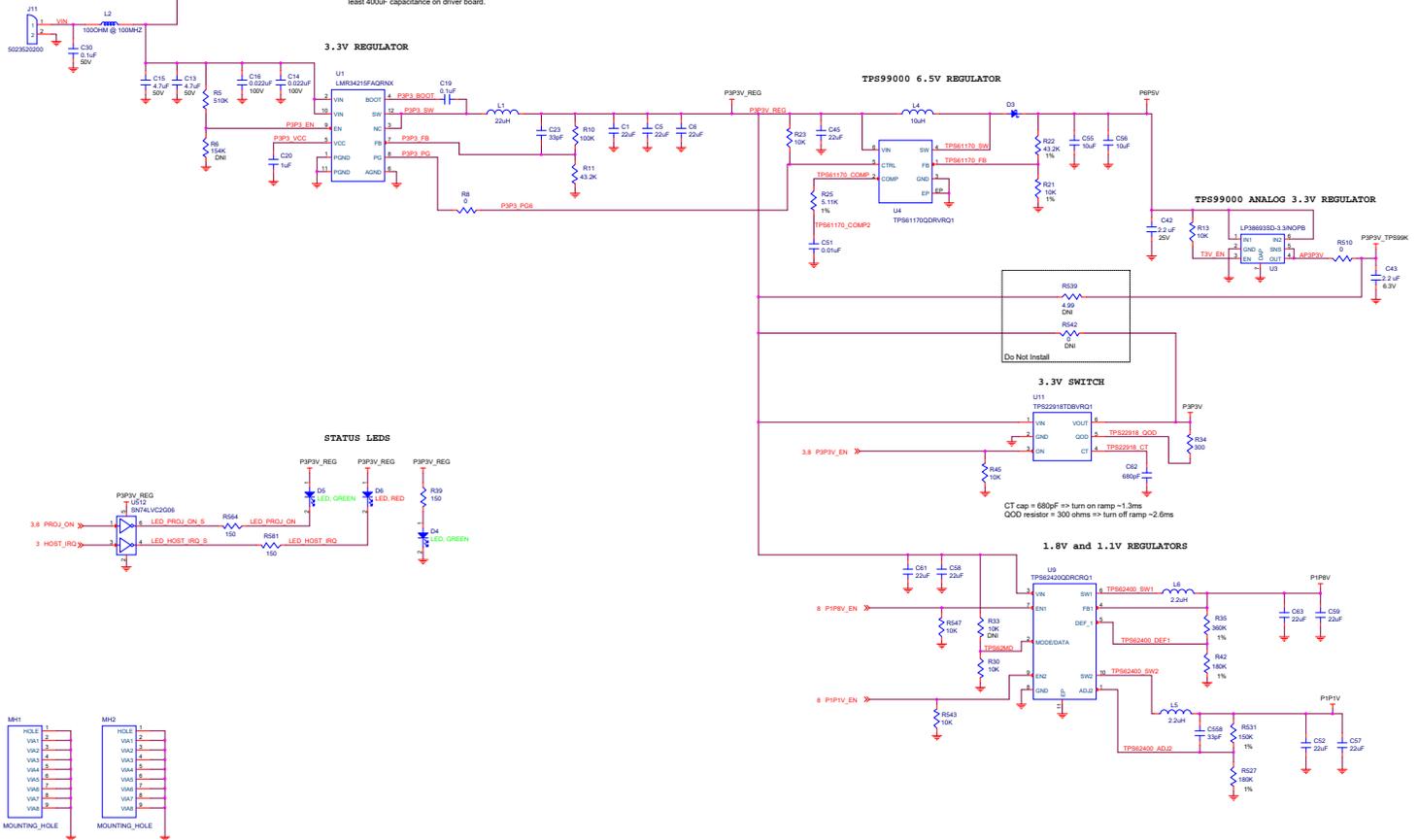


**TPS99000 DLPC230 INTERFACE**



INPUT VOLTAGE FROM DRIVER

VIN\_MAIN to TPS99000 to detect voltage dropping to park DMD. Assumes there is at least 400uF capacitance on driver board.



SYSTEM POWER