

TUSB501 HSPICE model

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TUSB501_HSPICE.zip

hspice model set

- **Testbench**

sim_tusb501.hsp

- **Encrypted netlist encrypted netlist**

TOP_TUSB501_PKG_HSP.hsp.en

- **Process corners models Encrypted netlist**

model_slow.encrypted

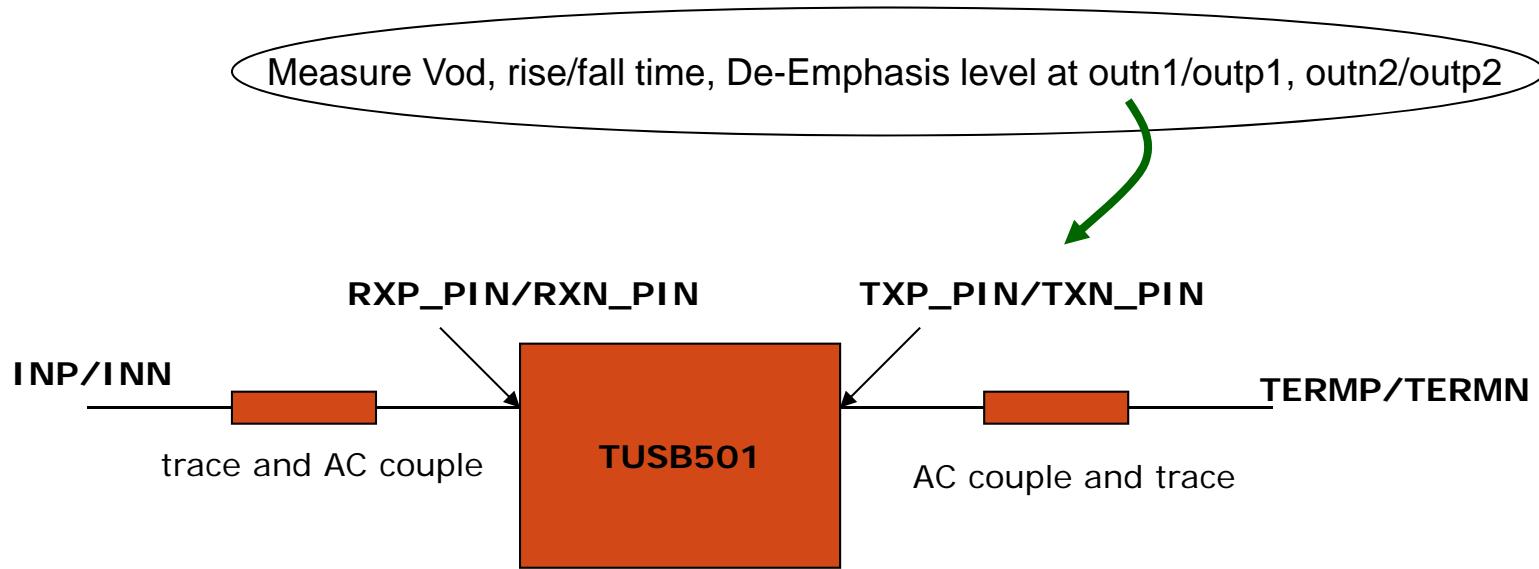
model_nominal.encrypted

model_fast.encrypted

- **FR4 Trace model**

FR4_1c_4mil.rlgc

HSPICE TESTBENCH



HSPICE testbench

HSPICE model simulation example

```
*** process
.inc ./model_nominal.encrypted
*.inc model_slow.encrypted
*.inc model_fast.encrypted
.param sh_bjt=1

*** power supply
*** nom=3.3
.param pvcc=3.3
*.param pvcc=3.0
*.param pvcc=3.6

*** temperature
.temp 25
*.temp 125
*.temp -40

*** de-emphasis setting
*** 0..5/0/1
*** DE=0/-3.5/-6dB (OS=0.5)
.param de=0.5
*.param de=1
*.param de=0

*** equalizer setting
*** 0/0.5/1
*** EQ=3/6/9dB
.param eq=0.5
*.param eq=0
*.param eq=1

*** swing setting
*** 0/1
*** 930/1300mV
.param os=0
*.param os=1

*** testbench parameter
*** trace length in inch(input trance and output trace FR4)
.param ltrc_in=40
.param ltrc_out=10
```

Process set to nominal

Power set to 3.3v

Temp set to 25C

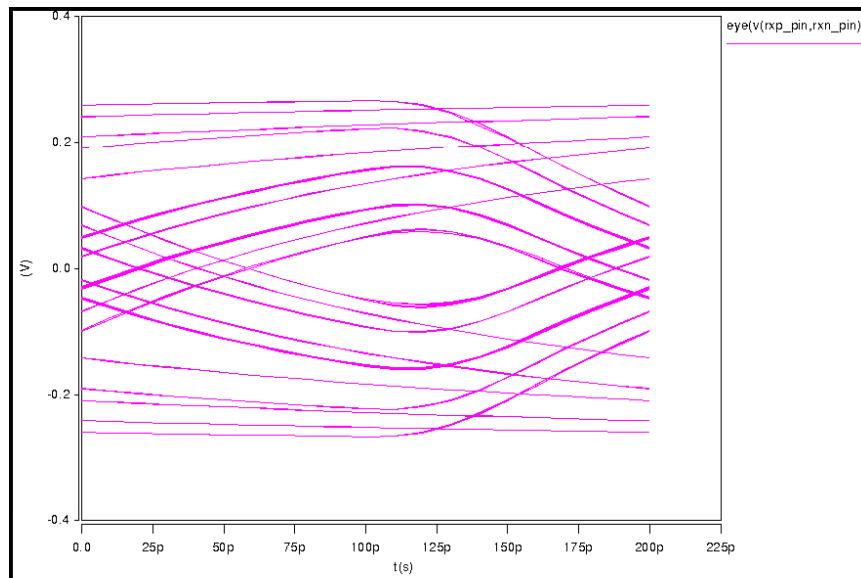
DE set to -3.5dB

EQ set to 6dB

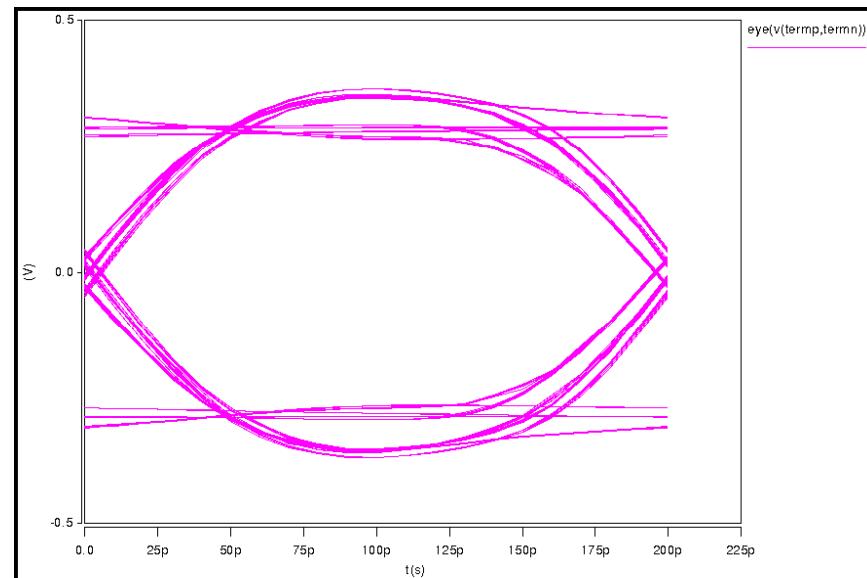
OS set to 930mV

Input/output trace set to 40/10inch

Sample simulation result
vcc=3.3V, temp=25C, process=nom
with 40" input FR4 trace and 10" output trace



Input eye



Output eye