Texas Instruments

Application Note
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DS110DF1610 IBIS-AMI Models

User's Guide

Version 00.03.00
March 2024

Disclaimer

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1 Introduction

This document describes the organization, structure, and proper usage of the TI DS110DF1610 IBIS-AMI models (compiled and approved for external customer release), hereafter referred to as the "model" for short. The model is intended for use by the DS110DF1610 design team and by DS110DF1610 customers for system-level modeling and verification. This document assumes that you are familiar with the relevant IBIS-AMI modeling specifications.

1.1 Formatting Conventions

The help readability, various formatting conventions are used throughout this document:

- Hyperlinks to material within and outside this document are marked in blue.
- Courier font is used for file names, code, variables, structures, parameters, and terminal commands.

1.2 Charter of the SerDes IBIS-AMI models

The models are designed in accordance with the IBIS-AMI standard and attempts to model the significant characteristics of most components in the DS110DF1610. The models are not intended to be an exact representation of DS110DF1610 components implemented. Rather, the models seek to provide as high a degree of accuracy as is feasible outside of Spice-based models and simulations.

1.3 Is / Is Not Table

The following table describes the features and purposes of the models, as well as the limitations of the models.

Table 1: Model Is / Is Not Table

Is	Is Not
Compiled for 32-bit AMI EDA tool that run in Windows platform Compiled for 64-bit AMI EDA tool that run in Linux platform	Compiled for any other platform (i.e. 32-Linux or 64 Windows)
Compliant to IBIS-AMI 5.0	Compliant to a more recent BIRD revisions, if they exist
Model of DS110DF1610 functionality, nonidealities, and performance	Exact representation of implemented components

2 About This Release

2.1 IBIS-AMI Model Files

Table 2 shows the key IBIS-AMI model files delivered with the model release as part of the compressed archive.

Table 2: IBIS-AMI files included with the model release

File Name	Type	Description
DS110DF1610_AMI_users_guide.pdf	PDF	TI DS110DF1610 AMI model user's guide.
ds110df1610.ibs	IBIS	Top-level IBIS wrapper for the Tx and Rx AMI model.
ds110df1610_tx.ami	AMI	Parameters file for the Tx model as required by the IBIS-AMI standard. This is a text file which is common for all OS/execution platforms.
ds110df1610_tx.dll ds110df1610_tx_x64.so	DLL	Windows 32-bit and Linux 64-bit compiled shared library for the Tx model. This shared library includes the AMI_Init, AMI_GetWave, and AMI_Close functions defined in the IBIS-AMI standard.
ds110df1610_rx.ami	AMI	Parameters file for the Rx model as required by the IBIS-AMI standard. This is a text file which is common for all OS/execution platforms.
ds110df1610_rx.dll ds110df1610_rx_x64.so	DLL	Windows 32-bit and Linux 64-bit compiled shared library for the Rx model. This shared library includes the AMI_Init, AMI_GetWave, and AMI_Close functions defined in the IBIS-AMI standard.
Demo projects for ADS		

2.2 Retimer AMI model specific parameters

DS110DF1610 is a retimer that consists of receiver and transmitter. The ibs file has included the pre AMI standard adopted repeater_pin syntax. EDA tool that supports the repeater_pin syntax are capable to fully simulate the function of this retimer AMI model. EDA tool that do not support repeater_pin syntax can simulate this retimer AMI model as a transmitter and a receiver respectively.

The following settings correspond to the following values for this model.

Table 3. Model Specific Parameters for Transmitter

c0_sgn cp_sgn cn_sgn	Main cursor sign, 0 is positive 1 is negative Post cursor sign, 0 is positive 1 is negative Pre cursor sign, 0 is positive 1 is negative
c0 cp cn	Main cursor tap, range from 0 to 63 Post cursor tap, range from 0 to 63 Pre cursor tap, range from 0 to 63 The sum of the tap values should be 63
sel_i_max = 1 sel_rload_max = 0 sel_neg_gm = 1	Default setting for maximum bandwidth. At these settings output of Tx-FIR is 800mV pk-pk diff. Other settings are not captured in this AMI model
Sel_edge	Edge –rate setting, 0 is slowest and 7 is fastest.
Tx_bypass	Setting 1 to bypass the transmitter equalization, default is 0
vod	(see table below)

sel_vod	VOD(V)
0	0.045
1	0.083
2	0.121
3	0.159
4	0.198
5	0.236
6	0.274
7	0.312
8	0.350
9	0.388
10	0.426
11	0.470
12	0.516
13	0.563
14	0.609
15	0.655
16	0.701
17	0.748
18	0.794
19	0.840
20	0.887
21	0.931
22	0.971
23	1.011
24	1.050
25	1.090
26	1.130
27	1.170
28	1.210
29	1.250
30	1.290

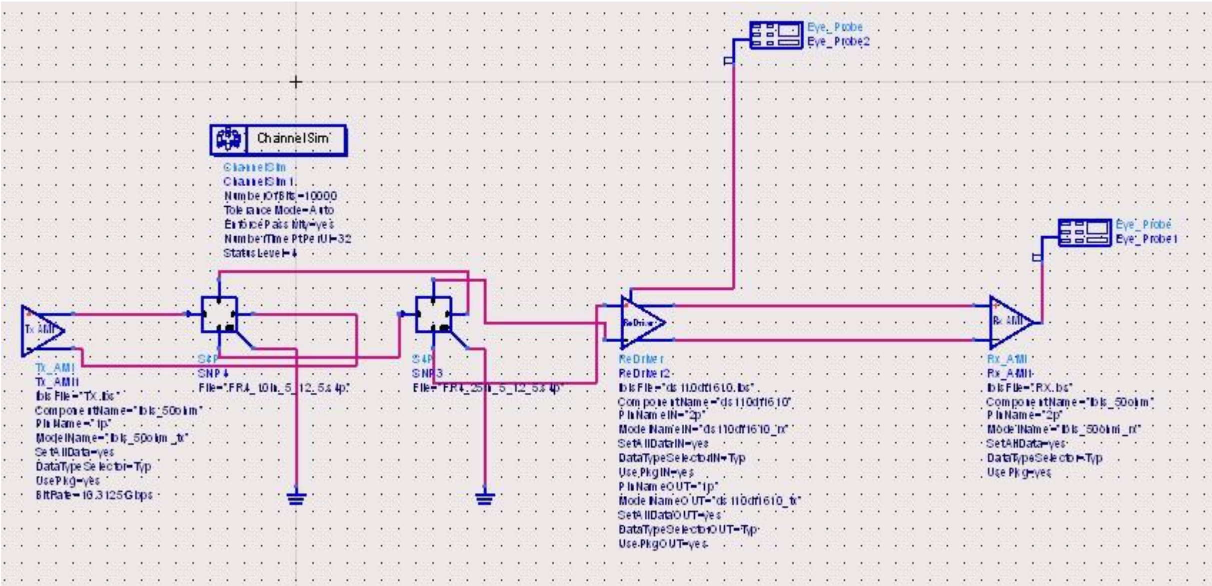
		31	1.330	

Table 4. Model Specific parameters for Receiver

Vga_gain	VGA gain. 0 is low gain and 1 is high gain
Vga_bw	VGA bandwidth. 0 is low bandwith and 1 is high bandwidth
ctleAdapt	1 turns on the auto adaptation. 0 to set the ctle setting through ctleSelect
ctleSelect	Work in conjunction with ctleAdapt =0 to set the CTLE. 0 has less gain and 64 has highest gain
monitor	0 connect the CTLE output to the transmitter in retimer mode. 1 connectb the VGA output to the transmitter in retimer mode. 2 connect the DFE output to the transmitter in retimer mode. 3 connect the slicer output to the transmitter in retime mode.
EOM_Window	This is the number of bits to be evaluated by the receiver before it makes an adjustment. The default value 5000 is based on empirical data that optimize the runtime and still give good accuracy as the hardware implementation. User can increase this value in the penalty of receiver taking more number of bits to reach steady-state.

3 ADS Simulation results

1. EQ Performance setup

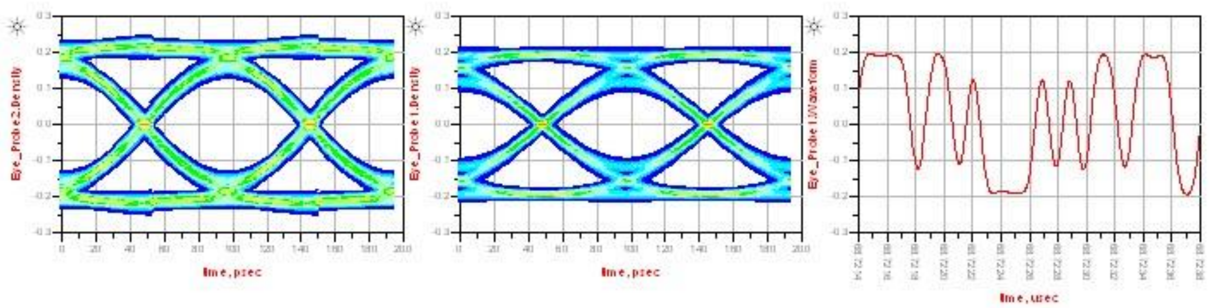


a. Channels : Rx channel = 25’’ 5mil stripline, Tx channel = 0’’ stripline
Parameters:

RX Settings	Vga_gain=0	Vga_bw=1	ctleAdapt=1	ctleSelect	monitor=2	EOM_Window =5000
TX Settings	c0_sgn=0	cp_sgn=0	cn_sgn=0	c0=63	cp=0	cn=0
TX Settings	sel_imax=1	sel_iload=0	sel_neg_gm=0	sel_edge=2	vod=31	tx_bypass=1

Note: TX is bypassed, and observes the DFE output at the TX output

Input Source: BitRate=10.125 Gbps PRBS-31, Vp-p = 1V, DE = 0dB

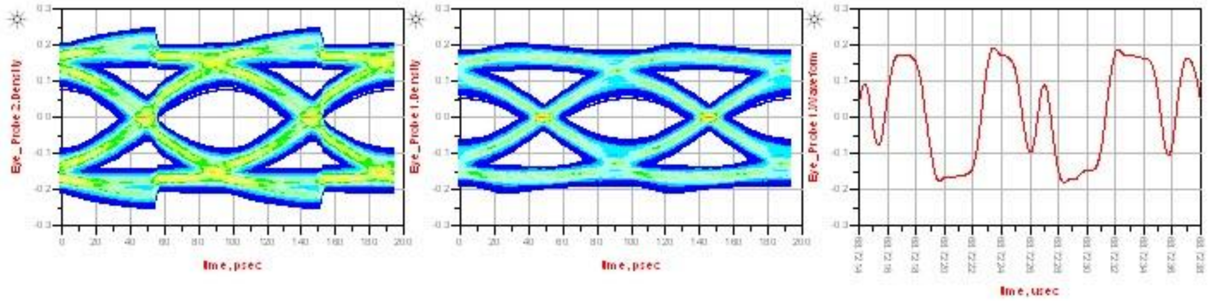


b. Channels : Rx channel = 35’’ 5mil stripline, Tx channel = 0’’ stripline
Parameters

RX Settings	Vga_gain=0	Vga_bw=1	ctleAdapt=1	ctleSelect	monitor=2	EOM_Window =5000
TX Settings	c0_sgn=0	cp_sgn=0	Cn_sgn=0	c0=63	cp=0	cn=0
TX Settings	sel_imax=1	sel_iload=0	Sel_neg_gm=0	sel_edge=2	vod=31	tx_bypass=1

Note: TX is bypassed, and observes the DFE output at the TX output

Input Source: BitRate=10.125 Gbps PRBS-31, Vp-p = 1V, DE = 0dB

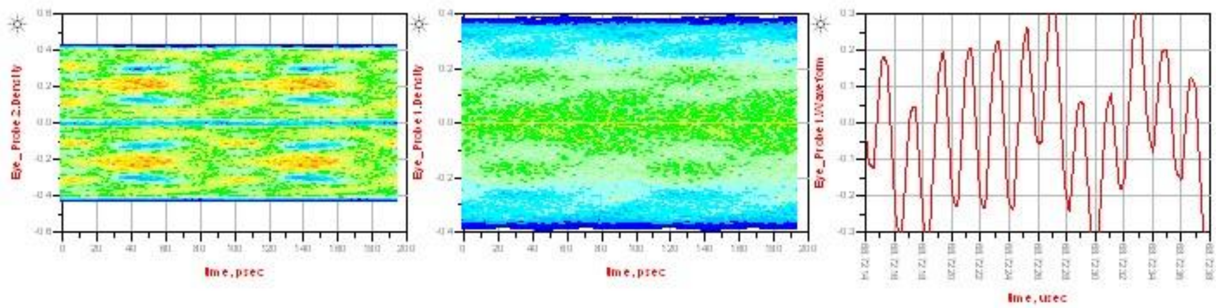


c. Channels : Rx channel = 40’’ 5mil stripline, Tx channel = 0’’ stripline
Parameters:

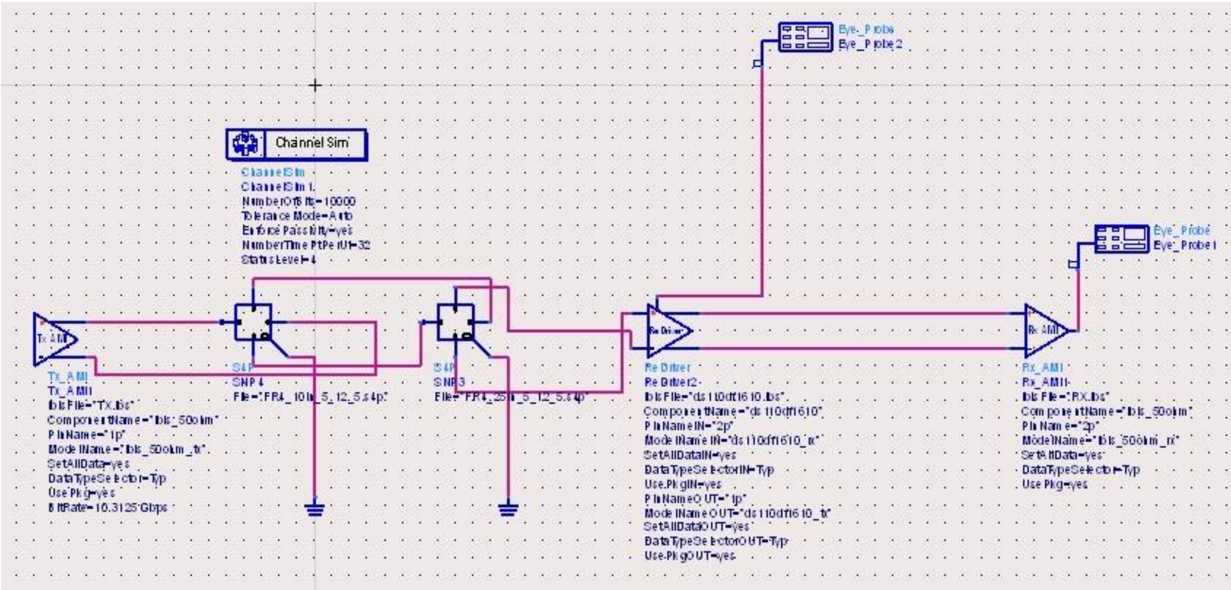
RX Settings	Vga_gain=0	Vga_bw=1	ctleAdapt=1	ctleSelect	monitor=2	EOM_Window =5000
TX Settings	c0_sgn=0	cp_sgn=0	Cn_sgn=0	c0=63	cp=0	cn=0
TX Settings	sel_imax=1	sel_iload=0	Sel_neg_gm=0	sel_edge=2	vod=31	tx_bypass=1

Note: TX is bypassed, and observes the DFE output at the TX output

Input Source: BitRate=10.125 Gbps PRBS-31, Vp-p = 1V, DE = 0dB



2. CDR Performance setup



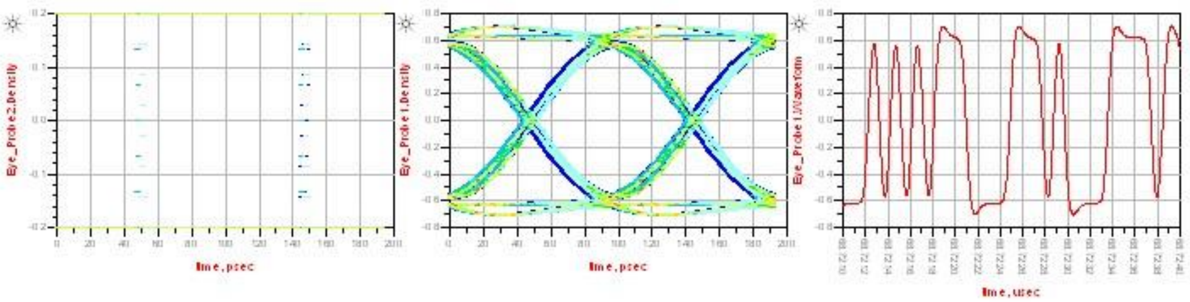
a. Channels : Rx channel = 35’’ 5mil stripline, Tx channel = 0’’ stripline

Parameters:

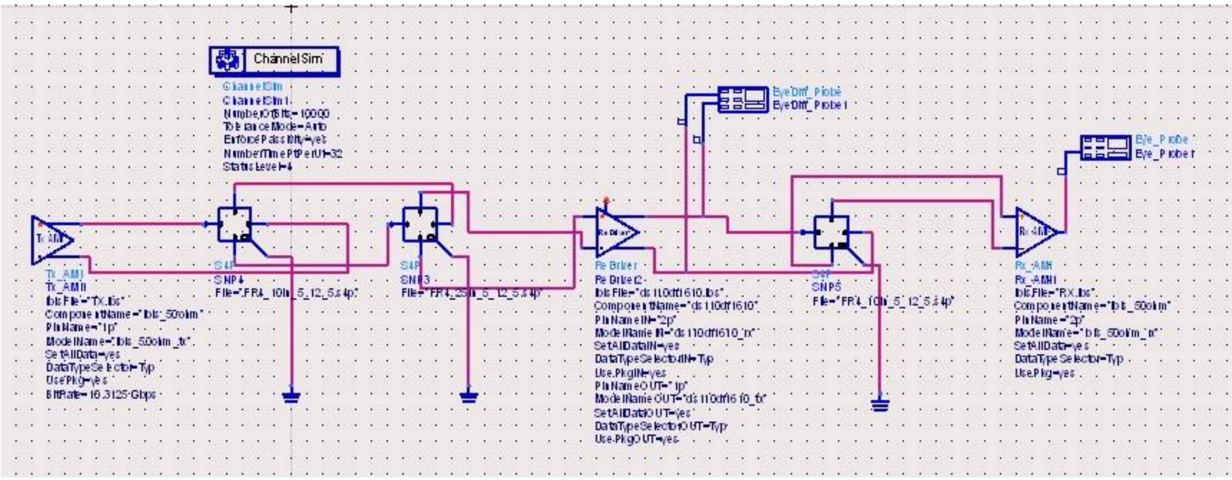
RX Settings	Vga_gain=0	Vga_bw=1	ctleAdapt=1	ctleSelect	monitor=3	EOM_Window =5000
TX Settings	c0_sgn=0	cp_sgn=0	cn_sgn=0	c0=63	cp=0	cn=0
TX Settings	sel_imax=1	sel_iload=0	sel_neg_gm=0	sel_edge=2	vod=31	tx_bypass=0

Note: The slicer output is sent to the TX oupt

Input Source: BitRate=10.125 Gbps PRBS-31, Vp-p = 1V, DE = 0dB



3. Transmitter Performance setup



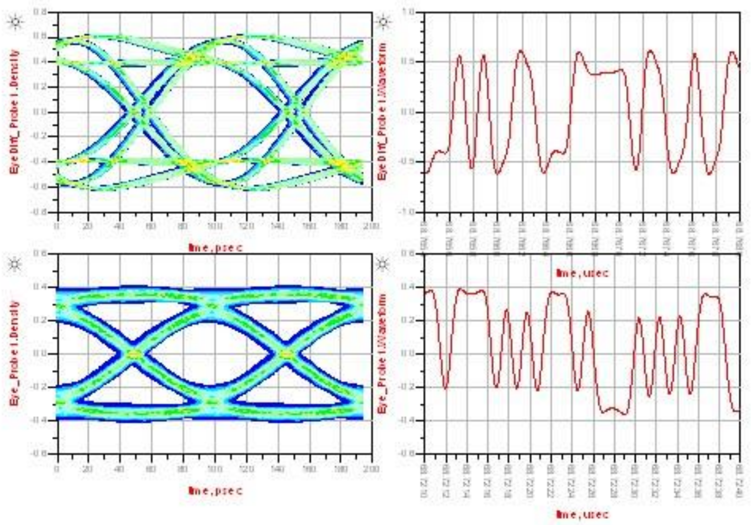
a. Channels : Rx channel = 35'' 5mil stripline, Tx channel = 10'' stripline

Parameters:

RX Settings	Vga_gain=0	Vga_bw=1	ctleAdapt=1	ctleSelect	monitor=3	EOM_Window =5000
TX Settings	c0_sgn=0	cp_sgn=1	Cn_sgn=1	c0=50	cp=10	cn=3
TX Settings	sel_imax=1	sel_iload=0	Sel_neg_gm=0	sel_edge=2	vod=31	tx_bypass=0

Note: The slicer output is sent to the TX oupt

Input Source: BitRate=10.125 Gbps PRBS-31, Vp-p = 1V, DE = 0dB



The TI IBIS-AMI models contain information on products that is based on high-level specifications. These may not accurately represent the product design in all cases. Please verify the accuracy of the models with TI before using the results.

4 Model Caveats

1) Due to the complexity of the adaptation loops of DS110DF1610 high-speed system, it requires about 5 minutes to run 1 millions bit in time-domain simulation for 32 samples per bit setting.

2) The Model utilizes the pulse response to optimize the CTLE setting and thus it requires the polarity of differential pair from the transmitter to channel and then to the input receiver to be consistent and not to be inverted. Invertion of the signal along the system path may cause the pulse response to be inverted and could break the CTLE adaptation.