TEXAS INSTRUMENTS

Modeling the AFE5808 family of components through IBIS

Texas Instruments

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1. LVDS BUFFER

Method of modeling the LVDS buffer through IBIS

Since the LVDS buffer has differential inputs and differential outputs, some additional considerations are involved while modeling it through IBIS.

AFE5808 LVDS buffer architecture

The internal structure of the LVDS buffer in AFE5808 family of products is shown in Figure 2.1. For simplicity, the enable pin has not been shown. HI and LO refer to the differential input to the buffer. VH and VL are internally regulated voltages of values 1.45V and 0.75V respectively. LOUTP and LOUTM form the differential output.
The buffer consists of 4 MOS switches that connect or disconnect the appropriate regulated voltages VH and VL to the output through the equivalent on-resistance of the switch.

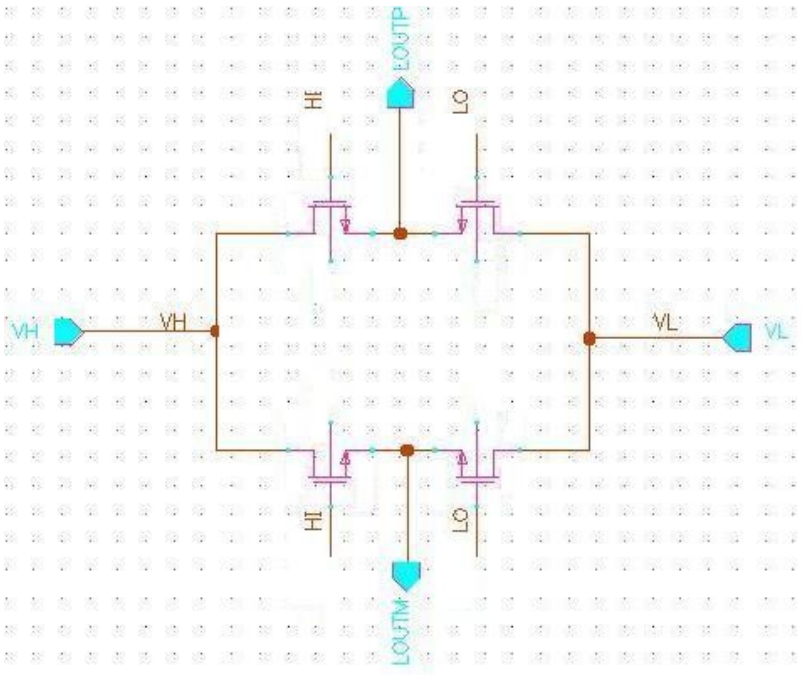

Figure 1.1. LVDS buffer architecture

Comparison of IBIS model with the actual circuit

The IBIS models were generated and compared with the actual circuit through SPICE simulations. Figure 1.2 shows the simulation environment for the actual LVDS buffer, while Figure 1.3 shows the identical environment used for the IBIS model.

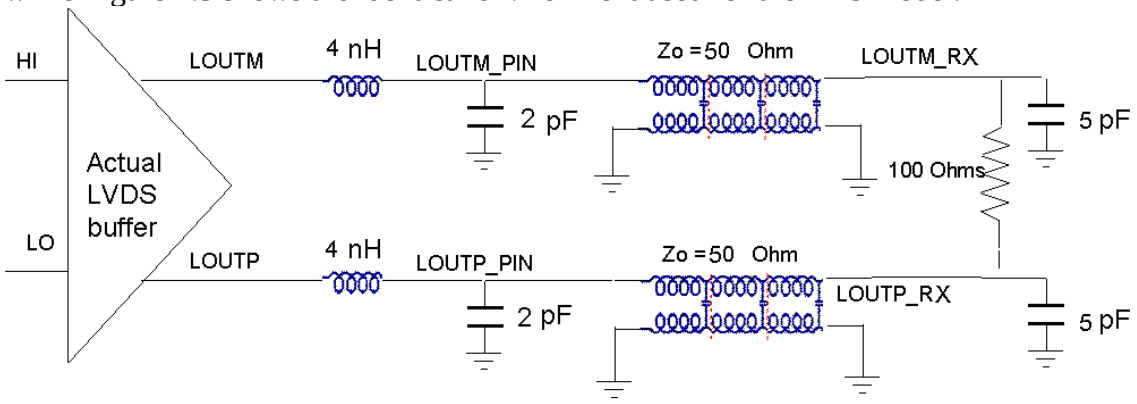

Figure 1.2. Simulation environment for the actual LVDS buffer

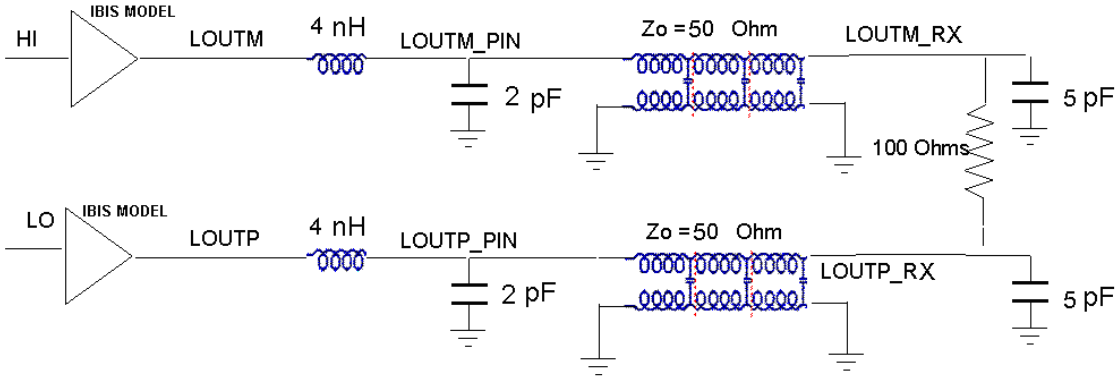

Figure 1.3. Simulation environment for the IBIS model of the LVDS buffer

Simulations were done with different values of the delay for the transmission line.

1. Figure 1.4 shows a comparison of the SPICE simulation results obtained from the IBIS model with those from the actual circuit. The delay of the transmission line was set to 0.50ns

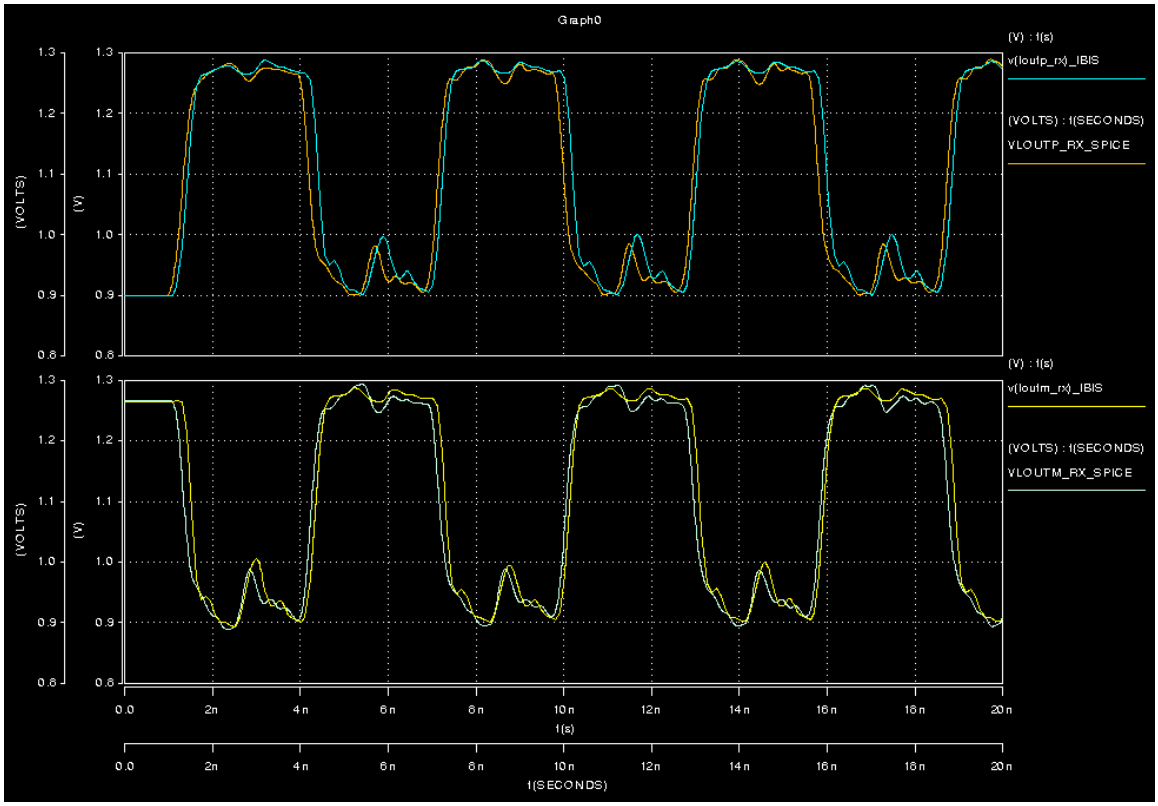

Figure 1.4. Comparison of results between full-transistor spice simulation and simulation using IBIS model for buffer.

As can be observed, there is a close match between the actual circuit and its IBIS model.

2. MODEL SUMMARY

Component name - AFE5808
Model types - Tristate, Terminator, series switch, series cap
Filename - lvds.ibs

Modeling conditions:

Condition	typ/ min/ max
DRVDD	1.8 V/ 1.7 V/ 1.9 V
VBG (Common mode reference)	1.065 V/ 1.045 V/ 1.1 V
Junction temperature (Tj)	25/ 125/ -40 (degree C)
Process setting	nominal/ weak/ strong

Package Characteristics:

Characteristics	typ/ min/ max
R_pkg:	0.16Ω/0.144Ω/0.176Ω
L_pkg	4nH/3.6 nH /4.4 nH
C_pkg	2.0pF / 1.8 pF /2.2 pF

3. Quality Verification:

The created IBIS models are verified as follows:

1. Visual check of each characteristics using the s2iplt tool
2. Syntax check by IBISCHK4
3. Behavior of IBIS models and actual circuit compared using SPICE

4. Simulation using IBIS models for the buffer

4.1 Sample instantiation of the IBIS models for the lvds buffer in HSPICE:

```
BOUTPUTP PU 0 LOUTP INP EN_LVDS
+FILE = 'lvds.ibs' MODEL = 'lvds_tx_5808’
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1

BOUTPUTM PU 0 LOUTM INM EN_LVDS
+FILE = 'lvds.ibs' MODEL = 'lvds_tx_5808'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1
```

5.1 Sample SPICE deck for simulation of buffer

```
.TEMP 27

* INPUT TO THE BUFFER
VINP INP 0 PULSE (0 1.8 0N 0.2N 0.2N 2.7N 5.8N)
VINM INM 0 PULSE (1.8 0 0N 0.2N 0.2N 2.7N 5.8N)

BOUTPUTP PU 0 LOUTP INP EN_LVDS
+FILE = 'lvds.ibs' MODEL = 'lvds_tx_5808'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1

BOUTPUTM PU 0 LOUTM INM EN_LVDS
+FILE = 'lvds.ibs' MODEL = 'lvds_tx_5808'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1


*ENABLE SIGNAL FOR THE BUFFER
VEN_LVDS EN_LVDS 0 0.0

* PIN INDUCTANCE
LOUTP LOUTP_EXT LOUTP 4N
LOUTM LOUTM_EXT LOUTM 4N
** PIN CAPACITANCE
COUTP LOUTP_EXT 0 2PF
COUTM LOUTM_EXT 0 2PF

** TRANSMISSION LINE LOAD
TDATALINKP LOUTP_EXT 0 LOUTP_RX 0 Z0=50 TD=0.5N
TDATALINKM LOUTM_EXT 0 LOUTM_RX 0 Z0=50 TD=0.5N

** LVDS TERMINATION AT RECEIVER END
RLOAD LOUTP_RX LOUTM_RX 100

** CAPACITANCE AT RECEIVER END
COUTP_RX LOUTP_RX 0 5PF
COUTM_RX LOUTM_RX 0 5PF

.OPTION POST
.TRAN 10PS 20NS
```

```
.PLOT TRAN V(LOUTP) V(LOUTM)
+ V(LOUTP_EXT) V(LOUTM_EXT)
+ V(LOUTP_RX) V(LOUTM_RX)
+ V(LOUTP_RX,LOUTM_RX)

.END
```