TPS6286900C PSpice Transient Model Features and Limitations

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* Model Usage Notes:
* A. The following features have been modelled
*          1. RON and variation with VIN
*          2. Power Save Mode or Forced PWM Mode.
*          3. Low-side FET Zero-Crossing
*          4. Current Sense and Positive Overcurrent Protection (OCP)
*          5. Low-side FET Negative Current Limit
*          6. Power Good
*          7. Output Voltage Discharge
*          8. UVLO Protection
*          9. Software Enable
*         10. Vout Ramp speed
*         11. Hiccup or latching protection
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* B. Features have not been modeled
*          1. Operating Quiescent Current
*          2. Shutdown Current
*          3. Temperature dependent characteristics
*          4. SCL and SDA pin functionalities.
*          5. Ground pins have been tied to 0V internally. Therefore, this model cannot be
*             used for inverting topologies.
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* C. Application Notes
*          1.The parameter STEADY_STATE has been used to reach the steady state faster.
*             Keep STEADY_STATE = 0 to observe startup behaviour
*             Keep STEADY_STATE = 1, Vout = output voltage value and appropriate IC on
*             Inductor and capacitor to observe for faster Steady state          .
*          2. Additional pins and parameters has been added to model I2C registers.
*          3. The SOFTWARE_ENABLE Pin maps to Control Register bit for Software Enable.
*             SOFTWARE_ENABLE= 0 - Disable the device. All registers values are still kept.
*             SOFTWARE_ENABLE= 1 - Re-enable the device with a new startup without the
*             tDelay.
*          4. The parameter ENABLE_FPWM_DURING_VOUT_CHANGE maps to Control
*             Register bit for Enable FPWM mode during output voltage change and the
*             ENABLE_FPWM pin maps to Control Register bit for Enable FPWM Mode.
*             If ENABLE_FPWM_DURING_VOUT_CHANGE=1 and ENABLE_FPWM=0, and if
*             the device goes from CCM to DCM, 128 cycles of FPWM is activated.
*             After that the device goes to PFM.
*             If ENABLE_FPWM_DURING_VOUT_CHANGE= 0, then, ENABLE_FPWM takes
*             control.
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*        5. The parameter VOUT_RAMP_SPEED maps to Control Register bit for Voltage
*           ramp speed.
*          The ramp speed is defined by VOUT_RAMP_SPEED (0->20mV/us,1->10mV/us,2-
*          >5mV/us,3->1mV/us)
*        6. The parameter ENABLE_HICCUP maps to Control Register bit for Enable HICCUP.
*           ENABLE_HICCUP= 1 - Enable HICCUP, Disable latching protection.
*           ENABLE_HICCUP= 0 - Disable HICCUP. Enable latching protection.
*        7. The parameter ENABLE_OUTPUT_DISCHARGE maps to Control Register bit for
*           Enable Output Discharge.
*           When ENABLE_OUTPUT_DISCHARGE=1, VOUT discharges through Discharge
*           Resistor, Else discharge is only through load.
*        8. The Pin VOUT_REG maps to Vout Register available in the device. The device has
*           fixed startup output voltage of 0.5V, thereafter it ramps up/down to the Vout
*           value provided via Vout Register.
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