Model FeaturesandLimitations: Buck Topology

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* Model Usage Notes:
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* A. Features have been modelled
*   1. Fixed Fsw = 2.25 MHz
*   2. Peak Switch Current Limit
*   3. Internal fixed Soft Start Time
*   4. Enable functionality
*   5. VIN UVLO and EN UVLO
*   6. Power Good & FPWM functionality
*   7. Pre-biased Startup
*   8. PWM & PFM Operations
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* B. Features haven't been modelled
*   1. Operating Quiescent Current
*   2. Shutdown Current & Leakage Currents
*   3. Temperature dependent characteristic
*   4. I2c Interface, DVS & few supply or input/output pins
*   5. Ground Pins have been tied to 0V internally and hence model does not support Inverting topologies
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* C. Application Notes
*   1. SS = 0 for Start-up behaviour & SS = 1 for model to work in Steady state
*   2. FAST_MODE = 0 for normal operation & FAST_MODE = 1 for faster operation to cut tStart & tRamp by 50%
*   3. DEF_RES= 0 for output voltage set by DEFDCDC3 logic levels & DEF_RES = 1 output voltage set by Resister divider
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