ADC12DJ3200 IBIS & IBIS-AMI Models

User's Guide

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1. Introduction

This document describes the organization, structure, and proper usage of the TI ADC12DJ3200 IBIS-AMI models (compiled and approved for external customer release), hereafter referred to as the "model" for short. The model is intended for use by the ADC12DJ3200 design team and by ADC12DJ3200 customers for system-level modeling and verification. This document assumes that you are familiar with the relevant IBIS-AMI modeling specifications. In addition there are also 3 flavors of IBIS models included in this package (for AAV, CCGA, CLGA packages).

1.1 Formatting Conventions

The help readability, various formatting conventions are used throughout this document:

- Hyperlinks to material within and outside this document are marked in blue.
- Courier font is used for `file names`, `code`, `variables`, `structures`, `parameters`, and `terminal commands`.

1.2 Charter of the SerDes IBIS-AMI

The models are designed in accordance with the IBIS-AMI standard and attempt to model the significant characteristics of most components in the ADC12DJ3200. The models are not intended to be an exact representation of ADC12DJ3200 components implemented. Rather, the models seek to provide as high a degree of accuracy as is feasible outside of Spice-based models and simulations.

1.3 Is / Is Not Table

The following table describes the features and purposes of the models, as well as the limitations of the models.

Table 1: Model Is / Is Not Table

Is	Is Not
Compiled for 64-bit AMI EDA tool that run in Linux & Windows platform. The reference simulator is Keysight – ADS.	
Compliant to IBIS-AMI 6.0	Compliant to a more recent BIRD revisions, if they exist
Model of ADC12DJ3200 I/O functionality, non-idealities and I/O performance	Exact representation of implemented components

2. About This Release

2.1 IBIS Model Files

Table 2: IBIS Model Files

File Name	Type	Description
adc12djxx00aav.ibs	IBIS	Marketing part# ADC12DJ2700AAV, ADC12DJ3200AAV, ADC08DJ3200AAV Package-type BGA #pins/pkg drawing 144-pin AAV
adc12dj3200qml-sp_ccga.ibs	IBIS	Marketing part# ADC12DJ3200QML-SP Package-type CCGA [BGA] #pins/pkg drawing 196-pin NWE CCGA Ceramic Package with columns (ceramic column grid array)
adc12dj3200qml-sp_clga.ibs	IBIS	Marketing part# ADC12DJ3200QML-SP Package-type CLGA [BGA] #pins/pkg drawing 196-pin ZMX CLGA Ceramic Package without columns (ceramic land grid array)

2.2 IBIS-AMI Model Files (ADS workspace)

Table 3: IBIS-AMI files, ../data/TI_ADC12DJ3200/

File Name	Type	Description
ADC12DJ3200.ibs	IBIS	Top-level IBIS wrapper for the Tx AMI model.
ADC12DJ3200_typ.ami ADC12DJ3200_leakage.ami ADC12DJ3200_slow.ami ADC12DJ3200_fast.ami ADC12DJ3200_tempinv.ami	AMI	Parameters file for the Tx model as required by the IBIS-AMI standard (version 6.0)
ADC12DJ3200_x64.dll ADC12DJ3200_x64.so	DLL, SO	Windows/Linux 64-bit compiled shared library for the Tx model (IBIS-AMI standard version 6.0)

Table 4: IBIS-AMI files, ../data/

File Name	Type	Description
TX3200_typ.s4p TX3200_leakage.s4p TX3200_slow.s4p TX3200_fast.s4p TX3200_tempinv.s4p	S4P	driver terminations to capture the output reflection and cross-couple signal
DAxaav.s4p, DBxaav.s4p	S4P	Package S4P single lanes for AAV package
DAxccga.s4p, DBxccga.s4p	S4P	Package S4P single lanes for CCGA package
DAxclga.s4p, DBxlcga.s4p	S4P	Package S4P single lanes for CLGA package

Table 5: additional data files

File Name	Type	Description
../data/ADC12DJ3200AAV/ ADC12DJ3200_AAV_DAx.s32p ADC12DJ3200_AAV_DBx.ss32p	S32P	Package 32port covering interlane coupling for AAV package
../data/ADC12DJ3200QML-SP_CCGA/ ADC12DJ3200_CCGA_DAx.s32p ADC12DJ3200_CCGA_DBx.s32p	S32P	Package 32port covering interlane coupling for CCGA package
../data/ADC12DJ3200QML-SP_CLGA/ ADC12DJ3200_CLGA_DAx.s32p ADC12DJ3200_CLGA_DAx.s32p	S32P	Package 32port covering interlane coupling for CLGA package
../data/ fr4_100mm.s4p fr4_150mm.s4p fr4_200mm.s4p	S4P	100/150/200mm FR4 line for test and example purposes

3. IBIS files

adc12djxx00aav.ibs
adc12dj3200qml-sp_ccga.ibs
adc12dj3200qml-sp_clga.ibs

3.1 Device conditions for IBIS corners

Table 6: IBIS corner conditions

Case	Silicon model	VDD18 supply	VDD11 supply	Temperature ambient
Typ	nom	1.9V	1.1V	25degC
Min	weak	1.8V	1.05V	125degC
Max	strong	2.0V	1.15V	-40degC

3.2 Component configurations

adc12djxx00aav.ibs
Two different device component definitions are possible which affect the termination of following differential input pins:

B1, C1	TMSTP+-
F1, G1	CLK+-
K1, L1	SYSREF+-

1. ADC12DJxx00AAV_PECL
In this case each pin is terminated with 50Ohm to ground.

2. ADC12DJxx00AAV_LVDS
In this case a termination of typical 100Ohm between the differential pins is defined.

adc12dj3200qml-sp_ccga.ibs
Two different device component definitions are possible which affect the termination of following differential input pins:

C1, D1	TMSTP+-
G1, H1	CLK+-
L1, M1	SYSREF+-

1. ADC12DJ3200QML-SP_CCGA_PECL
In this case each pin is terminated with 50Ohm to ground.

2. ADC12DJ3200QML-SP_CCGA_LVDS
In this case a termination of typical 100Ohm between the differential pins is defined.

adc12dj3200qml-sp_clga.ibs
Two different device component definitions are possible which affect the termination of following differential input pins:

C1, D1	TMSTP+-
G1, H1	CLK+-
L1, M1	SYSREF+-

1. ADC12DJ3200QML-SP_CLGA_PECL
In this case each pin is terminated with 50Ohm to ground.

2. ADC12DJ3200QML-SP_CLGA_LVDS
In this case a termination of typical 100Ohm between the differential pins is defined.

4. IBIS-AMI Simulation

4.1 IBIS-AMI case definitions

The IBIS-AMI models are defined for 5 different corner cases. The device conditions are listed below.

Table 6: IBIS-AMI case definitions

case	Silicon model	VDD11 supply	Temperature junction
typ	nom	1.1V	90degC
leakage	strong	1.15V	150degC
slow	weak	1.05V	150degC
fast	strong	1.15V	-55degC
temp-inv	weak	1.05V	-55degC

4.2 IBIS-AMI basic set-up in ADS

- Open basic set-up from ADS workspace: ADC12DJ3200_TX – schematic.
  Make sure EnforcePassivity=no in ChannelSim
- Select IBIS-AMI case combination for Tx_AMI1 and SNP1 instances.
- Select package option and output lane S4P data for SNP2

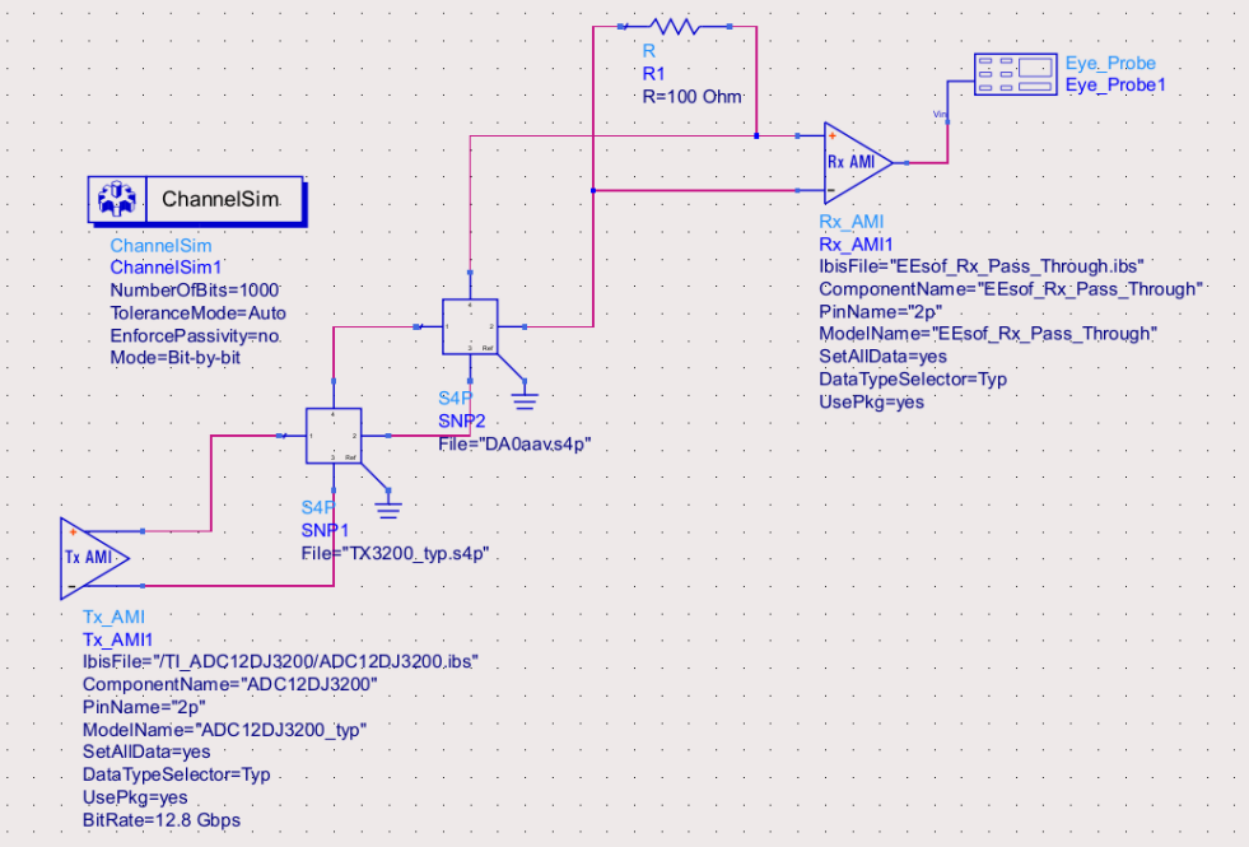

Figure 1. Basic IBIS-ADI schematic set-up in ADS

Expected result at Eye_Probe in this example

- typical case, 12.8Gbps
- lane DA0 in AAV package
- preemphasis value = 0
- ideal 100Ohm termination

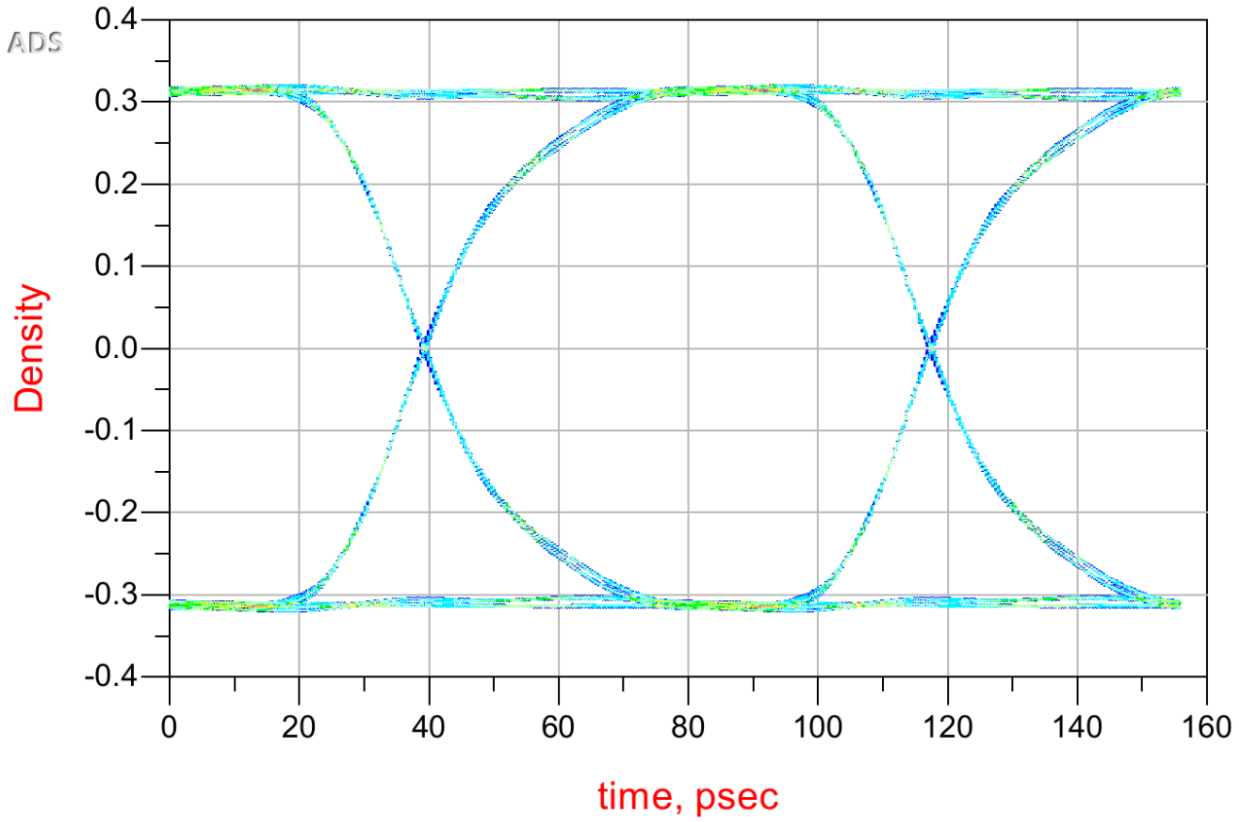

Figure 2. Eyeprobe output in ADS

4.3 IBIS-AMI Model Features

IBIS-AMI simulation case can be selected under “Pin”. There are 5 cases defined (see Table 6). Make sure S4P data for SNP1 instance matches the selected simulation case.

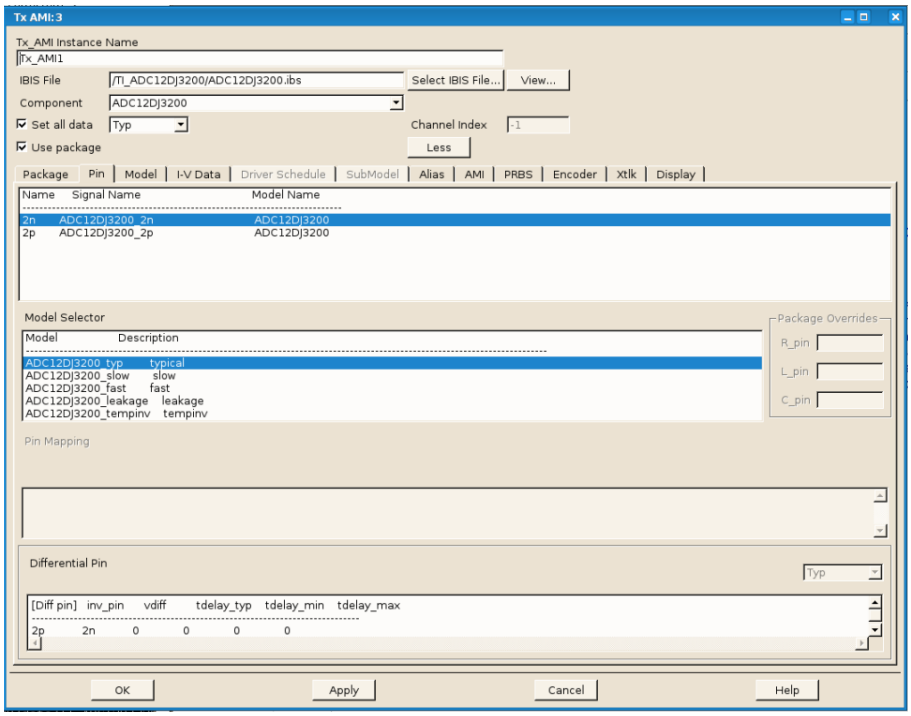

Figure 3. selection of simulation case

There are two possibilities to set the preemphasis value
“AMI” selector – Autoinit

Autoinit = 1 = Yes (default) -> auto adapt to optimum preemphasis value
Autoinit = 0 = No -> manual selection of preemphasis value

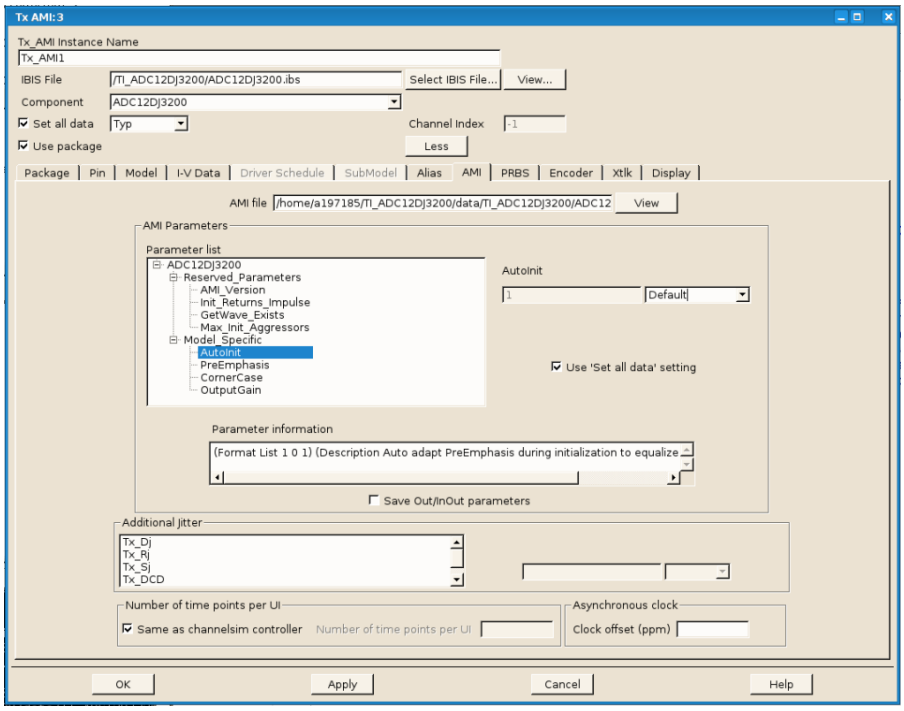

Figure 4. Automatic Preemphasis selection

For manual preemphasis selection use
“AMI” selector – PreEmphasis

Manual selection of preemphasis value if Autoinit = 0.
Choose value between 0 (no preemphasis) and 15 (decimal, max. preemphasis)

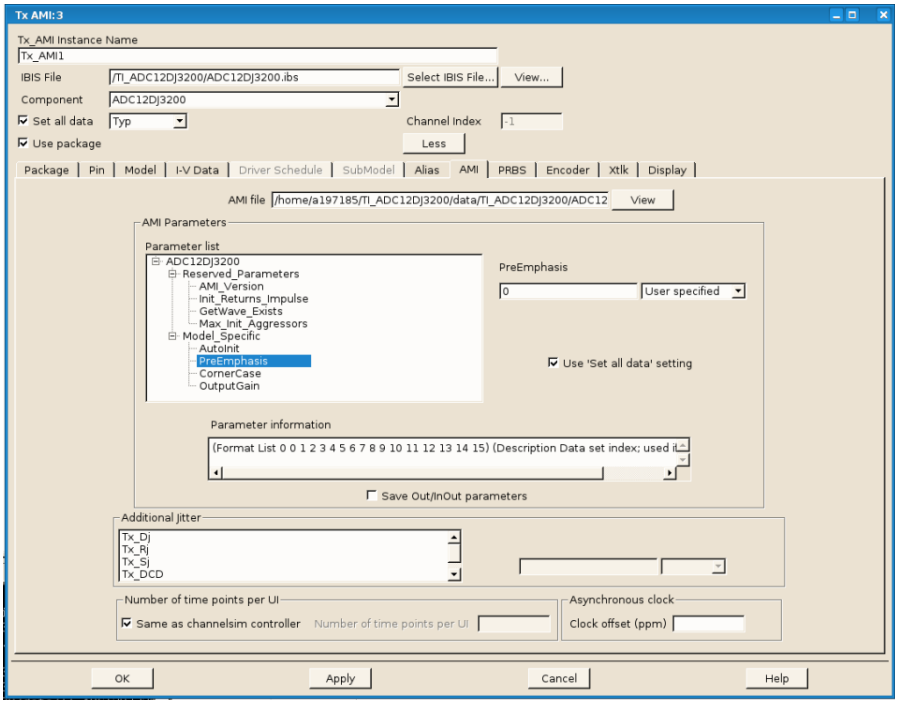

Figure 5. Manual Preemphasis selection

4.4 IBIS-AMI example case in ADS

The following application example in ADS can be found under ADC12DJ3200_TX_example – schematic. A 200mm FR4 line is used as a channel. The “Autoinit” feature is active and chooses preemphasis = 10 (decimal) as the optimum setting.

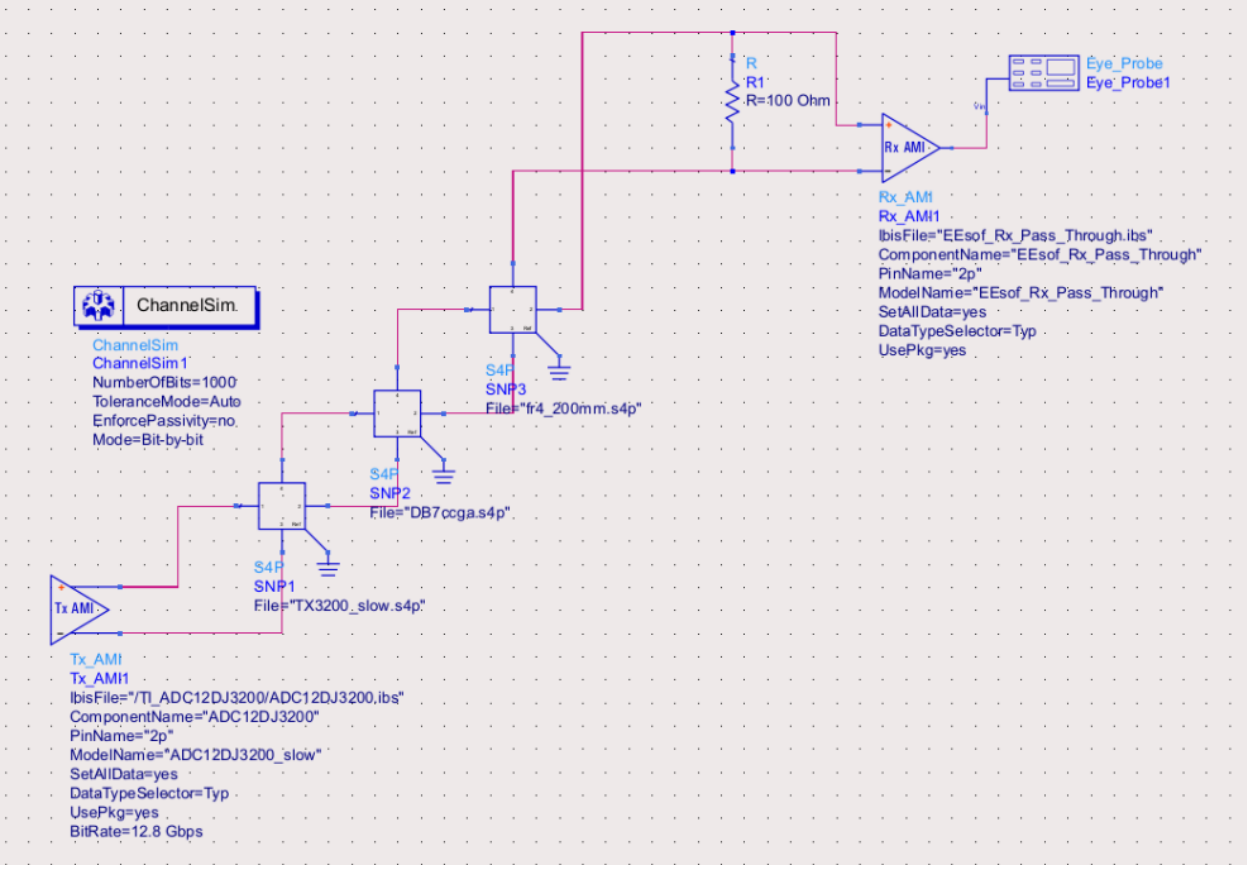

Figure 6. ADS channel example with 200mm FR4 line

- IBIS-AMI slow case, 12.8Gbps
- Lane DB7 CCGA package
- 200mm FR4 channel attached
- With “Autoinit” = 1 optimum preemphasis setting calculated to “PreEmphasis” = 10 (decimal)
- ideal termination 100Ohm

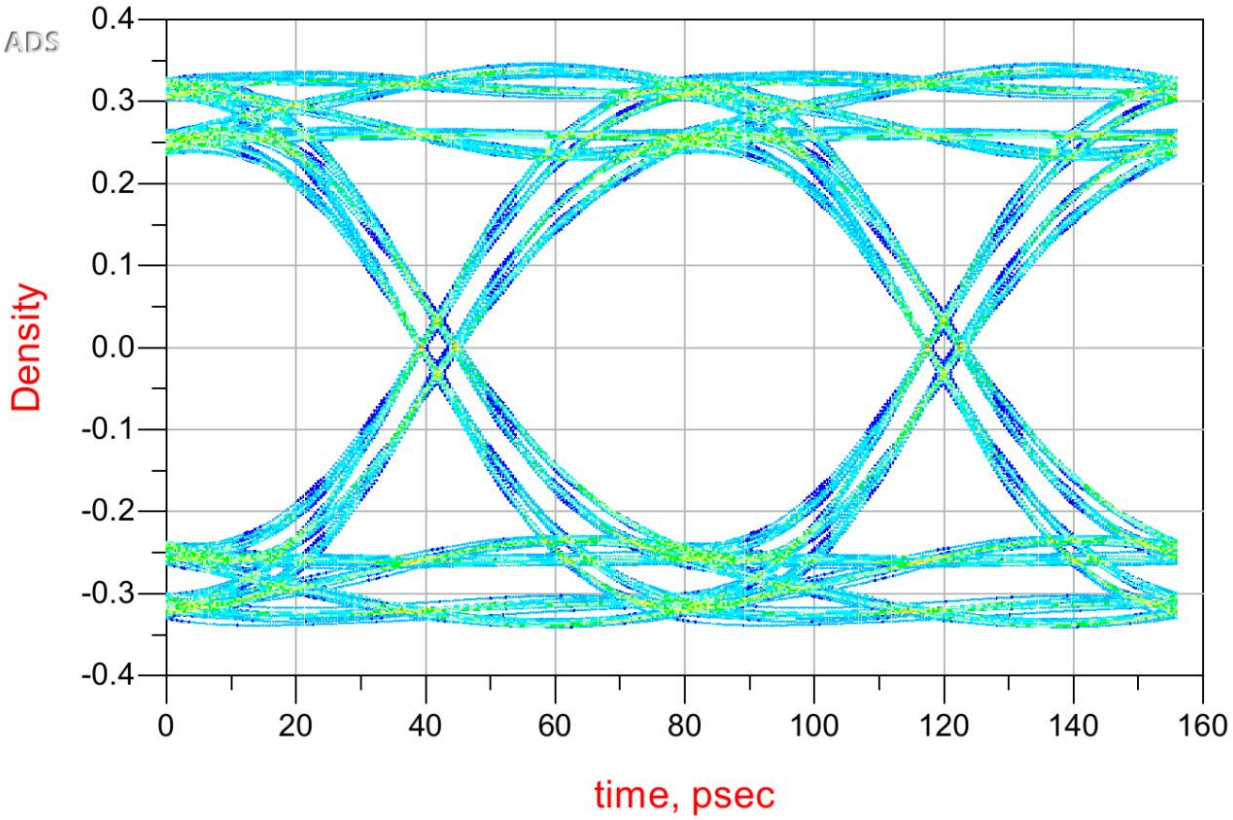

Figure 7. ADS simulation output