LMH1983 IBIS Model User Note

National Semiconductor
Model User Note
May 4, 2010

SCOPE

This model supports the LVDS Clock Output pins only on the LMH1983SQ (CLKout1, CLKout2, CLKout3, and CLKout4). Control and other pins are not modeled.

SPECIFICS

Part Number: LMH1983SQ (40 LLP Package)
IBIS File Name: lmh1983.ibs
IBIS Version: 4.2
File Revision: 1.1

TEST BENCH

The LVDS outputs are intended to drive a 100 Ohm differential transmission line terminated with a 100 Ohm DC coupled termination resistor between the pair. The load is typically is a high impedance differential input which presents mainly a small capacitive load. Being a clock output, a clock wave shape is the stimulus and is in the 20 to 150 MHz range. Differential output voltage of +/- 350mV (700mVp-p) is expected with transition times in the 500ps range.

Figure 1 shows a typical test bench. Figure 2 shows a simulation output using the IBIS model. Figure 3 shows a bench measurement in a similar environment (SD1983EVK).

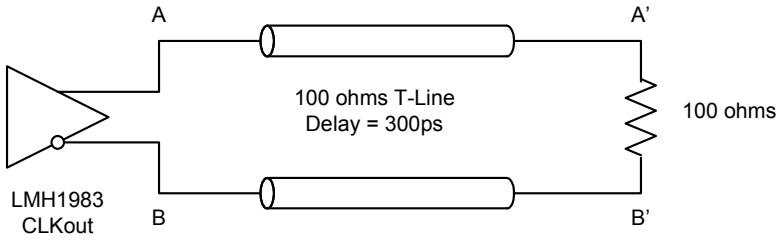
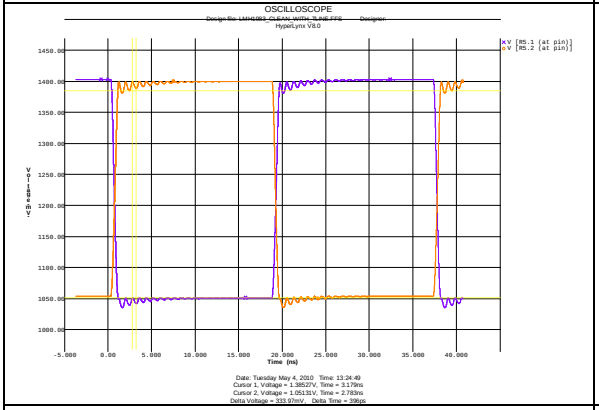
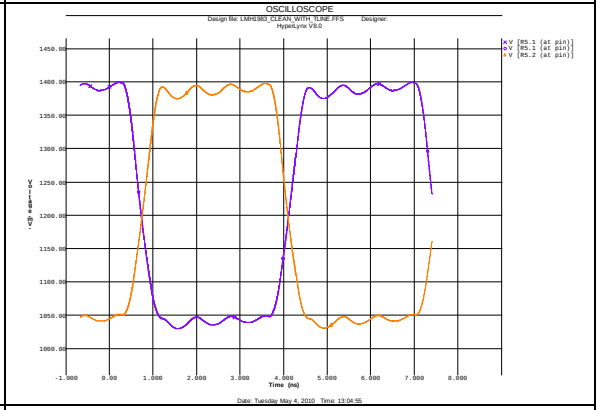


FIGURE 1. Simulation Test Bench

CLKout1: 27MHz	CLKout2: 148.5MHz
	
Rise Time = 413.79ps	Rise Time = 397.77ps

Fall Time = 359.04ps V_{OD} = 335mV V_{ODpp} = 368mV V_{OS} = 1.225V	Fall Time = 368.36ps V_{OD} = 335mV V_{ODpp} = 370mV V_{OS} = 1.21V

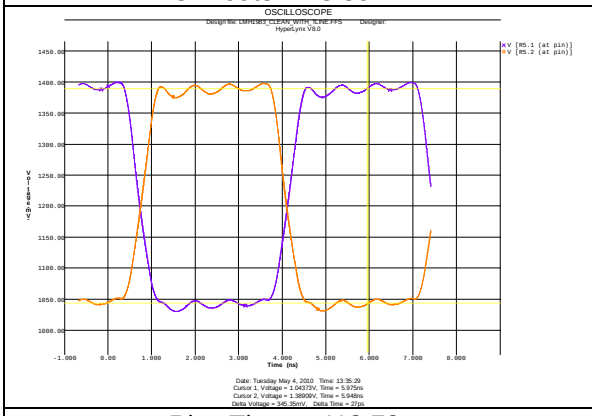
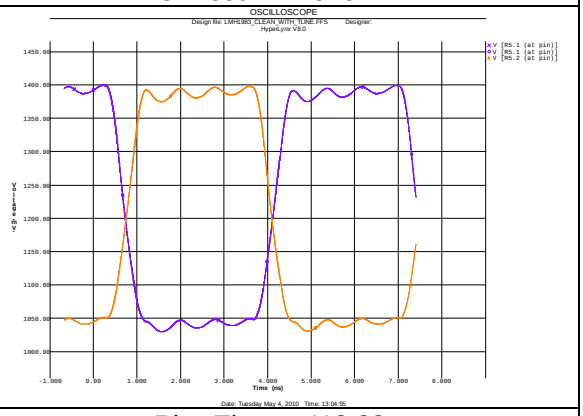
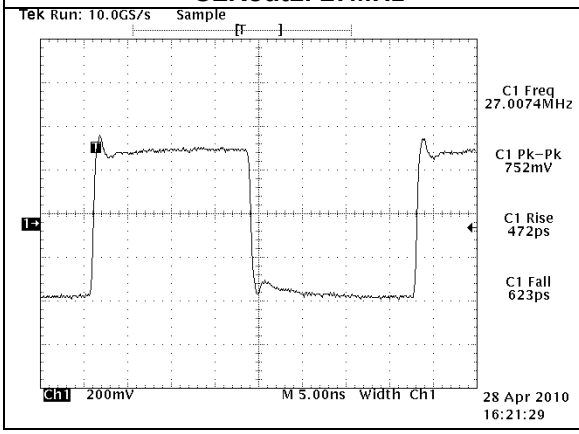
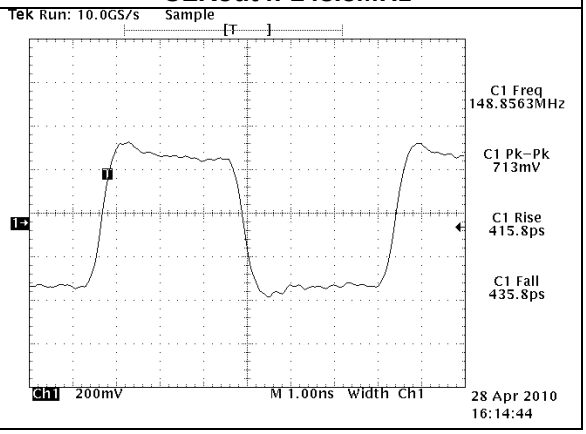
CLKout3: 148.35MHz	CLKout4: 24.576MHz
	
Rise Time = 413.79ps Fall Time = 398.01ps V_{OD} = 345mV V_{ODpp} = 370mV V_{OS} = 1.22V	Rise Time = 413.88ps Fall Time = 359.10ps V_{OD} = 350mV V_{ODpp} = 368mV V_{OS} = 1.23V

FIGURE 2. IBIS Model Simulation Results (TP: A' and TP B')

CLKout1: 27MHz	CLKout4: 148.5MHz
	

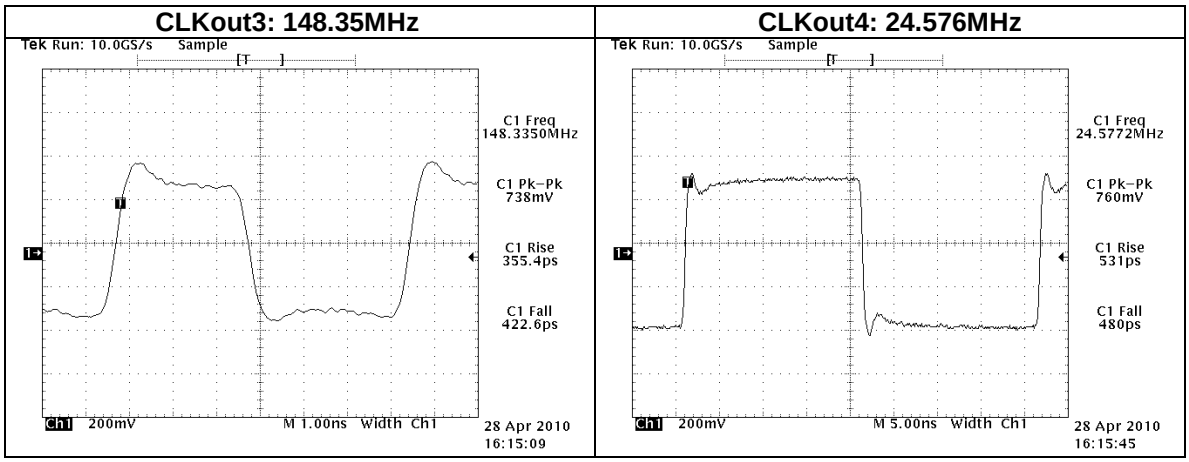


FIGURE 3. Bench Measurement

SUMMARY

This model passes IBIS checks, and simulates in a sample simulator with good correlation to the measured bench waveform with a similar load.