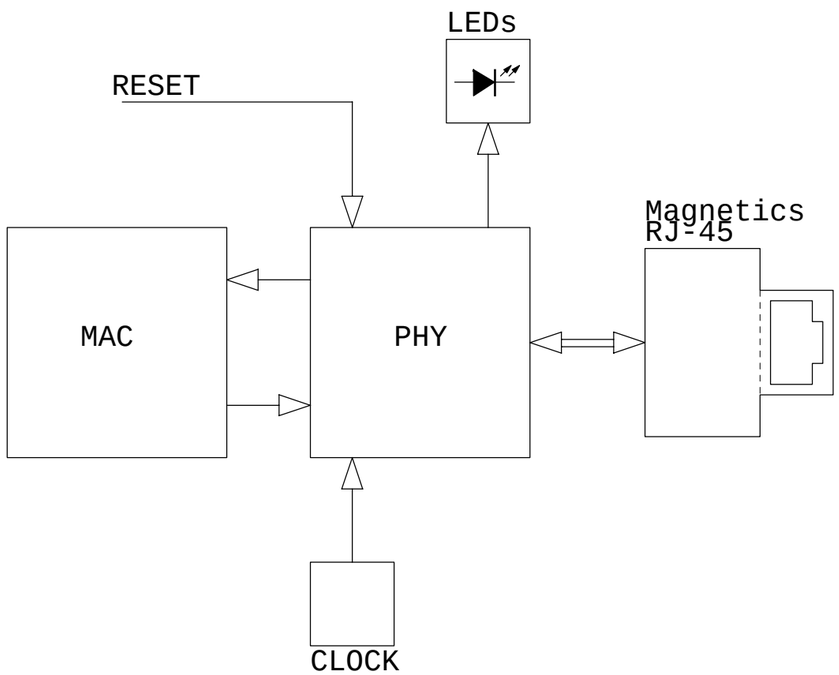
Reference design for DP83865DVH: Gigabit Ethernet PHY.

These schematics are provided for reference only. For any designs based on these schematics always contact National Semiconductor Corporation BEFORE initiating PCB manufacturing and ask for your design to be reviewed.

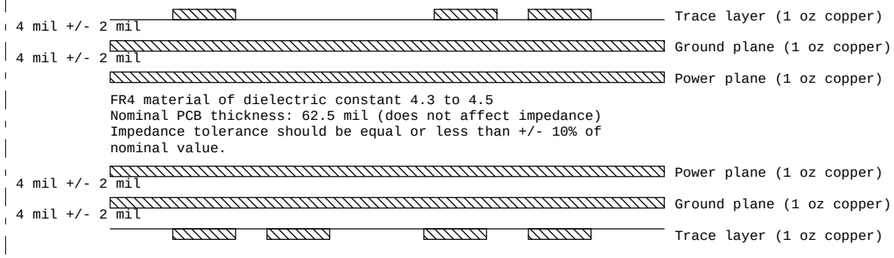
Application Block Diagram



Note on recommended PCB Layer Stack-up (diagram not drawn to scale)

Single ended trace with 50 Ohm controlled impedance: 7 mil trace width.

Differential pair with 100 Ohm controlled impedance: 5 mil trace width, 6 mil clearance.



Six layer PCB stack-up recommended. Use two ground planes for maximum EMI shielding. Keep trace layers on the outside for lowest propagation delay. Use two power planes (1.8V and 2.5V) for low impedance current path. Minimize the gap between power and ground plane to maximize the effects of plane capacitance. Adjust trace width and gap to ground plane for controlled impedance. The geometry numbers above can be used as an example. Controlled impedance traces are either 50 Ohms single ended with respect to the ground plane or 100 Ohms differential impedance to each other with ground plane. Controlled impedance traces are noted as such. All other traces can be between 50 - 100 Ohm.

Note on Differential Pairs

=>Pairs must be routed for 100 Ohms differential imdedance.
=>All pairs must be routed with equal distance throughout the length of the pair.
=>Pairs of the same port are to be matched in length, not exceeding 0.7" (+/- 0.35) between the longest and shortest pair.
=>Clearance between pairs of the same port should be four time the distance between pair signals.
=>Clearance between pairs of different ports should be eight times the distance between pair signals.

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Suggested termination on MAC side. Place resistors close to source.
Actual values may differ for series termination resistors and depend on impedance of the MAC chip's output pins.
MDC/MDIO termination as suggested by IEEE spec.

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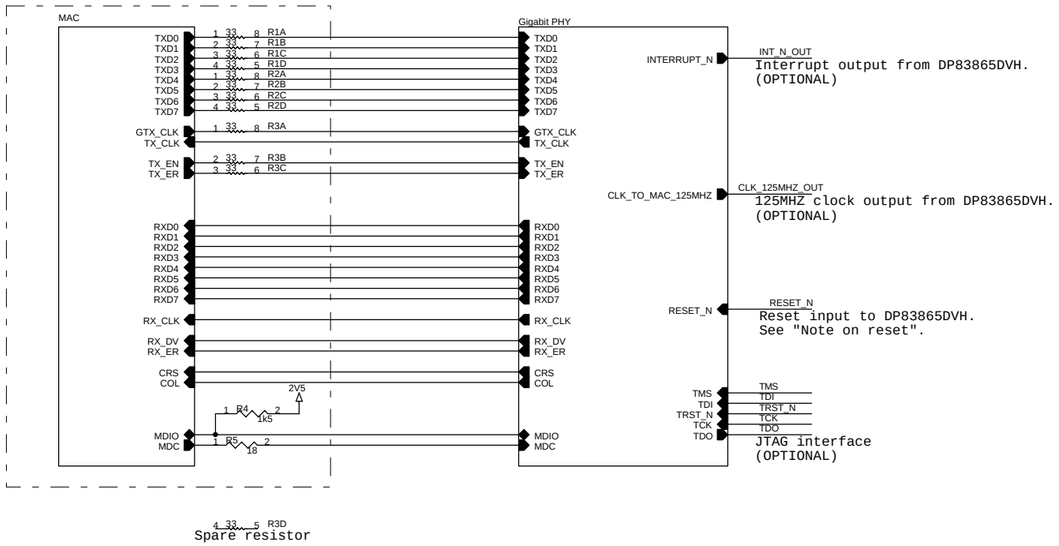
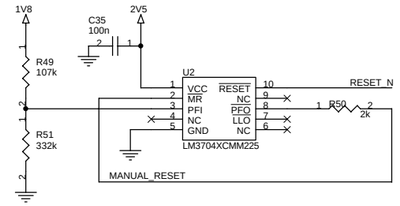


Note on reset:

Only use this circuit if the application does not provide a clean reset signal as specified in the datasheet.



This circuit produces a clean reset signal with a reset duration of 200ms. The CMOS output either drives the reset signal high or low (not tri-stated).
A reset will be triggered if the 2.5V supply voltage drops below 2.25V or if the 1.8V supply drops below 1.62V.
The signal MANUAL_RESET may be used to implement an external reset function (e.g. by adding a push-button). Pulling this signal to ground will issue a reset.

MAC interface configuration:

In this example schematic the MAC interface of the PHY is configured to GMII. Other applications may require this interface to be configured as RGMII. Follow these instructions to change design to RGMII. All other design notes still apply.

The MAC interface is configured through the strap options RGMII_SEL0 and RGMII_SEL1 according to this table:
RGMII_SEL0 RGMII_SEL1
---- 0 ---- ---- 0 ---- GMII mode
---- 0 ---- ---- 1 ---- GMII mode
---- 1 ---- ---- 0 ---- RGMII mode (HP original)
---- 1 ---- ---- 1 ---- RGMII mode (3COM)
If RGMII is to be used, 3COM mode is recommended. See "Note on Recommended PCB Layer Stack-up" and also refer to DP83865DVH datasheet for layout guidance.

All GMII signals must have the same trace length between PHY and MAC (including serial termination resistor). Tolerance +/- 0.5"

All RGMII signals in 3COM mode must have the same trace length between PHY and MAC (including serial termination resistor). Tolerance +/- 0.5"

Refer to DP83865DVH datasheet for layout instructions on RGMII HP mode (HP mode is not recommended).

RGMII only requires the following signals on the MAC interface:
RGMII_RDX0 - RGMII_RXD3 (on RXD0 - RXD3)
---RGMII_RCK (on RX_ER)
---RGMII_RXDV_ER (on RX_ER)
---RGMII_TXD0 - RGMII_TXD3 (on TXD0 - TXD3)
---RGMII_TCK (on GTX_CLK)
---RGMII_TXEN_ER (on TX_EN)
Other MAC interface signals may be removed from the design. Unused MAC interface pins should be left floating (outputs: RXD4 - RXD7, RX_CLK) or tied to ground (inputs: TXD4 - TXD7, TX_ER).

Series termination resistors are required for RGMII. May remove the resistors on signals not used in RGMII mode.

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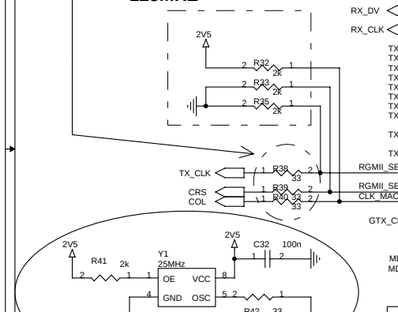
Note on MAC interface layout:

(See also "Note on recommended PCB Layer Stack-up".)
50 Ohm trace impedance recommended. The termination resistor values depend on actual PCB trace impedance. At 50Ohm impedance, use 33Ohm termination resistors.
Place resistors as close to chip as possible.

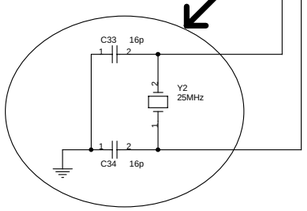
MAC interface configuration:

Strap options set for GMII and CLK_TO_MAC is 125MHZ

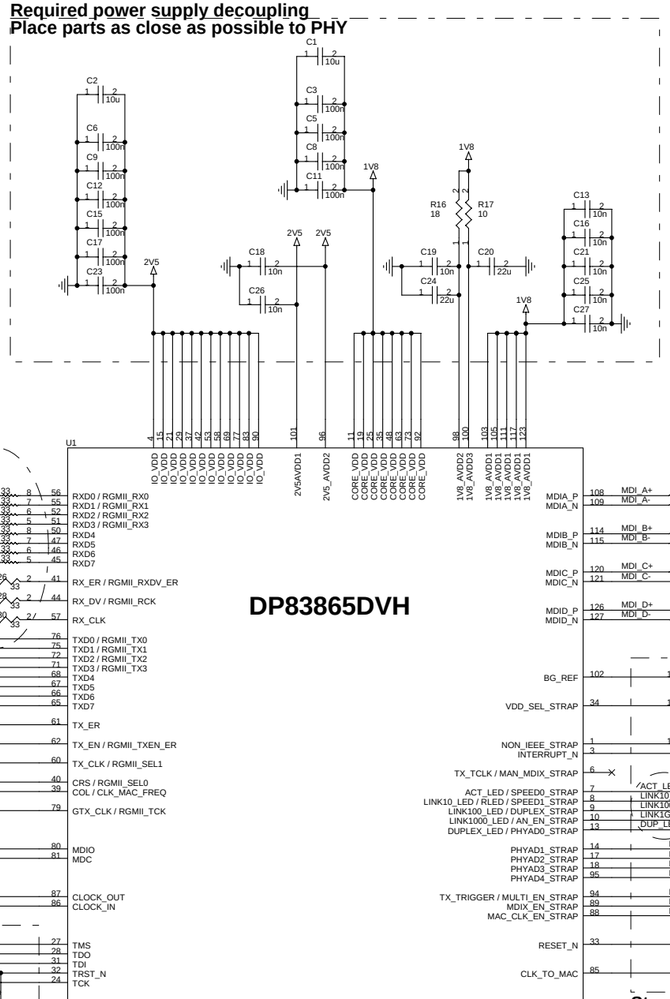


Use only one clock source. See datasheet on recommended Part No.

OR



Required power supply decoupling
Place parts as close as possible to PHY



Pull-down resistor on TRST_N always needed. If JTAG interface is not used, other pins can be left floating

MDI termination
Place close to chip

Strap options set for:

```
PHY-ID: 1
Auto-neg on
All speeds advertised
Auto-MDIX on
CLK_TO_MAC on
Non-IEEE mode off
VDD_IO 2.5V
```

If polarity of strap option changes, polarity of the LED must be changed as well!

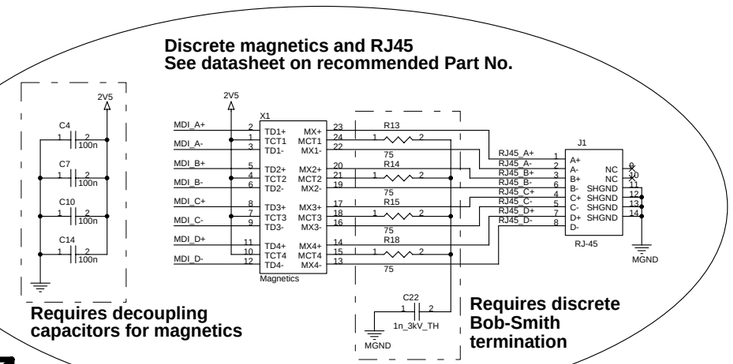
Note on MDI interface layout:

(See also "Note on recommended PCB Layer Stack-up" and "Note on Differential Pairs".)
100 Ohm differential trace impedance required. Traces must be routed differentially from PHY pins to magnetics and to RJ45 connector.
Must use controlled impendance on PCB.

Use only one connection. Do not place footprint for both. This is not an assembly option.

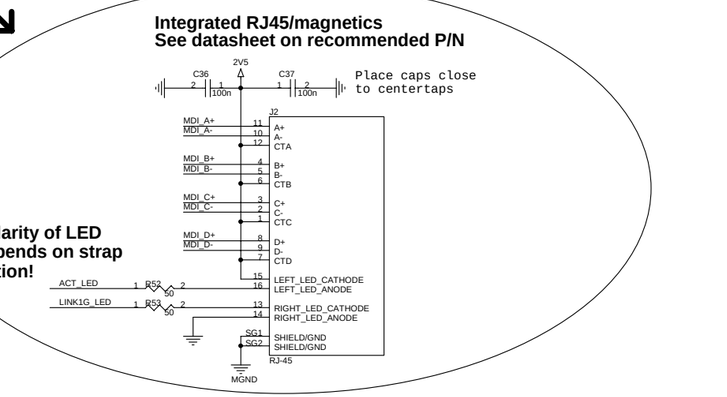
OR

Discrete magnetics and RJ45
See datasheet on recommended Part No.



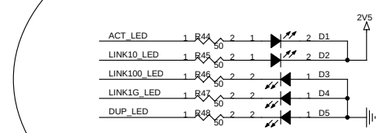
MGND is the chassis ground and must not be connected to the common ground plane of the PCB.

Integrated RJ45/magnetics
See datasheet on recommended P/N



Polarity of LED depends on strap option!

Available LED signals



Polarity of LED depends on strap option!

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