AM625 / AM623 Starter Kit SK (EVM) WITH TPS6521904 PMIC

TABLE OF CONTENTS

Revision Number

REV	A1
VER	0.12

R-Note:-

* Verify the DNI components configuration with respect to the SK schematics (Use PDF) after completion of board design before board assembly
* A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor
* Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)

KEY LINKS TO COLLATERALS

Hardware Design Guide :
https://www.ti.com/lit/an/sprad05b/sprad05b.pdf

Schematic Design and Review Checklist :
https://www.ti.com/lit/an/sprad21d/sprad21d.pdf

PMIC Power Solutions application note :
https://www.ti.com/lit/an/slvafd0b/slvafd0b.pdf

DDR Board Design and Layout Guidelines :
https://www.ti.com/lit/an/sprad06/sprad06.pdf

SKs (Starter Kits) for reference :
SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP

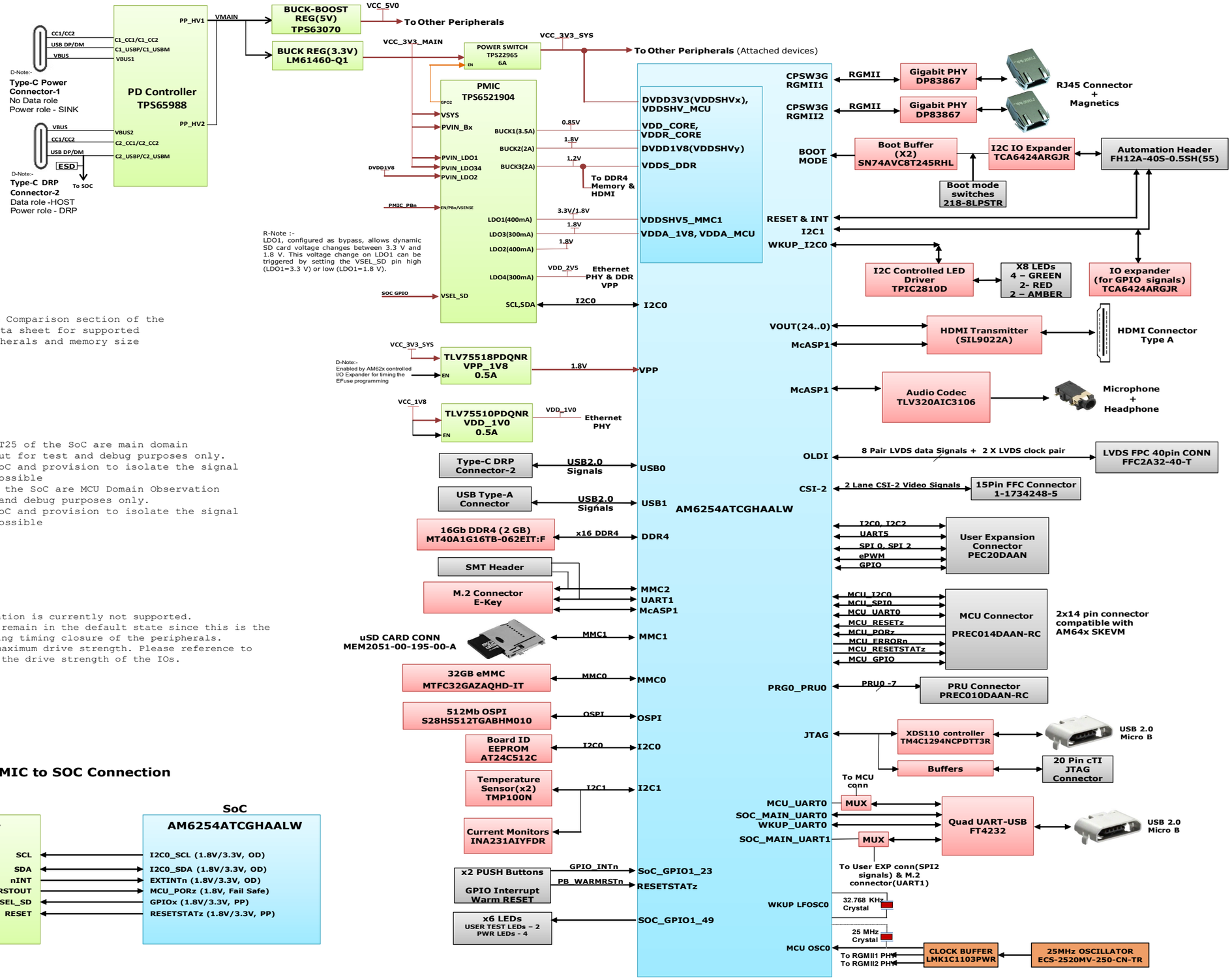
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	29 AUG 2022	Drafted from PROC142E1 Schematics. R651 value changed to 1K. DNI'd R618 and R676.Changed the I2C buffer parts to TCA9517DR. Changed the part SN74AVC4T245RSVR to SN74AVC4T245DGVR	Mistral Design Team		
0.02	08 SEP 2022	Added the second GPIO Expander U110 Part# TCA6408ARGTR	Mistral Design Team		
0.03	21 SEP 2022	Changed the Current monitors Res Filter values from 10E to 0E to the Sense pins.	Mistral Design Team		
0.04	19 OCT 2022	Added Testpoint to TEMP_DIODE_P pin of SoC. Changed the GPIO_OLDI_RSTn net name to GPIO_TS_RSTn.	Mistral Design Team		
0.05	24 OCT 2022	Changed the PMIC part from TPS6521903RHBR to TPS6521904RHBR. Mounted R699 and DNI'd R123. DNI'd the current monitor section of U36	Mistral Design Team		
0.06	3 Nov 2022	Changed the DDR4 part from MT40A1G16KD-062E IT:E to MT40A1G16TB-062E IT:F. Changed the eMMC part from MTFC16GAPALBH-IT to MTFC32GAZAQHD-IT.	Mistral Design Team		
0.07	15 Nov 2022	Removed the PMIC_STBY connection from SOC to PMIC.	Mistral Design Team		
0.08	22 Nov 2022	Added 2x 47uF on VCC_5V0. DNI'd C432, C433(10uF) and changed C415 to 4.7uF. Added 22pF CAP across R108	Mistral Design Team		
0.09	1 Dec 2022	Removed MMC2 connector section (J18) and associated resistors	Mistral Design Team		
0.10	11 APR 2023	Changed the HDMI external swing resistance to 7.5K. Added Standoff,Screw & Washer for M.2 connector. DNI'd R650 on SoC_USB1_DRVVBUS	Mistral Design Team		
0.11	16 MAY 2023	Depopulated Pull up of SOC_WLAN_IRQ_1V8 (R6)	Mistral Design Team		
0.12	20 MAY 2024	Updated SoC Part Number, Enabled Voltage ratings for all the capacitors and added Design Review notes Moved to DNI : R222, R650, C305, C303, C156, Q2, Y4 Moved to Mount : R319, R309, R318, R310, R306, R307, R308, R303, R538, R572 C86 - 1uF changed to 2.2uF ; C60 - 4.7uF changed to 1uF ; C46 - 0.1uF changed to 4.7uF ; C47,C389,C194,C12 - 1uF changed to 0.1uF ; C77, C33 - 4.7uF changed to 10uF ; C75,C79 - 9pF changed to 18pF ; C391,C14,C193 - 2.2uF changed to 1uF R651 - 1K_0.1% changed to Std 1K ; R404,R408 - 1K_0.1% changed to 1K_1% ; R89,R353,R354,R301,R302 - 22E_1% changed to 0E ; R12,R333 - 49.9K_1% changed to Std 10K ; R393,R475 - 10K_1% changed to Std 10K ; R315 - 100K changed to 10k	Mistral Design Team		

LINKS TO KEY FAQs

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1183910/faq-am625-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1184006/faq-am623-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-am62px-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1280721/faq-am625-am623-am625sip-am625-q1-am620-q1-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1332316/faq-am625-am623-custom-board-hardware-design---design-and-review-notes-for-reuse-of-sk-am62b-p1-schematics

BLOCK DIAGRAM



D-Note :-
Drive strength configuration is currently not supported.
The drive strength must remain in the default state since this is the only condition used during timing closure of the peripherals.
The devices are set to maximum drive strength. Please reference to the IBIS model to find the drive strength of the IOs.

PMIC to SOC Connection

Designed for TI by Mistral Solutions Pvt Ltd

Title	BLOCK DIAGRAM AM62x SKEVM		
Size	PROC142A1(002)	Rev	
C		A1	
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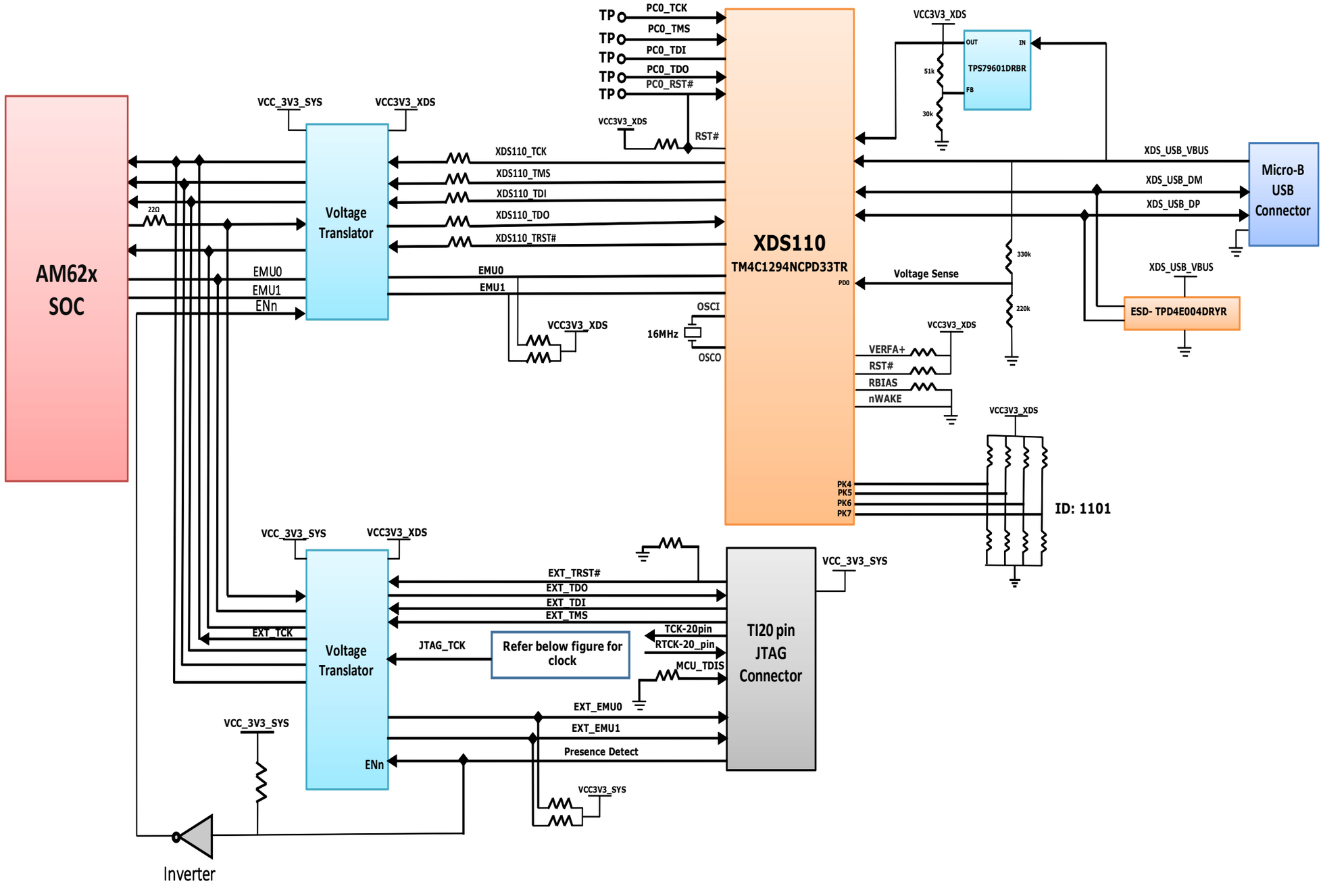
BLOCK DIAGRAM_XDS110

D-Note:-

Please follow SK-AM62P-LP implementations for latest updates on XDS110



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Title	BLOCK DIAGRAM_XDS110	
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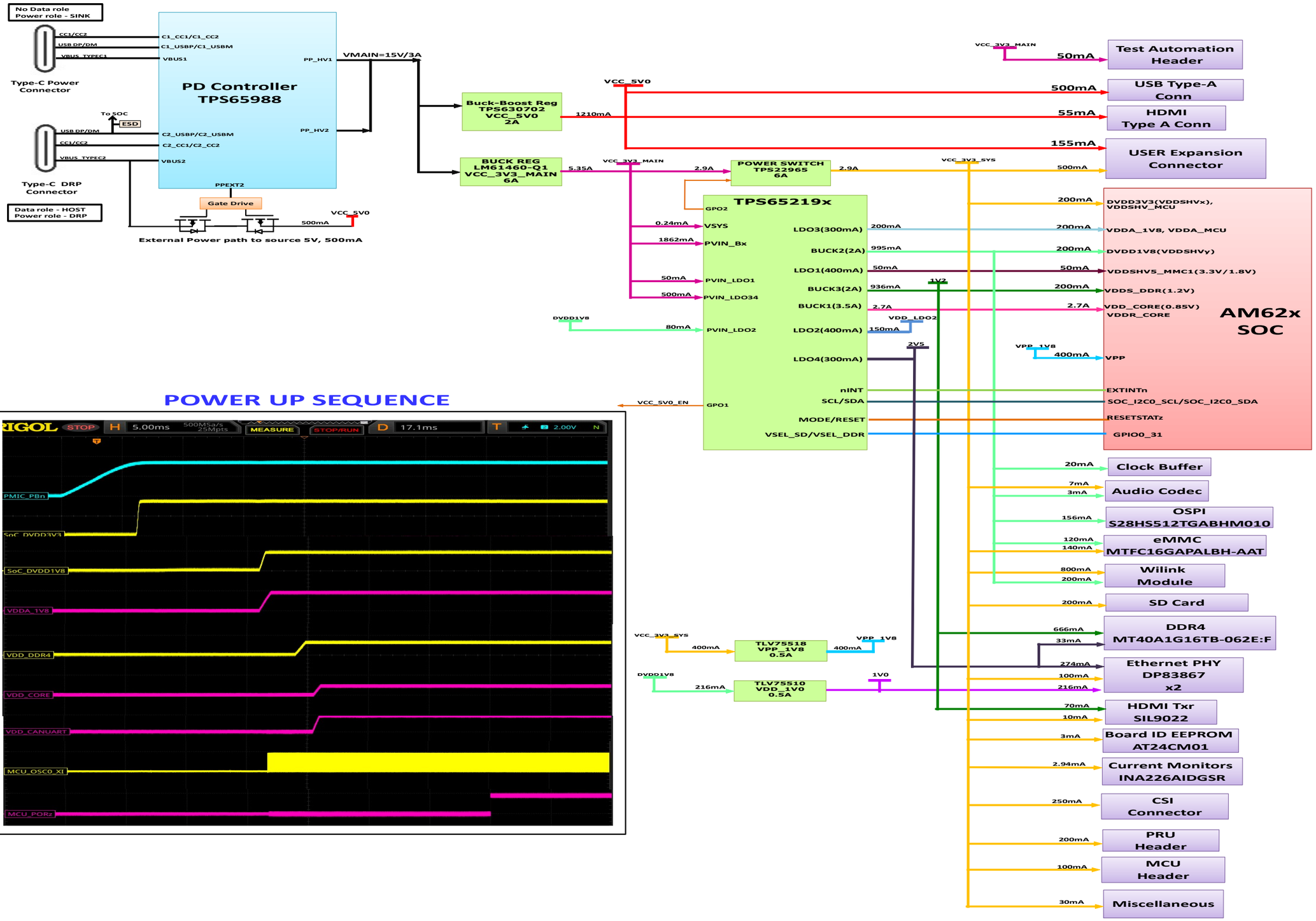
POWER BLOCK DIAGRAM



POWER UP SEQUENCE

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Title	POWER BLOCK DIAGRAM		
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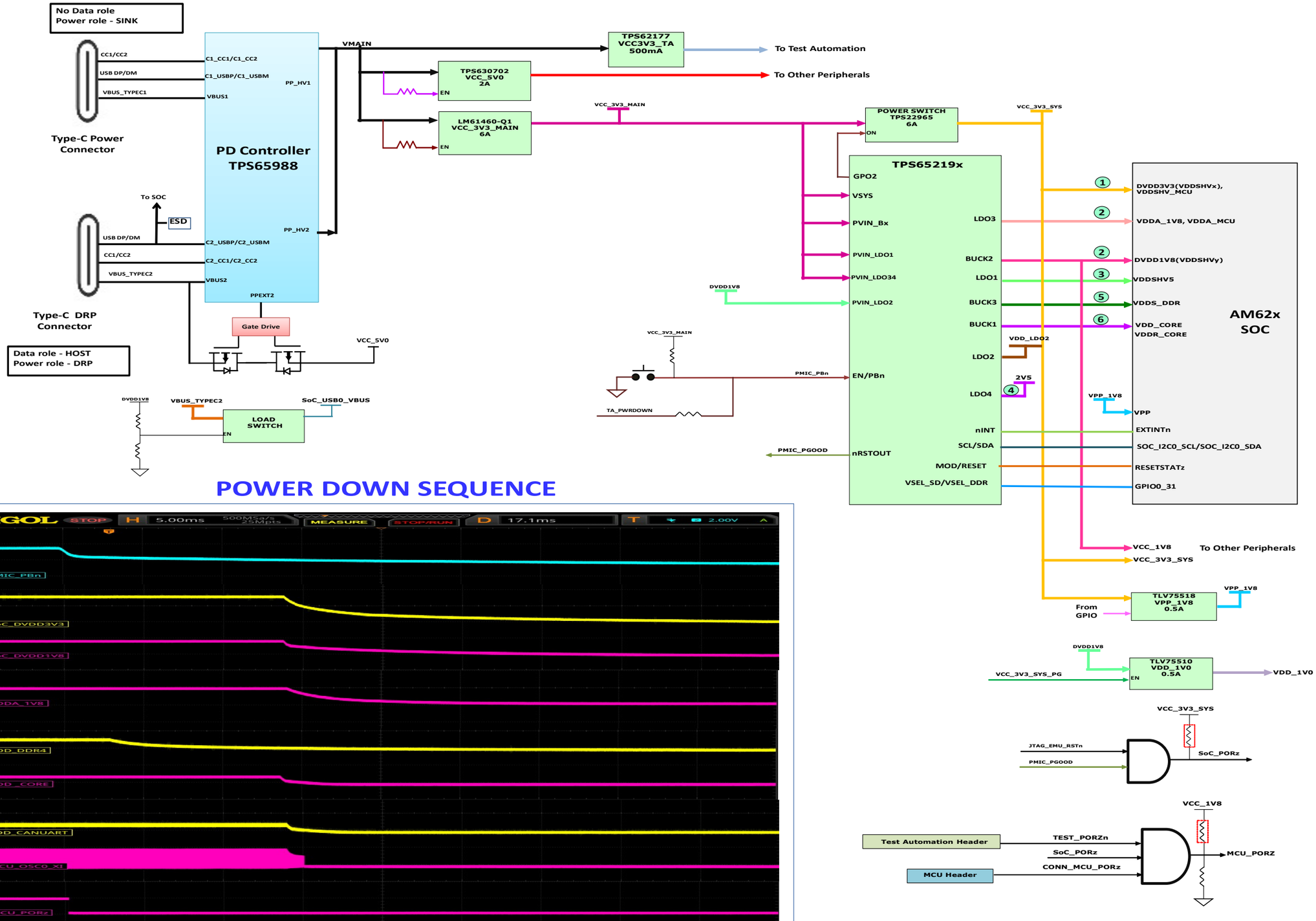
POWER SEQUENCE



POWER DOWN SEQUENCE

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Title	POWER SEQUENCE		
Size	PROC142A1(002)		Rev
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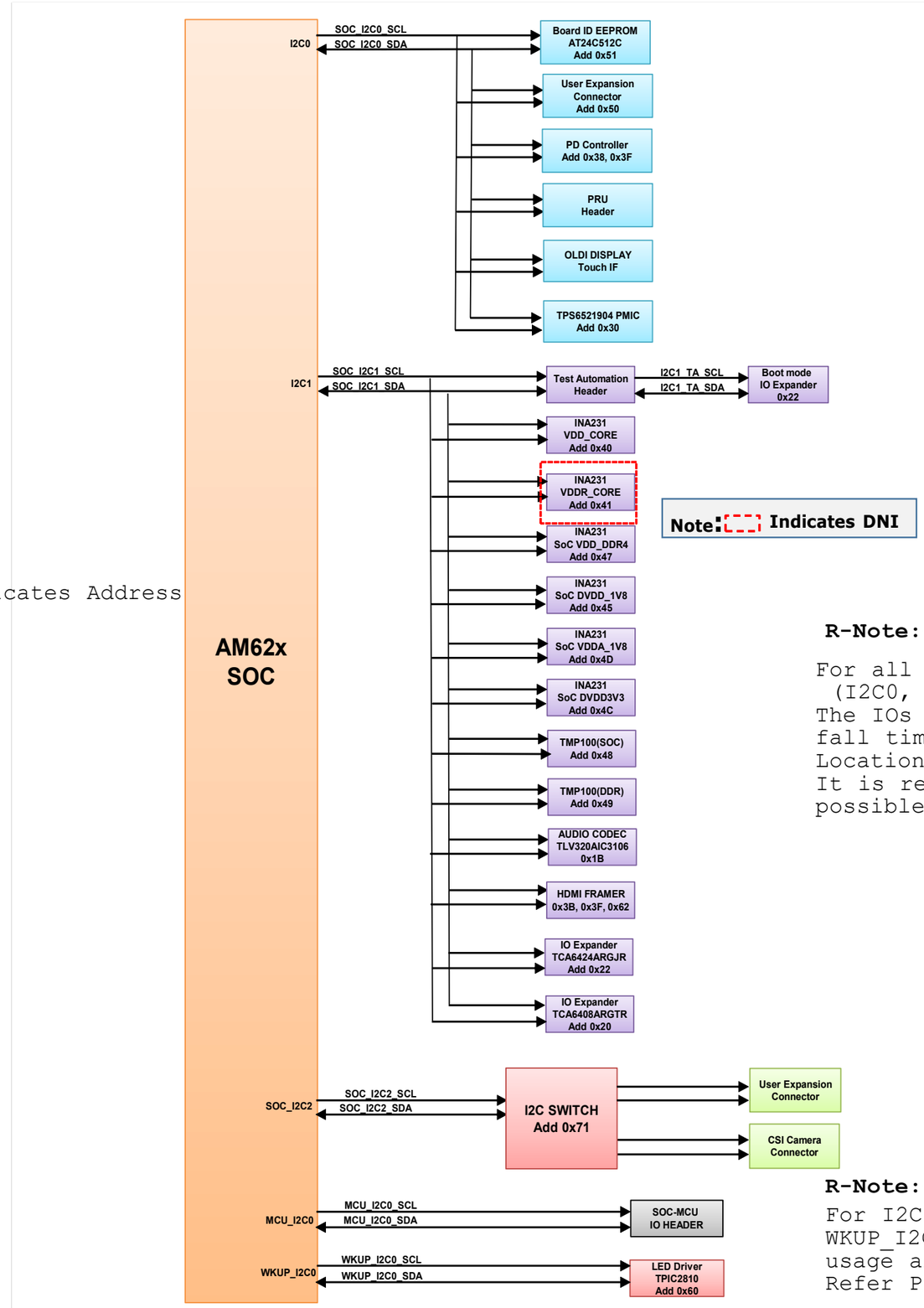
I2C TREE



R-Note
Add - Indicates Address

R-Note
Refer below section of the data sheet
Timing and Switching Characteristics
I2C Exceptions

R-Note:-

For all emulated open-drain output LVCMOS I2C interfaces.
(I2C0, I2C1, I2C2, I2C3) pullup resistors are recommended
The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification.
Location of the pullup is not a concern.
It is recommended to connect the pullups with the shortest possible stub

R-Note:-

For I2C interfaces with open-drain output type buffer (MCU_I2C0 and WKUP_I2C0), an external pullup is recommended irrespective of peripheral usage and IO configuration.
Refer Pin Connectivity Requirements section of SoC data sheet

GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	SoC_WLAN_EN_1V8	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	SoC_WLAN_IRQ_1V8	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC_3V3	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt PRU Connector Interrupt PMIC_INTn	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
	IO EXPANDER - 01									
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER -P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	M.2 Connector Alert	WLAN_ALERT_3V3	ALERT	IO EXPANDER – P10		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	M.2 Connector WAKEUP	BT_UART_WAKE_SOC_3V3	WAKEUP	IO EXPANDER – P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
	IO EXPANDER - 02									
1	M.2 Connector SDIO Reset Control GPIO	WLAN_SDIO_RST_3V3	RESET	IO EXPANDER – P0		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	OLDI Display Reset control	GPIO_TS_RSTn	RESET	IO EXPANDER – P1		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER – P2		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER – P3		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

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TEXAS INSTRUMENTS

MISTRAL

Title	GPIO MAPPING TABLE	
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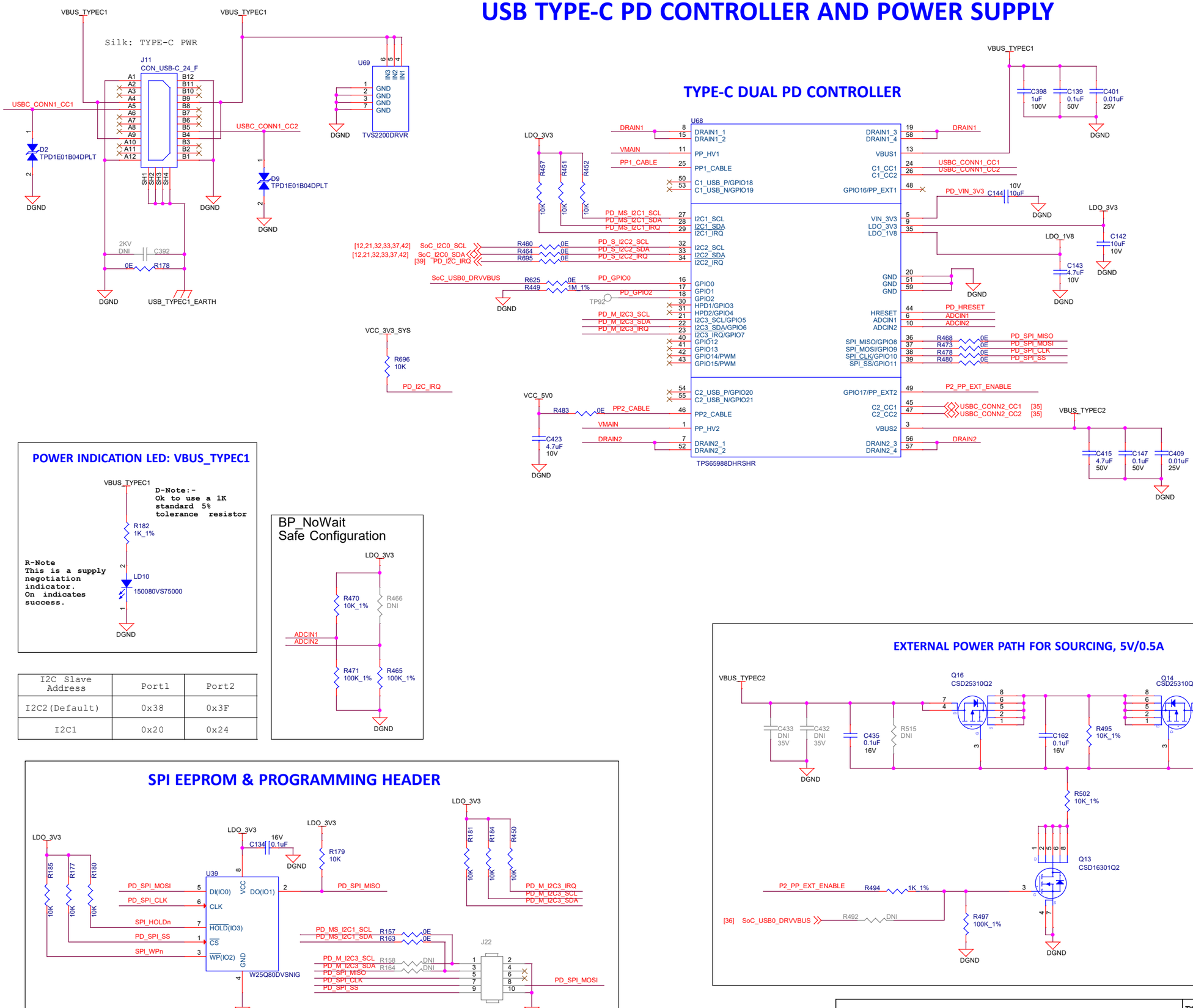
USB TYPE-C PD CONTROLLER AND POWER SUPPLY

TYPE-C DUAL PD CONTROLLER



POWER INDICATION LED: VBUS_TYPEC1

I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

SPI EEPROM & PROGRAMMING HEADER

EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A

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Title	USB TYPE-C POWER		
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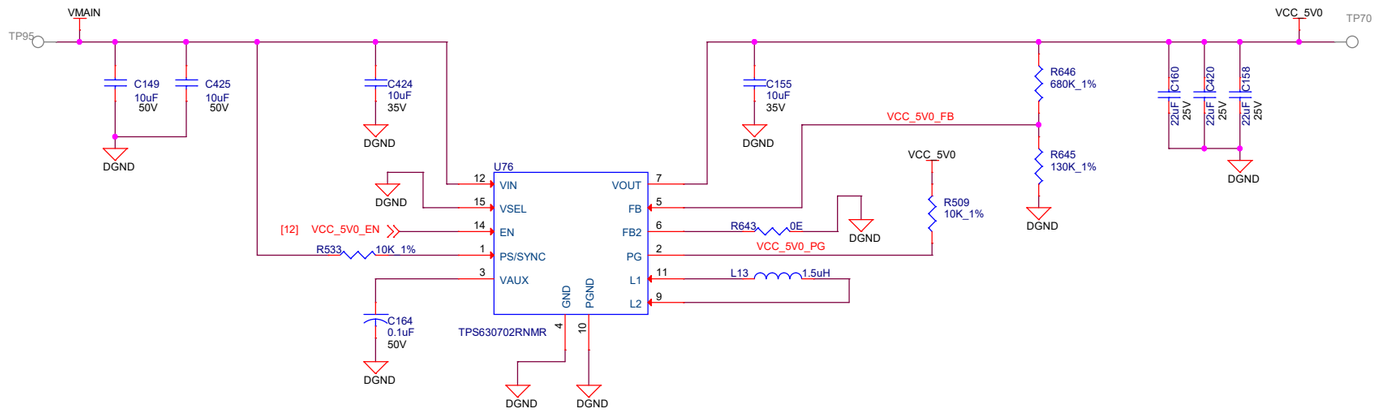
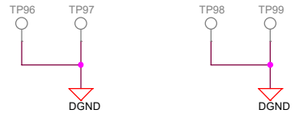
PERIPHERAL POWER SUPPLIES - 1



GROUND TEST POINTS



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Title	PERIPHERAL POWER SUPPLY -1	
Size: C	Variant Name = PROC142A1(002)	Rev: A1
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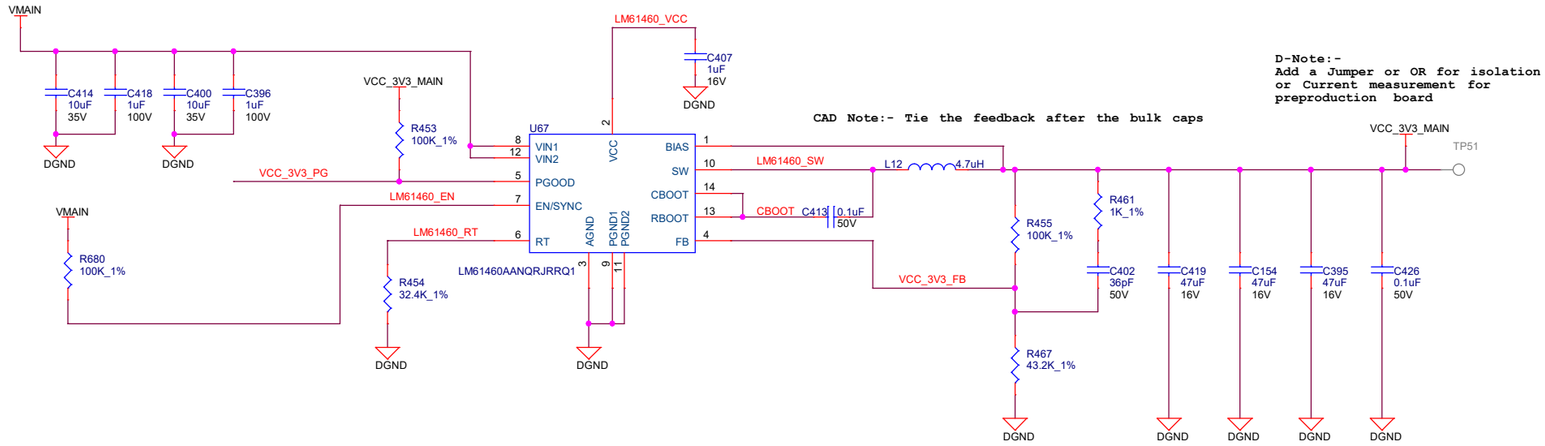
PERIPHERAL POWER SUPPLIES - 2

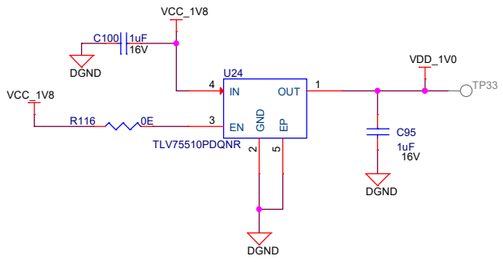
3.3V, 6.0 AMPS SUPPLY

VinMin = 4.5V
VinMax = 24V
Vout = 3.3V @ 6A



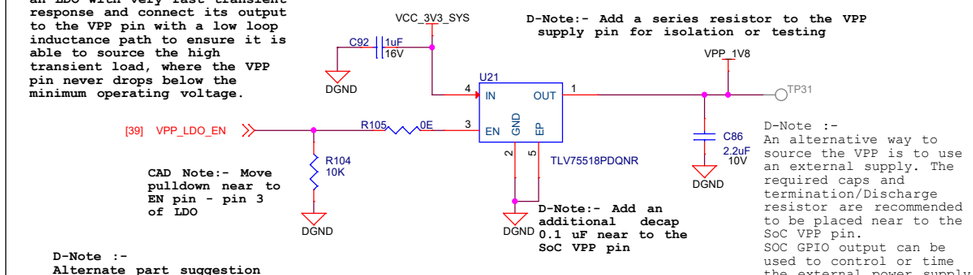
PERIPHERAL SUPPLY - ETHERNET PHY

1.0V, 0.5 AMPS



1.8V VPP, 0.5 AMPS SUPPLY

D-Note :-
It is very important to select an LDO with very fast transient response and connect its output to the VPP pin with a low loop inductance path to ensure it is able to source the high transient load, where the VPP pin never drops below the minimum operating voltage.



D-Note :-
Alternate part suggestion
TPS7A21-Q1, Automotive, 500mA, low-noise ultra-low-IQ high-PSRR low-dropout (LDO) voltage regulator

D-Note :-
Given the transient current requirement during eFuse programming, using load switch or FET switch may not be a recommended approach,
It is recommended to use an LDO. A load or FET switch is likely to have too much voltage drop that can't be compensated like when using an LDO.

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Title	PERIPHERAL POWER SUPPLY-2	
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SOC POWER SUPPLY PMIC
TPS6521904 PMIC

D-Note :-
Verify the PMIC data sheet for the recommended caps for the DC/DC and LDO outputs and provide the recommended caps

D-Note :-
Show the bulk caps connection for each of the DC/DC inputs separately
Add a 0.1 uF across the bulk caps
PVIN_B1_1, PVIN_B1_2 can share the same bulk cap

PMIC REGULATORS	VOLTAGE RAIL	CURRENT(mA)
BUCK 1	VCC_CORE(0.85V)	2700
BUCK 2	VCC_1V8	995
BUCK 3	VDD_1V2	936
LDO 1	VDDSHV_SDIO	50
LDO 2	VDD_LDO2	150
LDO 3	VDDA1V8	200
LDO 4	VDD_2V5	300

R-Note :-
Refer PMIC data sheet and schematics review checklist for reviewing the implementation of PMIC section

D-Note
Add a 0R resistor or Jumper at the output of the DC/DC for isolation or testing

SILK SCREEN :
TP45 - VCC_CORE (configured to 0.85V)
TP41 - VCC_1V8
TP40 - VDD_1V2
TP29 - VDDSHV_SDIO
TP42 - VDD_2V5

Devices Powered : HDMI interface DDR

Devices Powered : Ethernet PHY DDR

R-Note
SD card interface IO supply voltage switching (3.3V/1.8V) is required to support higher speed data rates
Refer SOC data sheet for supported rates and IO voltage levels

CAD Note:- Tie the feedback after the DC/DC output bulk caps

I2C ADDRESS: 0x30

SOC 3.3V IO SUPPLY

VCC_3V3_SYS LOAD SWITCH

D- Note:- Add a cap (220 pF or Higher) to the CT pin for SoC IO supply slew rate control.
SoC IO supplies have slew rate requirements specified

PMIC ON/OFF PUSH BUTTON LOGIC

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Title	SOC POWER SUPPLY	
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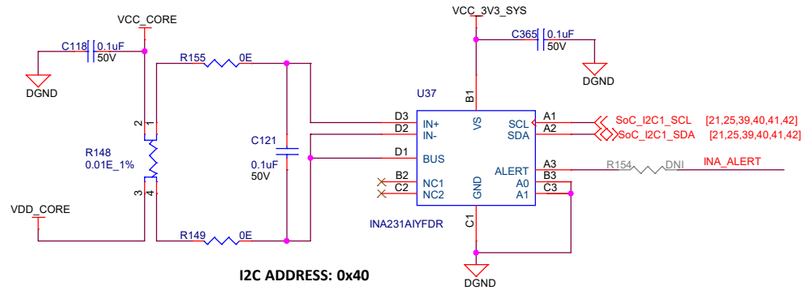
CURRENT MONITORING DEVICES

D-Note:- Note the supply rail name change across the shunt when optimizing the design (Deleting the current sense resistor)

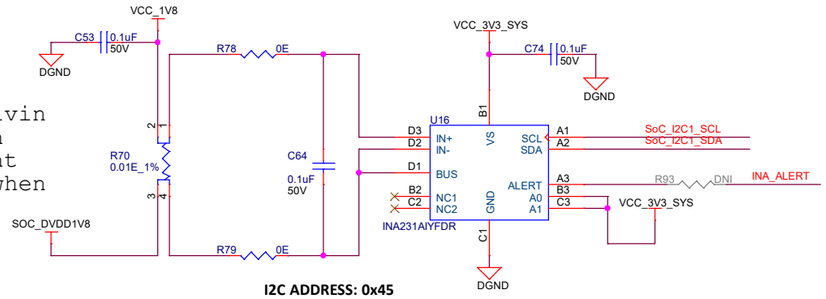
VDD_CORE



I2C ADDRESS: 0x40

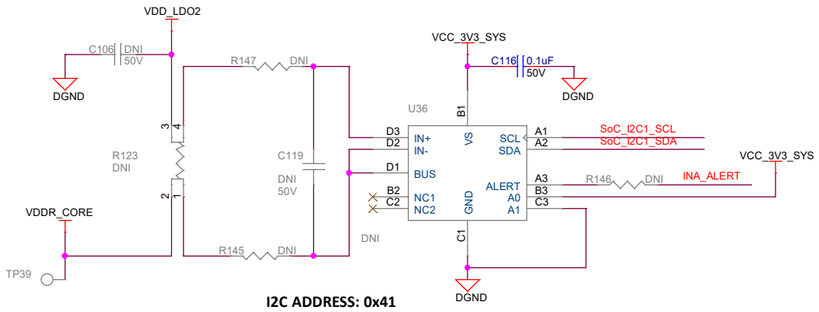
SoC_DVDD1V8

CAD Note:
Follow Kelvin connection for Current Sensing when using 2 terminal resistors



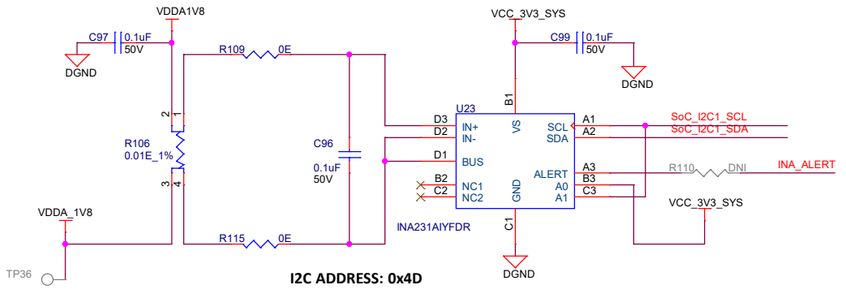
I2C ADDRESS: 0x45

VDDR_CORE



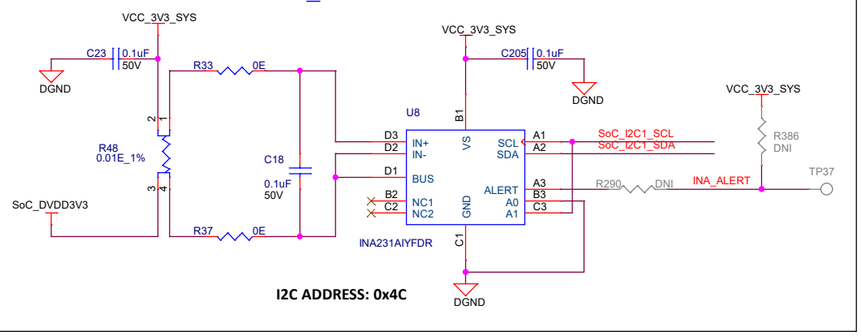
I2C ADDRESS: 0x41

VDDA_1V8



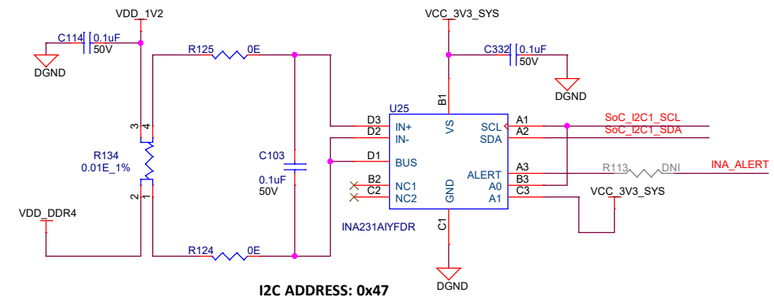
I2C ADDRESS: 0x4D

SoC_DVDD3V3



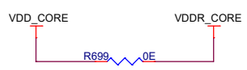
I2C ADDRESS: 0x4C

VDD_DDR4



I2C ADDRESS: 0x47

D-Note :-
RES Option to short VDD_CORE and VDDR_CORE rails when both are 0.85V(Both should be generated from the same source)



CORE SUPPLY	ARRAY CORE SUPPLY	Assembly
0.75 VDD_CORE	0.85 VDDR_CORE	DNI R699 and Mount R123
0.85 VDD_CORE	0.85 VDDR_CORE	DNI R123 and Mount R699

INA I2C SLAVE ADDRESS

POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V2_DDR	VDD_DDR4	47

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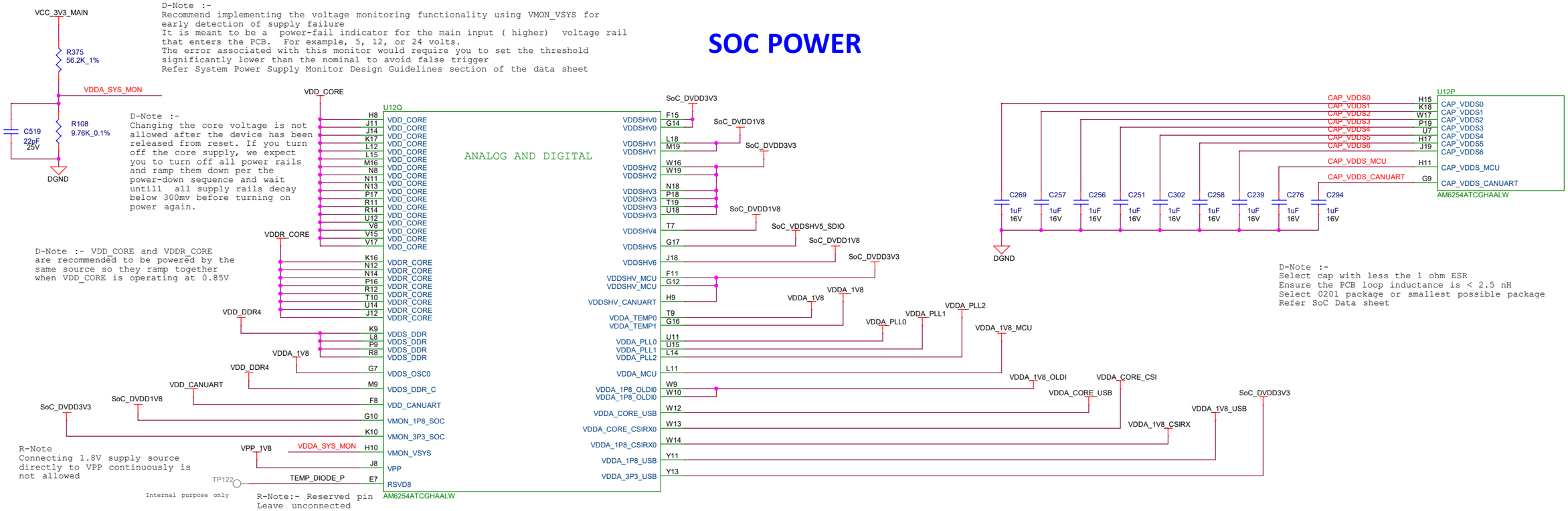
TEXAS INSTRUMENTS MISTRAL

Title	CURRENT MONITORING DEVICES	
Size C	PROC142A1(002)	Rev A1
Date: Monday, May 20, 2024	Sheet 13 of 44	

SOC POWER

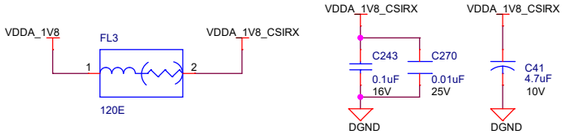
D-Note :-
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure
It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts.
The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid false trigger
Refer System Power Supply Monitor Design Guidelines section of the data sheet

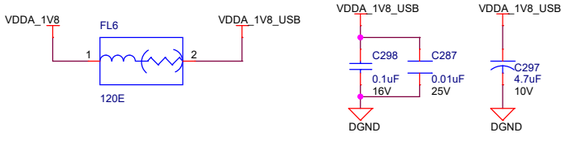


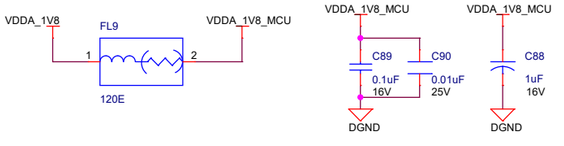
D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used.
It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen.
Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

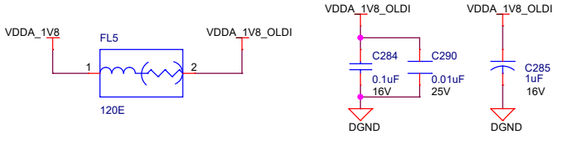
D-Note :-
Refer Pin connectivity requirements to connect the CSI0 supplies (analog and core) when CSI0 interface is not used
Ferrite and Bulk Caps are optional when CSI0 is not used and Boundary scan functionality is required

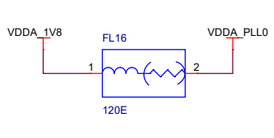
1.8V ANALOG SUPPLIES

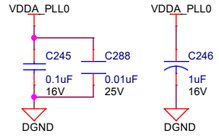


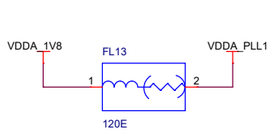


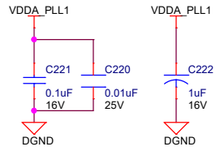


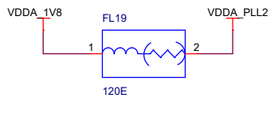


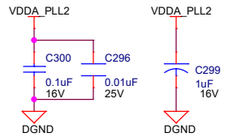








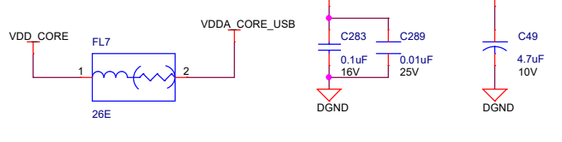


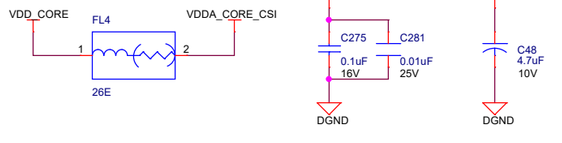


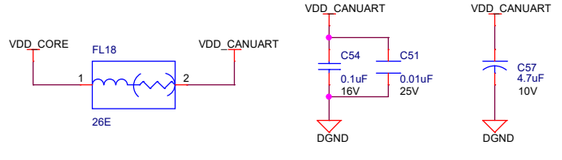
D-Note :-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IOs
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise.
A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the highest impedance end of the signal.
By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

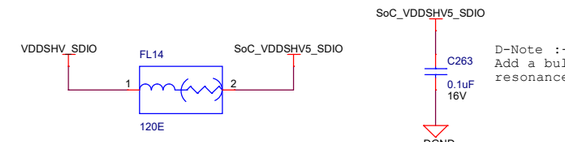
CORE SUPPLIES







3.3V/1.8V MMC1 SUPPLY



D-Note :-
Add a bulk cap 1 uF to minimize resonance

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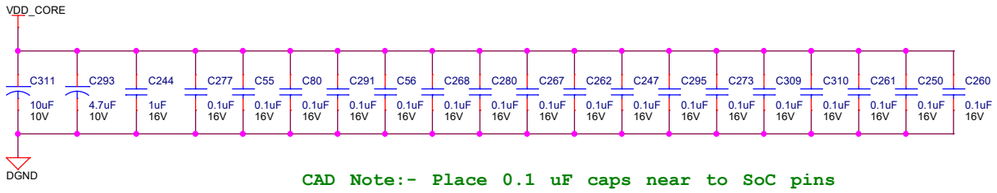
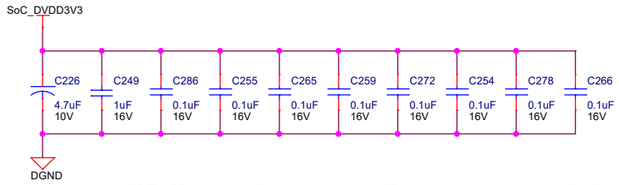
Title	SOC POWER	
Size: C	Variant Name = PROC142A1(002)	Rev: A1
Date: Monday, May 20, 2024	Sheet 14 of 44	

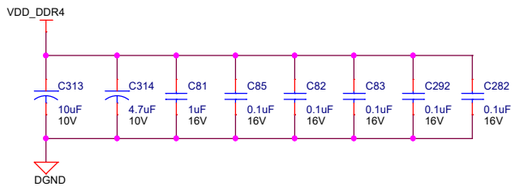
SOC POWER SUPPLIES - DECAPS

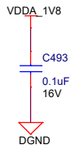


CAD Note:- Place 0.1 uF caps near to SoC pins

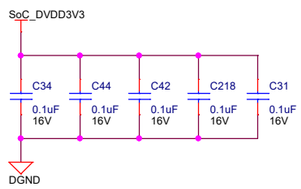


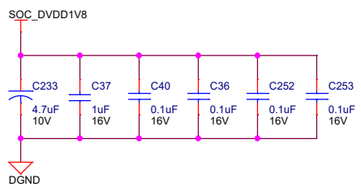
CAD Note:- Place 0.1 uF caps near to SoC pins



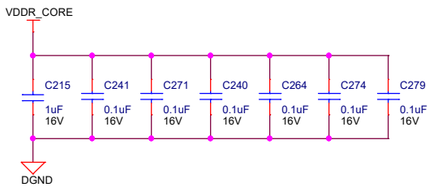


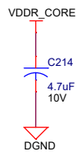
CAD Note:- Place 0.1 uF caps near to SoC pins





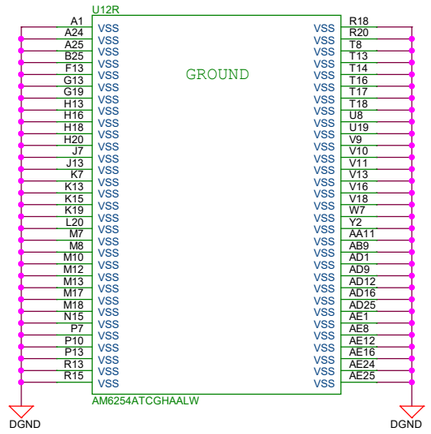
CAD Note:- Place 0.1 uF caps near to SoC pins





CAD Note:- Place 0.1 uF caps near to SoC pins

SOC VSS



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Title	SOC POWER CAPS & SOC VSS	
Size C	Variant Name = PROC142A1(002)	Rev
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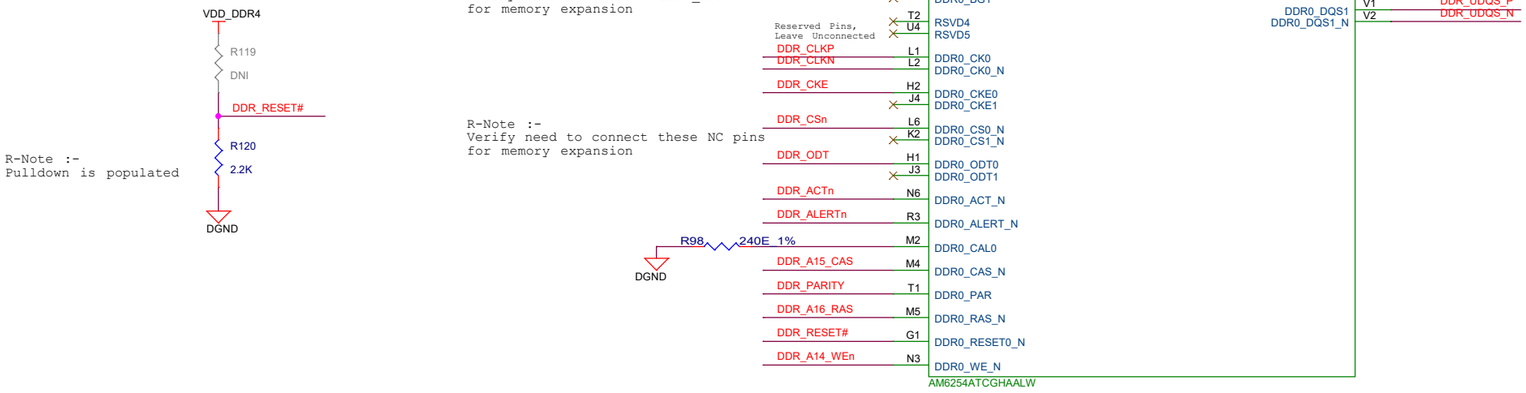
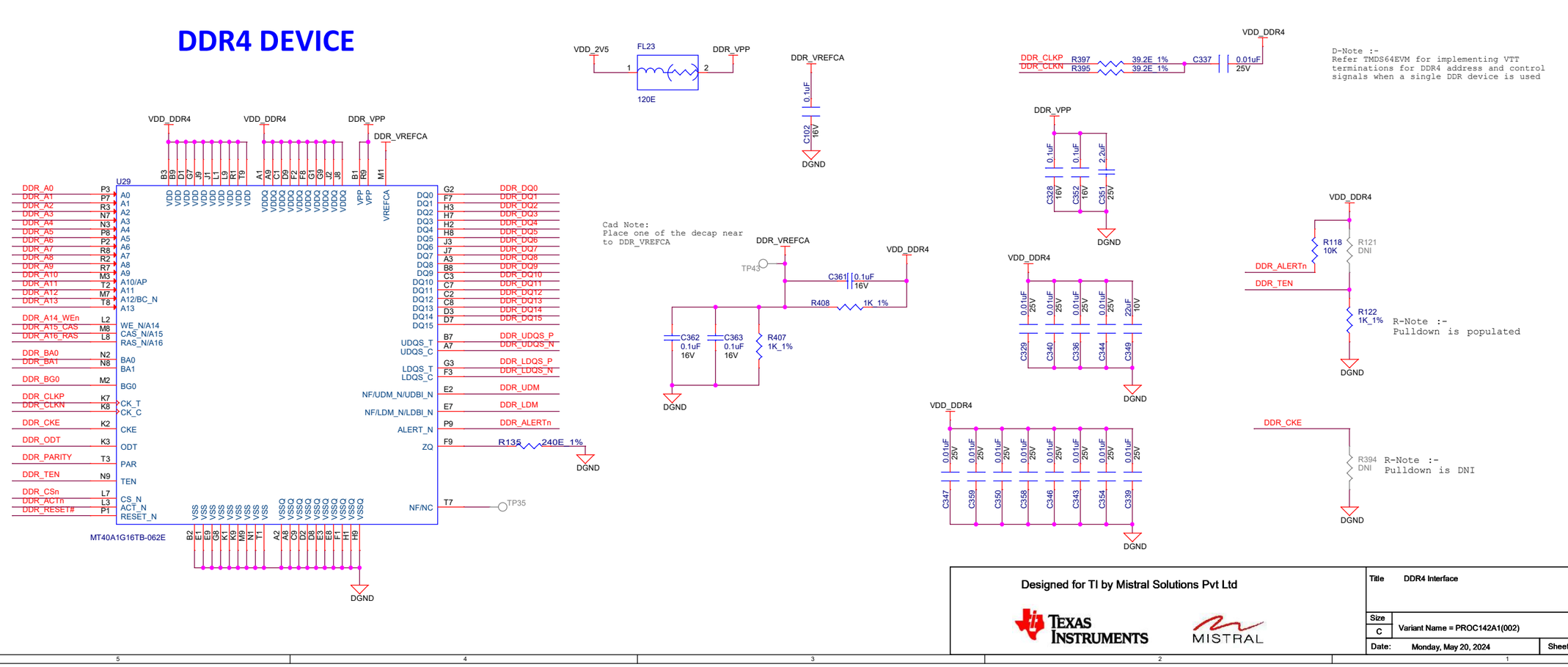
SOC DDR4 INTERFACE



DDR4 DEVICE



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Title	DDR4 Interface	
Size C	Variant Name = PROC142A1(002)	Rev A1
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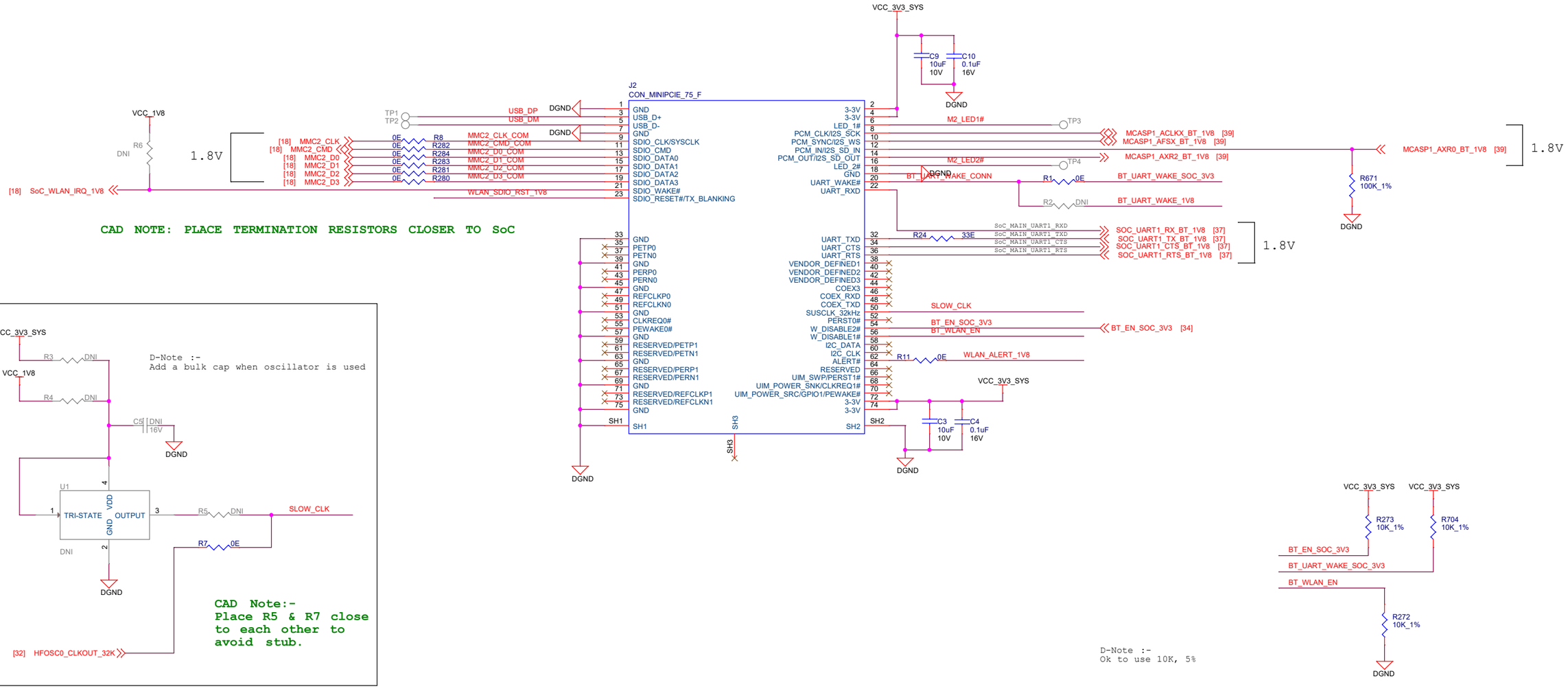
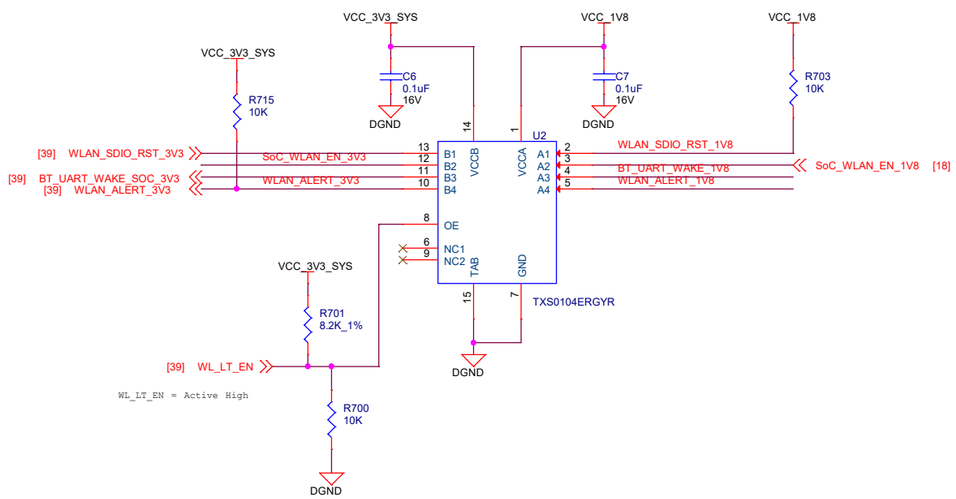
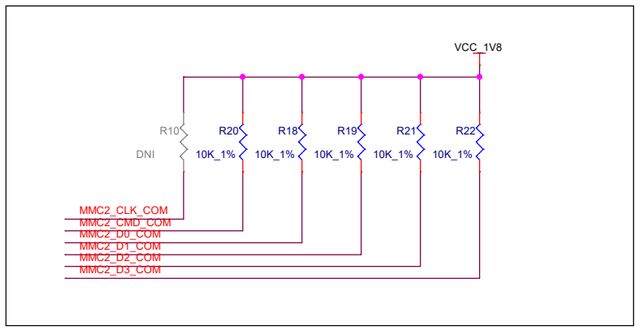
M.2 INTERFACE







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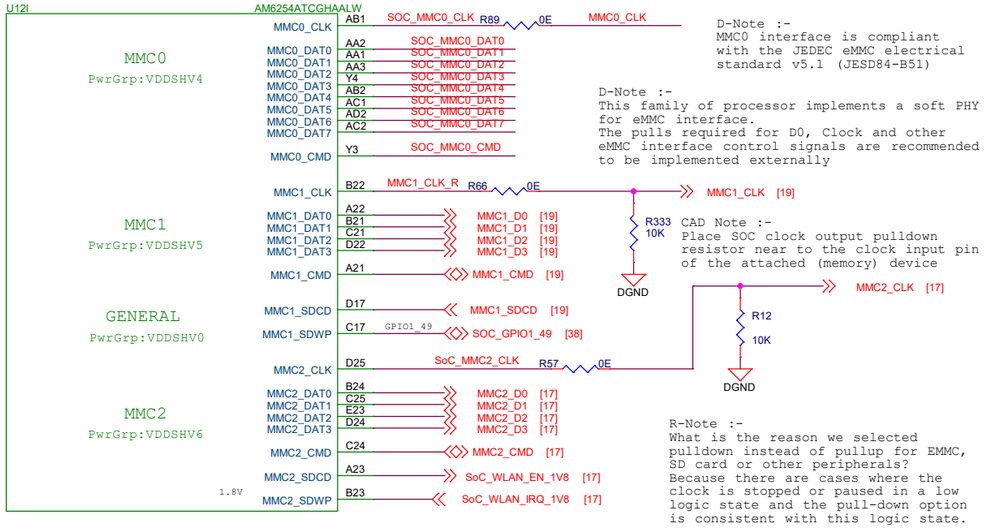
Title	M.2 CONNECTOR	
Size: C	PROC142A1(002)	Rev: A1
Date: Monday, May 20, 2024	Sheet 17 of 44	

SOC - MMC Interface



D-Note :-
0E provision on MMC0_CLK
Helps improve signal integrity

D-Note :-
MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)

D-Note :-
This family of processor implements a soft PHY for eMMC interface.
The pulls required for D0, Clock and other eMMC interface control signals are recommended to be implemented externally

CAD Note :-
Place SOC clock output pulldown resistor near to the clock input pin of the attached (memory) device

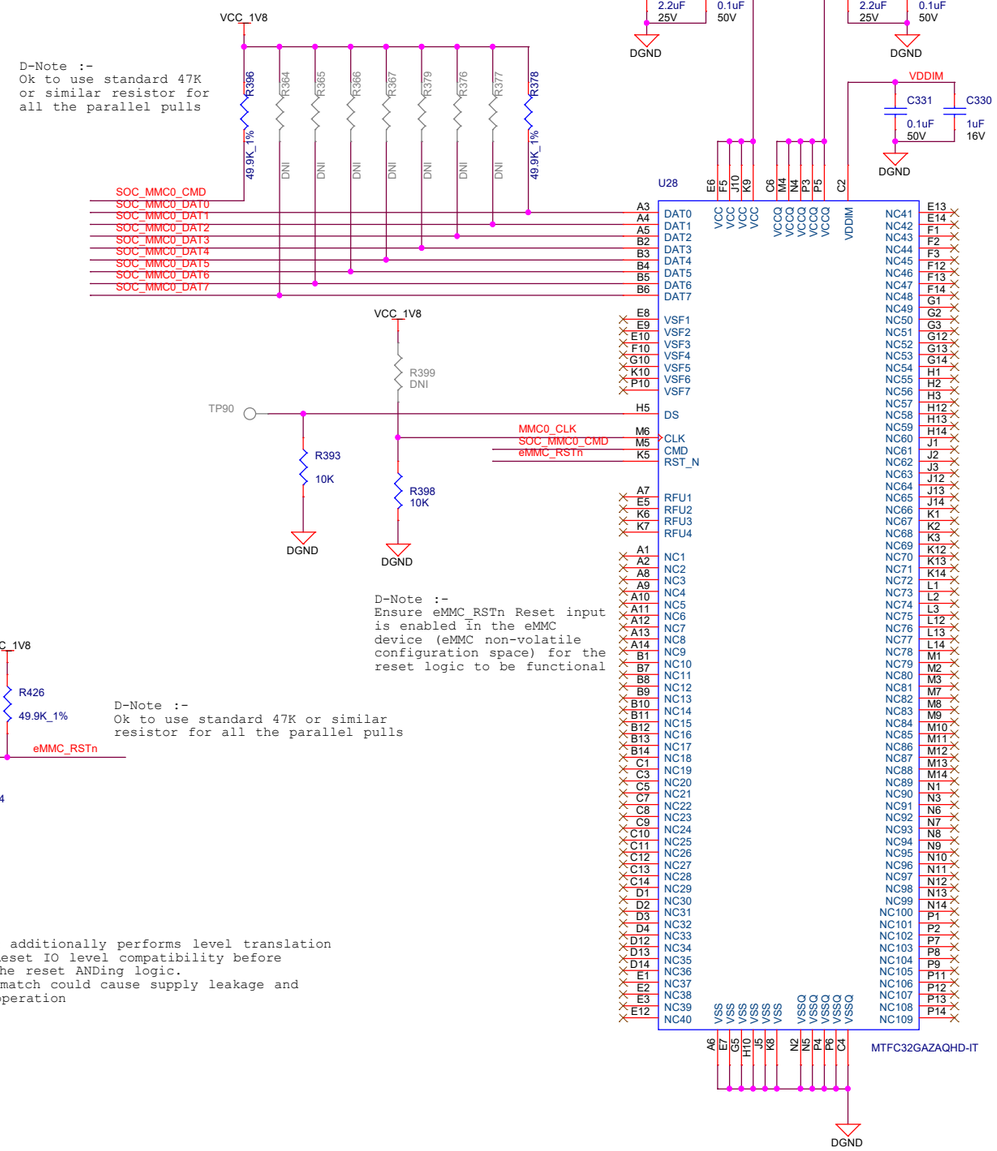
R-Note :-
What is the reason we selected pulldown instead of pullup for EMMC, SD card or other peripherals?
Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

eMMC FLASH

D-Note :-
For D7..D1 eMMC device is expected to have the pullups enabled by default.
The eMMC host/phy disables the eMMC device pullups and enables SOC internal pullups.
Provision for external pullups is optional or the pullups can be deleted.

D-Note :-
Add additional decaps as required
Refer SK-AM62P-LP schematics

D-Note :-
Ok to use standard 47K or similar resistor for all the parallel pulls



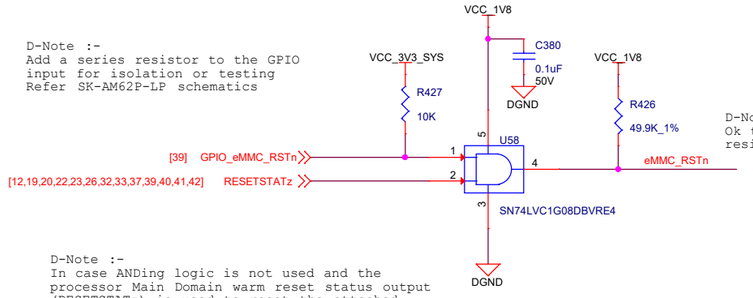
D-Note :-
Ensure eMMC_RSTn Reset input is enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional

eMMC FLASH RESET

D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDI or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note :-
You could eliminate the GPIO option and only use the reset output (Warm or Cold), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics



D-Note :-
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level.A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected.If too high the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If too low it will cause the AM62x to source too much steady-state current during normal operation.

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

D-Note :-
Ok to use standard 47K or similar resistor for all the parallel pulls

Designed for TI by Mistral Solutions Pvt Ltd

Title	eMMC FLASH INTERFACE	
Size C	PROC142A1(002)	Rev A1
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SD CARD INTERFACE

D-Note :-
This power switch, along with the power switch supply reset logic, and the host IO power supply circuit is required to support UHS-I SD Cards which begins communications using 3.3V signal levels and later change to 1.8V signal levels when changing to one of the faster data transfer speeds.
Cycling power to the SD Card is the only way to put it back into 3.3V mode since SD Cards do not have a reset pin.
The host IO power supply must power off/on and change voltage at the same time as the SD Card. These circuits and the software driver operating the signals sourcing these circuits ensure both devices are off, or on and operating at the same IO voltage at the same time.

SD CARD LOAD SWITCH RESET LOGIC

D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

[39] MMC1_SD_EN
[12,18,20,22,23,26,32,33,37,39,40,41,42] RESETSTATz
[22,23,26,42] PORz_OUT

VCC_3V3_SYS
R117 10K
C94 0.1uF 50V
DGND
U22
SN74LVC1G11DRYR
R374 10K
MMC1_SD_LS_EN

D-Note :-
Anding logic could be optimized to 2 input AND gate
Use RESETSTATz and the SoC IO as inputs

LOAD SWITCH

VCC_3V3_SYS
C47 0.1uF 25V
C46 4.7uF 16V
U13
TPS22918DBVR
VIN VOUT ON CT GND QOD
VDD_MMC1
FL8 120E
VDD_MMC1_SD
C60 1uF 25V

D-Note :-
CT - Add a 220 pF or higher cap for SD card supply slew rate control

D-Note :-
For UHS-I operation, the pullups are recommended to be connected to the 3.3V/1.8V switched LDO output

Note :-
MMC1_CLK pullup is a DNI

D-Note :-
Ensure internal pullups are not configured when 10K external pullups are used. As a good design practice, a 47K pullup is recommended to ensure the pullup value is within the SD card specification, when internal pulls are enabled unexpectedly. This way the resulting pull resistance will still be within the specified.

VDDSHV_SDIO
R92 10K
R91 10K
R81 10K
R80 10K
R90 DNI
R82 10K
VCC_3V3_SYS
R96 10K
C66 0.1uF 50V
C65 2.2uF 25V

[18] MMC1_D0
[18] MMC1_D1
[18] MMC1_D2
[18,19] MMC1_D3
[18] MMC1_CLK
[18] MMC1_CMD
[18] MMC1_SDCD

J20
MMC1_D0 7 DAT0
MMC1_D1 8 DAT1
MMC1_D2 1 DAT2
MMC1_D3 2 CD/DAT3
MMC1_CLK 5 CLK
MMC1_CMD 3 CMD
MMC1_SDCD 9 CD
4 VDD
6 VSS
SH1 SH2 SH3 SH4
CON_SDCARD9_MEM2051-00-195-00-A

U15
TPD6E001RSER
IO1 IO2 IO3 IO4 IO5 IO6 VCC GND NC1 NC2
C72 0.1uF 50V

U18
TPD2E001DRLR
IO1 IO2 VCC GND NC

D-Note :-
Add a filter cap

CAD Note :-
Place near SD Card Connector

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Title	SD CARD INTERFACE	
Size C	PROC142A1(002)	Rev A1
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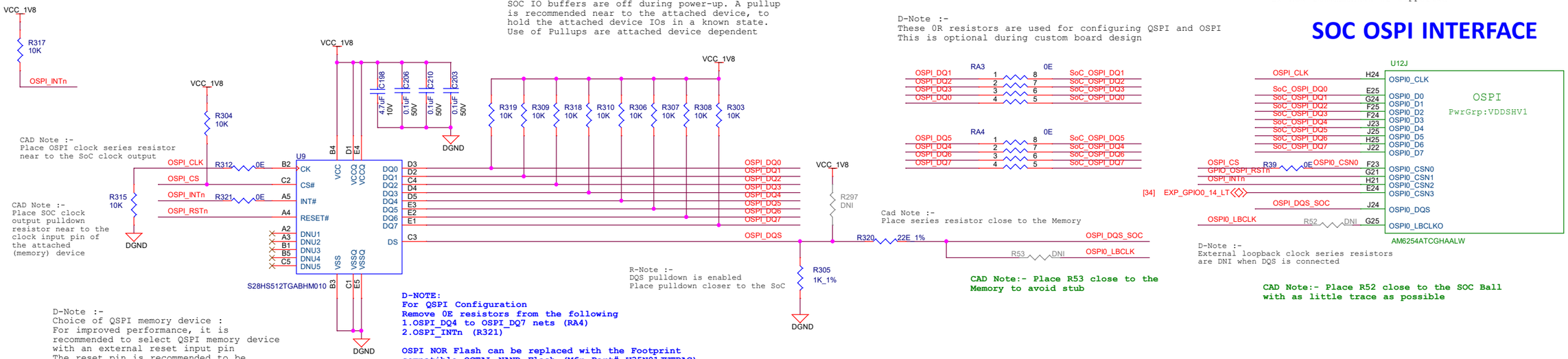
OSPI FLASH

R-Note
SOC IO buffers are off during power-up. A pullup is recommended near to the attached device, to hold the attached device IOs in a known state. Use of Pullups are attached device dependent

D-Note :-
These 0R resistors are used for configuring QSPI and OSPI
This is optional during custom board design

D-Note :-
Connecting OSPI interface to multiple devices is not recommended or supported

SOC OSPI INTERFACE

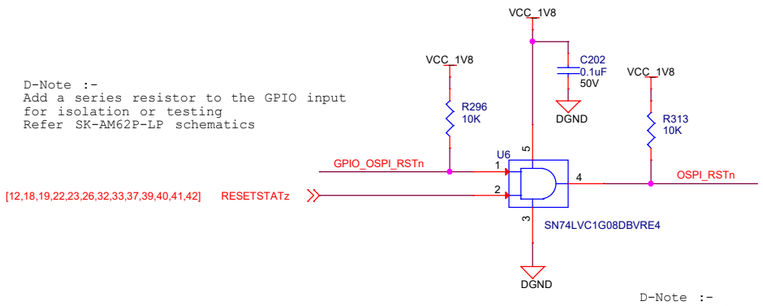


D-Note :-
Choice of QSPI memory device :
For improved performance, it is recommended to select QSPI memory device with an external reset input pin
The reset pin is recommended to be controlled using SOC reset status output or an ANDing logic as implemented in the starter kit

D-NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (RA4)
2.OSPI_INTn (R321)

OSPI NOR Flash can be replaced with the Footprint compatible OCTAL NAND Flash (Mfr Part# W35N01JWTBAG)

OSPI FLASH RESET



D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

Designed for TI by Mistral Solutions Pvt Ltd

Title	OSPI INTERFACE	
Size C	PROC142A1(002)	Rev A1
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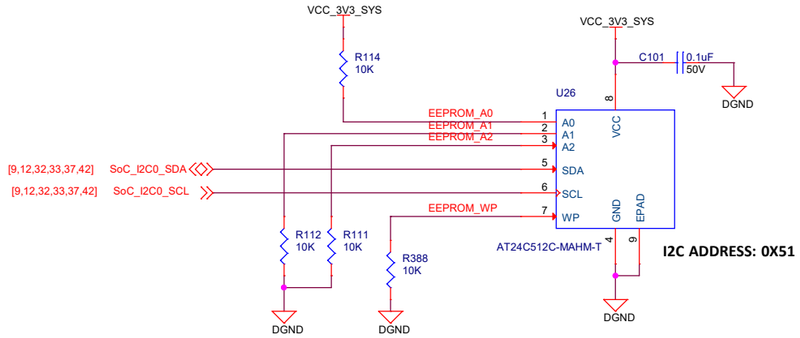
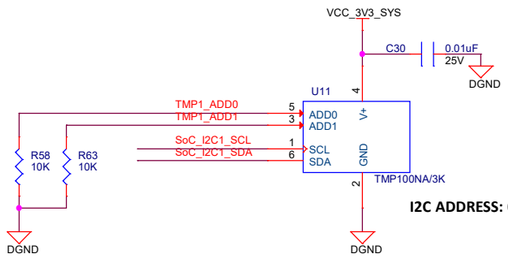
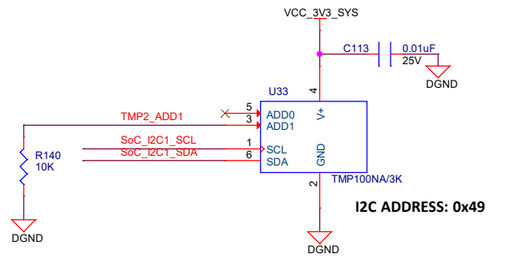
BOARD ID EEPROM



DIGITAL TEMPERATURE SENSORS





CAD NOTE: PLACE TEMP SENSOR CLOSE TO SoC

CAD NOTE: PLACE TEMP SENSOR CLOSE TO DDR4

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOARD ID EEPROM & TEMPERATURE SENSORS	
Size: C	PROC142A1(002)	Rev: A1
Date: Monday, May 20, 2024	Sheet 21 of 44	

CPSW3G RGMII 1 - ETHERNET PHY

D-Note :-
The caps and values used are as per the EPHY data sheet recommendations

D-Note :-
Refer to DP83867ERGZ-R-EVM when using LAN Discrete Transformer Module and RJ45 connector

R-Note :-
Ferrite is DNI

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-
Provide provision for Series resistor based on EPHY for RX signals near to EPHY

D-Note :-
XI clock Input amplitude allowed is 1.8V irrespective of the IO supply
Use a CAP DIVIDER when the clock amplified is 3.3V

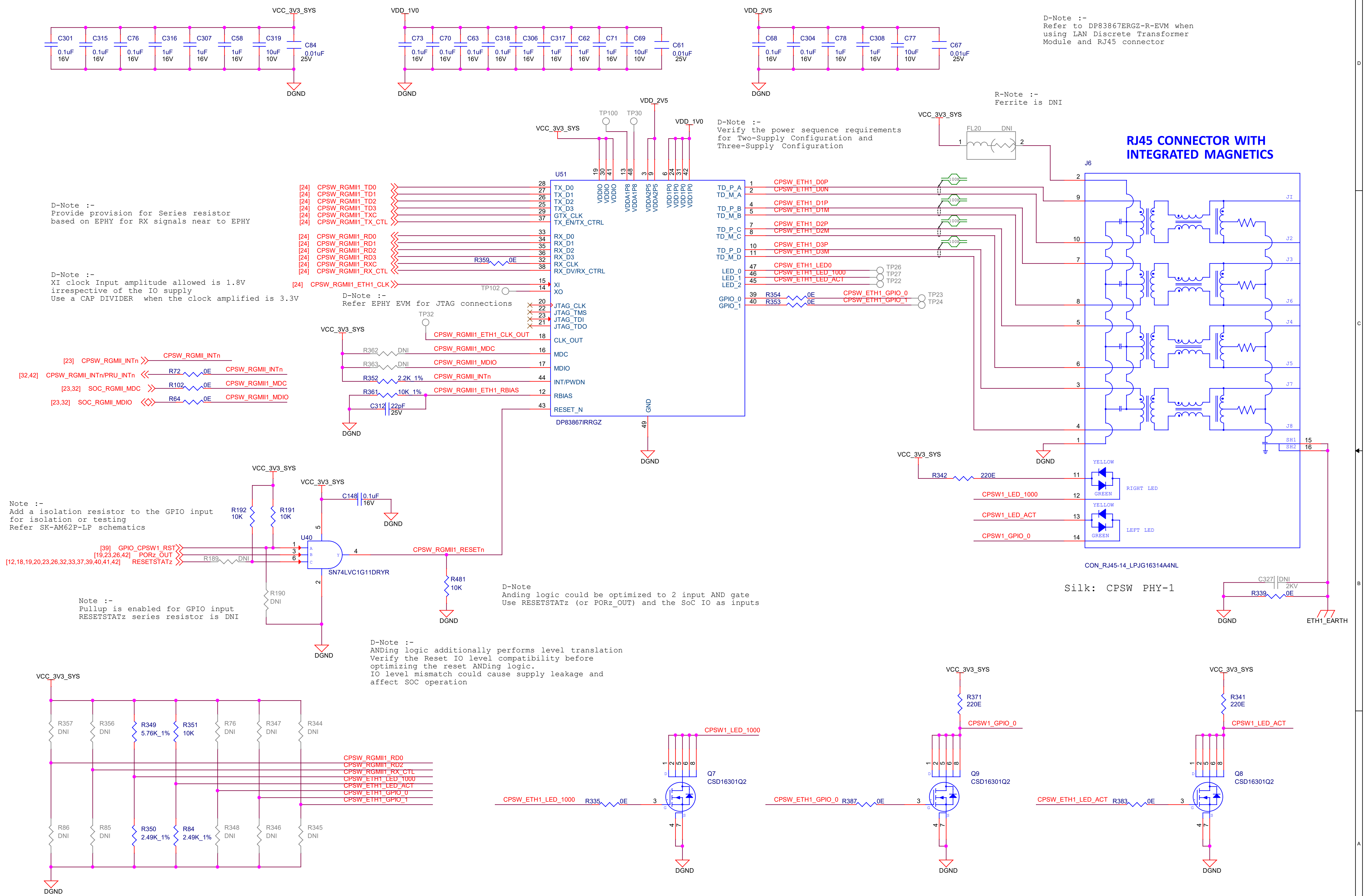
D-Note :-
Refer EPHY EVM for JTAG connections

Note :-
Add a isolation resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

Note :-
Pullup is enabled for GPIO input
RESETSTATz series resistor is DNI

D-Note
Anding logic could be optimized to 2 input AND gate
Use RESETSTATz (or PORz_OUT) and the SoC IO as inputs

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation



PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_1 ETHERNET PHY	
Size C	PROC142A1(002)	Rev A1
Date: Monday, May 20, 2024	Sheet 22 of 44	

CPSW3G RGMII 2 - ETHERNET PHY

D-Note :-
The caps and values used are as per the
EPHY data sheet recommendations

VCC_3V3_SYS: C235 0.1uF 16V, C32 0.1uF 16V, C208 0.1uF 16V, C236 1uF 16V, C19 1uF 16V, C227 1uF 16V, C242 10uF 10V, C38 0.01uF 25V → DGND

VDD_1V0: C27 0.1uF 16V, C238 0.1uF 16V, C22 0.1uF 16V, C29 0.1uF 16V, C237 1uF 16V, C224 1uF 16V, C21 1uF 16V, C28 1uF 16V, C39 10uF 10V, C26 0.01uF 25V → DGND

VDD_2V5: C216 0.1uF 16V, C25 0.1uF 16V, C35 1uF 16V, C228 1uF 16V, C33 10uF 10V, C24 0.01uF 25V → DGND

D-Note :-
Refer to DP83867ERGZ-R-EVM when
using LAN Discrete Transformer
Module and RJ45 connector

R-Note :-
Ferrite is DNI

D-Note :-
Verify the power sequence requirements
for Two-Supply Configuration and
Three-Supply Configuration

TP101, TP19, VCC_3V3_SYS, VDD_2V5, VDD_1V0

U49 DP83867IRRGZ

Pin	Name	Net
28	TX_D0	[24] CPSW_RGMII2_TD0
27	TX_D1	[24] CPSW_RGMII2_TD1
26	TX_D2	[24] CPSW_RGMII2_TD2
25	TX_D3	[24] CPSW_RGMII2_TD3
29	GTX_CLK	[24] CPSW_RGMII2_TXC
37	TX_EN/TX_CTRL	[24] CPSW_RGMII2_TX_CTL
33	RX_D0	[24] CPSW_RGMII2_RD0
34	RX_D1	[24] CPSW_RGMII2_RD1
35	RX_D2	[24] CPSW_RGMII2_RD2
36	RX_D3	[24] CPSW_RGMII2_RD3
32	RX_CLK	[24] CPSW_RGMII2_RXC
38	RX_DV/RX_CTRL	[24] CPSW_RGMII2_RX_CTL
15	XI	[24] CPSW_RGMII2_ETH2_CLK
14	XO	TP103
20	JTAG_CLK	
22	JTAG_TMS	
23	JTAG_TDI	
21	JTAG_TDO	
18	CLK_OUT	CPSW_RGMII2_ETH2_CLK_OUT
16	MDC	CPSW_RGMII2_MDC
17	MDIO	CPSW_RGMII2_MDIO
44	INT/PWDN	CPSW_RGMII_INTn
12	RBIAS	CPSW_RGMII2_ETH2_RBIAS
43	RESET_N	
49	GND	DGND
19, 30, 41	VDDIO	VCC_3V3_SYS
13, 48	VDDA1P8	VCC_3V3_SYS
3, 9	VDDA2P5	VDD_2V5
6, 24, 31, 42	VDD1P0	VDD_1V0

D-Note :-
Provide provision for Series resistor based
on EPHY for RX signals near to EPHY

R324 0E

D-Note :-
Refer EPHY EVM for JTAG connections

TP20

VCC_3V3_SYS: R330 1.5K, R329 DNI, R672 DNI

[22] CPSW_RGMII_INTn

R328 10K 1% → DGND

C234 22pF 25V → DGND

[22,32] SOC_RGMII_MDC — R673 0E — CPSW_RGMII2_MDC

[22,32] SOC_RGMII_MDIO — R674 0E — CPSW_RGMII2_MDIO

TD_P_A	1	CPSW_ETH2_D0P
TD_M_A	2	CPSW_ETH2_D0N
TD_P_B	4	CPSW_ETH2_D1P
TD_M_B	5	CPSW_ETH2_D1M
TD_P_C	7	CPSW_ETH2_D2P
TD_M_C	8	CPSW_ETH2_D2M
TD_P_D	10	CPSW_ETH2_D3P
TD_M_D	11	CPSW_ETH2_D3M
LED_0	47	CPSW_ETH2_LED0
LED_1	46	CPSW_ETH2_LED_1000
LED_2	45	CPSW_ETH2_LED_ACT
GPIO_0	39	R302 0E — CPSW_ETH2_GPIO_0
GPIO_1	40	R301 0E — CPSW_ETH2_GPIO_1

TP15, TP17, TP11, TP12, TP13

VCC_3V3_SYS → FL15 DNI

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

J4

Pin	Net
2	CPSW_ETH2_D0P
9	CPSW_ETH2_D0N
10	CPSW_ETH2_D1P
7	CPSW_ETH2_D1M
8	CPSW_ETH2_D2P
5	CPSW_ETH2_D2M
6	CPSW_ETH2_D3P
3	CPSW_ETH2_D3M
4	CPSW_ETH2_LED0
1	DGND
11	CPSW2_LED_1000
12	CPSW2_LED_ACT
13	CPSW2_GPIO_0
14	
SH1	15
SH2	16

J1, J2, J3, J6, J4, J5, J7, J8

VCC_3V3_SYS: R286 220E → CPSW2_LED_1000, CPSW2_LED_ACT, CPSW2_GPIO_0

YELLOW / GREEN — RIGHT LED

YELLOW / GREEN — LEFT LED

CON_RJ45-14_LPJG16314A4NL

C195 DNI 2KV, R29 0E → DGND, ETH2_EARTH

Silk: CPSW PHY-2

VCC_3V3_SYS: R197 10K, R196 10K, C157 0.1uF 16V → DGND

U41 SN74LVC1G11DRYR

[39] GPIO_CPSW2_RST
[19,22,26,42] PORz_OUT
[12,18,19,20,22,26,32,33,37,39,40,41,42] RESETSTATz
R194 DNI

CPSW_RGMII2_RESETn — R35 10K → DGND

R195 DNI

Note :-
Add a isolation resistor to the GPIO input
for isolation or testing
Refer SK-AM62P-LP schematics

Note :-
Pullup is enabled for GPIO input
RESETSTATz series resistor is DNI

D-Note
Anding logic could be optimized to 2 input AND gate
Use RESETSTATz (or PORz_OUT) and the SoC IO as inputs

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before
optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and
affect SOC operation

VCC_3V3_SYS: R322 10K, R311 DNI, R298 5.76K_1%, R300 10K, R38 DNI, R294 DNI, R291 DNI

CPSW_RGMII2_RD0
CPSW_RGMII2_RD2
CPSW_RGMII2_RX_CTL
CPSW_ETH2_LED_1000
CPSW_ETH2_LED_ACT
CPSW_ETH2_GPIO_0
CPSW_ETH2_GPIO_1

R54 2.49K_1%, R49 DNI, R299 2.49K_1%, R47 2.49K_1%, R295 DNI, R293 DNI, R292 DNI → DGND

PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

CPSW2_LED_1000 — Q4 CSD16301Q2 (1, 2, 5, 6, 8 / 4, 7)
CPSW_ETH2_LED_1000 — R289 0E — 3

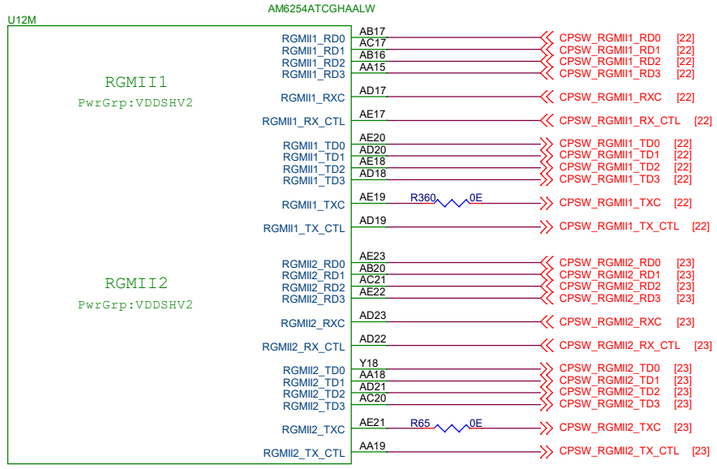
VCC_3V3_SYS — R334 220E — CPSW2_GPIO_0 — Q6 CSD16301Q2
CPSW_ETH2_GPIO_0 — R340 0E — 3

VCC_3V3_SYS — R288 220E — CPSW2_LED_ACT — Q5 CSD16301Q2
CPSW_ETH2_LED_ACT — R338 0E — 3

Designed for TI by Mistral Solutions Pvt Ltd

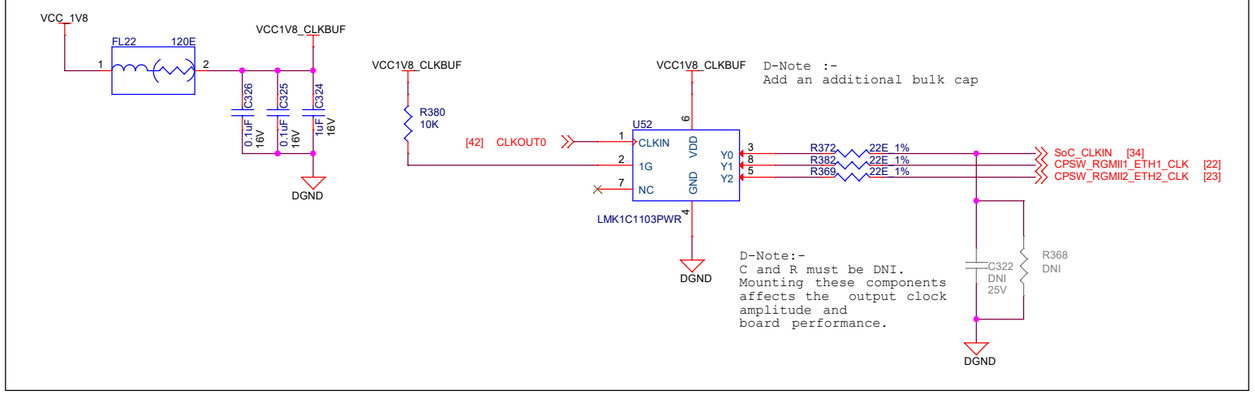
Title	CPSW RGMII_2 ETHERNET PHY		
Size	C	PROC142A1(002)	Rev A1
Date:	Monday, May 20, 2024	Sheet 23 of 44	

SOC MAC INTERFACE

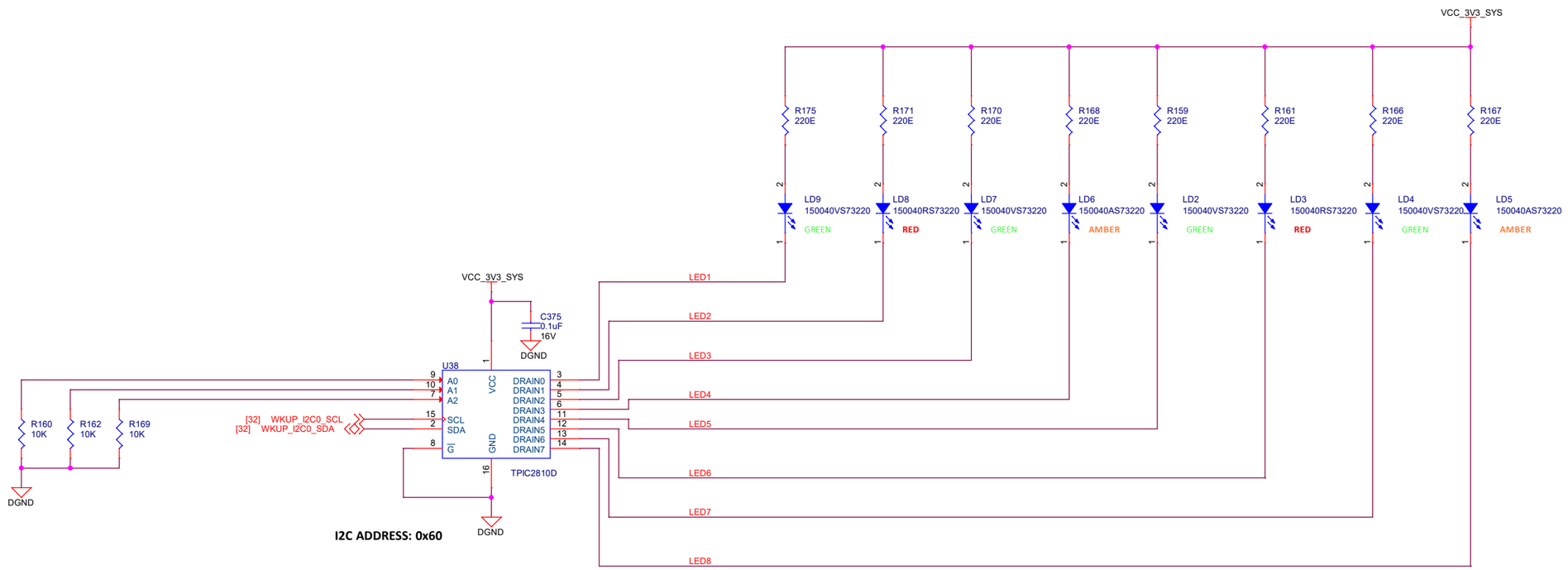


D-Note :-
Add series resistors 22 R on the Ethernet interface TX (TDx) signals near to the SoC

CLOCK BUFFER FOR SOC AND ETHERNET PHYs



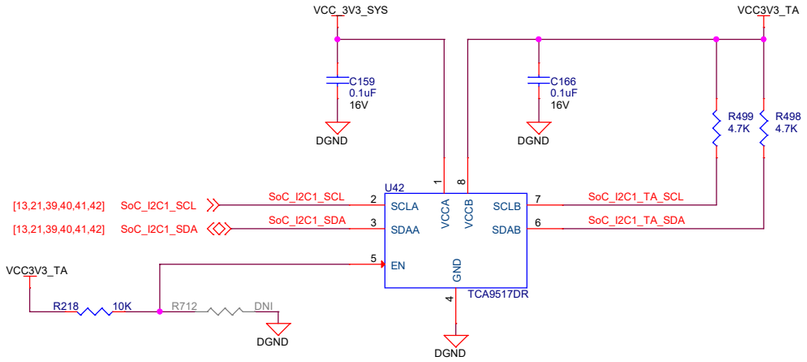
LED DRIVER



Designed for TI by Mistral Solutions Pvt Ltd

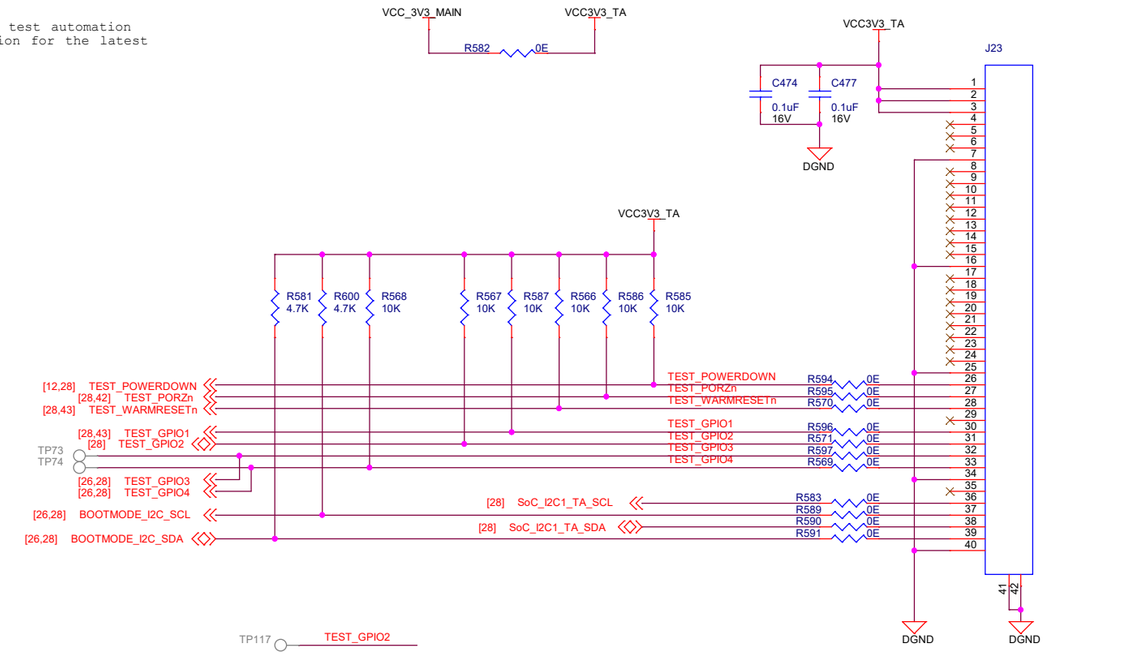
Title	ETHERNET PHY CLOCK BUFFER & LED DRIVER	
Size C	PROC142A1(002)	Rev A1
Date: Monday, May 20, 2024	Sheet 24 of 44	

I2C BUS BUFFER



40-PIN TEST AUTOMATION HEADER

D-Note :-
Refer AM62P test automation implementation for the latest updates



Silk: AUTOMATION HDR

TEST AUTOMATION GPIO MAPPING

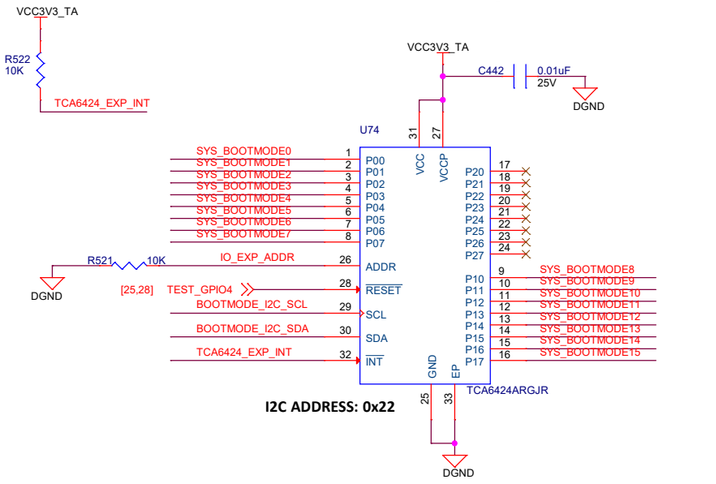
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on MCU_GPIO0_15 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to a Testpoint	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

Designed for TI by Mistral Solutions Pvt Ltd

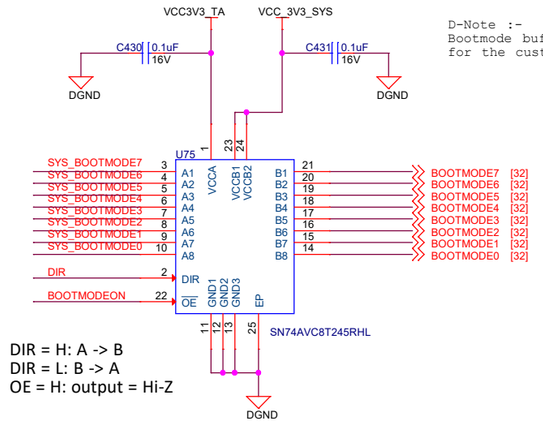
Title TEST AUTOMATION

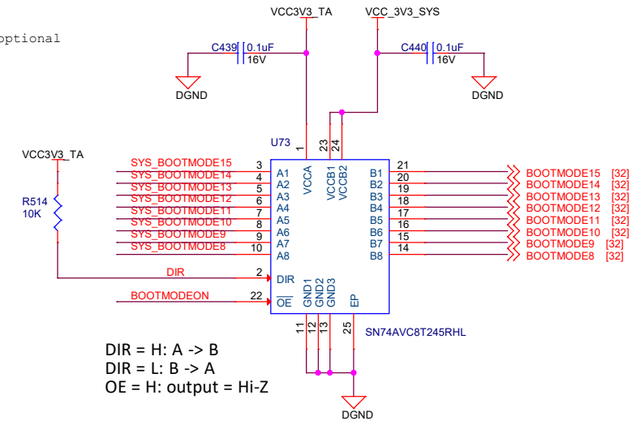
Size		Rev
C	PROC142A1(002)	A1
Date: Monday, May 20, 2024	Sheet 25 of 44	

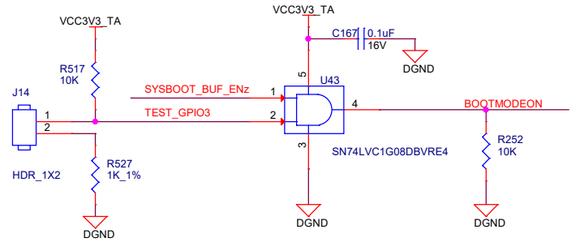
BOOTMODE IO EXPANDER



BOOT MODE BUFFERS





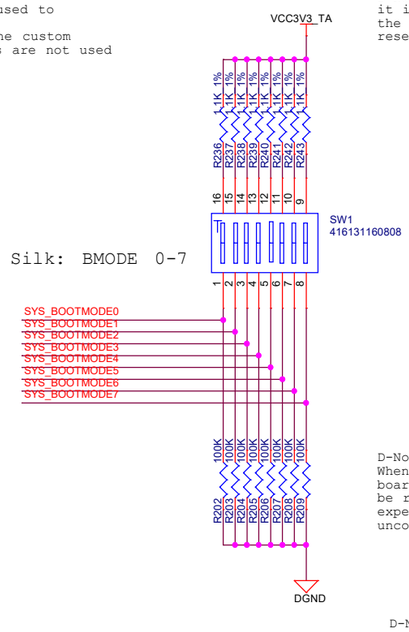


BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES

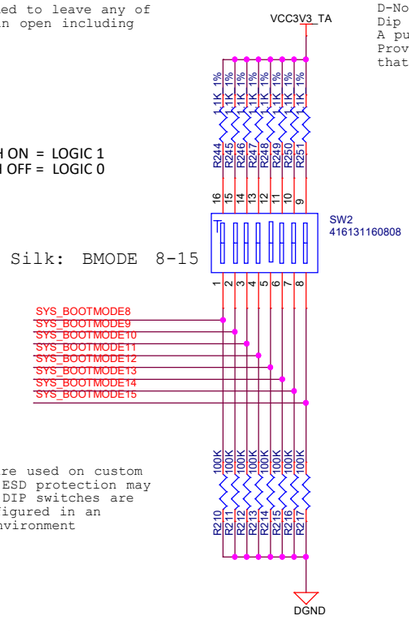
D-Note :-
VCC3V3_XDS_TA supply is used to
support test automation.
Connect SoC_DVDD3V3 in the custom
board design when buffers are not used

D-Note :-
it is not recommended to leave any of
the the bootmode pin open including
reserved pins

D-Note :-
Dip switch is optional and used on the SK for ease of configuration
A pullup or pulldown resistor can be used to set the BOOTMODE configuration
Provide provision for Pullup and Pulldown resistors for the bootmode pins
that have configuration capability



SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0



D-Note :-
When dip switches are used on custom
board, an external ESD protection may
be required if the DIP switches are
expected to be configured in an
uncontrolled ESD environment

D-Note :-
When DIP switches are used, reduce the
resistor values used for the divider to
47K and 470R maintaining the ratio

BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. BACKUP BOOT OPTION

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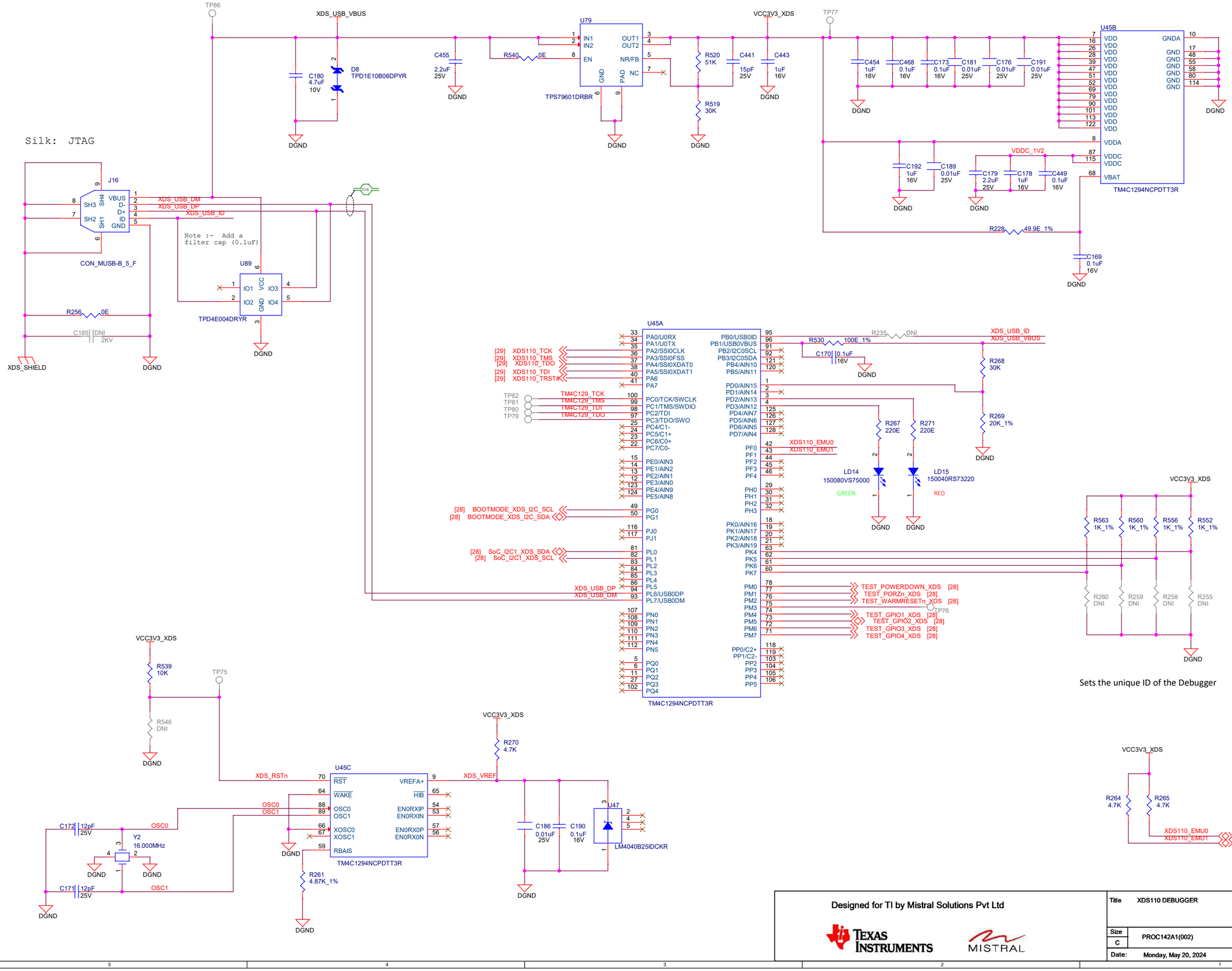
Title	BOOT MODE BUFFER & SWITCHES		
Size	PROC142A1(002)		Rev
C			A1
Date:	Monday, May 20, 2024	Sheet 26 of 44	

XDS110 DEBUGGER

D-Note :-
Please follow SK-AM62P-LP EVM implementations for latest updates on XDS110

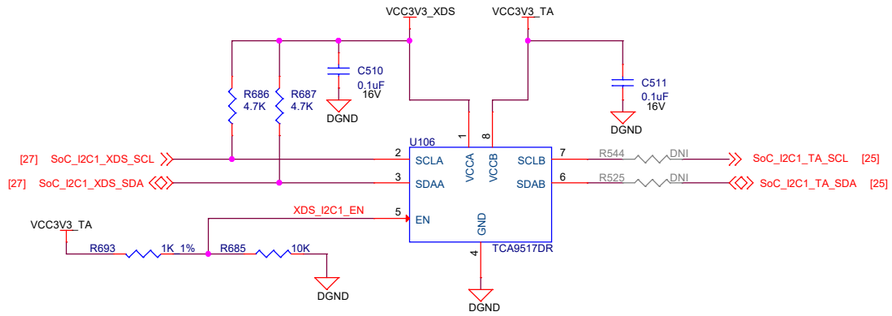
Silk: JTAG



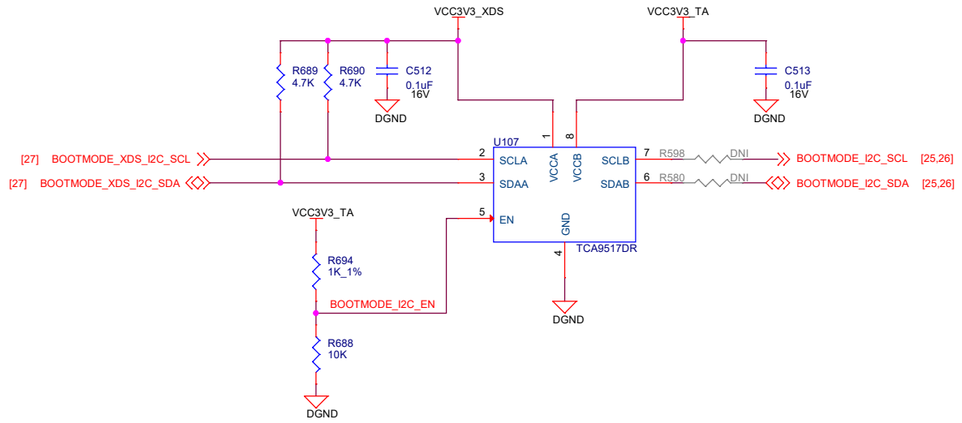
Designed for TI by Mistral Solutions Pvt Ltd

Title	XDS110 DEBUGGER	
Size: C	PROC142A1(002)	Rev: A1
Date: Monday, May 20, 2024	Sheet 27 of 44	

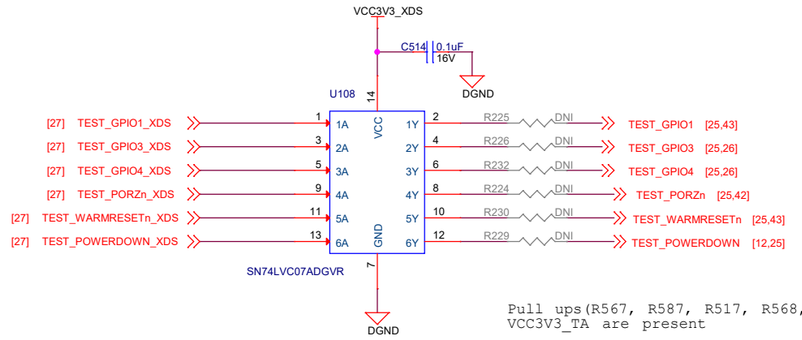
I2C_TA BUS BUFFER



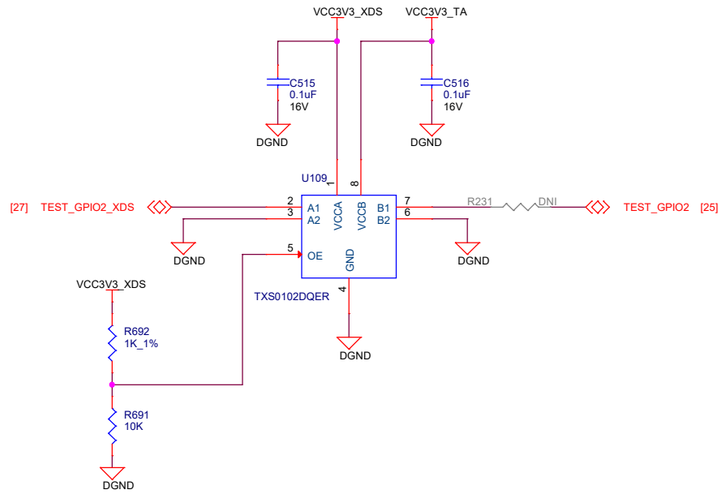
BOOTMODE_I2C_TA BUFFER



ISOLATION BUFFERS FOR TA SIGNALS



Pull ups(R567, R587, R517, R568, R585, R586 & R566) to VCC3V3_TA are present



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUTOMATION SIGNALS BUFFER		
Size C	PROC142A1(002)		Rev A1
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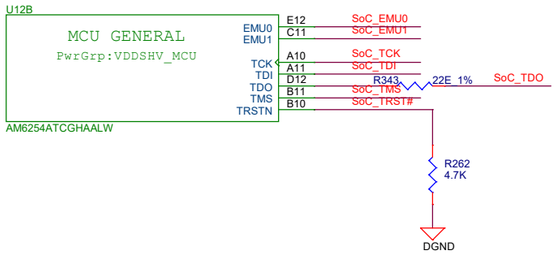
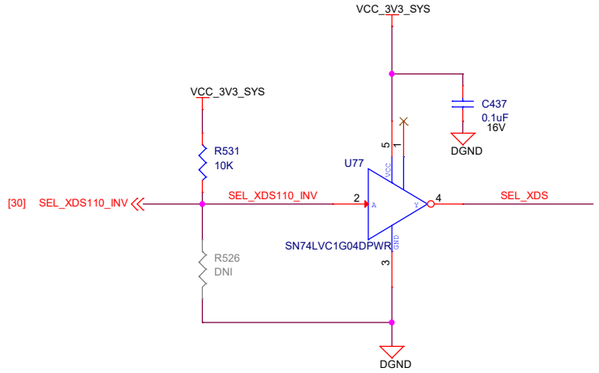
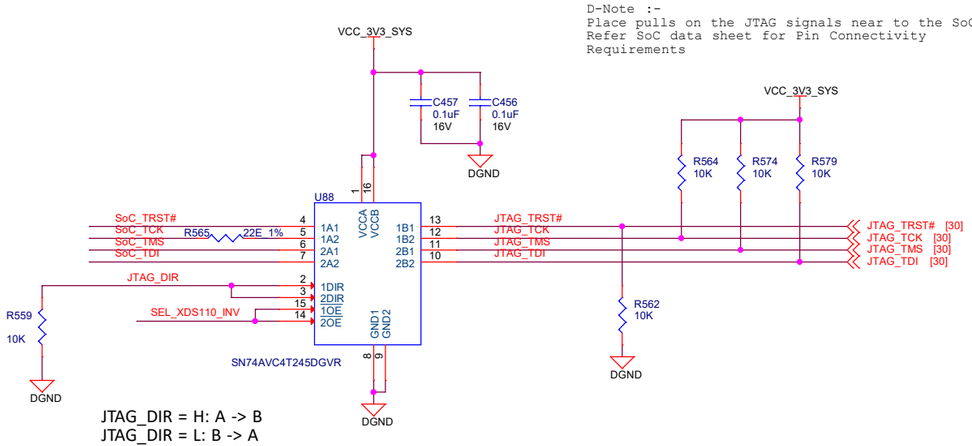
JTAG SOC SECTION

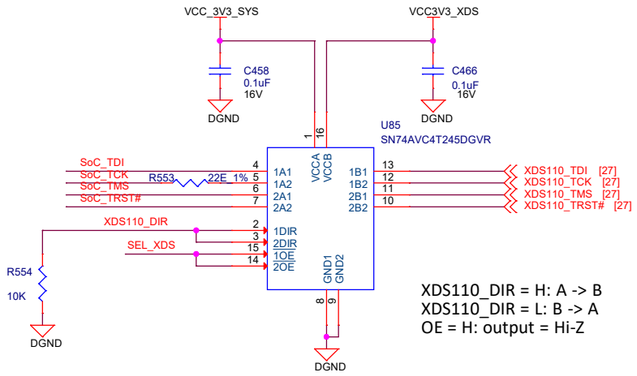


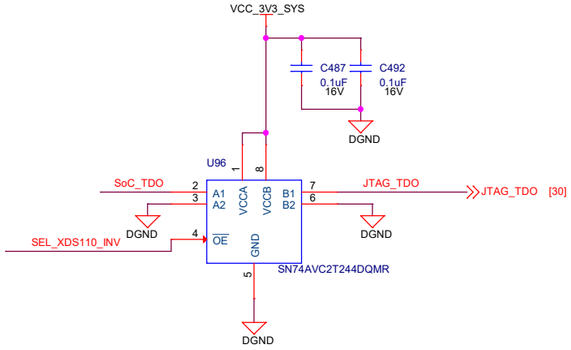


cTI20 JTAG BUFFERS

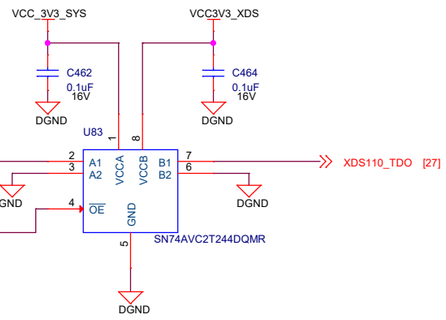


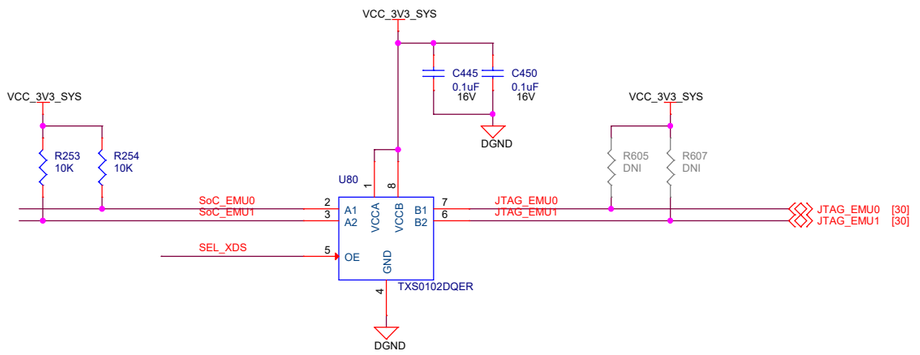
BUFFER XDS110

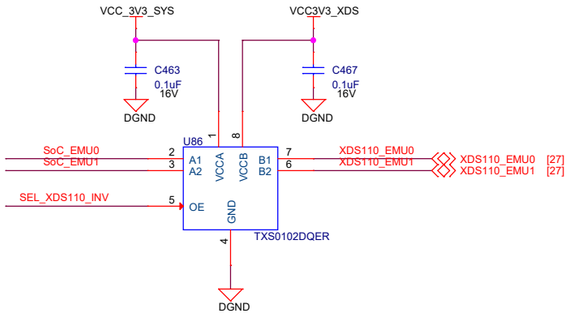




CAD NOTE: Buffers U88 and U96 need to be placed closer to the cTI-20pin connector J17 to reduce Stub length of the JTAG signals.







Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG BUFFER	
Size C	PROC142A1(002)	Rev A1
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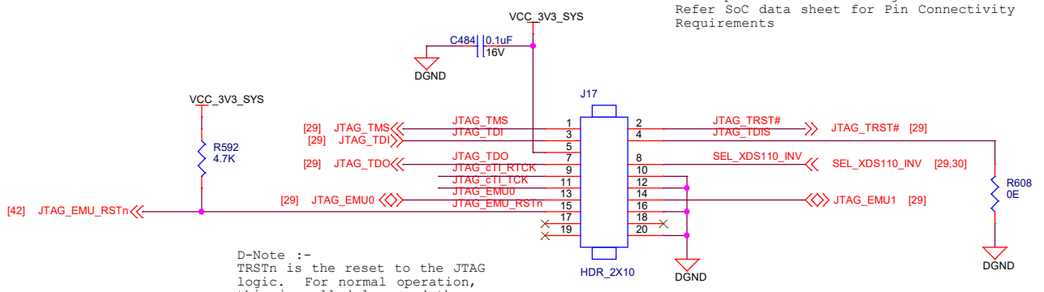
JTAG 20 PIN cTI CONNECTOR



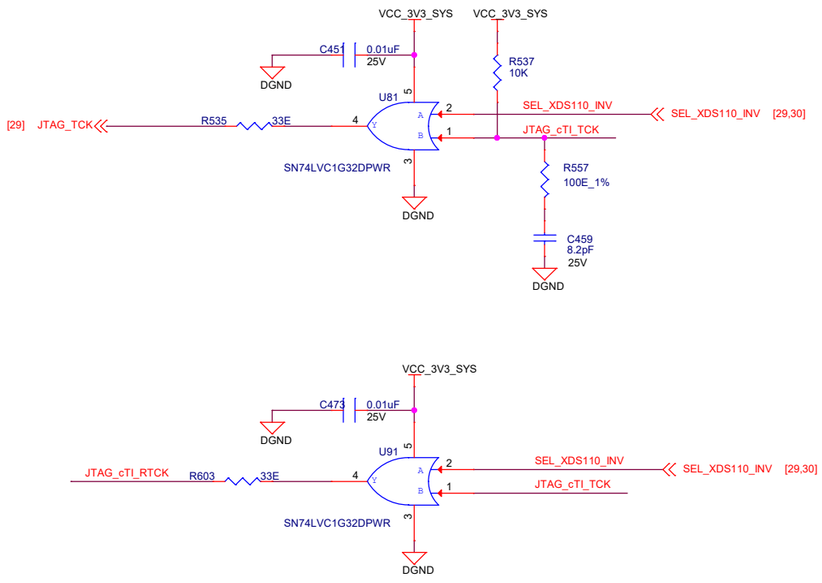
D-Note :-
Place pulls on the JTAG signals near to the SoC
Refer SoC data sheet for Pin Connectivity
Requirements

D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled low, and thus the JTAG remains in reset as it is not being used. When a JTAG pod is connected, the pod will eventually drive this signal high to release the JTAG logic from reset and enable a JTAG connection.

Silk: cTI

D-Note :-
Add an external ESD protection to provide system level ESD protection when external connector is used for debug
Follow the connectivity table for connecting the required pulls for the SOC JTAG interface
Add Test points, and external ESD protection when JTAG connector is not used

JTAG CLOCK BUFFER

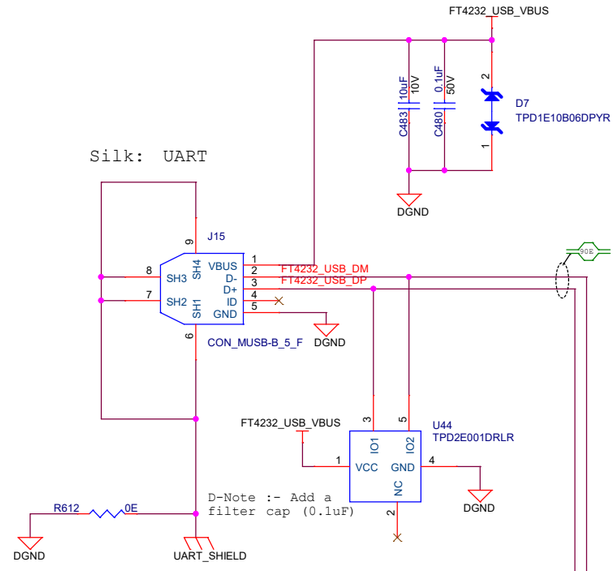


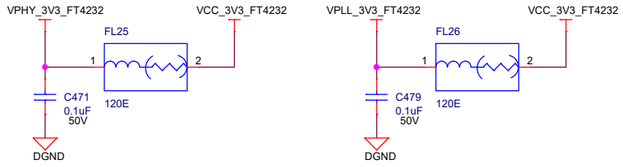
Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG 20 PIN cTI CONNECTOR	
Size C	PROC142A1(002)	Rev A1
Date: Monday, May 20, 2024	Sheet 30 of 44	

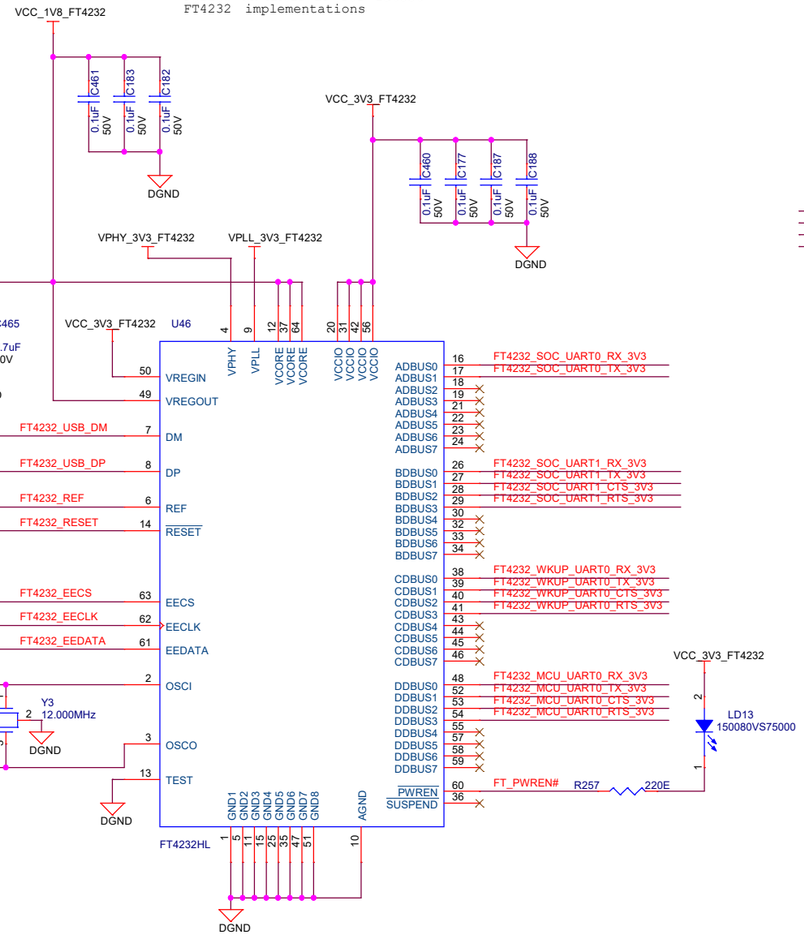
FT4232 UART

Silk: UART

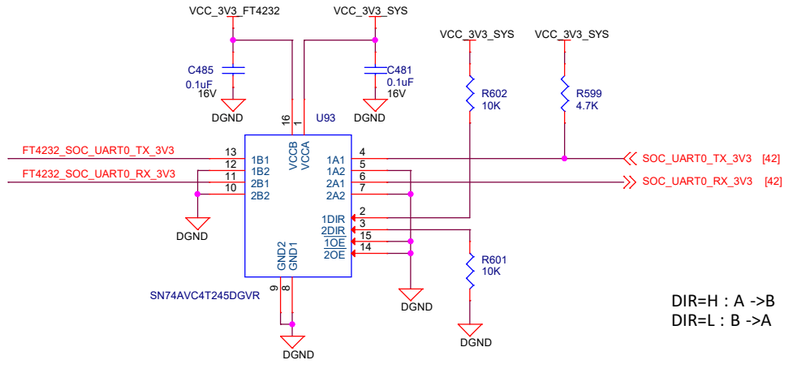


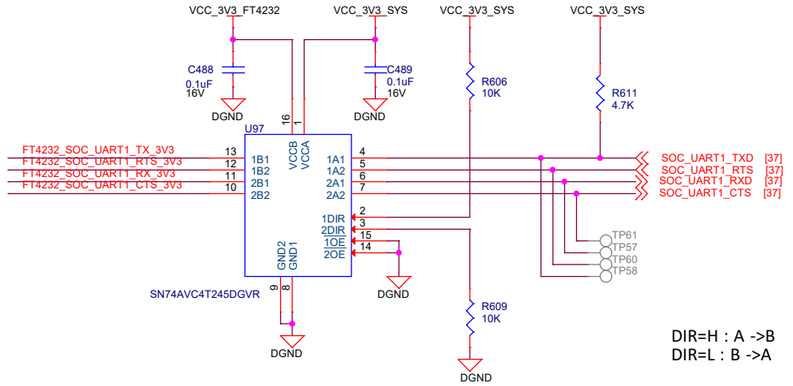


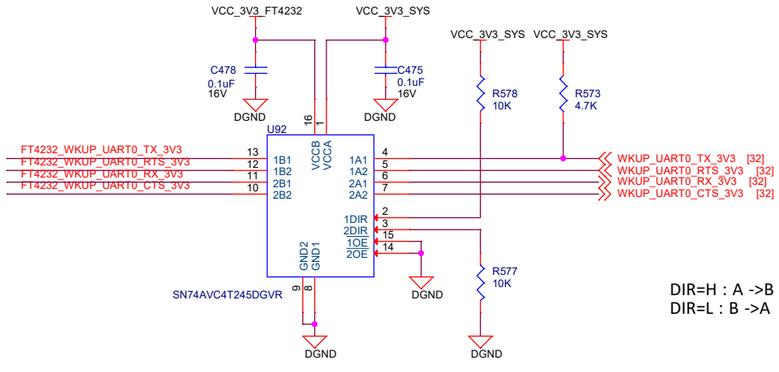
D-Note :-
Follow SK-AM62P-LP for latest
FT4232 implementations

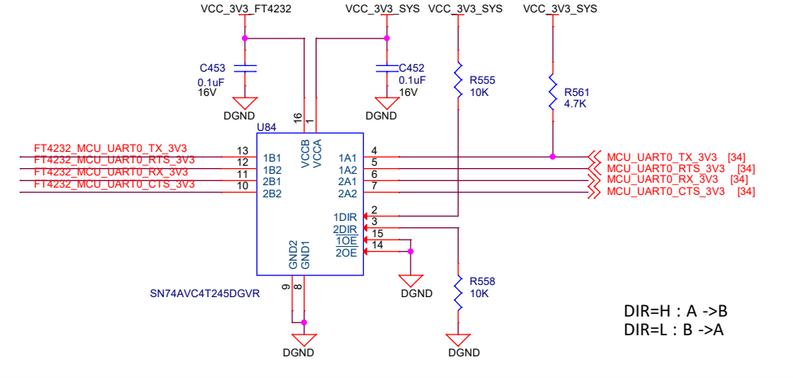


R-Note:-
Verify the implementation with
the device manufacturer

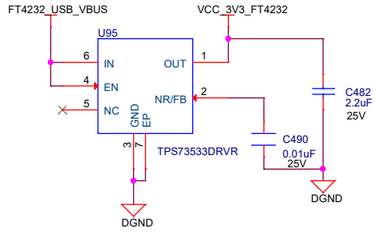




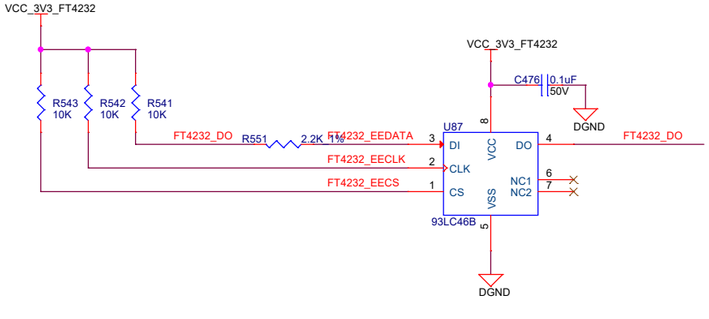




FT4232: 5V to 3.3V@500mA LDO



EEPROM



Designed for TI by Mistral Solutions Pvt Ltd

Title	FT4232 UART TO USB BRIDGE	
Size C	PROC142A1(002)	Rev A1
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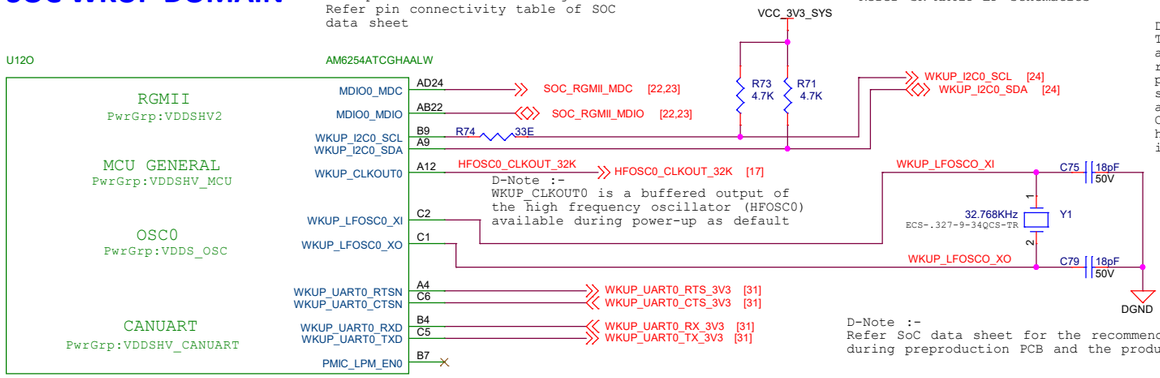
SOC WKUP DOMAIN

D-Note :-
A pullup is recommended for Open drain output type I2C interfaces irrespective of the IO configuration
Refer pin connectivity table of SOC data sheet

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V.
An RC is recommended for slew rate control
Refer SK-AM62P-LP schematics

D-Note :-
The only LFOSC0 register bits that should be changed by the customer are BP_C, PD_C, and CTRLMMR_WKUP_LFXOSC_TRIM[18:16], where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source.The CTRLMMR_WKUP_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation. The load capacitance range of the crystal will be half of the recommended capacitor value range since there are connected in series with the crystals resonate circuit.



D-Note :-
WKUP_CLKOUT0 is a buffered output of the high frequency oscillator (HFOSC0) available during power-up as default

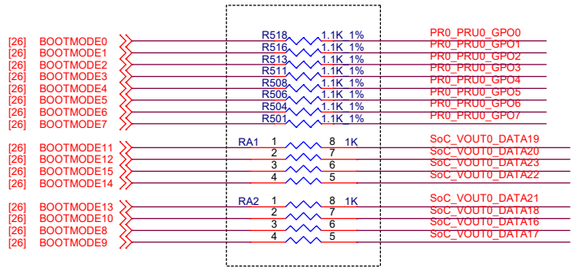
D-Note :-
WKUP LFOSC0 has limited use case. Provide provision to ground Xi when not used. Refer SOC data sheet

D-Note :-
Refer SoC data sheet for the recommended circuit configuration during preproduction PCB and the production PCB

D-Note :-
Delete or reduce the series resistor value to 0R when buffers are not used,
This resistor could be used to isolate the alternate function during testing
Ok to use 1K standard resistor

D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot
Shorting the bootmode pins directly to VCC or ground directly is not recommended
Connect each of the bootmode pins through separate resistor
Choose the bootmode resistor value based on the use case (10K or similar)

BOOTMODE PINS



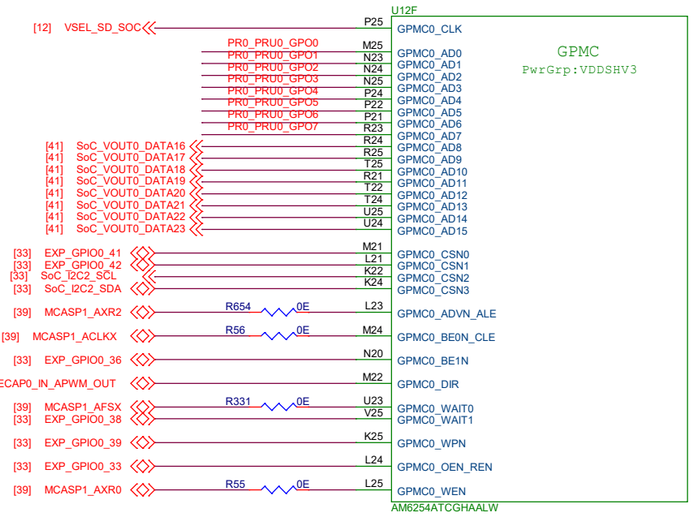
R-Note :- Resistors are used to isolate the BOOTMODE control logic after the value is latched

D-Note :-
When bootmode Isolation buffers are not used, connect the bootmode configuration resistors directly to the SOC bootmode input pins.
Connect the SOC bootmode signal used for alternate function to the attached device through 0R for isolation or testing.

SOC GPMC INTERFACE

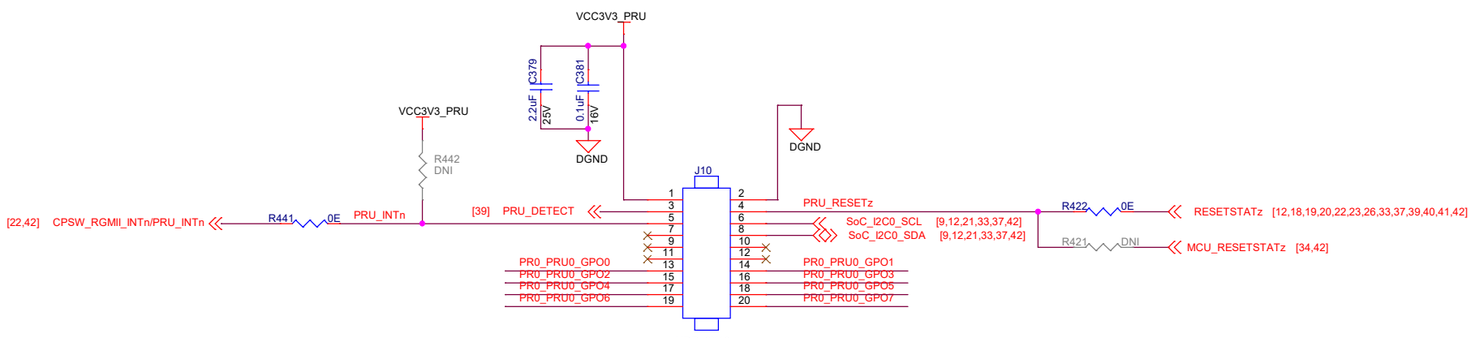
D-Note
Add a series resistor 0R when used as GPMC0_CLK

D-Note :-
SOC IO buffers for signals used for GPMC interface are disabled during reset
The required pulls for the interfaced signals are provided on the GPMC interface card



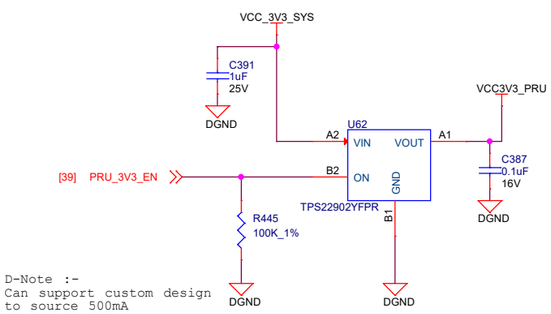
D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull.
When adding pull is not feasible, ensure the traces are routed away from noisy signals

PRU HEADER



Silk: PRU HDR

POWER SWITCH FOR PRU HEADER



D-Note :-
Can support custom design to source 500mA

3V3 supply of PRU Header is limited to sourcing 500mA max.

D-Note:- Processor IOs connected to PRU Header are not fail-safe.
No external input shall be driven when Starter Kit is not powered-up.

Designed for TI by Mistral Solutions Pvt Ltd

Title	PRU HEADER	
Size C	PROC142A1(002)	Rev A1
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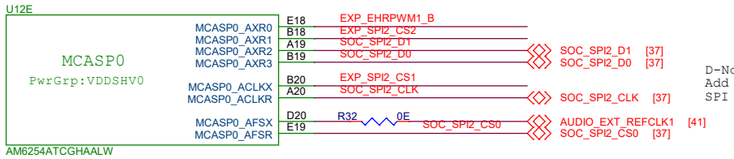
USER EXPANSION CONNECTOR

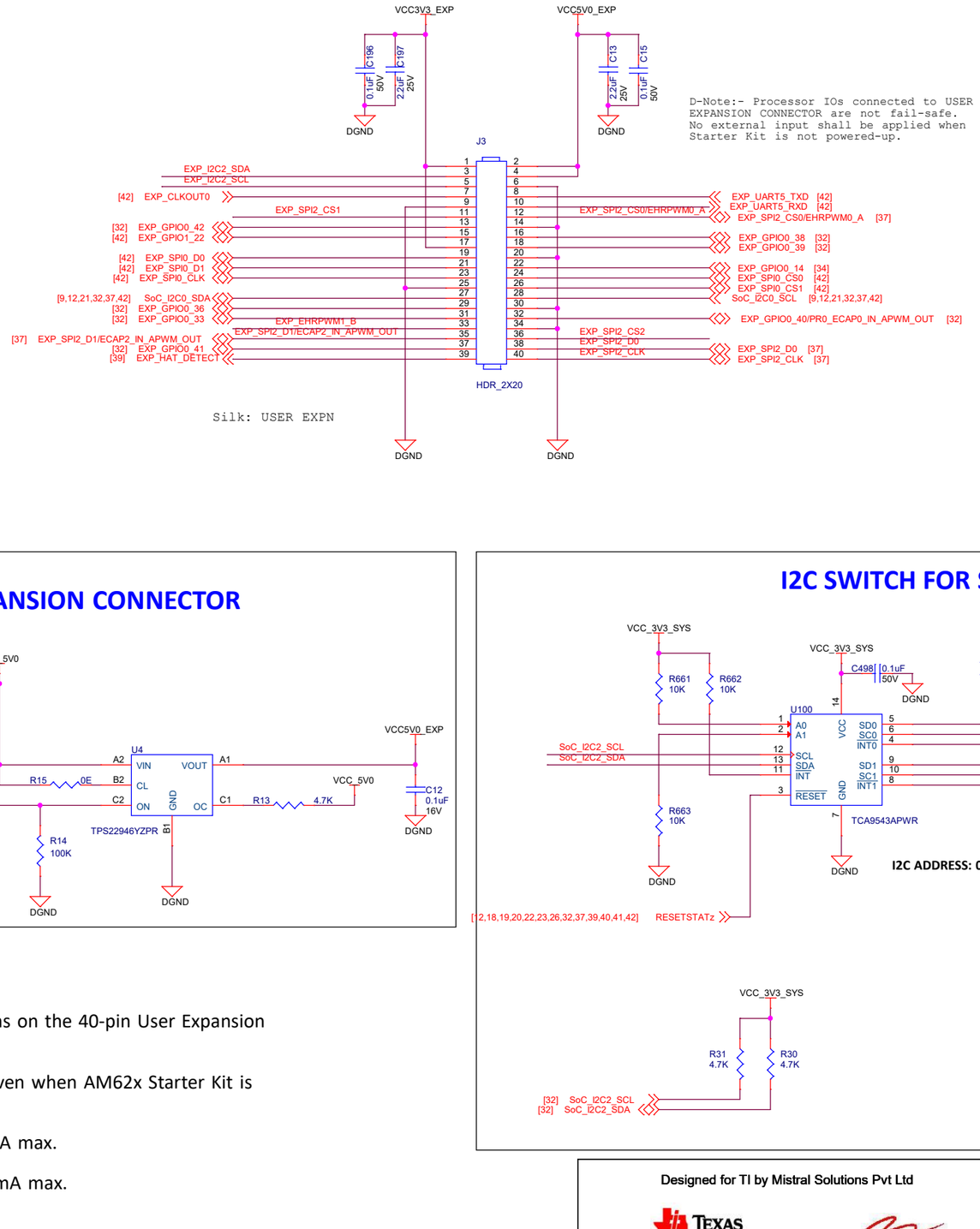
D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO



CAD Note:- R32(Series damping resistor) should be placed close to SoC

D-Note:-
Add a series resistor 22R on the SPI clock output signal near to the SoC

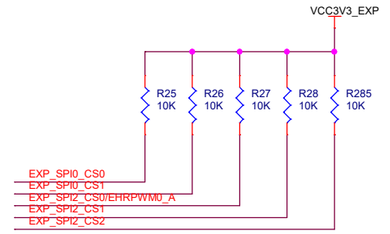
R-Note :-
These supplies are off by default
The supplies are controlled by the below load switches and needs to be enabled



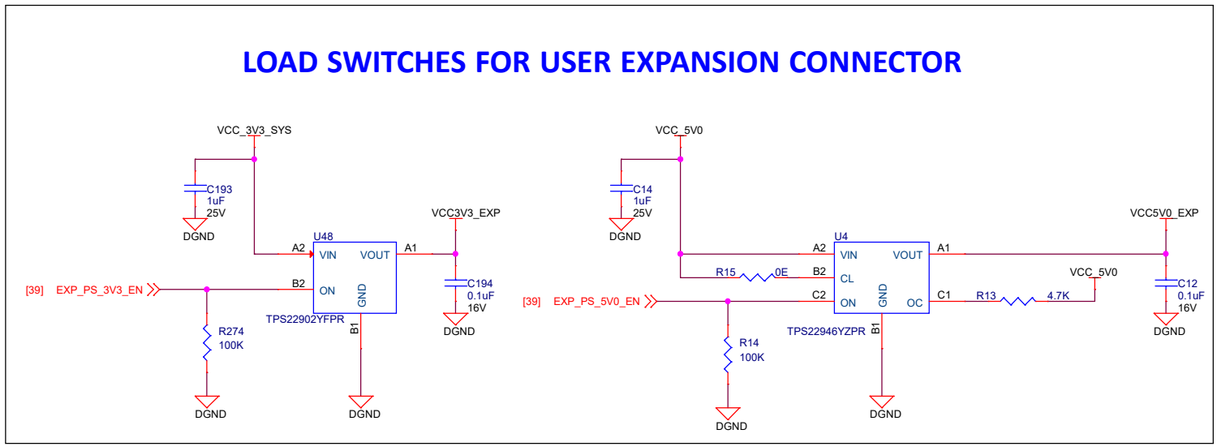
D-Note:- Processor IOs connected to USER EXPANSION CONNECTOR are not fail-safe. No external input shall be applied when Starter Kit is not powered-up.

Silk: USER EXPN

D-Note:- Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



LOAD SWITCHES FOR USER EXPANSION CONNECTOR



I2C SWITCH FOR SoC_I2C2

R-NOTE:-

AM62x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

Designed for TI by Mistral Solutions Pvt Ltd

Title	USER EXPANSION CONNECTOR	
Size C	PROC142A1(002)	Rev A1
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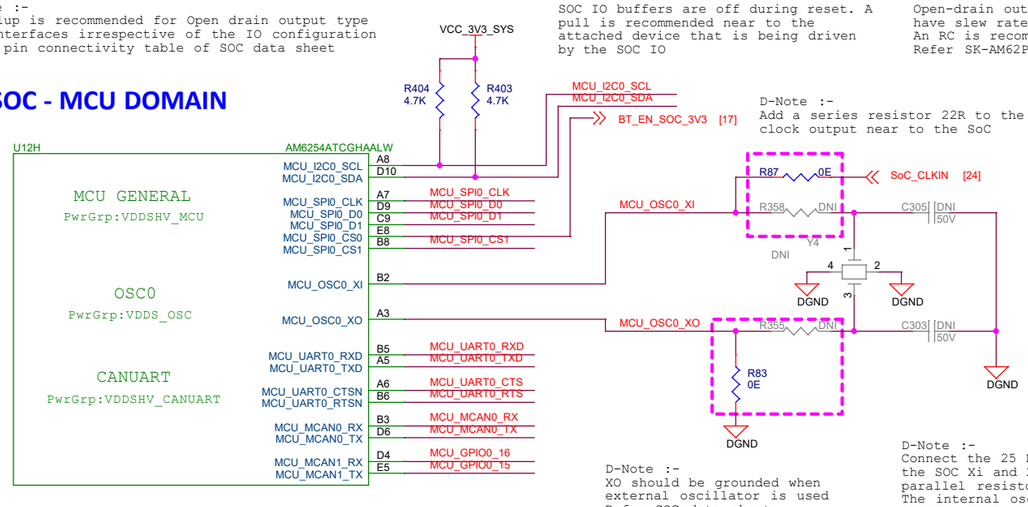
D-Note :-
A pullup is recommended for Open drain output type I2C interfaces irrespective of the IO configuration Refer pin connectivity table of SOC data sheet

D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V An RC is recommended for slew rate control Refer SK-AM62P-LP schematics

SOC - MCU DOMAIN



D-Note :-
Add a series resistor 22R to the SPI0 clock output near to the SoC

D-Note :-
No HFOSC0 registers are required to be changed. These registers should remain in their default state.
Select the appropriate crystal circuit components that are compliant to the values defined in the MCU_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

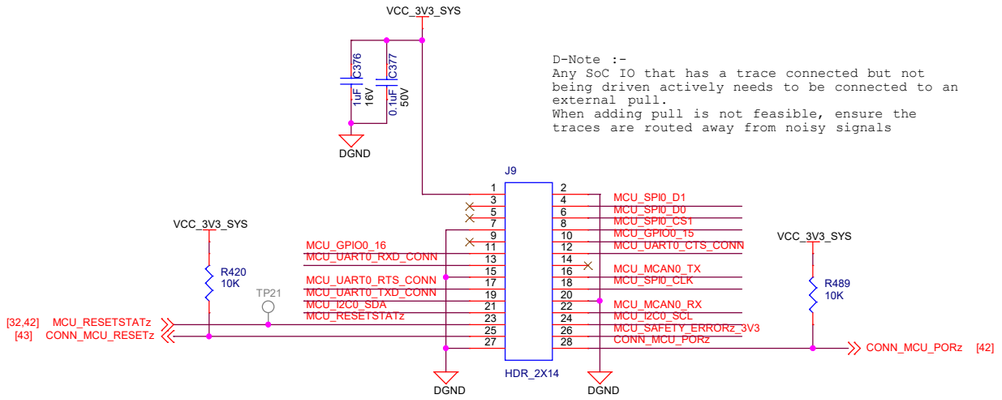
D-Note :-
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines Oscillator Routing

D-Note :-
MCU_OSC0 has been validated only with a 25 MHz clock source, so that is the only frequency supported.
The datasheet shows MCU_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD_CORE is valid. In most cases it will start as early as VDDS_OSC0, but this may not always be the case.
This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.

D-Note :-
XO should be grounded when external oscillator is used Refer SOC data sheet

D-Note :-
Connect the 25 MHz crystal directly to the SOC Xi and Xo pins (No Series or parallel resistors are recommended).
The internal oscillator implements AGC (Automatic Gain Control) for amplitude control
Match the SOC and the EPHY crystal specs

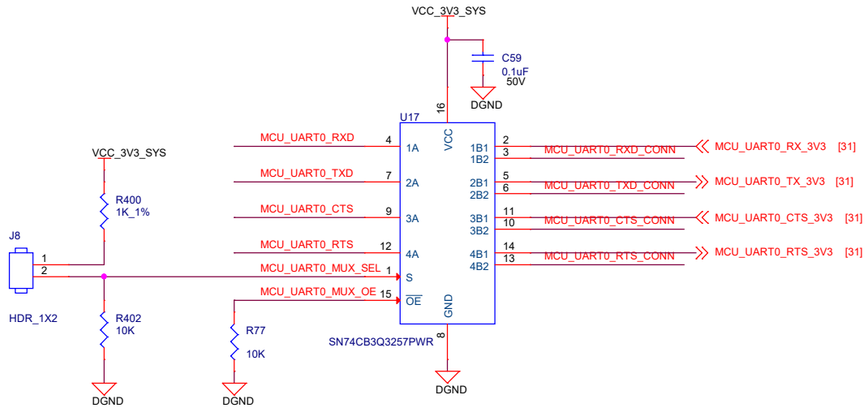
SOC-MCU HEADER



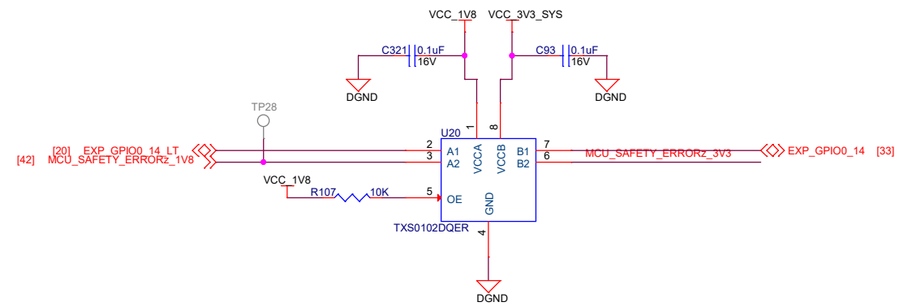
D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull.
When adding pull is not feasible, ensure the traces are routed away from noisy signals

Silk: MCU HDR

SOC - MCU_UART0 MUX



OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER



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Title	MCU HEADER	
Size C	PROC142A1(002)	Rev A1
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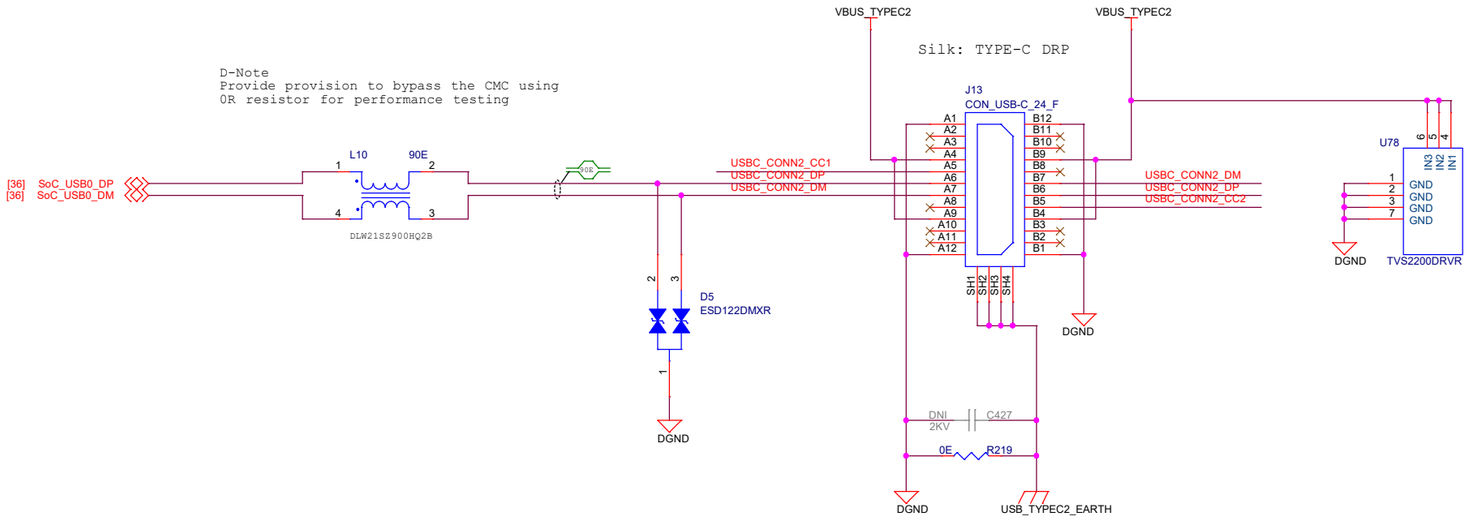
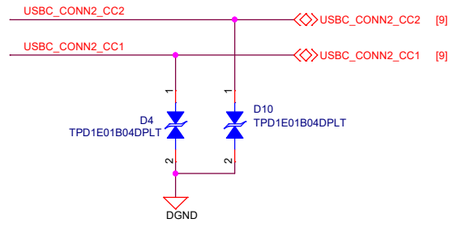
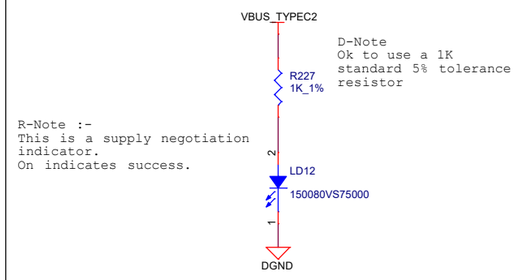
USB0 TYPE-C DRP

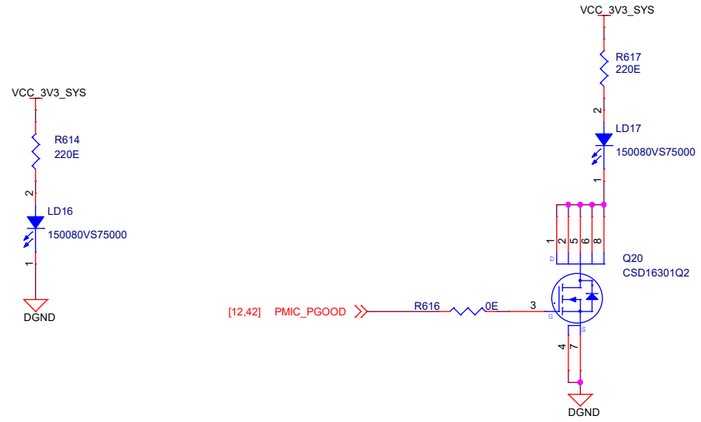




POWER INDICATION LED: VBUS_TYPEC2



POWER RAIL LEDS



Designed for TI by Mistral Solutions Pvt Ltd

Title	USB0 TYPE-C DRP	
Size C	PROC142A1(002)	Rev A1
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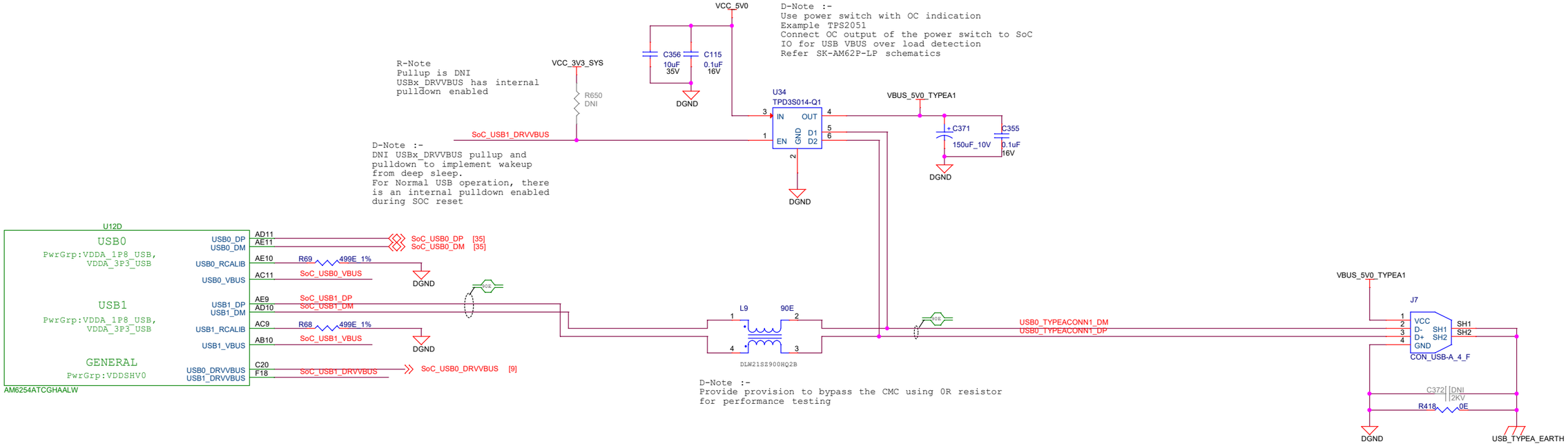
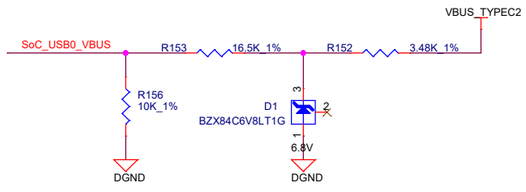
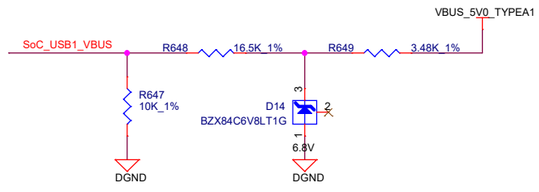
USB1 - USB 2.0 TYPE-A



D-Note:- VBUS connection is optional for Host configuration





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Title	USB1 TYPE-A		
Size C	PROC142A1(002)		Rev A1
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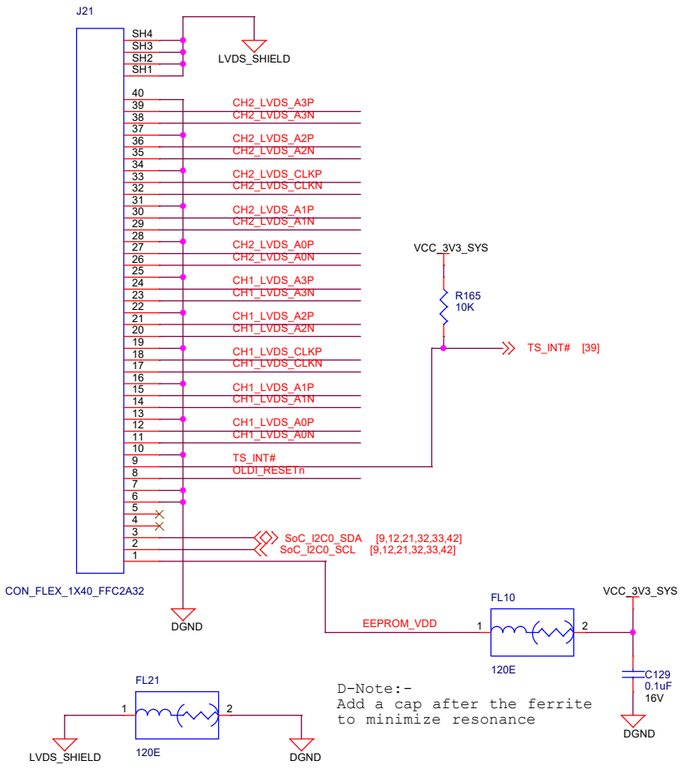
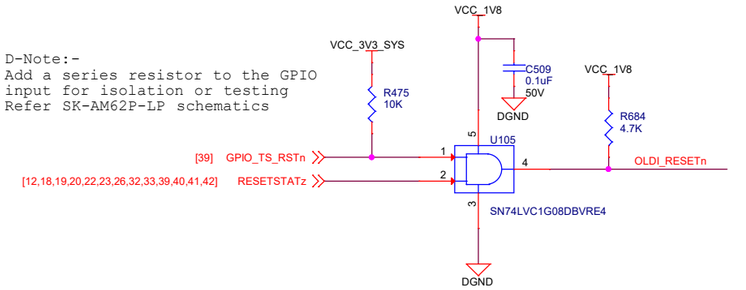
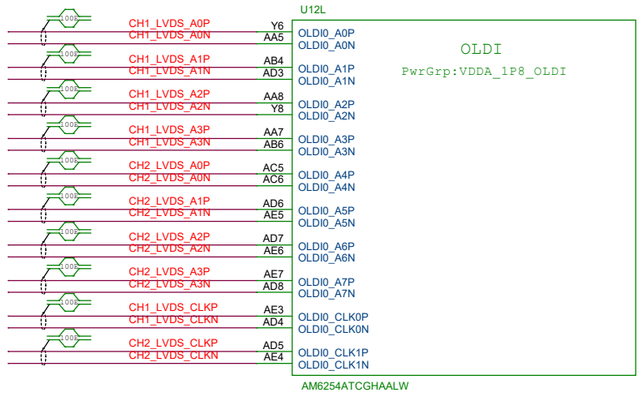
OLDI DISPLAY INTERFACE

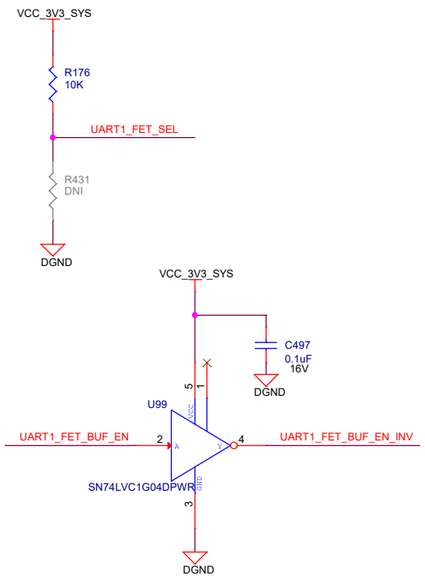


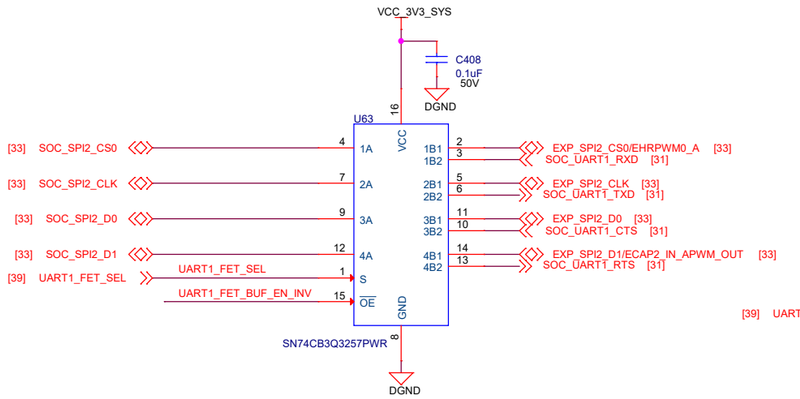
OLDI RESET

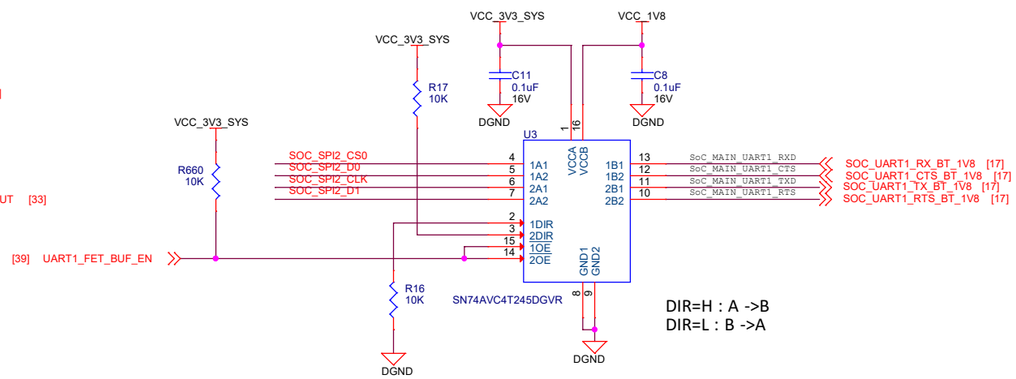




SoC UART1 FET SWITCH & BUFFER







OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	FT4232
L	L	An=nB1	USER EXPANSION CONNECTOR

Designed for TI by Mistral Solutions Pvt Ltd

Title	OLDI DISPLAY INTERFACE	
Size: C	PROC142A1(002)	Rev: A1
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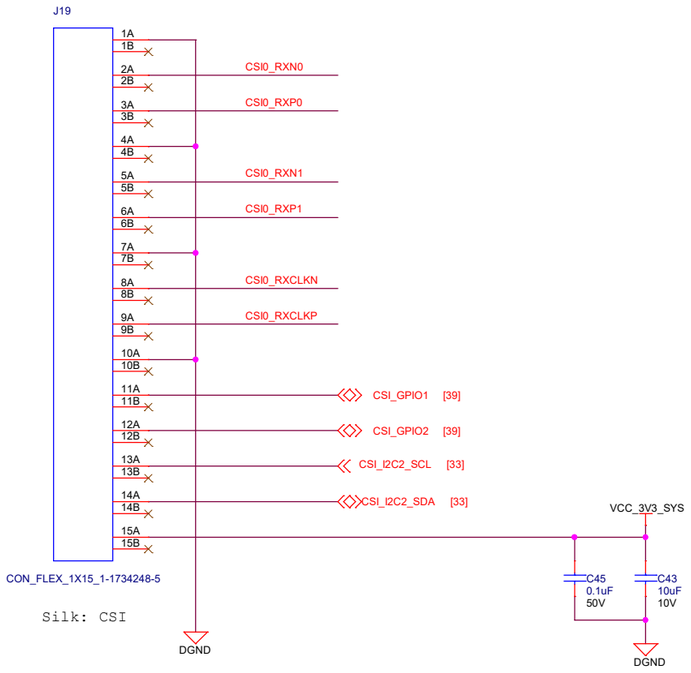
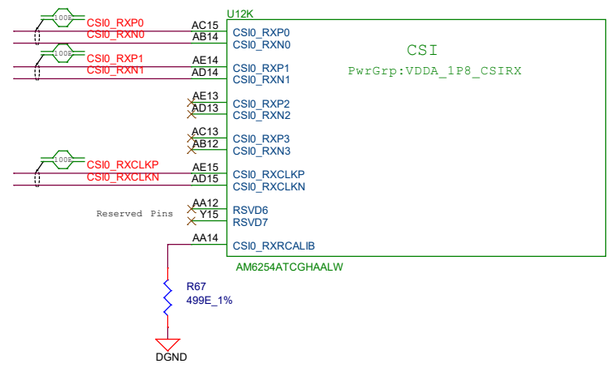
CSI INTERFACE

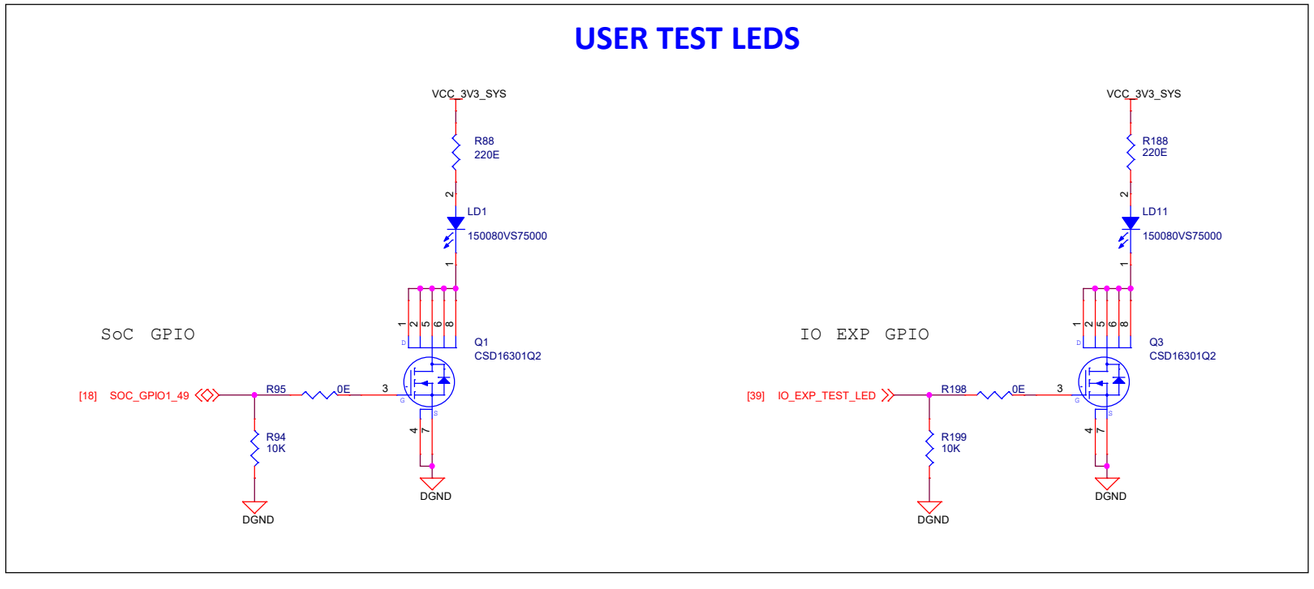
R-Note :-
Based on End product requirement, interface
the CSI signals to respective attach devices

CSI CAMERA HEADER





USER TEST LEDS



Designed for TI by Mistral Solutions Pvt Ltd

Title	CSI INTERFACE & USER TEST LEDS	
Size C	PROC142A1(002)	Rev A1
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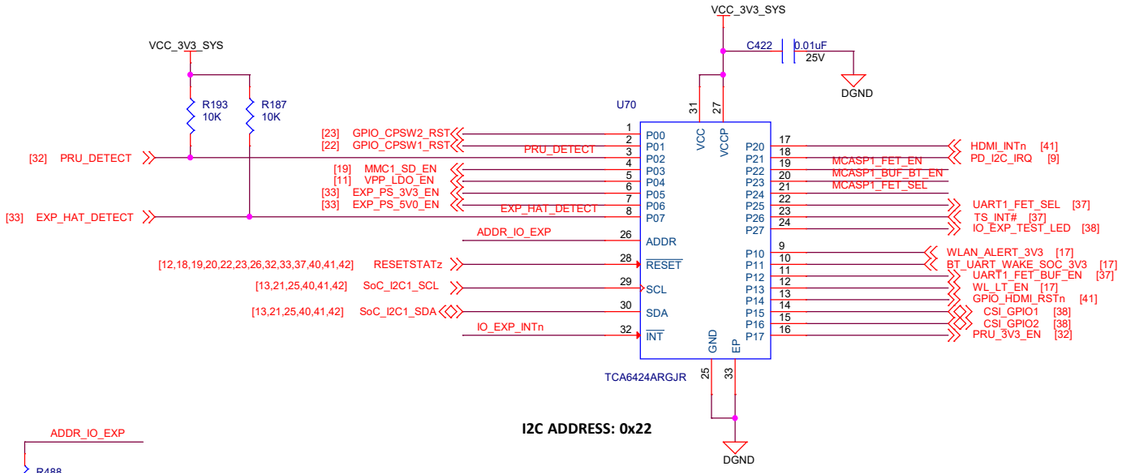
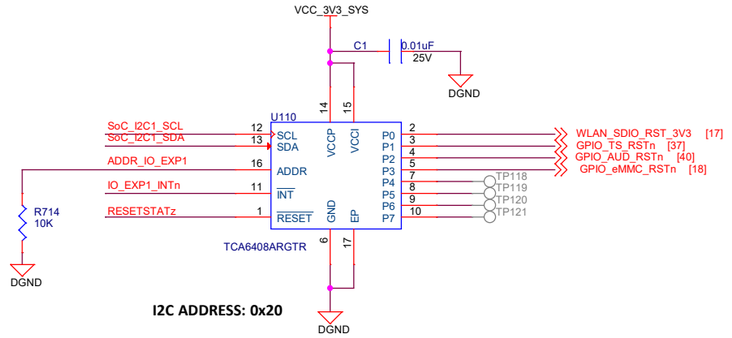
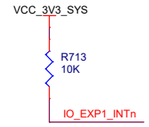
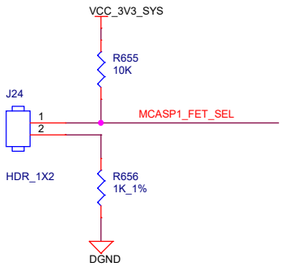
IO EXPANDERS

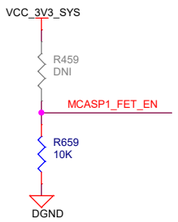


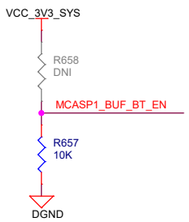


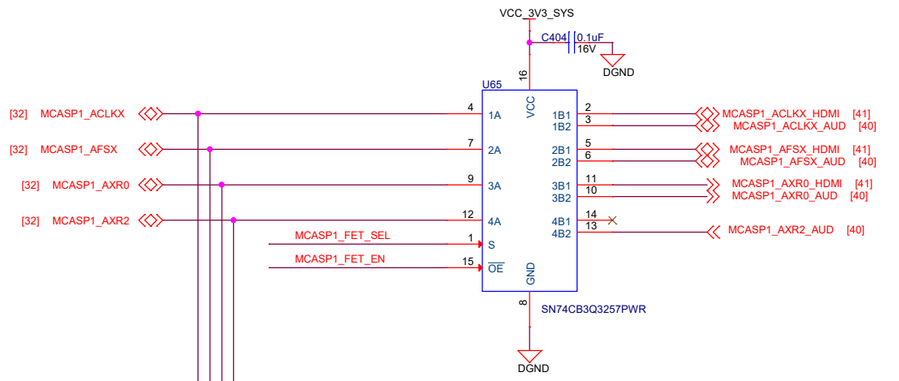


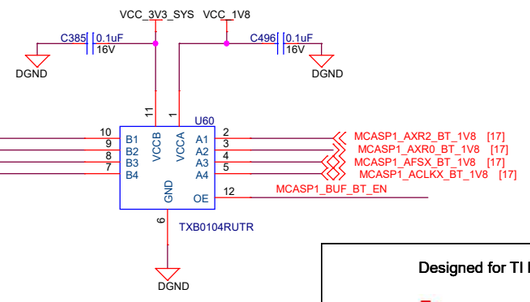
MCASP1 FET SWITCH & BUFFER











OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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Title	IO EXPANDER	
Size	PROC142A1(002)	Rev
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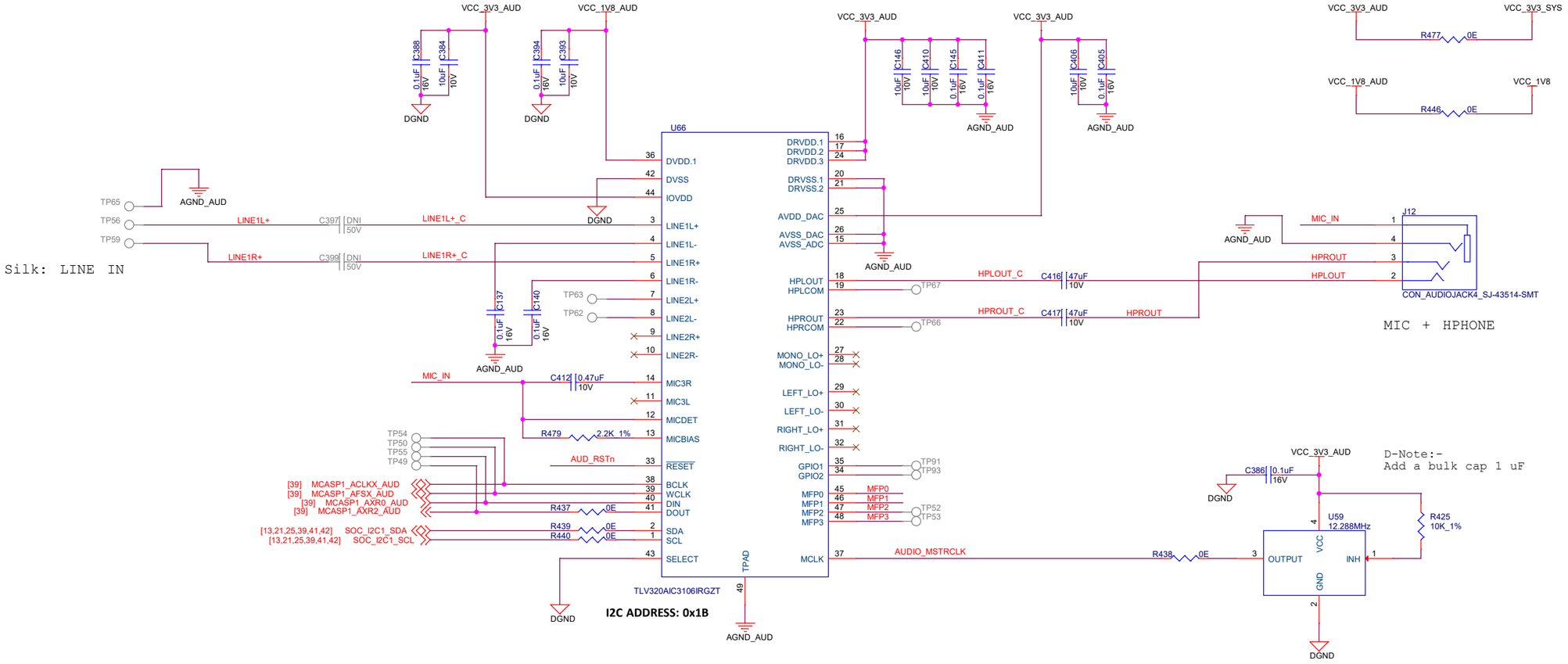
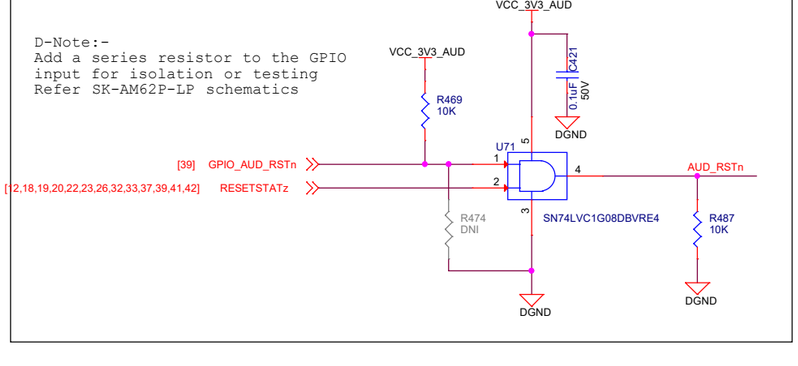
AUDIO CODEC

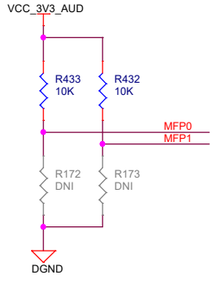


AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



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Title	AUDIO CODEC	
Size C	PROC142A1(002)	Rev A1
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HDMI INTERFACE

R-Note :-
Verify the implementation with
the device manufacturer

U12N AM6254ATCGHAALW

VOUT0
PwrGrp:VDDSHV3

VOUT0_DATA0	U22	SoC_VOUT0_DATA0
VOUT0_DATA1	V24	SoC_VOUT0_DATA1
VOUT0_DATA2	W25	SoC_VOUT0_DATA2
VOUT0_DATA3	W24	SoC_VOUT0_DATA3
VOUT0_DATA4	Y25	SoC_VOUT0_DATA4
VOUT0_DATA5	Y24	SoC_VOUT0_DATA5
VOUT0_DATA6	Y23	SoC_VOUT0_DATA6
VOUT0_DATA7	AA25	SoC_VOUT0_DATA7
VOUT0_DATA8	V21	SoC_VOUT0_DATA8
VOUT0_DATA9	W21	SoC_VOUT0_DATA9
VOUT0_DATA10	V20	SoC_VOUT0_DATA10
VOUT0_DATA11	AA23	SoC_VOUT0_DATA11
VOUT0_DATA12	AB25	SoC_VOUT0_DATA12
VOUT0_DATA13	AA24	SoC_VOUT0_DATA13
VOUT0_DATA14	Y22	SoC_VOUT0_DATA14
VOUT0_DATA15	AA21	SoC_VOUT0_DATA15
VOUT0_PCLK	AC24	SoC_VOUT0_PCLK
VOUT0_DE	Y20	SoC_VOUT0_DE
VOUT0_VSYNC	AC25	SoC_VOUT0_VSYNC
VOUT0_HSYNC	AB24	SoC_VOUT0_HSYNC

SoC_VOUT0_PCLK — R60 0E — HDMI_PCLK

VDD_1V2 — FB3 300E — VHDMI_AVCC_1V2
C232 22uF 10V — DGND
C230 10uF 10V, C231 0.1uF 16V, C229 0.1uF 16V — DGND

VHDMI_CVCC_1V2 — FB2 300E — VDD_1V2
C213, C209, C200, C207, C225, C217: 0.1uF 16V — DGND
C201 10uF 10V — DGND

D-Note:-
Add an additional decap
VHDMI_IOVCC_3V3 — FB1 300E — VCC_3V3_SYS
C223 0.1uF 16V, C212 0.1uF 16V, C199 10uF 10V — DGND
C204 10uF 10V — DGND

VHDMI_IOVCC_3V3
R61 4.7K
R316 DNI, R323 DNI, R325 10K

U10

[13,21,25,39,40,42] SoC_I2C1_SCL	1	CSCL	
[13,21,25,39,40,42] SoC_I2C1_SDA	2	CSDA	
	72	CI2CA	
HDMI_RSTn	51	RESET#	
HDMI_PCLK	22	IDCK	
SoC_VOUT0_DATA0	32	D0	
SoC_VOUT0_DATA1	31	D1	
SoC_VOUT0_DATA2	30	D2	
SoC_VOUT0_DATA3	29	D3	
SoC_VOUT0_DATA4	28	D4	
SoC_VOUT0_DATA5	27	D5	
SoC_VOUT0_DATA6	25	D6	
SoC_VOUT0_DATA7	24	D7	
SoC_VOUT0_DATA8	23	D8	
SoC_VOUT0_DATA9	20	D9	
SoC_VOUT0_DATA10	19	D10	
SoC_VOUT0_DATA11	18	D11	
SoC_VOUT0_DATA12	17	D12	
SoC_VOUT0_DATA13	16	D13	
SoC_VOUT0_DATA14	15	D14	
SoC_VOUT0_DATA15	14	D15	
[32] SoC_VOUT0_DATA16	13	D16	
[32] SoC_VOUT0_DATA17	11	D17	
[32] SoC_VOUT0_DATA18	10	D18	
[32] SoC_VOUT0_DATA19	9	D19	
[32] SoC_VOUT0_DATA20	8	D20	
[32] SoC_VOUT0_DATA21	7	D21	
[32] SoC_VOUT0_DATA22	6	D22	
[32] SoC_VOUT0_DATA23	4	D23	
SoC_VOUT0_HSYNC	34	HSYNC	
SoC_VOUT0_VSYNC	35	VSYNC	
SoC_VOUT0_DE	33	DE	
	36	SPDIF	
HDMI_MSTRCLK	38	MCLK	
[39] MCASP1_ACLKX_HDMI	45	SCK	
[39] MCASP1_AFSX_HDMI	44	WS	
	60, 66	AVCC12_1, AVCC12_2	
	5	CVCC12_1	
	12	CVCC12_2	
	26	CVCC12_3	
	42	CVCC12_4	
	47	CVCC12_5	
	53	CVCC12_6	
	3	IOVCC1	
	21	IOVCC2	
	46	IOVCC3	
HDMI_I2C_SDA	48	DSDA	
HDMI_I2C_SCL	49	DSCL	
HDMI_INTn [39]	52	INT	
HDMI_HPD	54	HPD	
HDMI_EXTSWING	56	EXT_SWING	
HDMI_CLK+	59	TXC+	
HDMI_CLK-	58	TXC-	
HDMI_TX0+	62	TX0+	
HDMI_TX0-	61	TX0-	
HDMI_TX1+	65	TX1+	
HDMI_TX1-	64	TX1-	
HDMI_TX2+	68	TX2+	
HDMI_TX2-	67	TX2-	
HDMI_CEC	71	CEC_A	
HDMI_CEC_D	50	CEC_D	
	55	RSVDL	
R62 0E	69	IO_SEL	
	70	VDDQ	
HDMI_AUDD1	41	SD0	
HDMI_AUDD2	40	SD1	
HDMI_AUDD3	39	SD2	
	37	SD3	
	57	IOGND	
	43	CGND	
	63	AGND	
	73	PAD	

R327 7.5K, R326 DNI — DGND DGND

D-Note:-
REXT_SWING modified to
7.5K 5%. Value changed
for Internal testing
(Radiated Emission)
Refer device data sheet
for the
recommended value

MCASP1_AXR0_HDMI [39]
HDMI_AUDD1 — TP16
HDMI_AUDD2 — TP14
HDMI_AUDD3 — TP88
HDMI_CEC_D — TP18

D-Note:-
Add bulk caps

HDMI ESD DEVICE

VCC_3V3_SYS — C248 10uF 10V — DGND
VCC_5V0 — C219 10uF 10V — DGND
VCC_5V0_HDMICONN — C211 10uF 10V — DGND
VCC_3V3_SYS — R314 0E

U50 TPD12S016PWR

HDMI_TX0+	18	D0+	
HDMI_TX0-	17	D0-	
HDMI_TX1+	21	D1+	
HDMI_TX1-	20	D1-	
HDMI_TX2+	23	D2+	
HDMI_TX2-	22	D2-	
HDMI_CLK+	16	CLK+	
HDMI_CLK-	15	CLK-	
HDMI_CONN_I2CSCL	8	SCL_B	
HDMI_CONN_I2CSDA	9	SDA_B	
HDMICONN_HPD	10	HPD_B	
HDMI_CONNCEC	7	CEC_B	
	24	VCCA	
	11	VCC5V	
	13	5V_OUT	
	12	CT_HPD	
	5	LS_OE	
	2	SCL_A	HDMI_I2C_SCL
	3	SDA_A	HDMI_I2C_SDA
	4	HPD_A	HDMI_HPD
	1	CEC_A	HDMI_CEC
	6, 14, 19	GND1, GND2, GND3	

D-Note:-
TPD12S016PWR has integrated pullup or pulldown resistors on the
I2C and HPD lines hence no external pullup or pulldown required.

D-Note:-
Add a bulk cap

VCC_3V3_SYS — C20 0.1uF 16V — DGND
R41 10K_1%
U7 12.288MHz: INH, VCC, OUTPUT, GND — DGND
R34 DNI
[33] AUDIO_EXT_REFCLK1

R-Note:-
M_CLK is not used

CAD Note:-
Move the net after the 0R and add a 0R
to choose the required configuration

R287 0E — Sil9022ACNU — DGND DGND

I2C ADDRESS: 0x3B, 0x3F, 0x62

HDMI CONNECTOR

J5 — CON_HDMI_1X19_F

HDMI_TX2+	1	
HDMI_TX2-	2	
HDMI_TX1+	3	
HDMI_TX1-	4	
HDMI_TX0+	5	
HDMI_TX0-	6	
HDMI_CLK+	7	
HDMI_CLK-	8	
HDMI_CONNCEC	9	
HDMI_CONN_I2CSCL	10	
HDMI_CONN_I2CSDA	11	
VCC_5V0_HDMICONN	12	
HDMICONN_HPD	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20, 21, 22, 23	

FL17 120E — DGND HDMI_EARTH

Silk: HDMI

HDMI RESET

D-Note:-
Add a series resistor to the GPIO
input for isolation or testing
Refer SK-AM62P-LP schematics

VCC_3V3_SYS — R389 10K
VCC_3V3_SYS — C323 0.1uF 50V — DGND
U54 SN74LVC1G08DBVRE4
[39] GPIO_HDMI_RST
[12,18,19,20,22,23,26,32,33,37,39,40,42] RESETSTATz
HDMI_RSTn
R390 DNI
R373 10K — DGND DGND

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Title	HDMI INTERFACE		
Size	PROC142A1(002)		Rev
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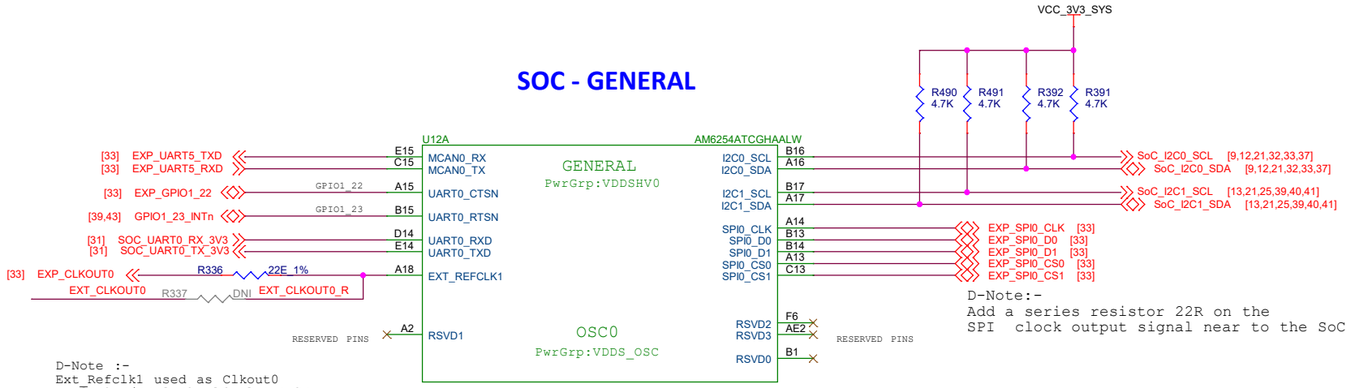
SOC - GENERAL

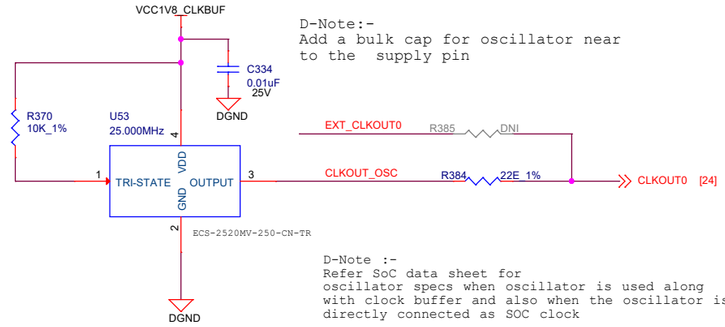


D-Note :-
Ext_Refclk1 used as Clkout0
A clock signal should always be connected point to point without any branches. When connecting Clkout0 to more than one (multiple) clock inputs, use a buffer with one input and multiple outputs.

D-Note:-
Add a series resistor 22R on the SPI clock output signal near to the SoC

OSCILLATOR

D-Note
Refer SoC data sheet for oscillator specs



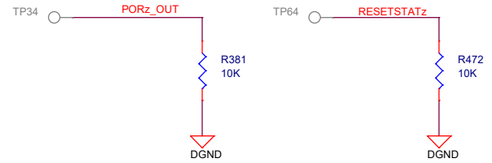
D-Note:-
Add a bulk cap for oscillator near to the supply pin

D-Note :-
Refer SoC data sheet for oscillator specs when oscillator is used along with clock buffer and also when the oscillator is directly connected as SOC clock

D-Note :-
EXTINTn is an open-drain output type buffer, fail-safe IO.
An external pullup is recommended when a trace or external input is connected

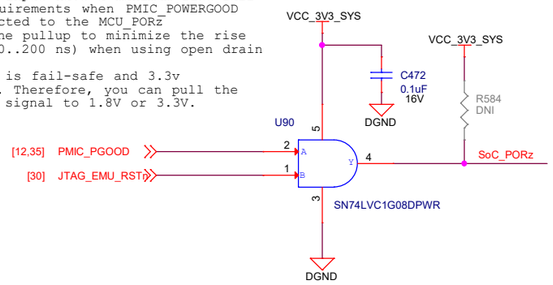
SOC - RESET

D-Note :-
Provide provision for a pulldown
Populate when attached device is connected
Refer SOC data sheet pin connectivity requirements



D-Note :-
Pull-down resistor on PORz_OUT and RESETSTATz is provided to hold the attached device in reset condition during SOC reset and power-up

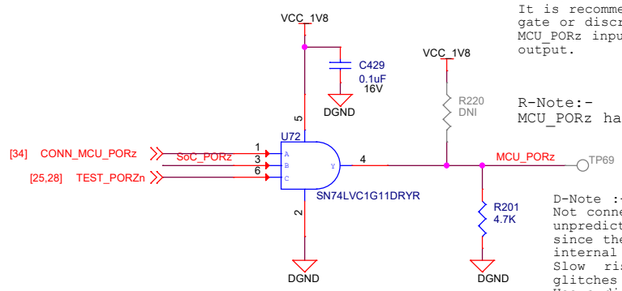
D-Note :-
MCU_PORz input have a maximum rise/fall time requirements when PMIC_POWERGOOD is connected to the MCU_PORz
Adjust the pullup to minimize the rise time (100..200 ns) when using open drain output
MCU_PORz is fail-safe and 3.3v tolerant. Therefore, you can pull the MCU_PORz signal to 1.8V or 3.3V.



MCU POWER ON RESET

D-Note :-
It is recommended to connect the output from logic gate or discrete buffer (with fast rise time) as MCU_PORz input rather that slow rising open drain output.

R-Note:-
MCU_PORz has pulldown configured



D-Note :-
Not connecting a valid MCU_PORz could cause unpredictable and probably random behavior, since the device is not getting a valid reset, internal circuits would be in random states. Slow rising reset signal could cause glitches internal to the SOC reset circuit. Use a discrete buffer and have the fast rising output of the buffer drive the MCU_PORz is recommended

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Title	OSCILLATOR	
Size: C	PROC142A1(002)	Rev: A1
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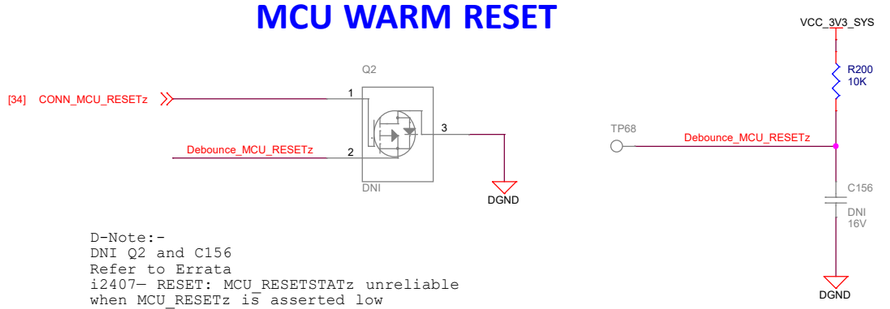
EXTERNAL RESET INPUT AND SCHMITT TRIGGER DEBOUNCE LOGIC

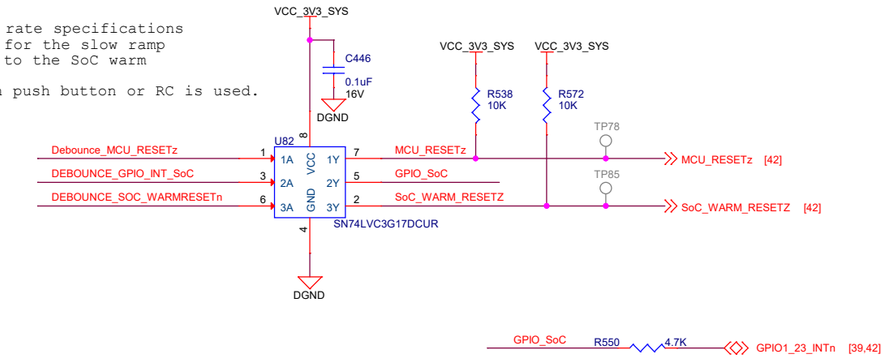
MCU WARM RESET



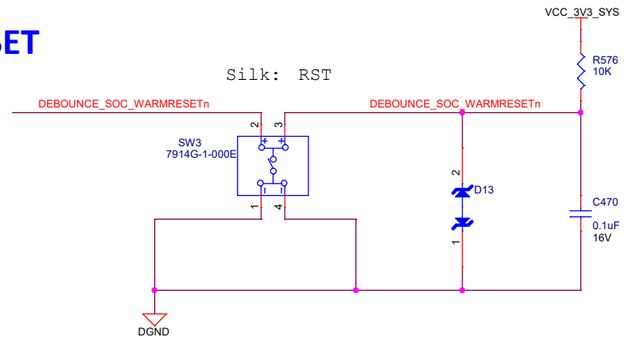
D-Note:-
DNI Q2 and C156
Refer to Errata
i2407– RESET: MCU_RESETSTATz unreliable
when MCU_RESETz is asserted low

DEBOUNCE CIRCUIT

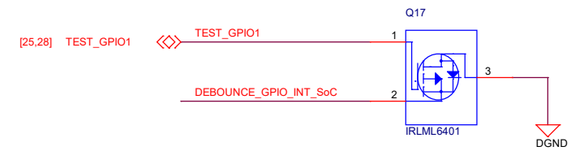
D-Note:-
LVCMOS inputs have slew rate specifications
Schmitt trigger is used for the slow ramp
pushbutton RC connected to the SoC warm
reset inputs
This is recommended when push button or RC is used.

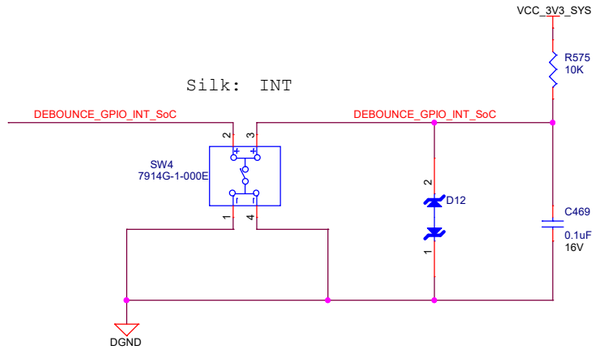


SOC WARM RESET



USER INTERRUPT





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Title	RESET	
Size	PROC142A1(002)	Rev
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MOUNTING HARDWARE

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

BARE PCB

PROC142E1

PROC142E1

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

LABELS

Board Serial No.

LBL1
PCB LABEL
DNI

Assembly Revision

LBL2
PCB LABEL
DNI

STANDOFF,SCREW & WASHER FOR PCIe M.2

ACC1
9774015243R

MH1
FLAT WASHER_M2
3356

MH2
PAN HEAD_M2 X 5
MPMS 002 0005 PH

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

ORDERABLE PART NO

LBL3
PCB LABEL
DNI

Oderable Part Number	
Variant	**Label Text**
001	SK-AM62-P1
002	SK-AM62B-P1

R-Note:-
Refer STRAP CONFIGURATION OF ETHERNET PHYS page from SK-AM64B schematics

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TEXAS INSTRUMENTS

MISTRAL

Title	HARDWARE SCHEMATICS	
Size C	PROC142A1(002)	Rev A1
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