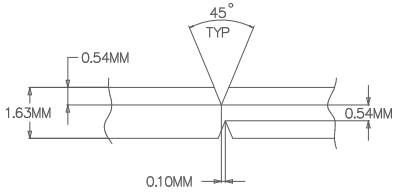
Symbol	Count	Hole Size	Plated	Hole Type	Hole Tolerance (+)	Hole Tolerance (-)	Hole Length
C	5	7.87mil (0.200mm)	PTH	Round			-
⌘	1546	8.00mil (0.203mm)	PTH	Round	3.00mil (0.076mm)	3.00mil (0.076mm)	-
D	4	10.00mil (0.254mm)	PTH	Round	3.00mil (0.076mm)	3.00mil (0.076mm)	-
A	39	12.00mil (0.305mm)	PTH	Round	3.00mil (0.076mm)	3.00mil (0.076mm)	-
✡	4	23.62mil (0.600mm)	PTH	Slot			51.18mil (1.300mm)
B	2	33.47mil (0.850mm)	NPTH	Round			-
⌑	4	33.47mil (0.850mm)	PTH	Round			-
◇	10	35.43mil (0.900mm)	PTH	Round			-
✪	30	39.37mil (1.000mm)	PTH	Round	7.87mil (0.200mm)	7.87mil (0.200mm)	-
✖	4	39.37mil (1.000mm)	PTH	Rectangle			(Mixed)
□	25	40.00mil (1.016mm)	PTH	Round			-
○	8	40.16mil (1.020mm)	NPTH	Round			-
◎	8	40.16mil (1.020mm)	PTH	Round			-
▽	6	47.24mil (1.200mm)	PTH	Round			-
✲	1	62.99mil (1.600mm)	NPTH	Round	3.94mil (0.100mm)	0.00mil (0.000mm)	-
⊕	4	66.93mil (1.700mm)	NPTH	Round			-
⊡	2	66.93mil (1.700mm)	PTH	Round			-
▽	2	127.95mil (3.250mm)	NPTH	Round			-
⊠	11	160.00mil (4.064mm)	NPTH	Round	2.00mil (0.051mm)	2.00mil (0.051mm)	-
	1715 Total						

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



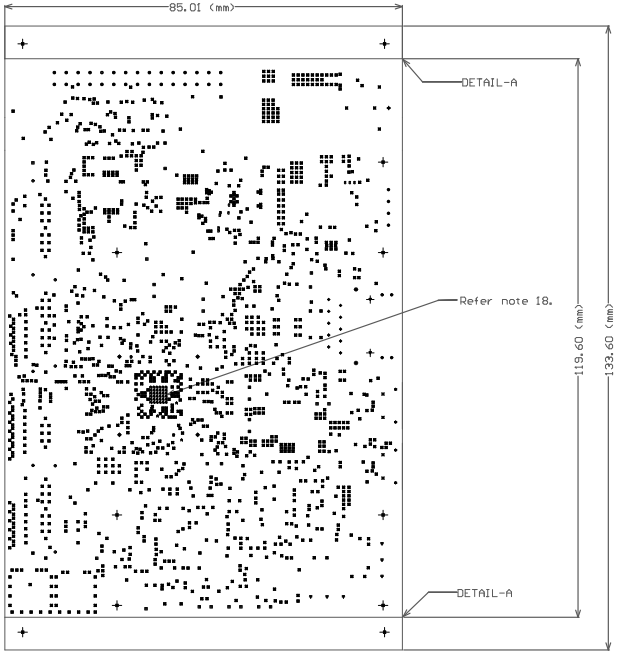
DETAIL-A(V. SCORE DETAILS)
SCALE:NTS

2 IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	MICROSTRIP	L1, L10	5.5	---	50	L02,L09
02	EDGE COUPLED MICROSTRIP	L1, L10	4	4.5	90	L02,L09
03	EDGE COUPLED MICROSTRIP	L1, L10	4	7	100	L02,L09
04	EDGE COUPLED MICROSTRIP	L1, L10	4	5.6	120	L04,L07
05	STRIPLINE	L3, L8	5.1	---	50	L02/L04,L07/L09
06	EDGE COUPLED STRIPLINE	L3	4	5	90	L02/L04
07	EDGE COUPLED STRIPLINE	L3, L8	4	8	100	L02/L04,L07/L09

THIS IS AN IMPEDANCE CONTROLLED BOARD.

NOTE :
EXTERNAL LAYER CU THICKNESSES ARE FINISHED THICKNESS AFTER PLATING.



2 LAYER STACKUP

Layer	Name	Material	Thickness	Constant		Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	2.00mil	3.9		
3	Top Layer	Copper	1.85mil			
4	Dielectric 1	FR-4 High Tg	3.70mil	3.79		
5	GND1	Copper	1.26mil			
6	Dielectric 2	FR-4 High Tg	6.00mil	4.46		
7	SIG1	Copper	1.26mil			
8	Dielectric 3	FR-4 High Tg	7.10mil	3.79		
9	GND2	Copper	1.26mil			
10	Dielectric 4	FR-4 High Tg	4.00mil	4.4		
11	PWR1	Copper	1.26mil			
12	Dielectric 5	FR-4	5.29mil	3.79		
13	PWR2	Copper	1.26mil			
14	Dielectric 6	FR-4 High Tg	4.00mil	4.4		
15	GND3	Copper	1.26mil			
16	Dielectric 7	FR-4 High Tg	7.10mil	3.79		
17	SIG2	Copper	1.26mil			
18	Dielectric 8	FR-4 High Tg	6.00mil	4.46		
19	GND4	Copper	1.26mil			
20	Dielectric 9	FR-4 High Tg	3.70mil	3.79		
21	Bottom Layer	Copper	1.85mil			
22	Bottom Solder	Solder Resist	2.00mil	3.9		
23	Bottom Overlay					

NOTES : UNLESS OTHERWISE SPECIFIED.

1. FABRICATE PER IPC-6012A CLASS 2.
2. FOR IMPEDANCE DETAILS REFER STACKUP & IMPEDANCE TABLE.
3. PRINTED WIRING BOARD SHALL COMPLY WITH REQUIREMENTS OF ANSI/J-STD-003.
4. SURFACE FINISH: IMMERSION GOLD
5. SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR RED.
6. SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK.
7. THIS PRINTED WIRING BOARD IS DESIGNED WITH A MINIMUM CONDUCTOR WIDTH AND SPACING OF 4 MIL & 3.5 MILS.
8. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
9. ALL VIAS SHOULD BE FILLED WITH NON CONDUCTIVE EPOXY AND SURFACE SHOULD BE FLAT
10. VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
11. MANUFACTURER'S IDENTIFICATION, DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
12. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL
13. BOARD DIMENSIONS ARE IN MM.
14. BOW AND TWIST SHALL NOT EXCEED 0.7% OF LONGEST SIDE
15. TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
16. PCB Material must meet or exceed UL94V-0 requirements.
    PCB must bear the UL94V-0 registered material ID number.
17. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL
18. ON BOTTOM LAYER SOLDER MASK SHOULD BE OPENED IN THE INDICATED AREA.

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 3.5 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.127mm (5MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 64 MIL (1.63mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER RED
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[X] 8 & 12 MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[X] BOARD IMPEDANCE SHALL BE FOLLOWED AS PER THE IMPEDANCE SPECIFICATION TABLE.
[ ]

TEXAS INSTRUMENTS

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC103	REV: C	SUN REV: Not In VersionControl
LAYER NAME = M23 Drill Drawing / M23 Drill Diagram / M23 Board Dimensions	TID #: N/A		
PLOT NAME = Fab Notes	GENERATED : 16-06-2022 19:51:08	TEXAS INSTRUMENTS	

PROJECT TITLE: TMDS273GPEVM	
DESIGNED FOR: Public Release	
FILE NAME: PROC103C_BRD.PcbDoc	
ENGINEER: Adrian Ozer/Mike Pridgen	LAYOUT BY: Mistral
SCALE: 0.62	ALTIUM DESIGNER VERSION: 19.0.14.431