AM62x STARTER KIT EVM

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VER	0.07

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TEXAS INSTRUMENTS

MISTRAL

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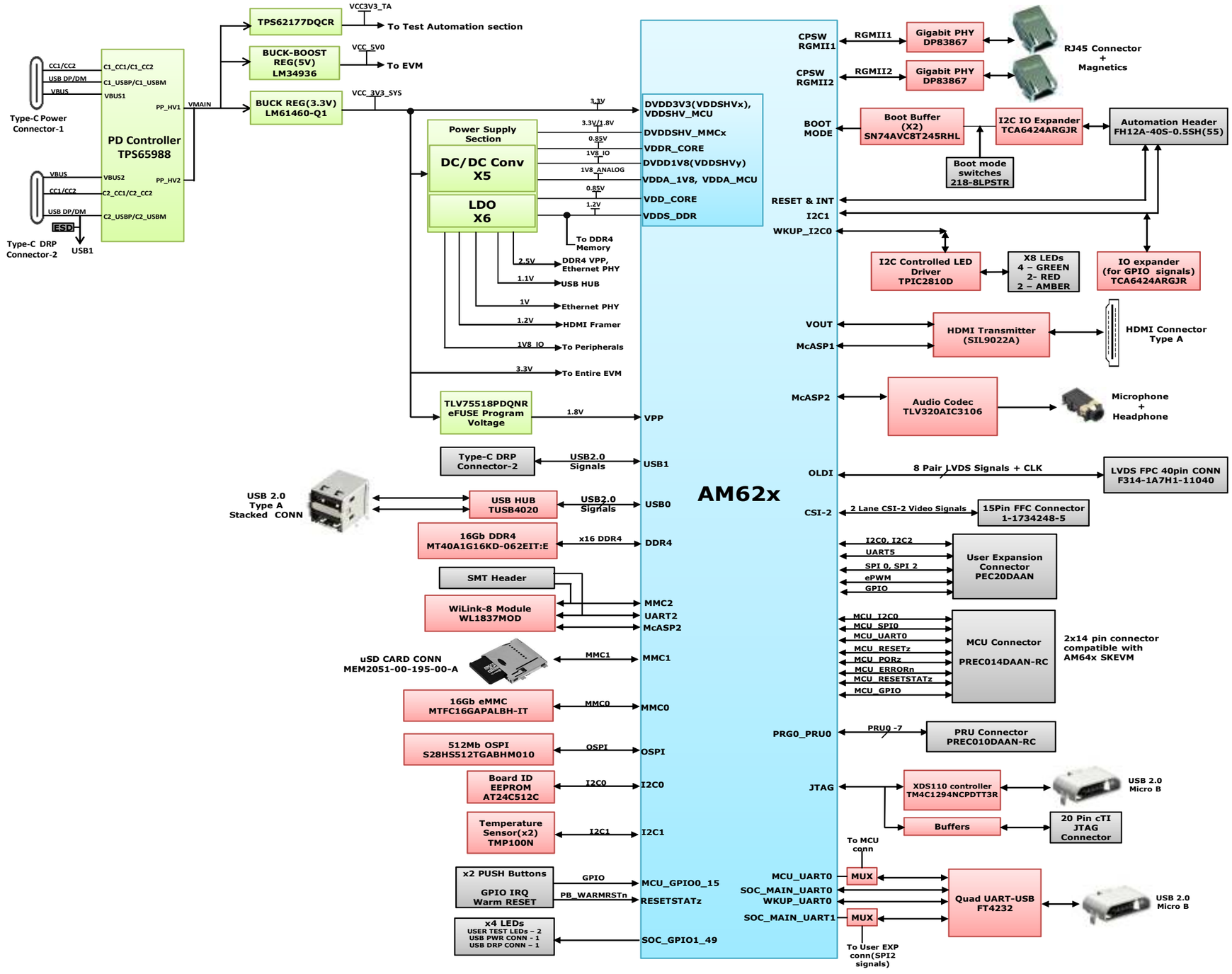
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	19 JULY 2021	Initial Draft	Mistral Design Team		
0.02	11 AUG 2021	Updated for TI's Part-1 Review comments	Mistral Design Team	TI	
0.03	06 SEPT 2021	Updated for Internal Review comments	Mistral Design Team		
0.04	24 SEPT 2021	Updated for TI's Part-2 Review comments	Mistral Design Team	TI	
0.05	1 OCT 2021	Updated for Internal and TI Review comments	Mistral Design Team	TI	
0.06	7 OCT 2021	Updated for TI Review comments	Mistral Design Team	TI	
0.07	11 NOV 2021	Baselined and Released	Mistral Design Team		

BLOCK DIAGRAM AM62x SKEVM



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Title	BLOCK DIAGRAM AM62x SKEVM		
Size	PROC114E1		Rev
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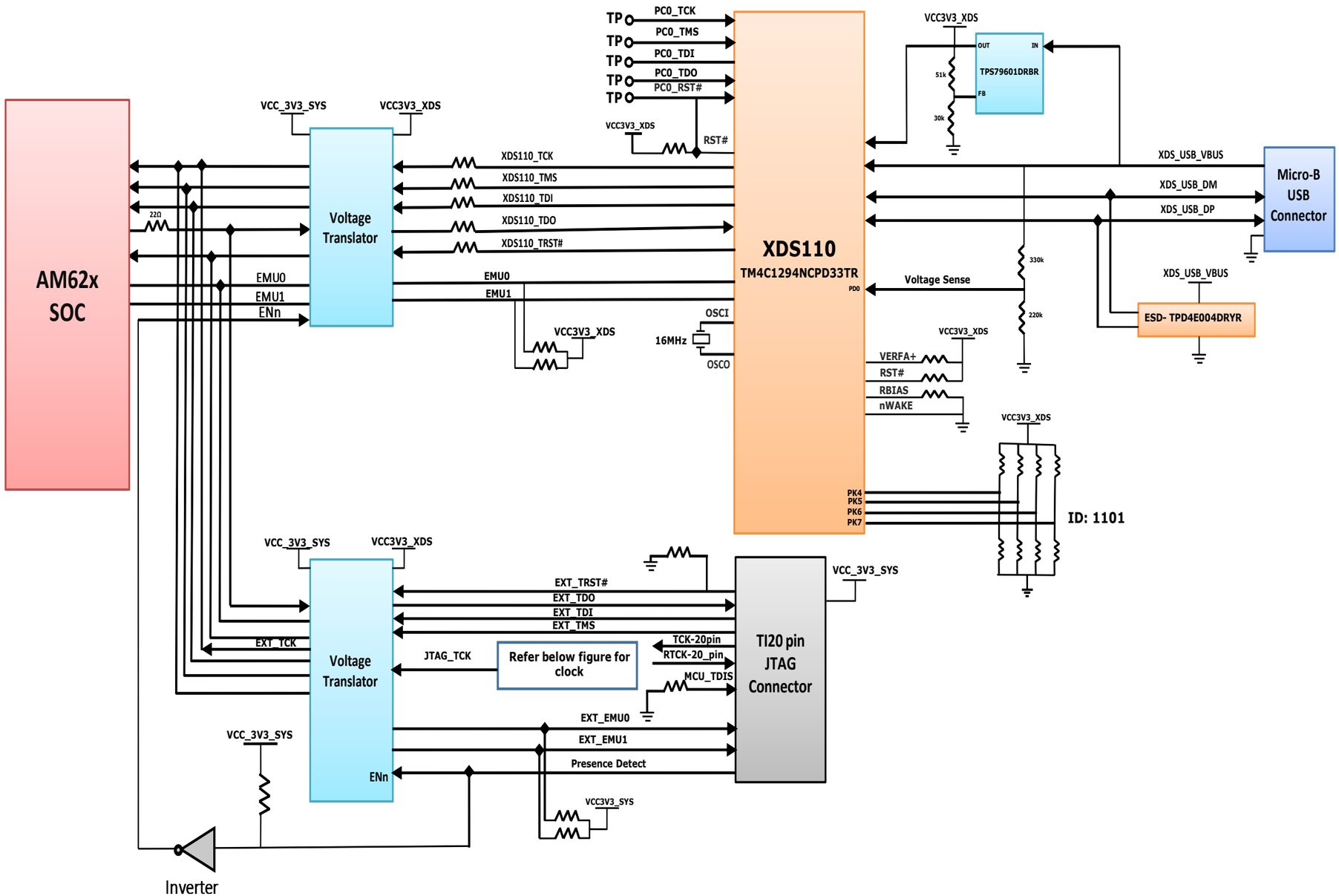
BLOCK DIAGRAM_XDS110



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Title	BLOCK DIAGRAM_XDS110	
Size: C	PROC114E1	Rev: E1
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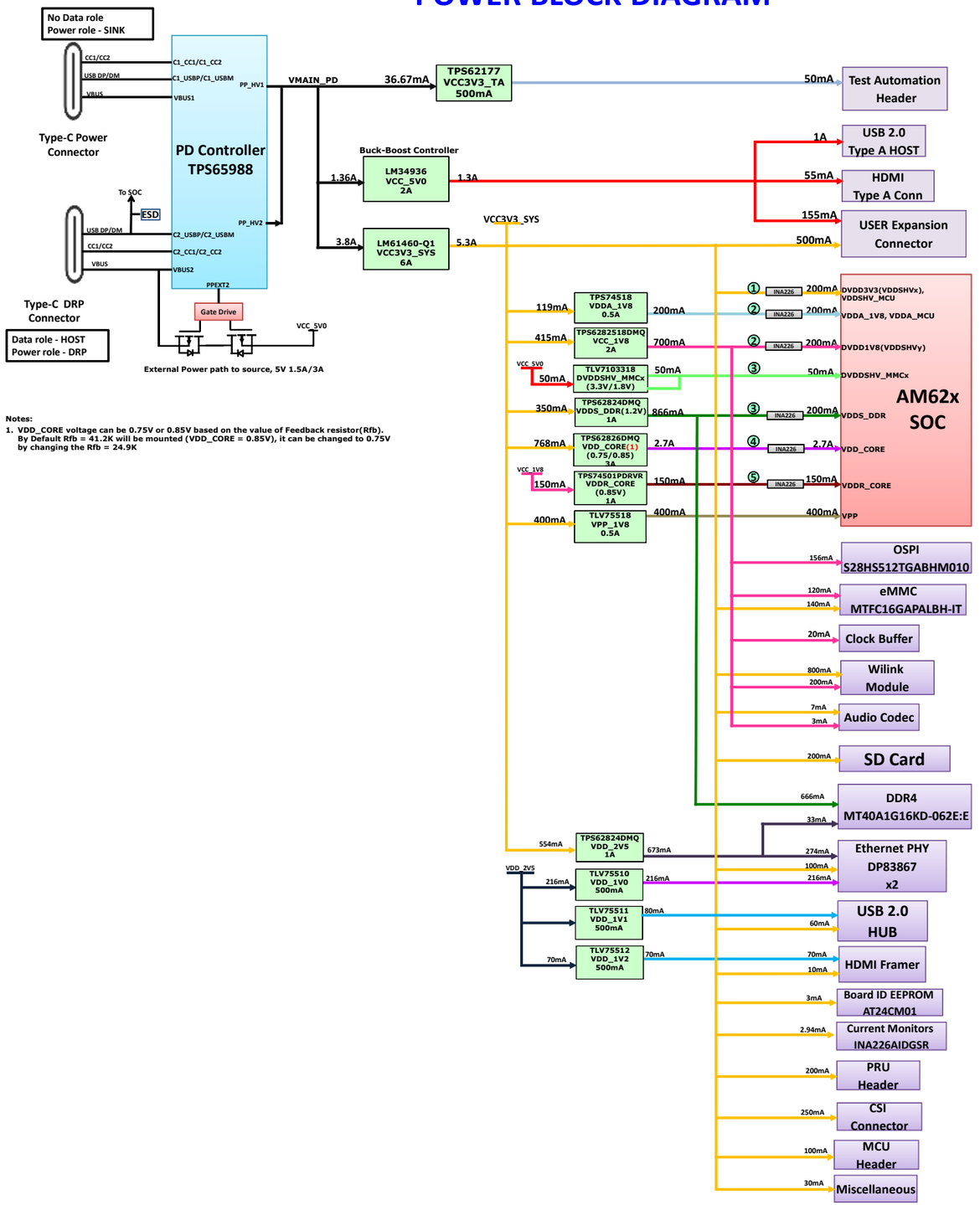
POWER BLOCK DIAGRAM



Notes:

1. VDD_CORE voltage can be 0.75V or 0.85V based on the value of Feedback resistor(Rfb). By Default Rfb = 41.2K will be mounted (VDD_CORE = 0.85V), it can be changed to 0.75V by changing the Rfb = 24.9K

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Title	POWER BLOCK DIAGRAM	
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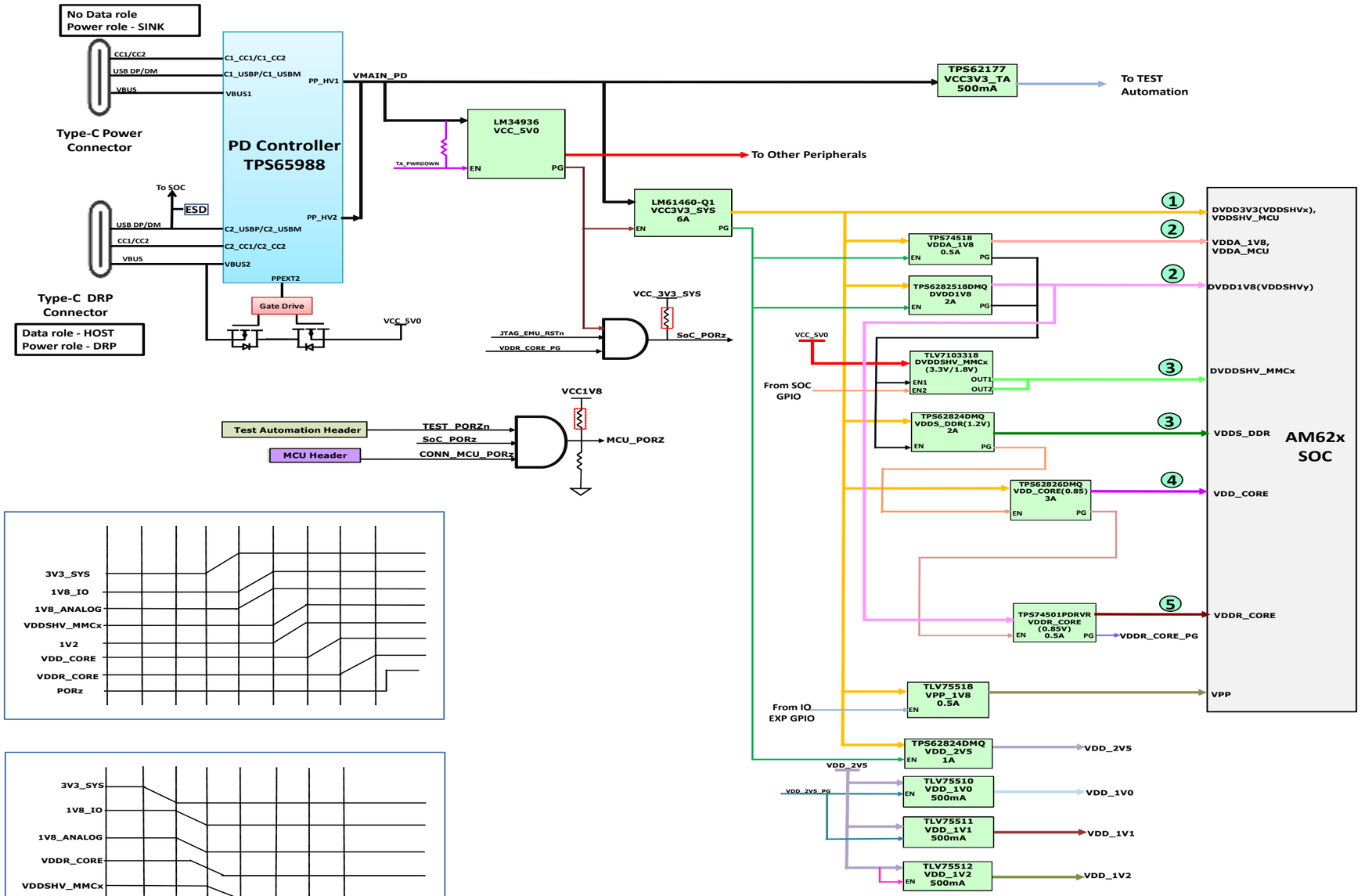
POWER SEQUENCE



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Title	POWER SEQUENCE		
Size C	PROC114E1		Rev E1
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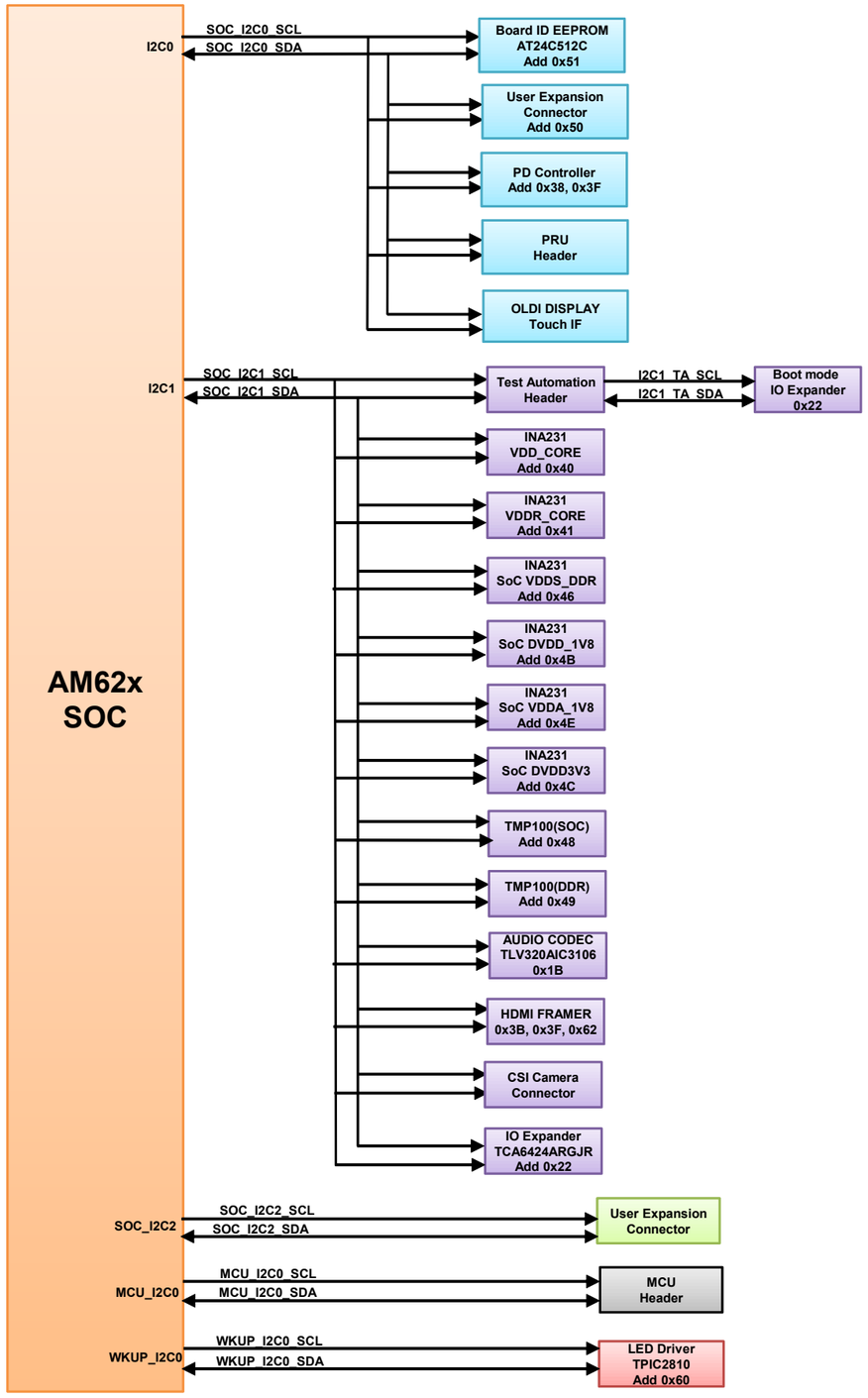
I2C TREE



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Title	I2C TREE	
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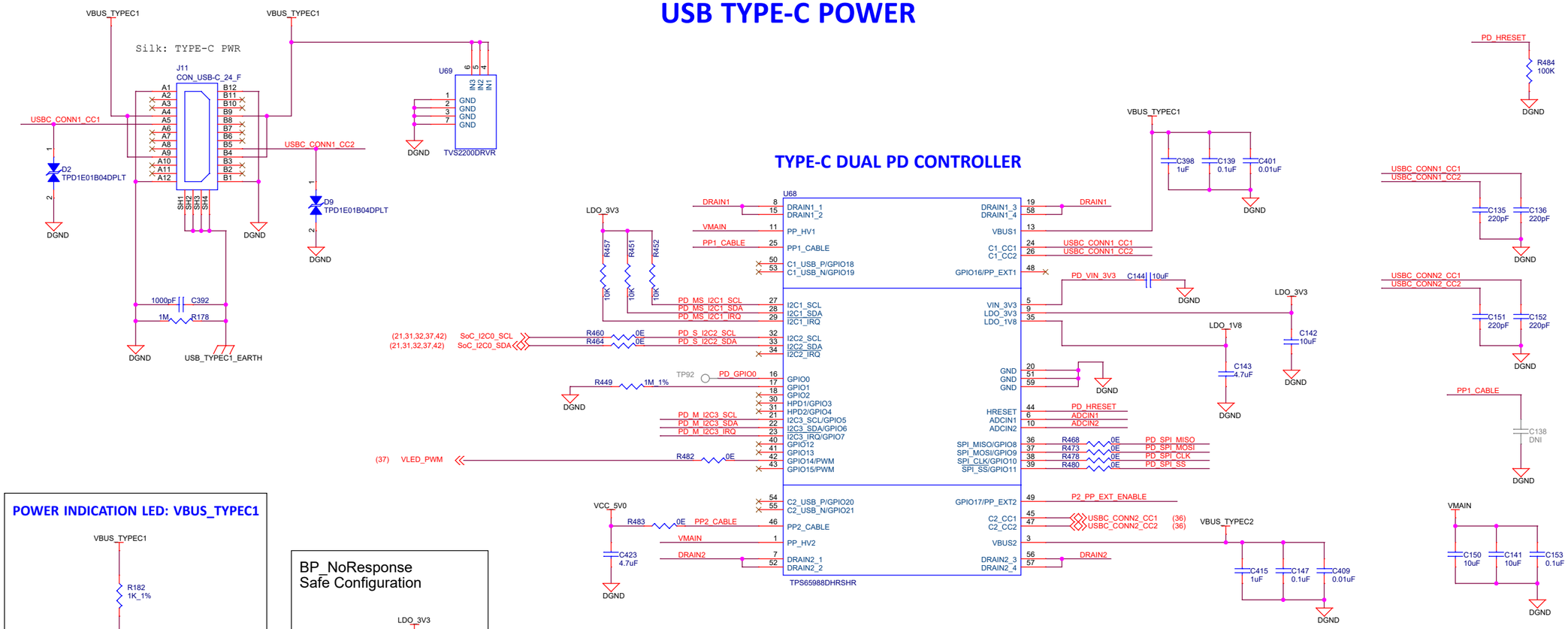
GPIO MAPPING TABLE

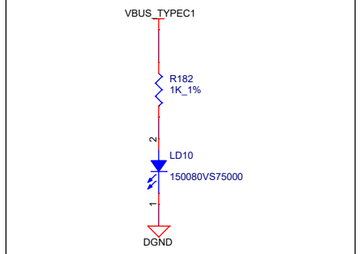
SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt PRU Connector Interrupt	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
11										
12										
IO EXPANDER - 01										
1	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER - P00		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P02		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER -P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	RPI_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	RPI_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER - P07		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P10		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P11		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Backlight Enable	VLED_ENB	ENABLE	IO EXPANDER - P26		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3

USB TYPE-C POWER

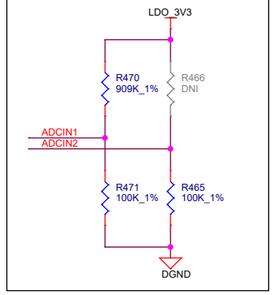
TYPE-C DUAL PD CONTROLLER



POWER INDICATION LED: VBUS_TYPEC1

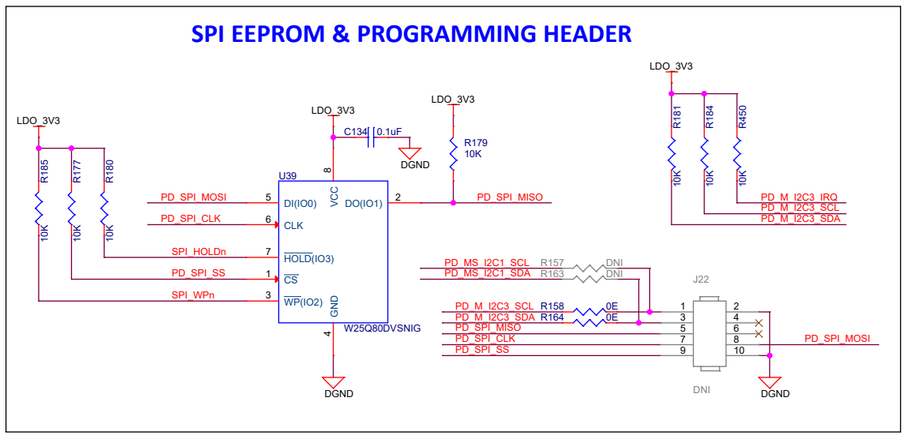


BP_NoResponse Safe Configuration

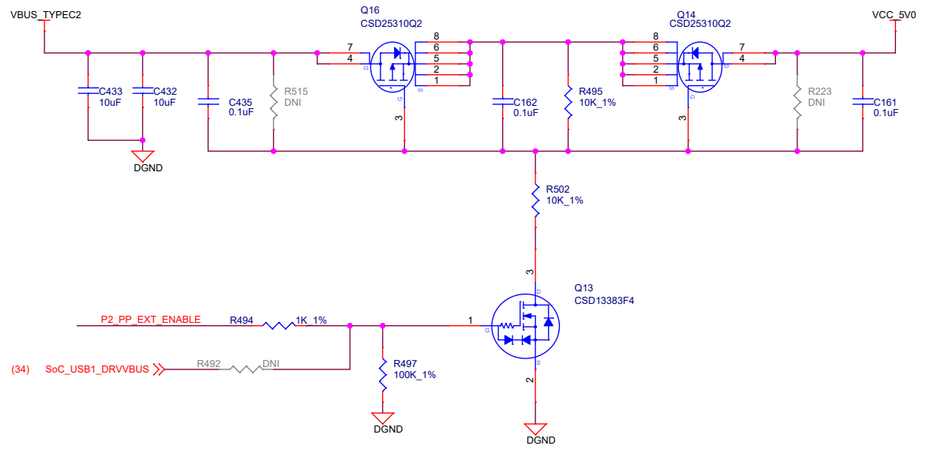


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

SPI EEPROM & PROGRAMMING HEADER



EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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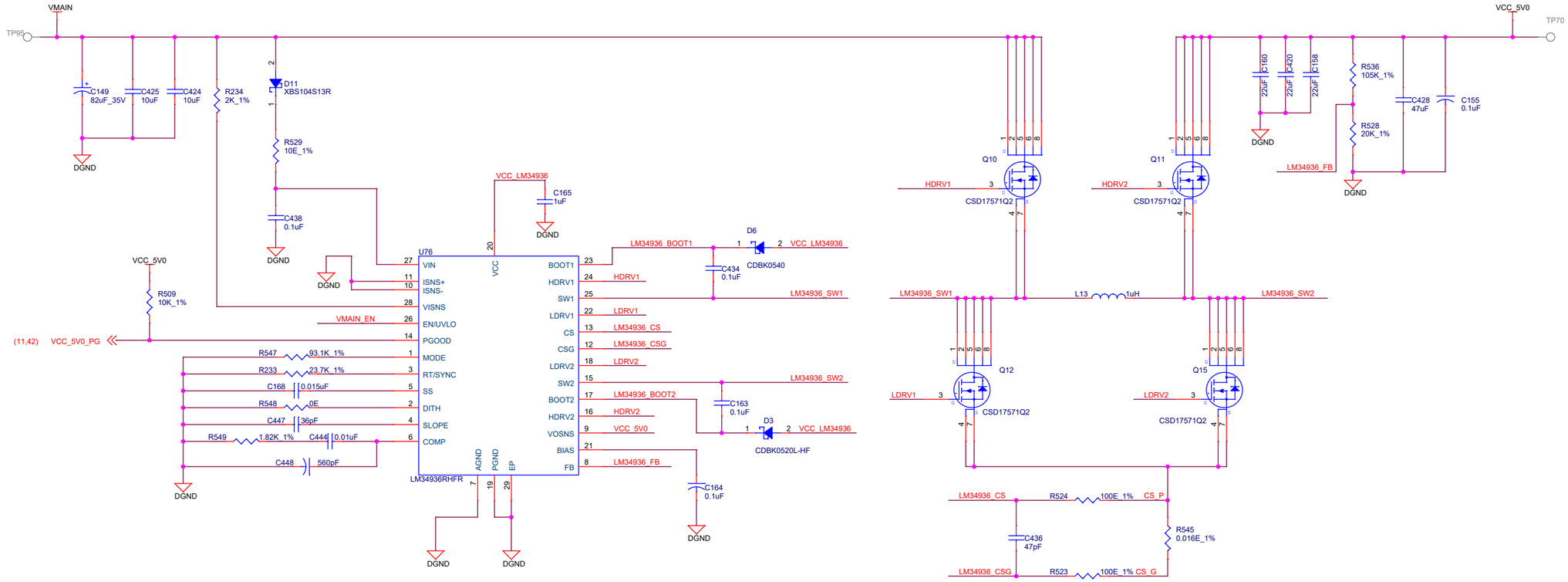
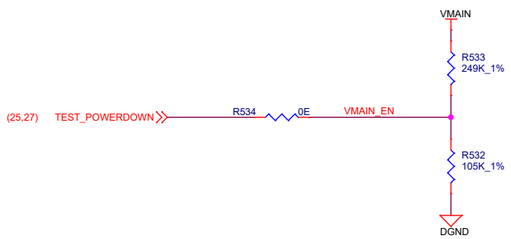
PERIPHERAL POWER SUPPLY-1

VinMin = 4.5V
VinMax = 24V
Vout = 5V @ 4A



Power Cycle control from Test Automation



GROUND TEST POINTS

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Title	PERIPHERAL POWER SUPPLY -1	
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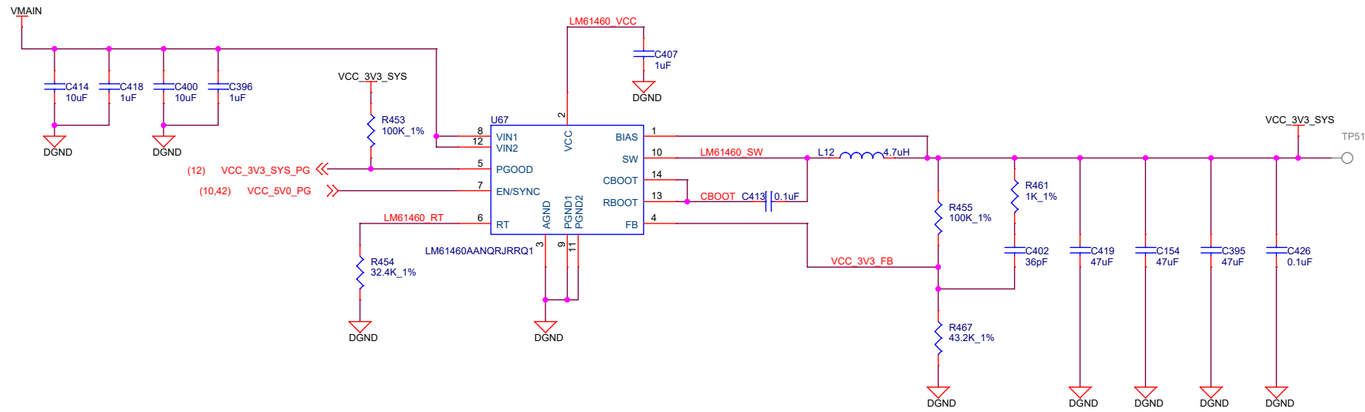
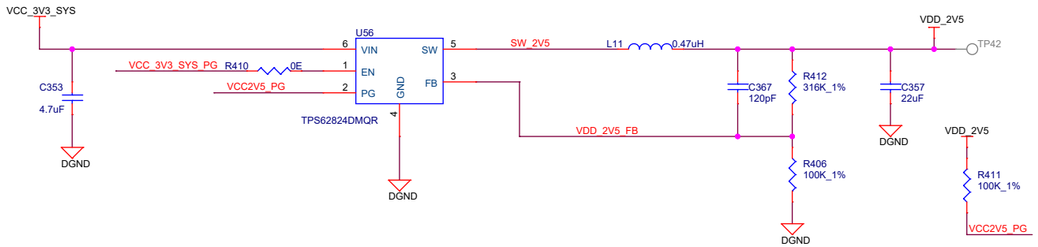
PERIPHERAL POWER SUPPLY-2

3.3V, 6.0AMPS SUPPLY

VinMin = 4.5V
VinMax = 24V
Vout = 3.3V @ 6A

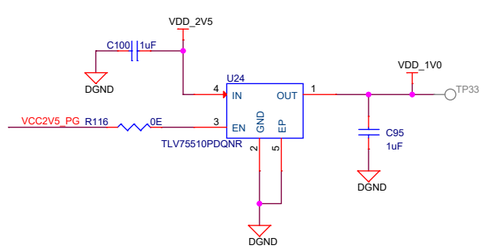


2.5V, 1.0AMPS SUPPLY

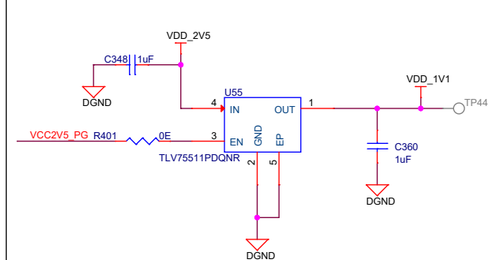


1.8V VPP, 0.5AMPS SUPPLY

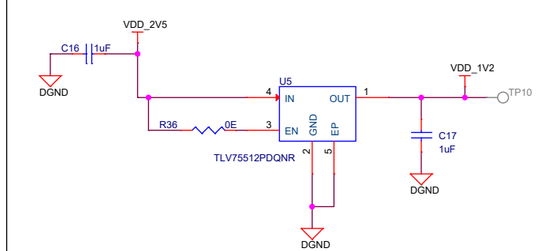
1.0V, 0.5AMPS SUPPLY



1.1V, 0.5AMPS SUPPLY



1.2V, 0.5AMPS SUPPLY



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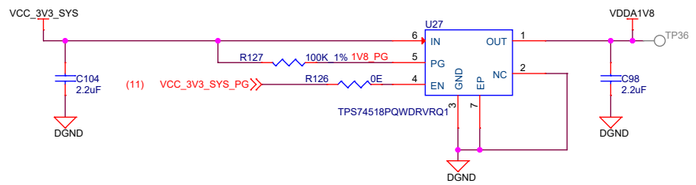
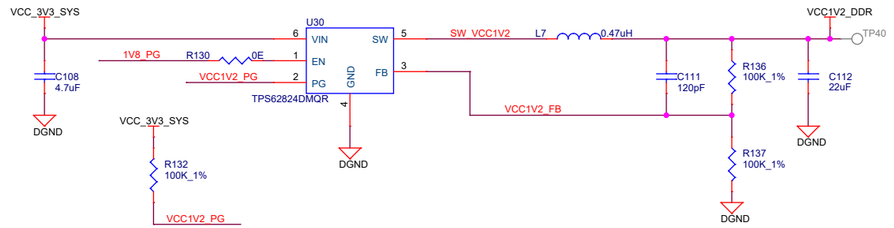
SOC POWER SUPPLY

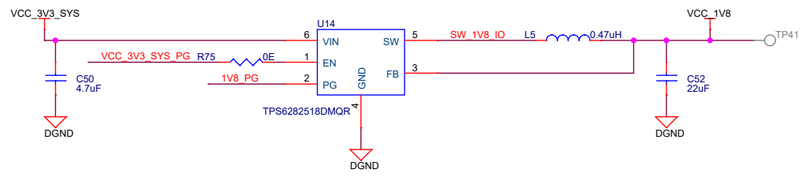
1.8V ANALOG, 0.5 AMPS SUPPLY



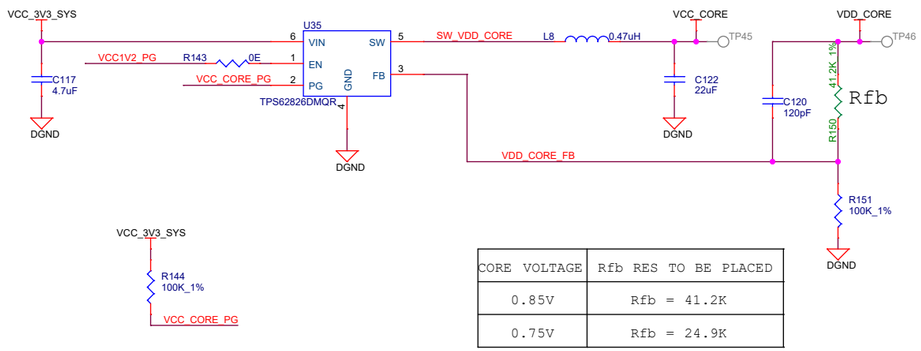
1.2V , 1.0 AMPS SUPPLY



1.8V IO, 2.0 AMPS SUPPLY

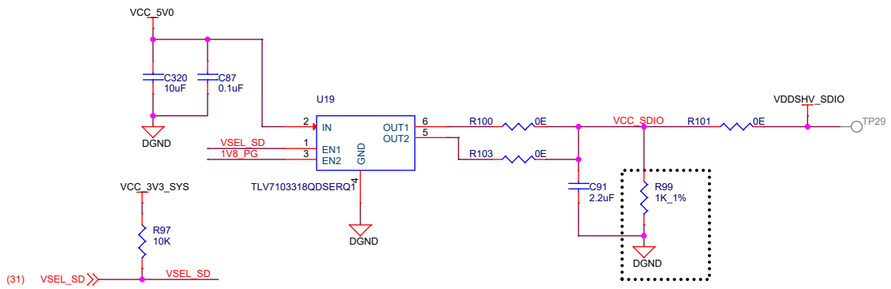


0.75V/0.85V , 3.0 AMPS SUPPLY



CORE VOLTAGE	Rfb RES TO BE PLACED
0.85V	Rfb = 41.2K
0.75V	Rfb = 24.9K

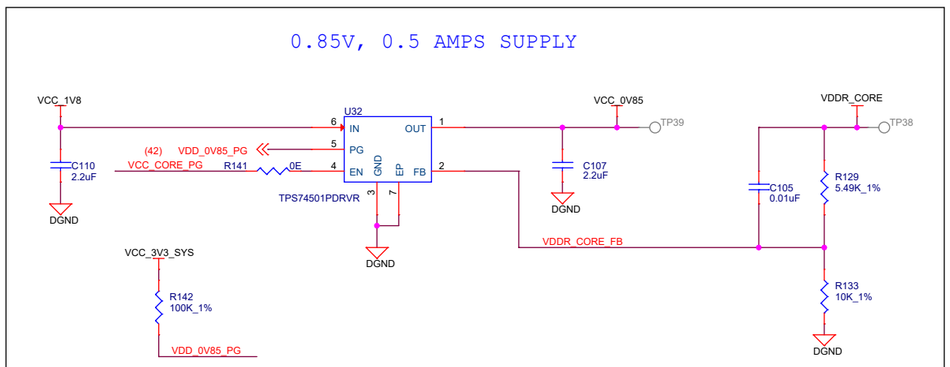
3.3V/1.8V SD CARD SUPPLY



VSEL_SD	SD VOLTAGE
HIGH(DEFAULT)	3.3V
LOW	1.8V

Note: Resistor is to 'bleed' off voltage.

0.85V, 0.5 AMPS SUPPLY



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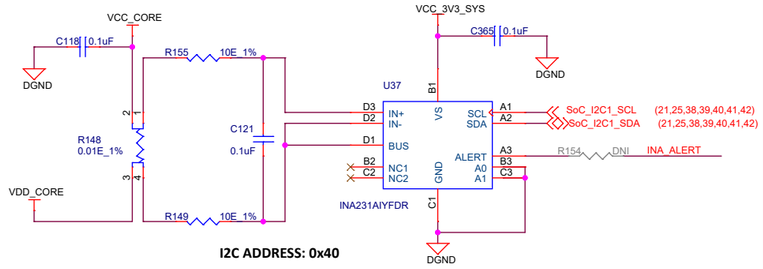
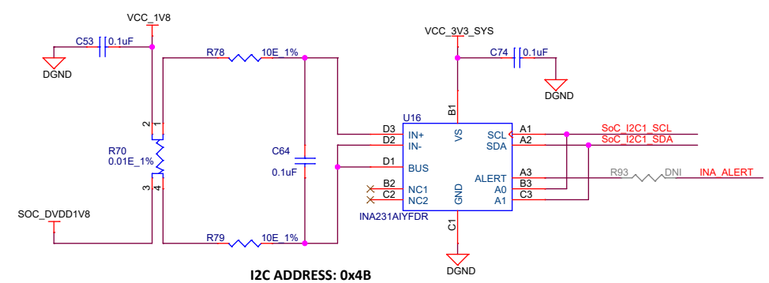
CURRENT MONITORING DEVICES

VDD_CORE



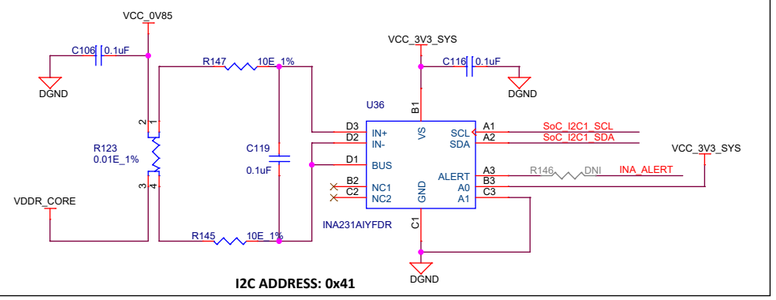
I2C ADDRESS: 0x40

SoC_DVDD1V8



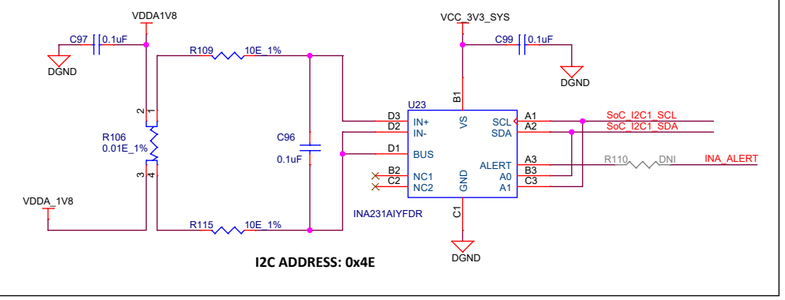
I2C ADDRESS: 0x4B

VDDR_CORE



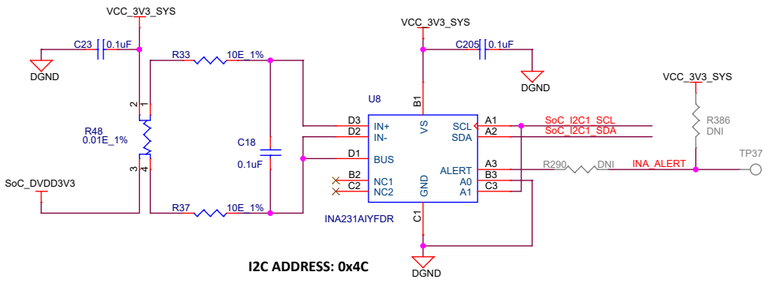
I2C ADDRESS: 0x41

VDDA_1V8



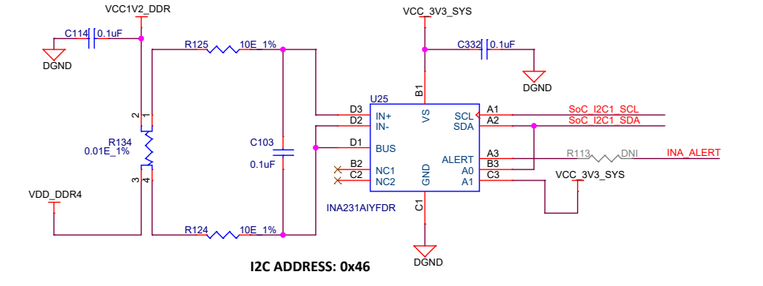
I2C ADDRESS: 0x4E

SoC_DVDD3V3



I2C ADDRESS: 0x4C

VDD_DDR4



I2C ADDRESS: 0x46

INA I2C SLAVE ADDRESS

POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46

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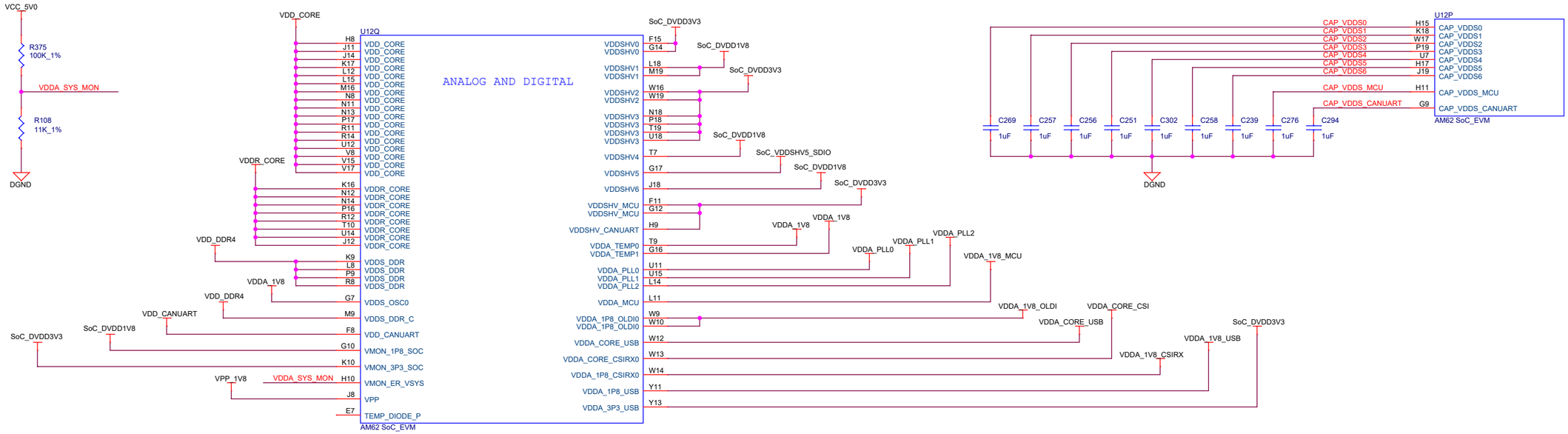
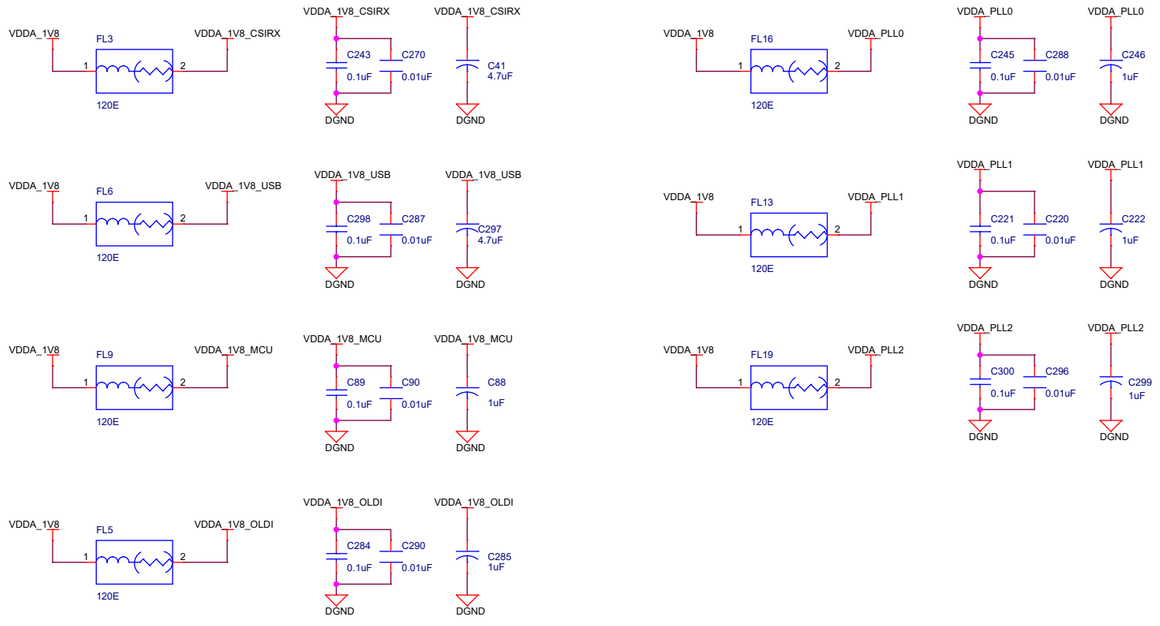
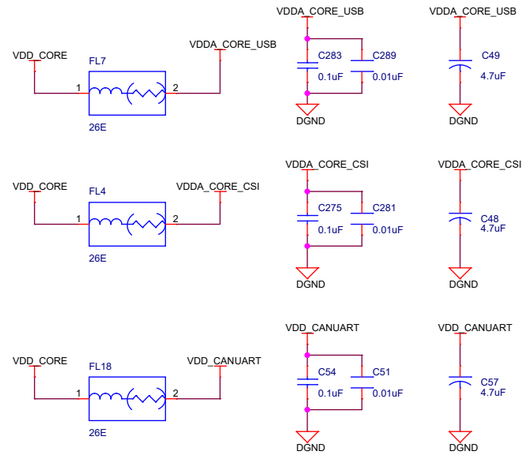
SOC POWER



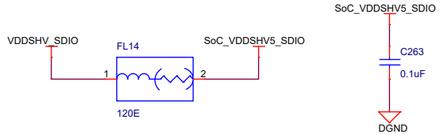
1.8V Analog SUPPLY



CORE SUPPLY



3.3V/1.8V MMC1 SUPPLY



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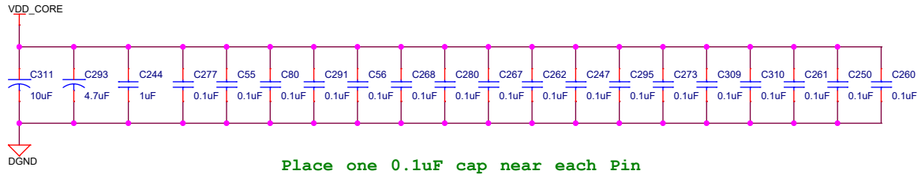
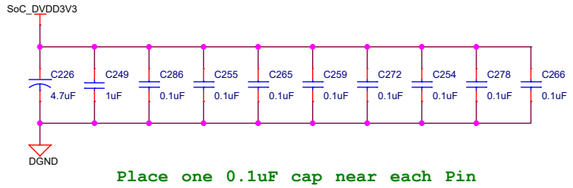
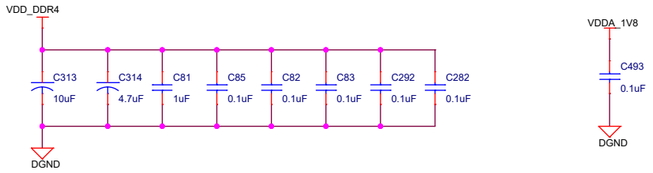
SOC POWER DECAPS



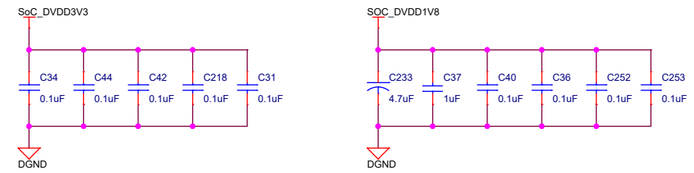
Place one 0.1uF cap near each Pin



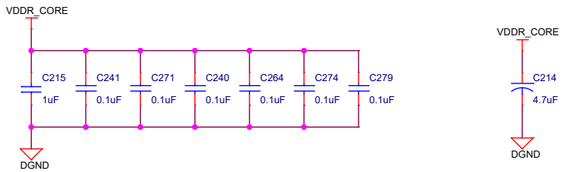
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin

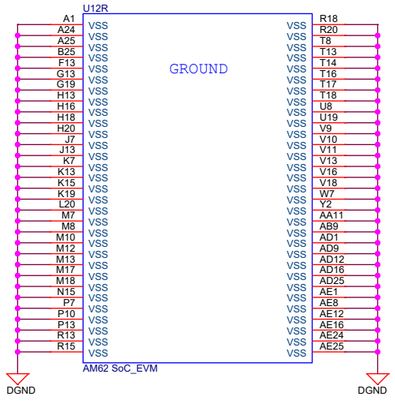


Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin

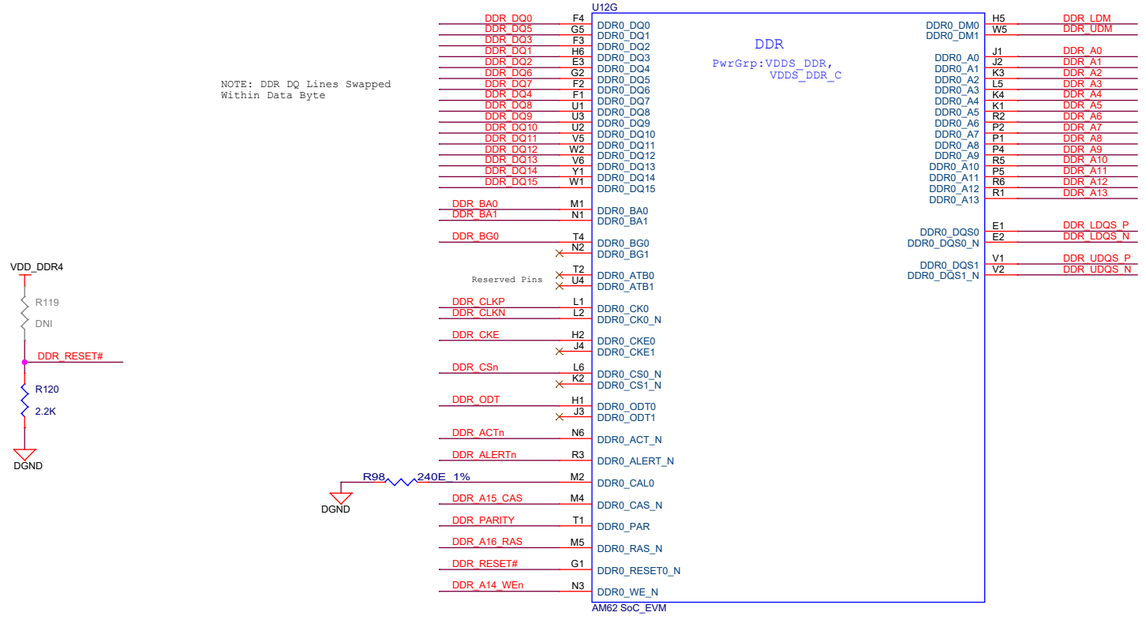
SOC VSS



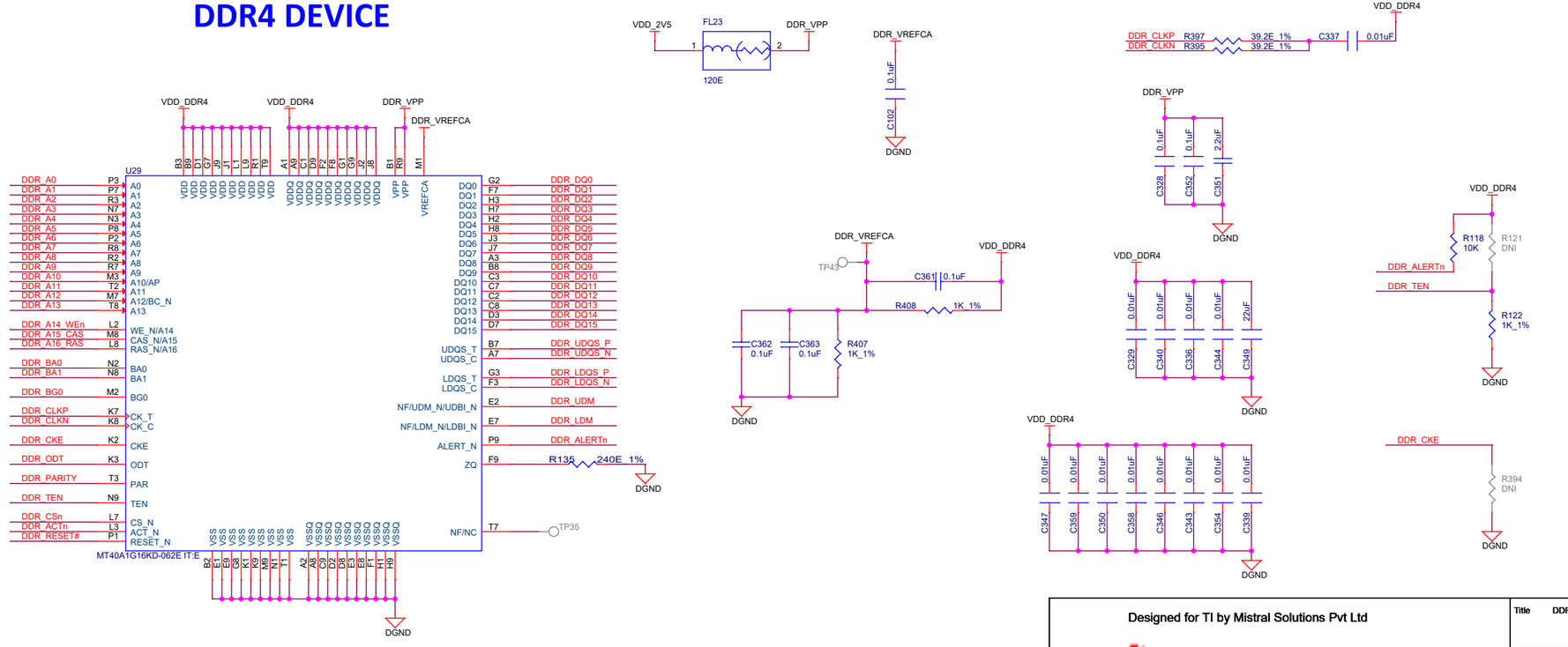
Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC POWER CAPS & SOC VSS	
Size C	Variant Name = PROC114E1	Rev
Date: Tuesday, November 02, 2021	Sheet 15 of 44	

SOC DDR INTERFACE



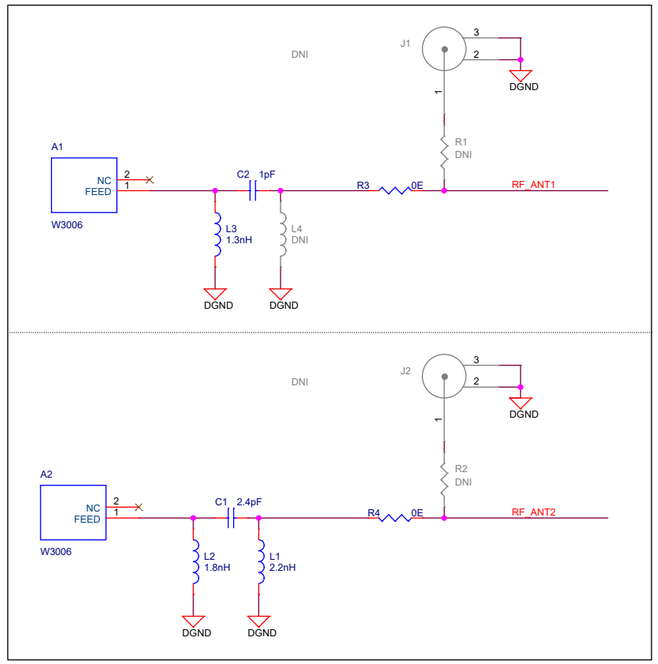
DDR4 DEVICE

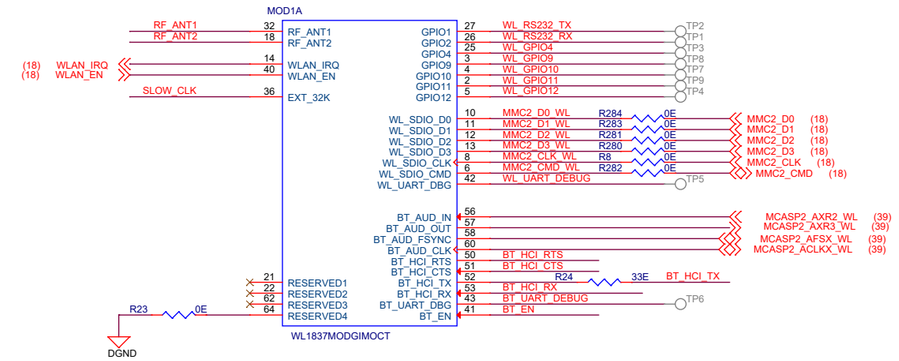


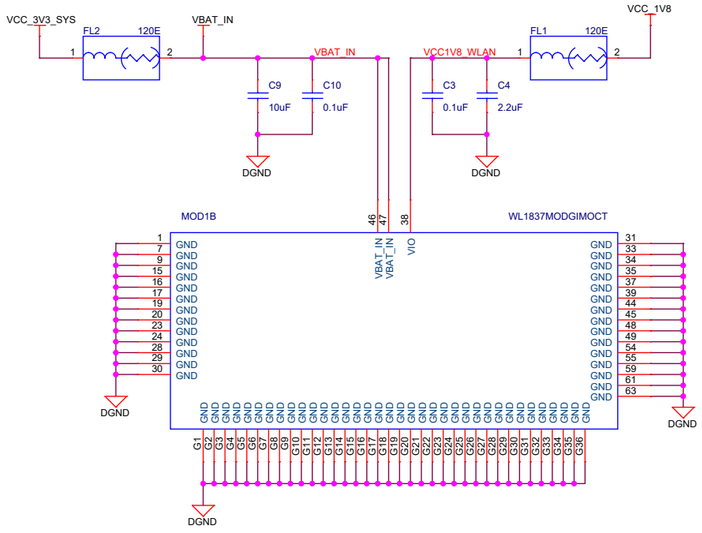
Designed for TI by Mistral Solutions Pvt Ltd

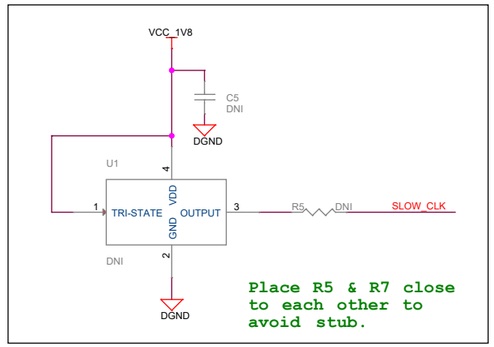
Title	DDR4 Interface	
Size C	Variant Name = PROC114E1	Rev E1
Date: Thursday, November 11, 2021	Sheet 16 of 44	

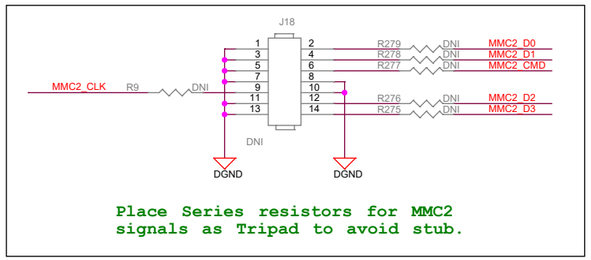
WL1837 MODULE

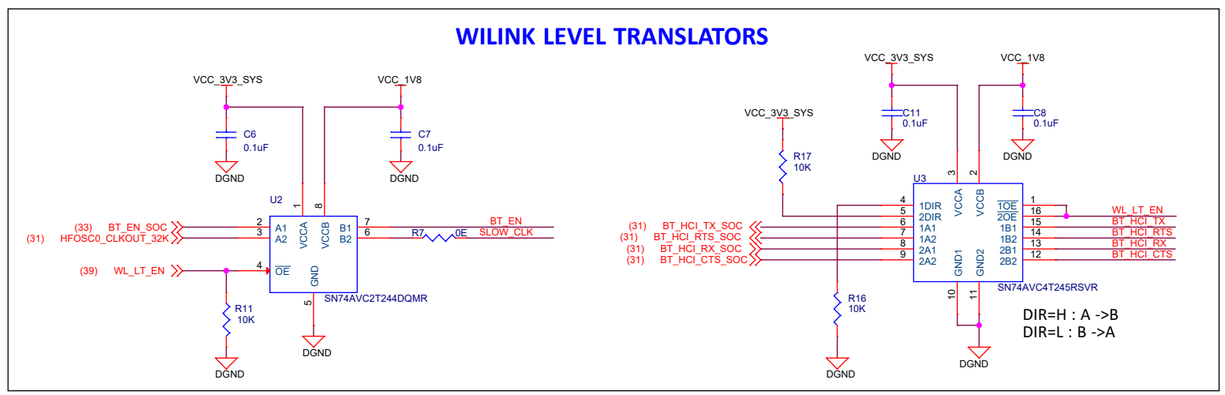


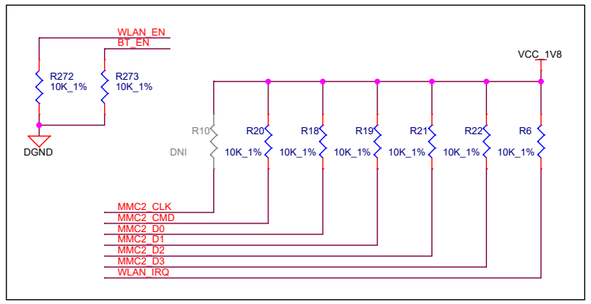








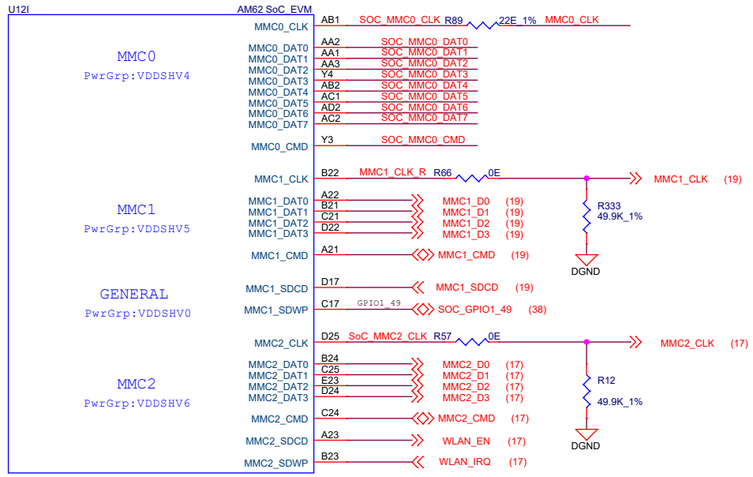




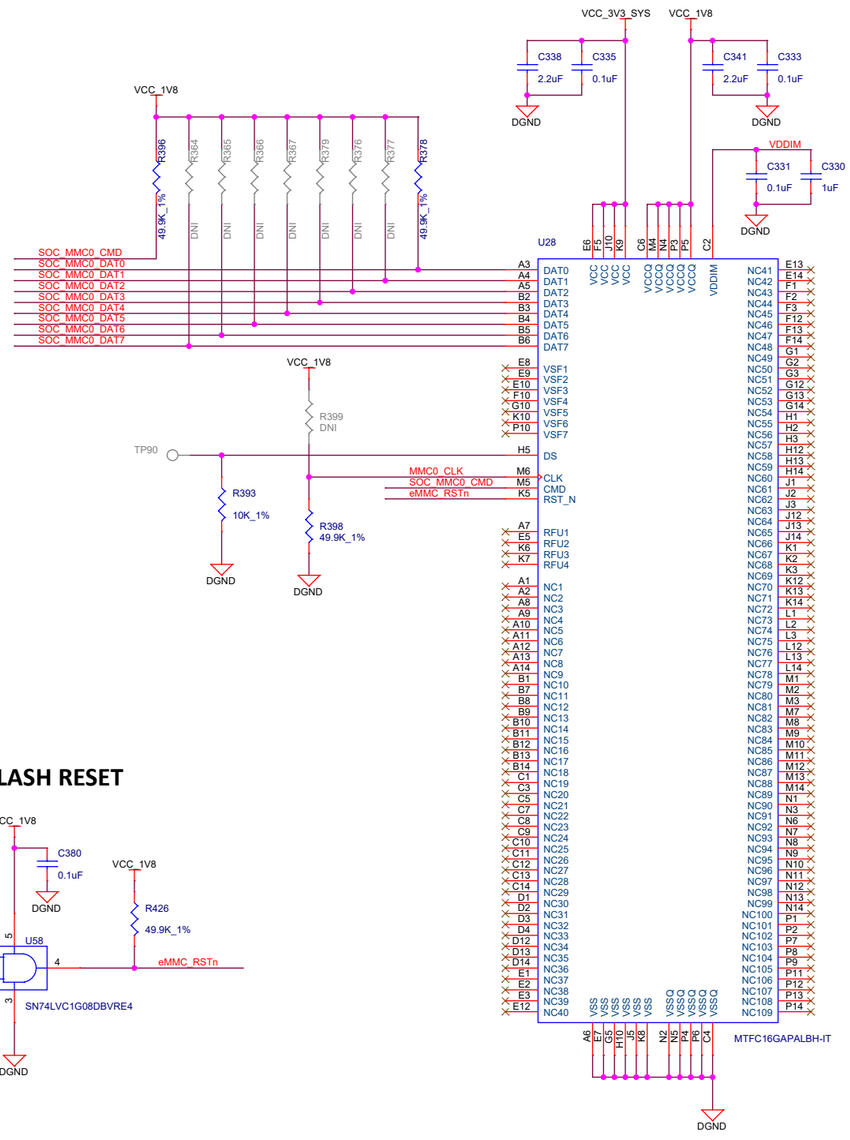
Designed for TI by Mistral Solutions Pvt Ltd

Title	WL1837 MODULE	
Size C	PROC114E1	Rev E2
Date: Thursday, November 11, 2021	Sheet 17 of 44	

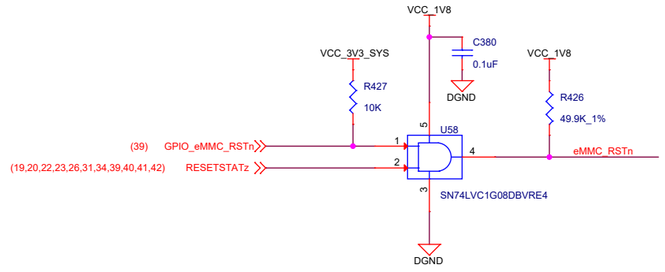
SOC - MMC Interface



eMMC FLASH



eMMC FLASH RESET



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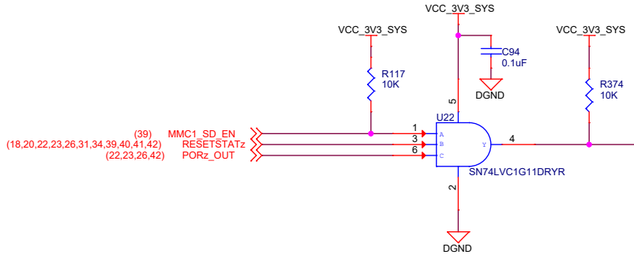
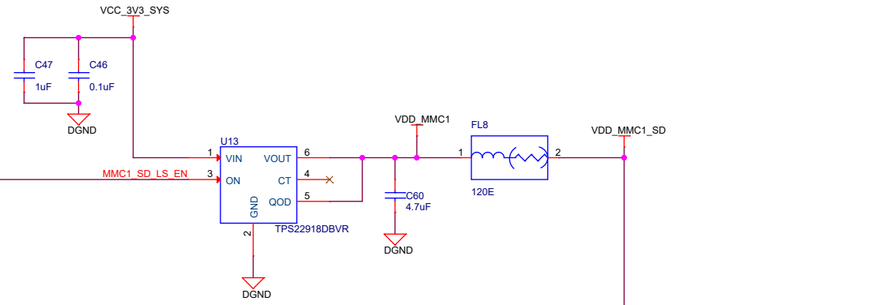
Title	eMMC FLASH INTERFACE	
Size C	PROC114E1	Rev E1
Date: Thursday, October 28, 2021	Sheet 18 of 44	

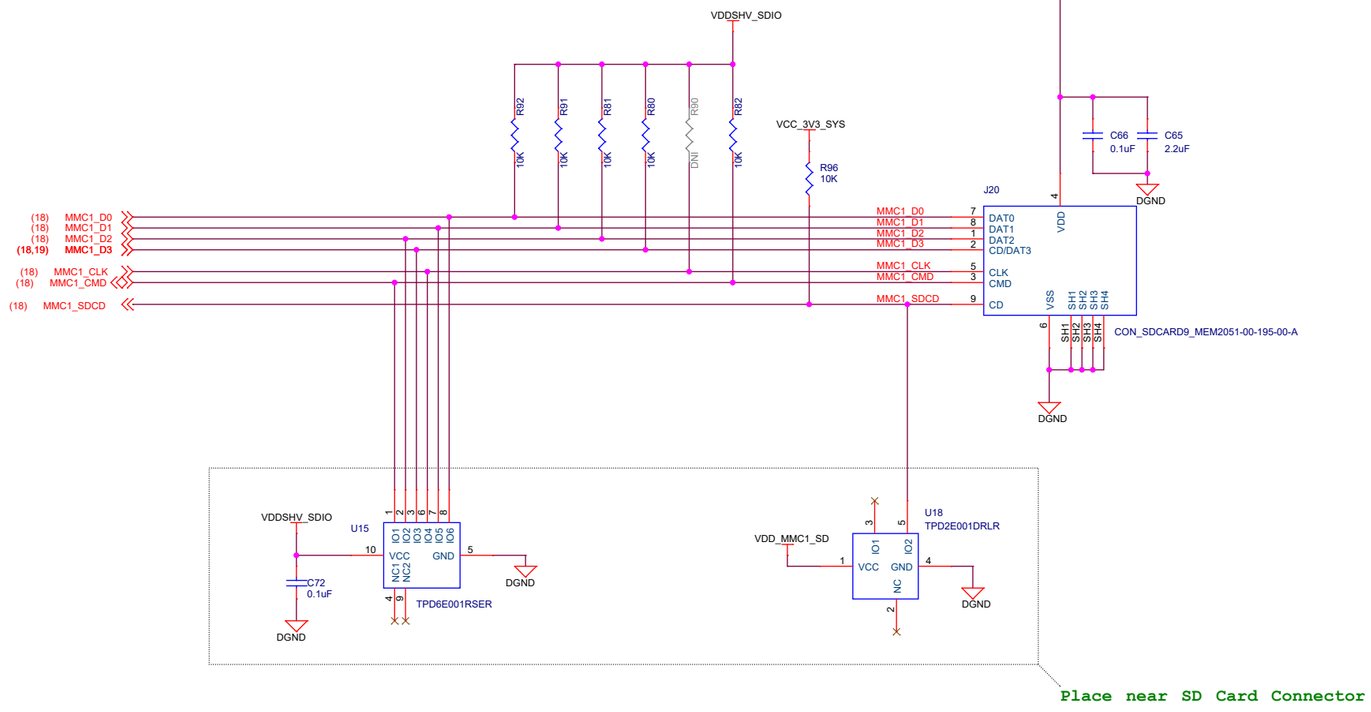
SD CARD INTERFACE

SD CARD RESET



POWER SWITCH





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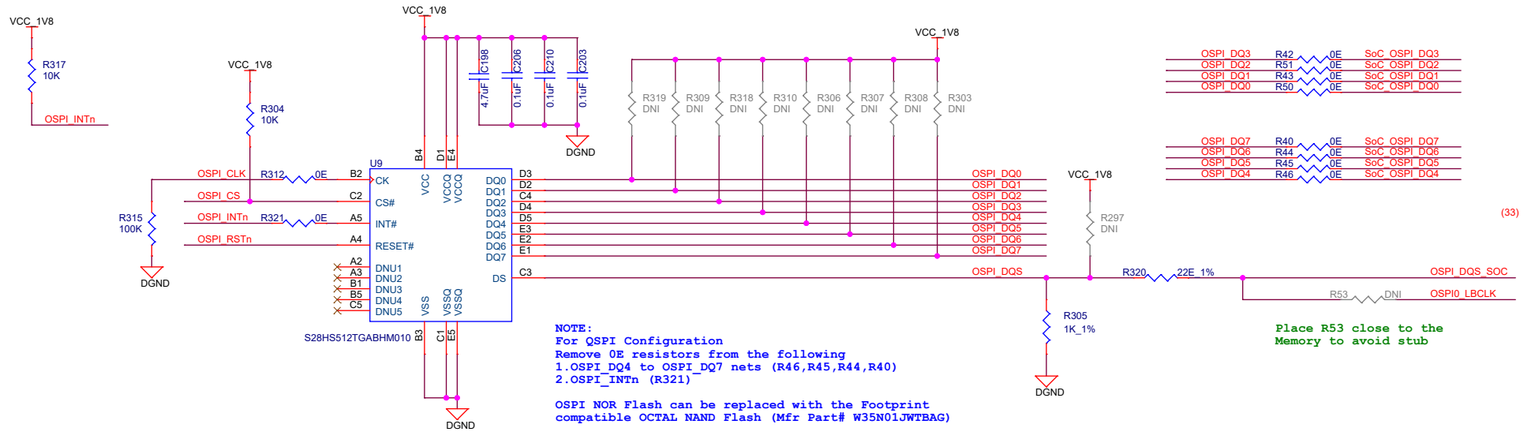
Title	SD CARD INTERFACE		
Size	PROC114E1		Rev
C			E1
Date:	Thursday, October 28, 2021	Sheet 19 of 44	

OSPI FLASH

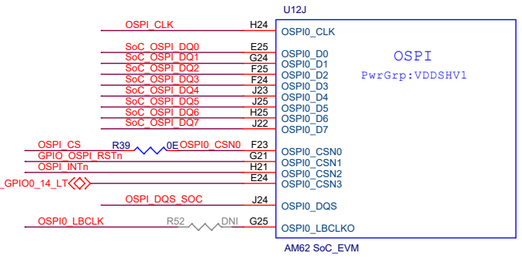


NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (R46,R45,R44,R40)
2.OSPI_INTn (R321)

OSPI NOR Flash can be replaced with the Footprint
compatible OCTAL NAND Flash (Mfr Part# W35N01JWTBAG)

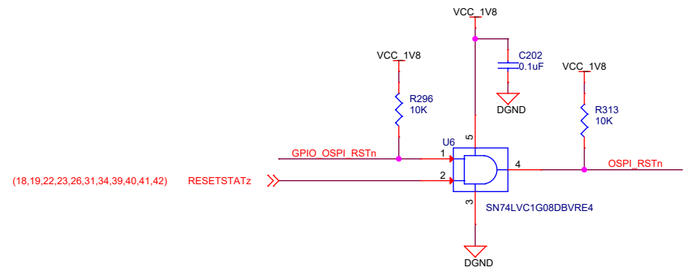
Place R53 close to the
Memory to avoid stub

SOC OSPI INTERFACE



Place R52 close to the SOC Ball
with as little trace as possible

OSPI FLASH RESET



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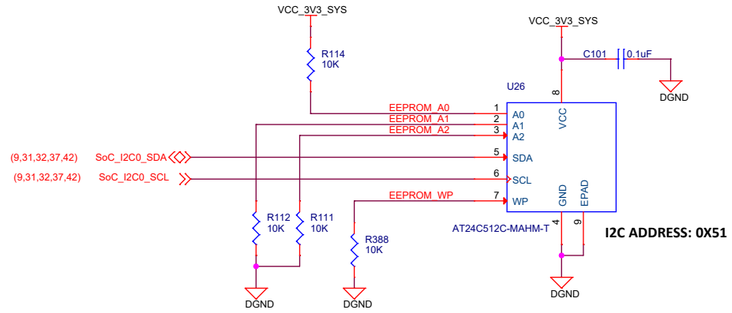
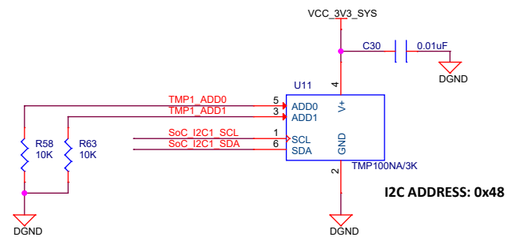
Title	OSPI INTERFACE	
Size C	PROC114E1	Rev E1
Date: Thursday, October 28, 2021	Sheet 20 of 44	

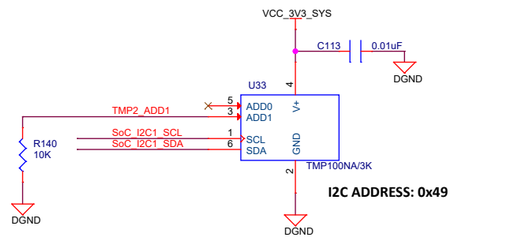
BOARD ID EEPROM



TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR U11 CLOSE TO SoC

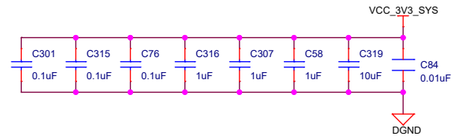


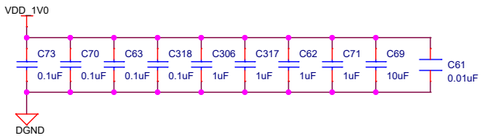
CAD NOTE: PLACE TEMP SENSOR U33 CLOSE TO DDR4

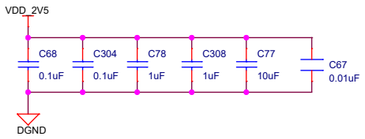
Designed for TI by Mistral Solutions Pvt Ltd

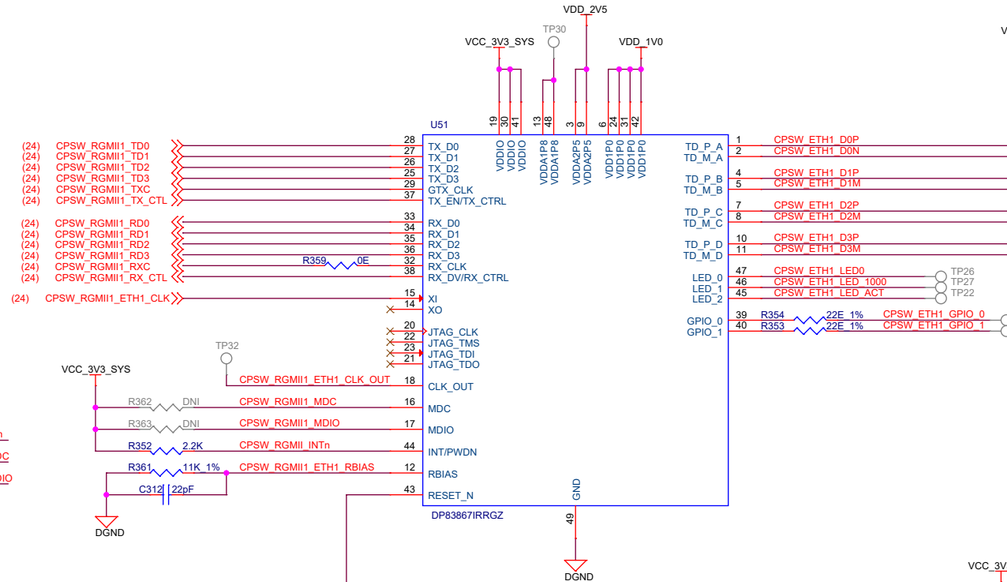
Title	BOARD ID EEPROM & TEMPERATURE SENSORS	
Size C	PROC114E1	Rev E1
Date: Thursday, October 28, 2021	Sheet 21 of 44	

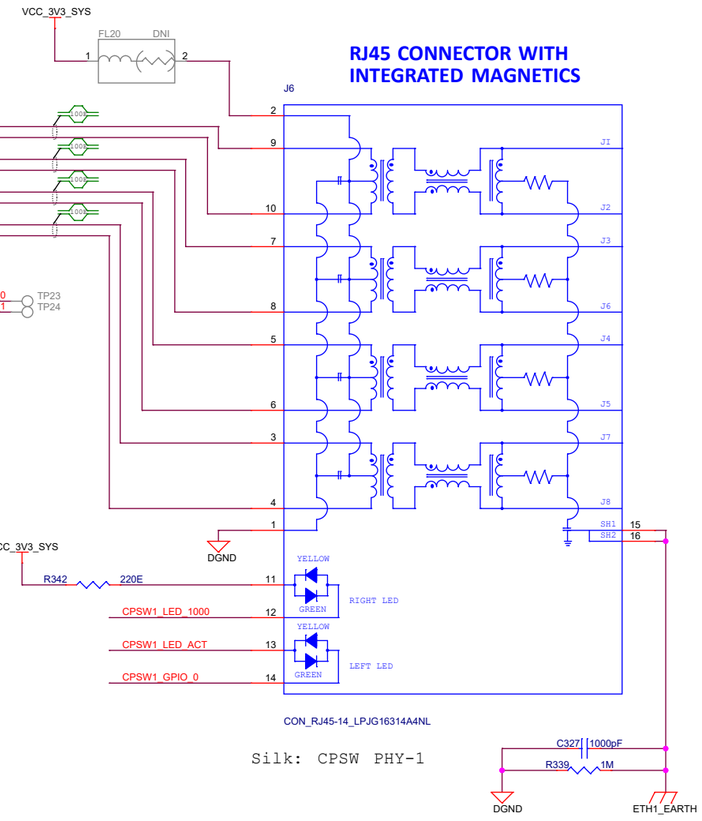
CPSW RGMII 1 - PHY



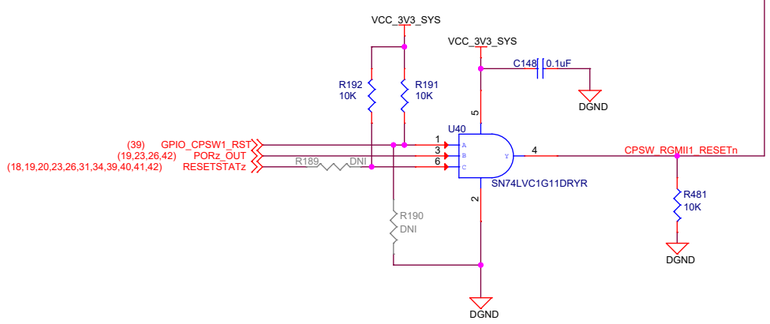


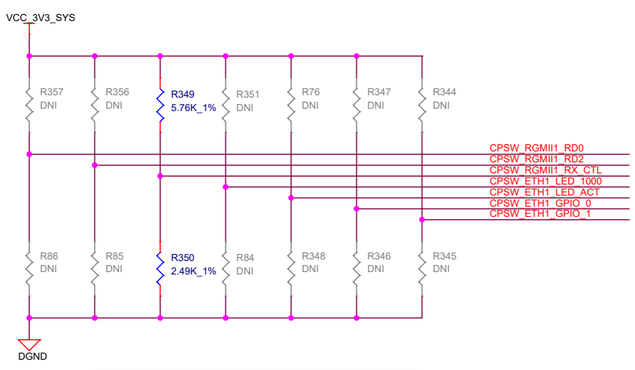


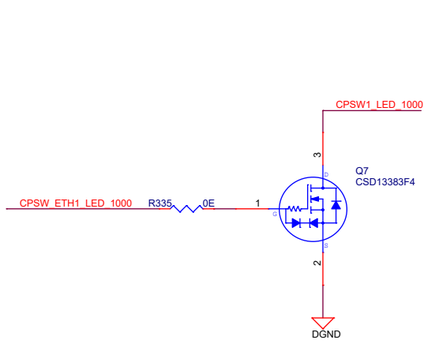


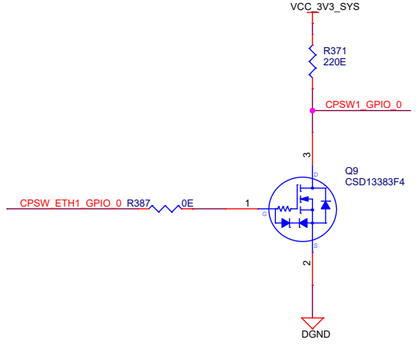


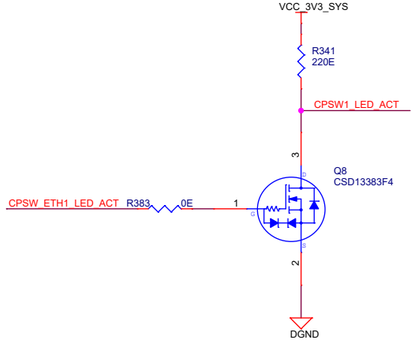
Silk: CPSW PHY-1









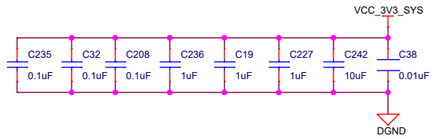


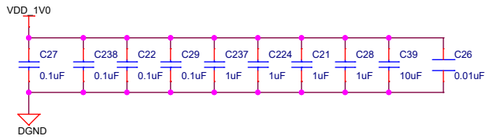

```
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 2ns
Rx Clock Skew = 2ns
```

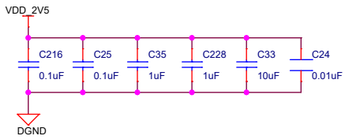
Designed for TI by Mistral Solutions Pvt Ltd

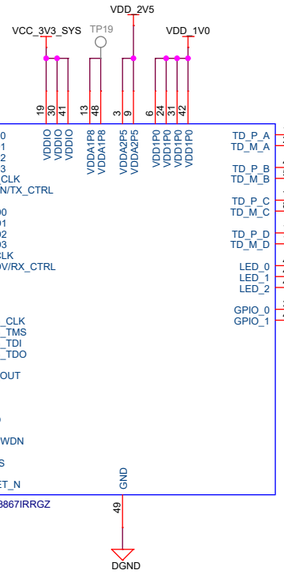
Title	CPSW RGMII_1 ETHERNET PHY	
Size: C	PROC114E1	Rev: E1
Date: Tuesday, November 02, 2021	Sheet 22 of 44	

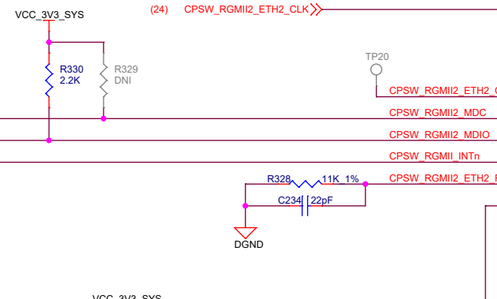
CPSW RGMII 2 - PHY

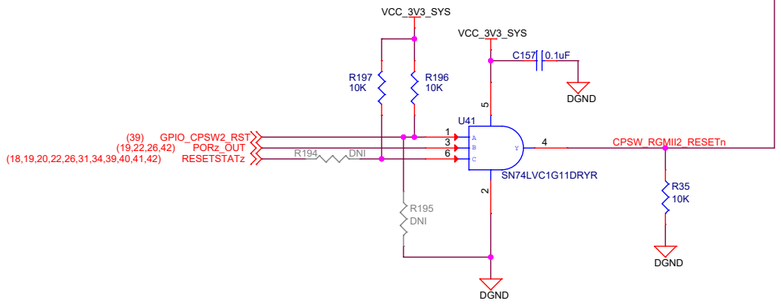




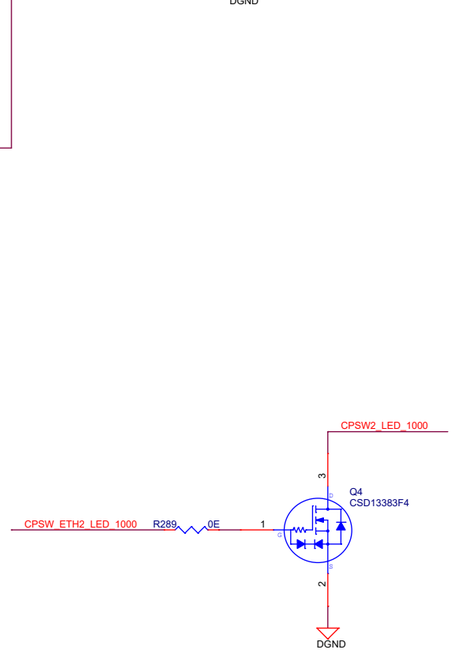


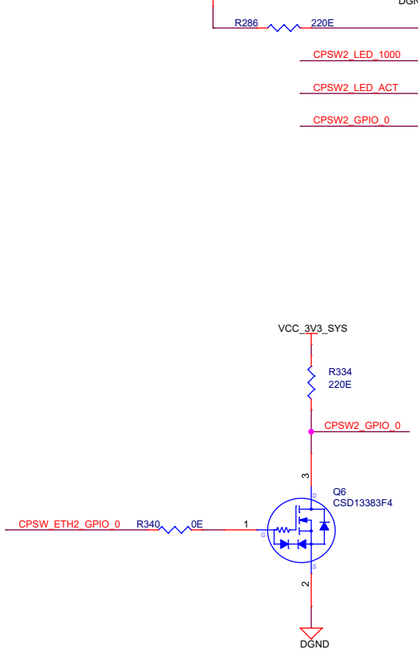


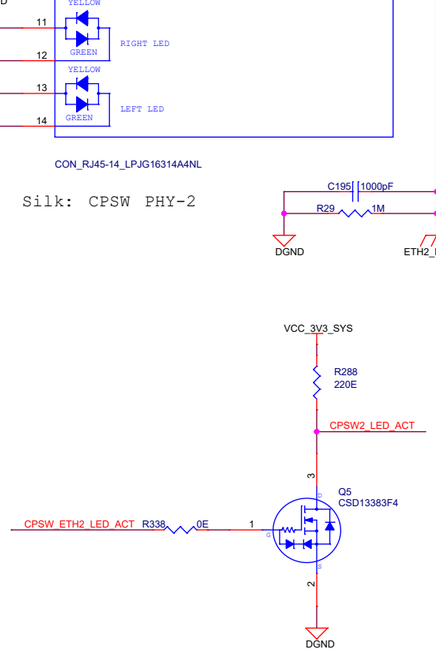


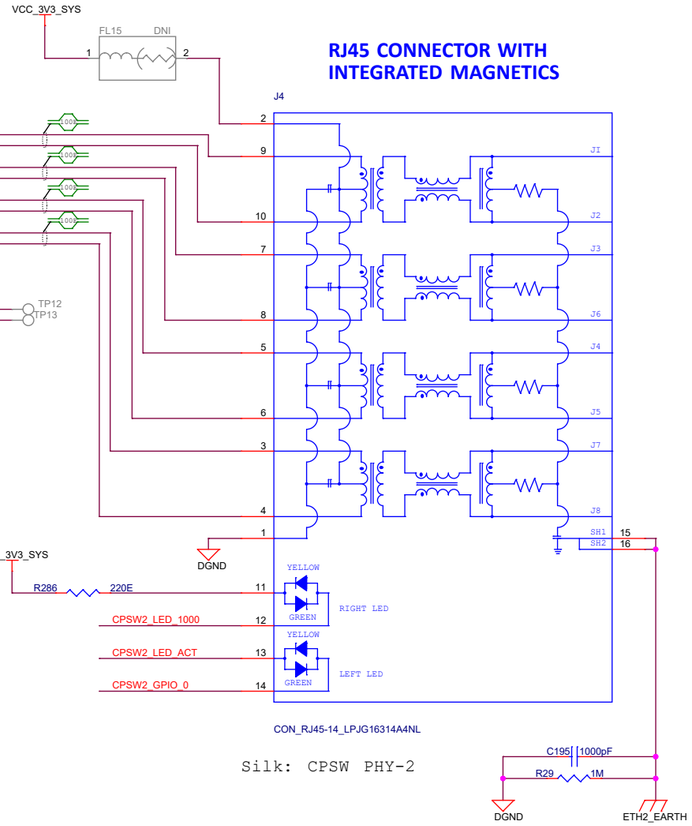


PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 2ns
Rx Clock Skew = 2ns







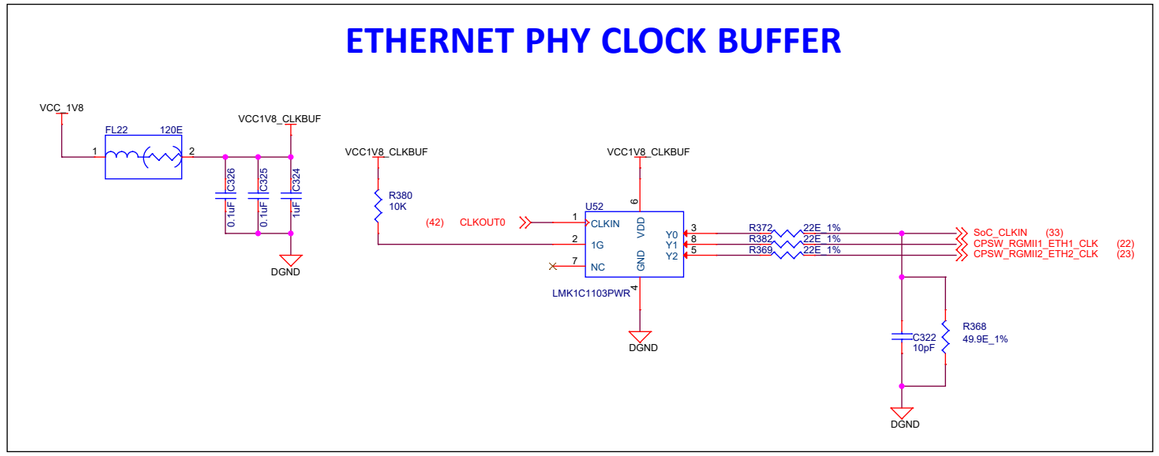


Silk: CPSW PHY-2

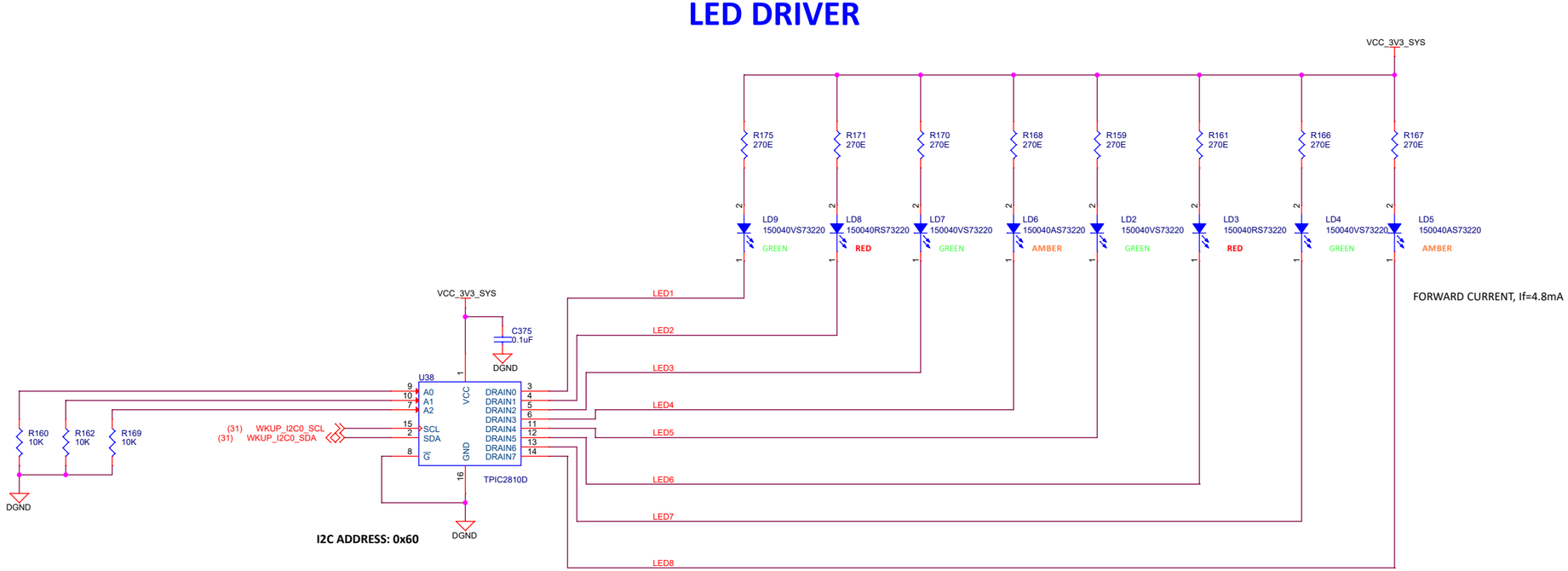
Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_2 ETHERNET PHY	
Size	PROC114E1	Rev
C		E1
Date:	Tuesday, November 02, 2021	Sheet 23 of 44

ETHERNET PHY CLOCK BUFFER



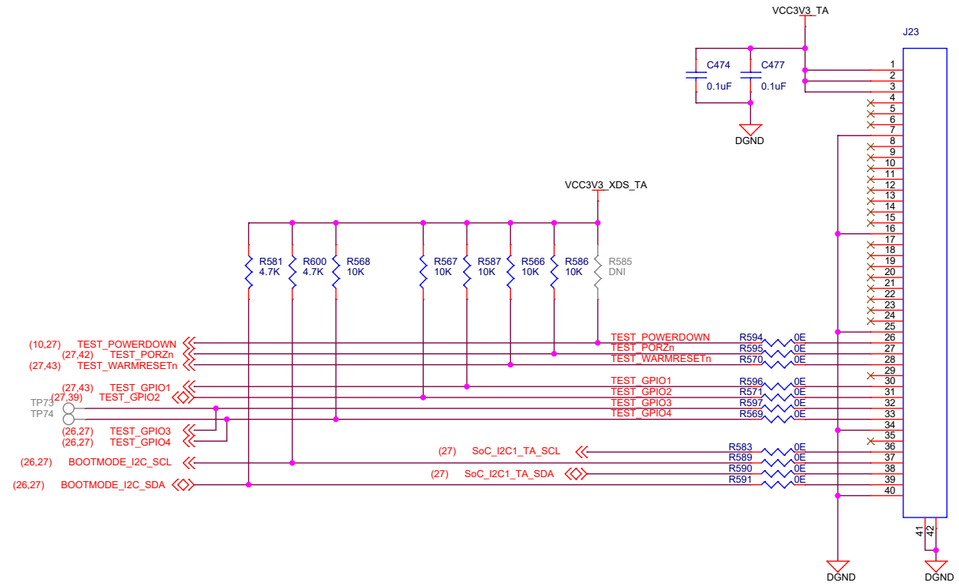
LED DRIVER



Designed for TI by Mistral Solutions Pvt Ltd

Title	ETHERNET PHY CLOCK BUFFER & LED DRIVER	
Size: C	PROC114E1	Rev: E1
Date: Thursday, October 28, 2021	Sheet 24 of 44	

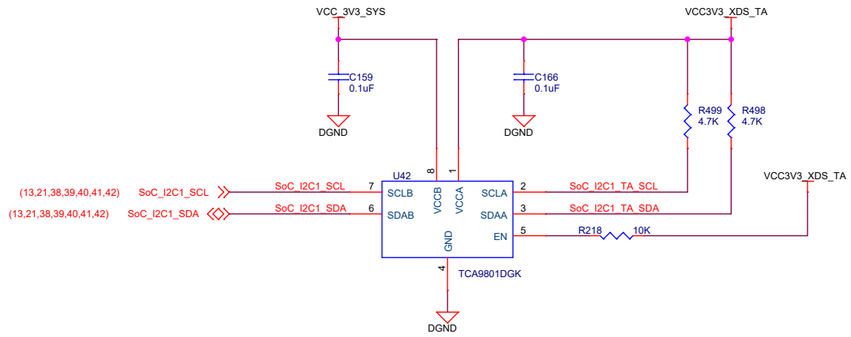
40-PIN TEST AUTOMATION HEADER

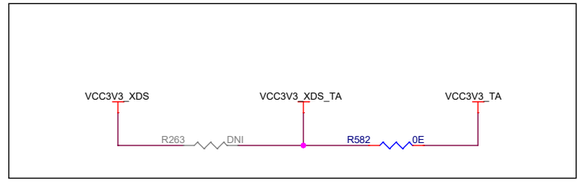


CON_FLEX_40X1_FH12A-40S-0.5SH

Silk: AUTOMATION HDR

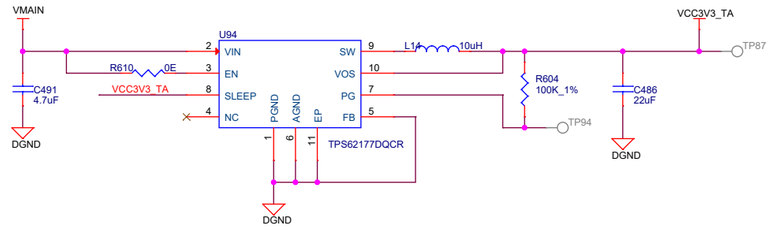
I2C BUS BUFFER





TEST AUTOMATION BOARD POWER

VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A



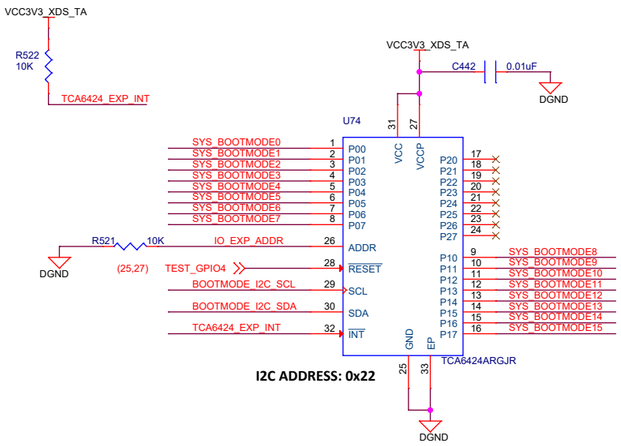
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on MCU_GPIO0_15 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

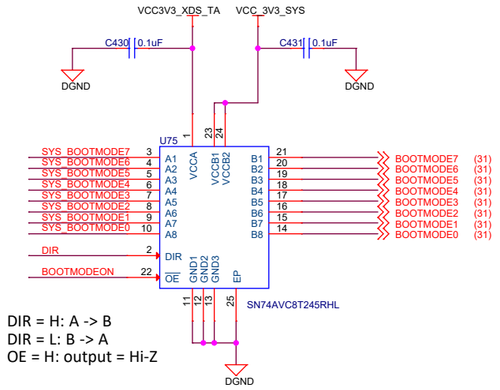
Designed for TI by Mistral Solutions Pvt Ltd

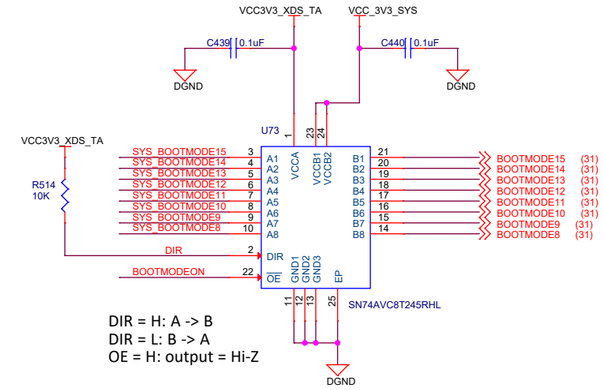
Title	TEST AUTOMATION	
Size C	PROC114E1	Rev E1
Date: Friday, October 29, 2021	Sheet 25 of 44	

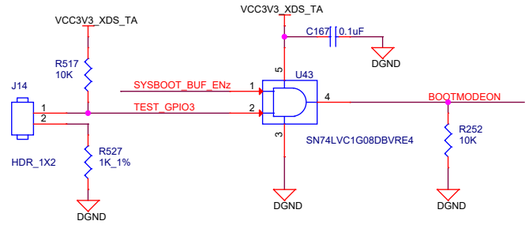
BOOTMODE IO EXPANDER



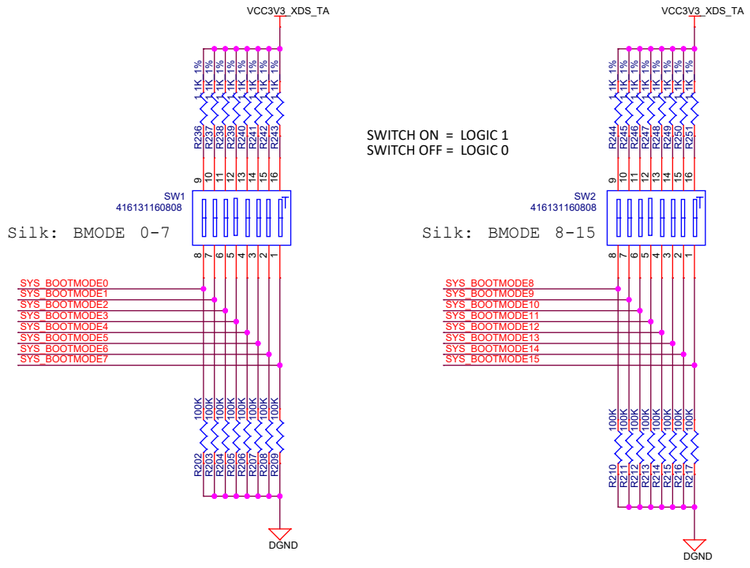
BOOT MODE BUFFERS







BOOT MODE SWITCHES



SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. BACKUP BOOT OPTION

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOOT MODE BUFFER & SWITCHES		
Size C	PROC114E1		Rev E1
Date:	Thursday, October 28, 2021	Sheet 26 of 44	

XDS110 DEBUGGER

TP86
XDS_USB_VBUS
C180 4.7uF
D8 TPD1E10B06DPYR
DGND
C455 2.2uF
R540 0E
U79
IN1 IN2 OUT1 OUT2 EN NR/FB GND PAD NC
TPS79601DRBR
R520 51K
C441 15pF
R519 30K
C443 1uF
VCC3V3_XDS
TP77
C454 1uF
C468 0.1uF
C173 0.1uF
C181 0.01uF
C176 0.01uF
C191 0.01uF
U45B
VDD GNDA GND VDDA VDDC VBAT
TM4C1294NCPDTT3R
C192 1uF
C189 0.01uF
VDDC_1V2
C179 2.2uF
C178 1uF
C449 0.1uF
R228 49.9E_1%
C169 0.1uF

Silk: JTAG

J16
VBUS D- D+ ID GND SH1 SH2 SH3 SH4
CON_MUSB-B_5_F
XDS_USB_DM
XDS_USB_DP
XDS_USB_ID
U89
IO1 IO2 IO3 IO4 VCC GND
TPD4E004DRYR
R256 1M
C185 1000pF
XDS_SHIELD

U45A
PA0/U0RX PA1/U0TX PA2/SSI0CLK PA3/SSI0FSS PA4/SSI0XDAT0 PA5/SSI0XDAT1 PA6 PA7
PC0/TCK/SWCLK PC1/TMS/SWDIO PC2/TDI PC3/TDO/SWO PC4/C1- PC5/C1+ PC6/C0+ PC7/C0-
PE0/AIN3 PE1/AIN2 PE2/AIN1 PE3/AIN0 PE4/AIN9 PE5/AIN8
PG0 PG1
PJ0 PJ1
PL0 PL1 PL2 PL3 PL4 PL5 PL6/USB0DP PL7/USB0DM
PN0 PN1 PN2 PN3 PN4 PN5
PQ0 PQ1 PQ2 PQ3 PQ4
TM4C1294NCPDTT3R
PB0/USB0ID PB1/USB0VBUS PB2/I2C0SCL PB3/I2C0SDA PB4/AIN10 PB5/AIN11
PD0/AIN15 PD1/AIN14 PD2/AIN13 PD3/AIN12 PD4/AIN7 PD5/AIN6 PD6/AIN5 PD7/AIN4
PF0 PF1 PF2 PF3 PF4
PH0 PH1 PH2 PH3
PK0/AIN16 PK1/AIN17 PK2/AIN18 PK3/AIN19 PK4 PK5 PK6 PK7
PM0 PM1 PM2 PM3 PM4 PM5 PM6 PM7
PP0/C2+ PP1/C2- PP2 PP3 PP4 PP5

XDS110_TCK (28)
XDS110_TMS (28)
XDS110_TDO (28)
XDS110_TDI (28)
XDS110_TRST# (28)
TP82 TP81 TP80 TP79
TM4C129_TCK
TM4C129_TMS
TM4C129_TDI
TM4C129_TDO
(25,26) BOOTMODE_I2C_SCL
(25,26) BOOTMODE_I2C_SDA
R598 DNI
R580 DNI
(25) SoC_I2C1_TA_SDA
(25) SoC_I2C1_TA_SCL
R525 DNI
R544 DNI
XDS_USB_DP
XDS_USB_DM

R530 100E_1%
R235 DNI
C170 0.1uF
XDS_USB_ID
XDS_USB_VBUS
R268 30K
R269 20K_1%
R267 220E
R271 220E
LD14 150080VS75000 GREEN
LD15 150040RS73220 RED
R229 DNI
R224 DNI
R230 DNI
R225 DNI
R231 DNI
R226 DNI
R232 DNI
TEST_POWERDOWN (10,25)
TEST_PORZn (25,42)
TEST_WARMRESETn (25,43)
TP76
TEST_GPIO1 (25,43)
TEST_GPIO2 (25,39)
TEST_GPIO3 (25,26)
TEST_GPIO4 (25,26)

VCC3V3_XDS
R563 1K_1%
R560 1K_1%
R556 1K_1%
R552 1K_1%
R260 DNI
R259 DNI
R258 DNI
R255 DNI

Sets the unique ID of the Debugger

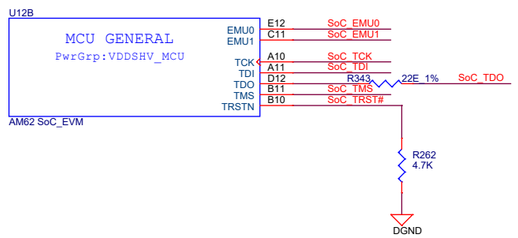
VCC3V3_XDS
R539 10K
TP75
R546 DNI
DGND
U45C
RST WAKE OSC0 OSC1 XOSC0 XOSC1 RBAIS VREFA+ HIB EN0RXIP EN0RXIN EN0RX0P EN0RX0N
TM4C1294NCPDTT3R
XDS_RSTn
OSC0
OSC1
C172 12pF
C171 12pF
Y2 16.000MHz
R261 4.87K_1%
R270 4.7K
XDS_VREF
C186 0.01uF
C190 0.1uF
U47
LM4040B25IDCKR

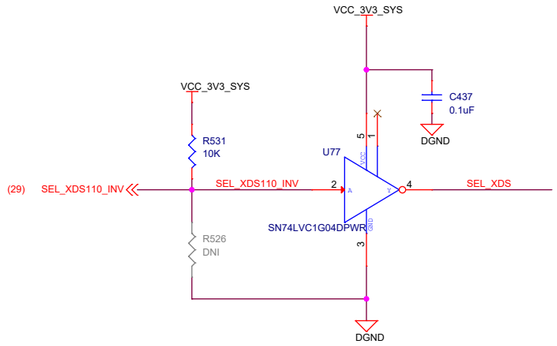
VCC3V3_XDS
R264 4.7K
R265 4.7K
XDS110_EMU0
XDS110_EMU1
XDS110_EMU0 (28)
XDS110_EMU1 (28)

Designed for TI by Mistral Solutions Pvt Ltd

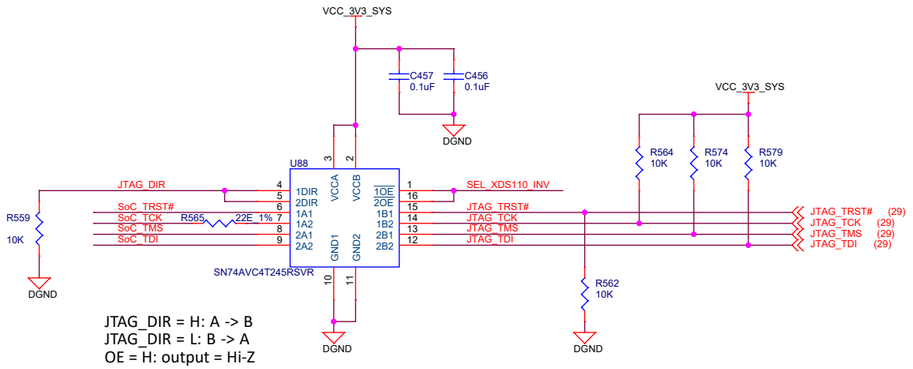
Title	XDS110 DEBUGGER	
Size	PROC114E1	Rev
C		E1
Date:	Thursday, October 28, 2021	Sheet 27 of 44

JTAG SOC SECTION



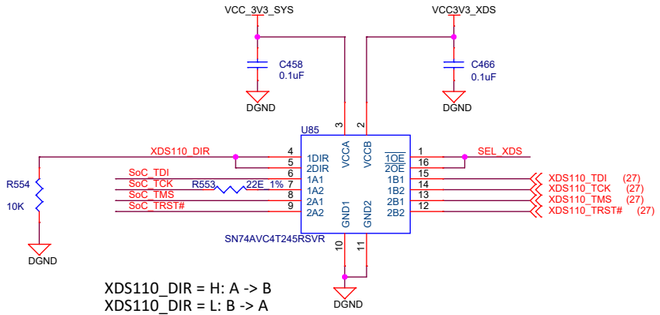


cTI20 JTAG BUFFERS

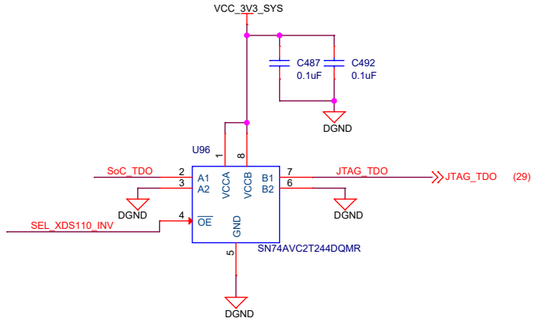


JTAG_DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z

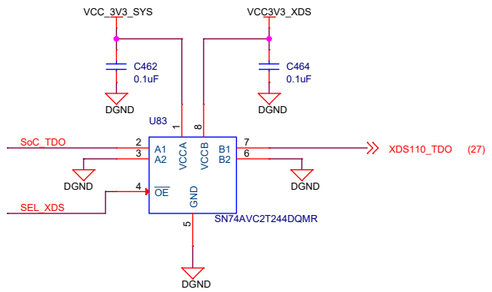
BUFFER XDS110

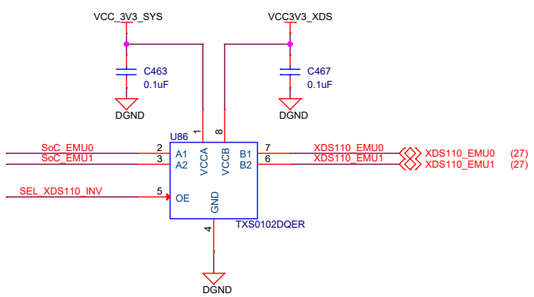


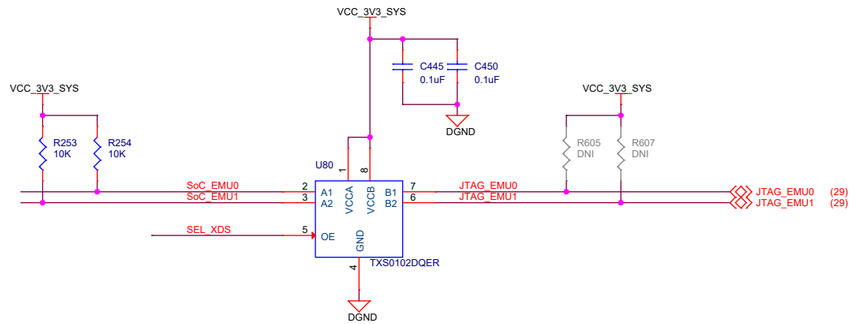
XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z



CAD NOTE: Buffers U88 and U96
need to be placed closer to the
cTI-20pin connector J17 to reduce Stub length of the JTAG signals.



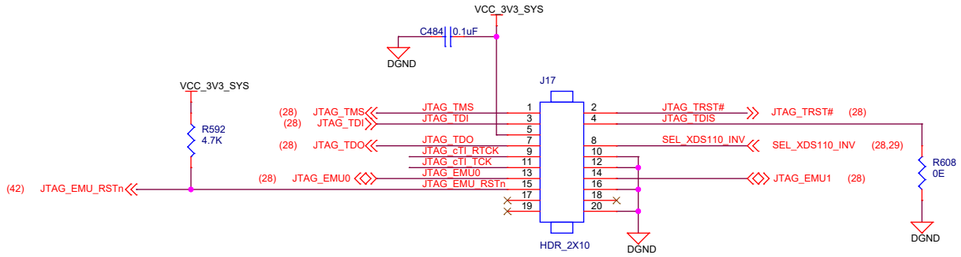




Designed for TI by Mistral Solutions Pvt Ltd

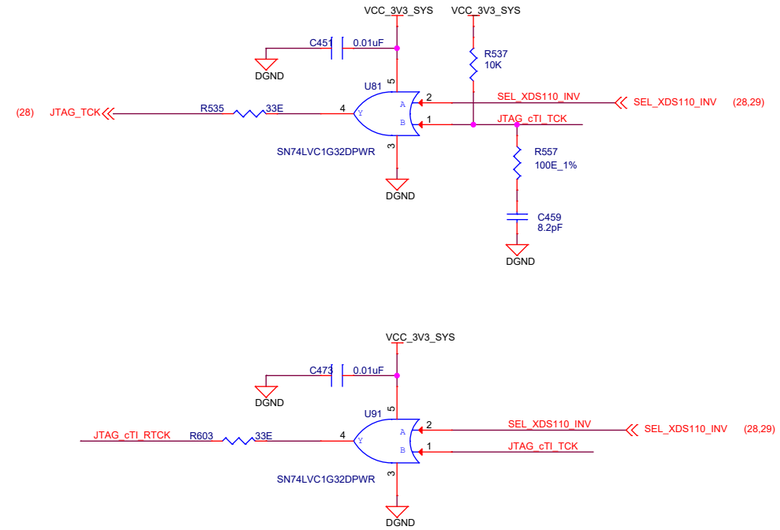
Title	JTAG BUFFER	
Size: C	PROC114E1	Rev: E1
Date: Thursday, October 28, 2021	Sheet 28 of 44	

JTAG 20 PIN cTI CONNECTOR



Silk: cTI

JTAG CLOCK BUFFER

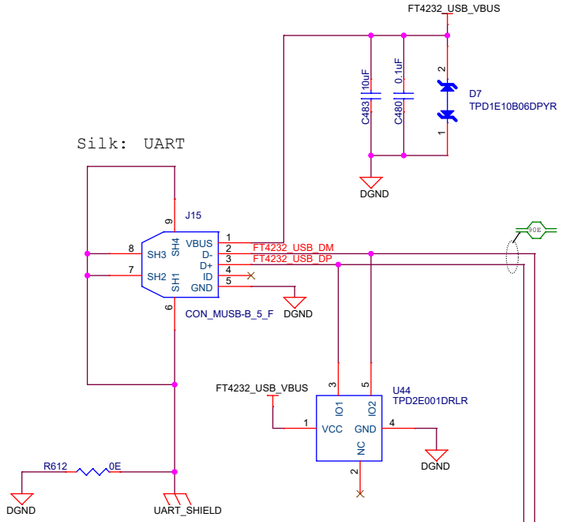


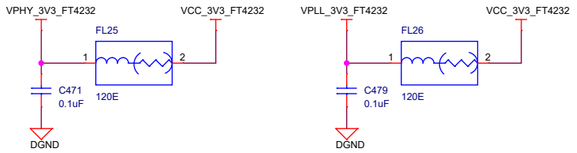
Designed for TI by Mistral Solutions Pvt Ltd

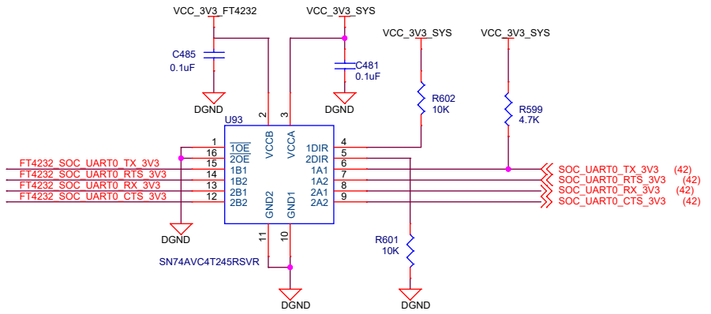
Title	JTAG 20 PIN cTI CONNECTOR		
Size	PROC114E1		Rev
C			E1
Date:	Thursday, October 28, 2021	Sheet 29 of 44	

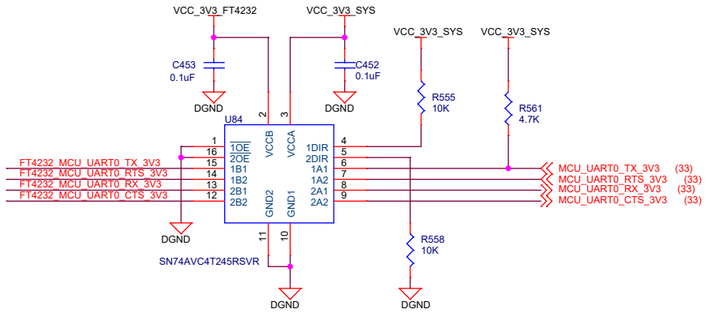
FT4232 UART

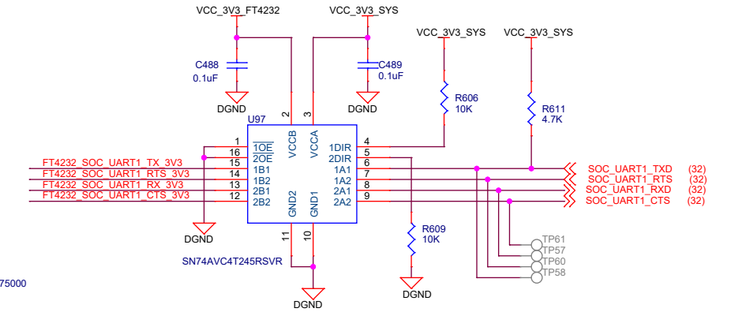
Silk: UART

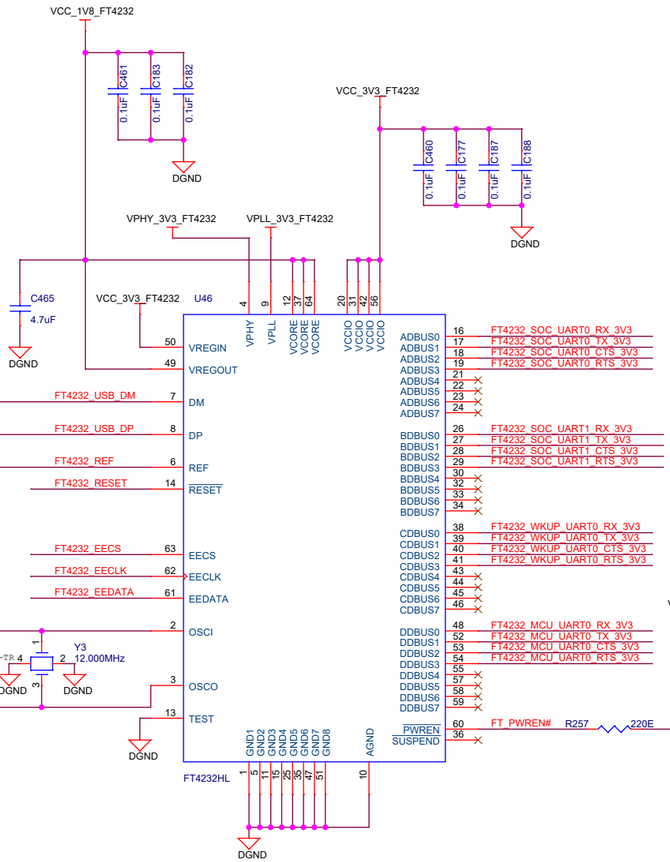


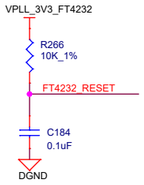




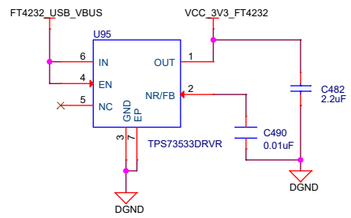




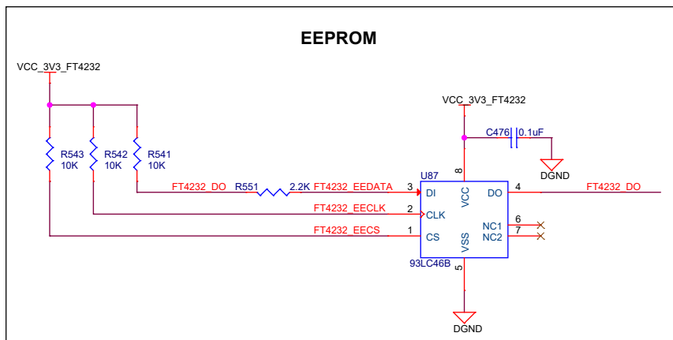


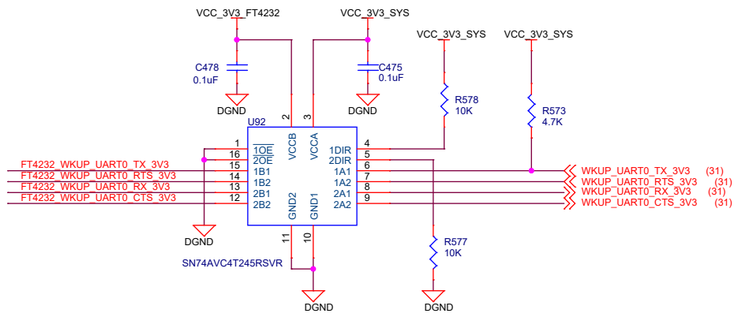


FT4232: 5V to 3.3V@500mA LDO



EEPROM

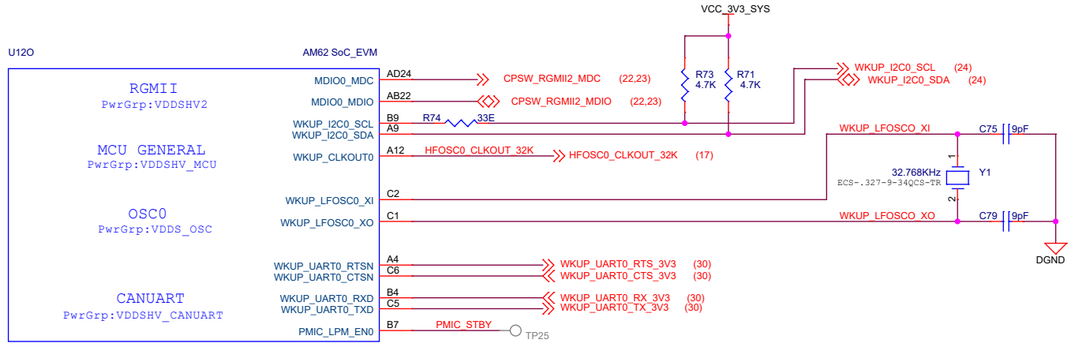




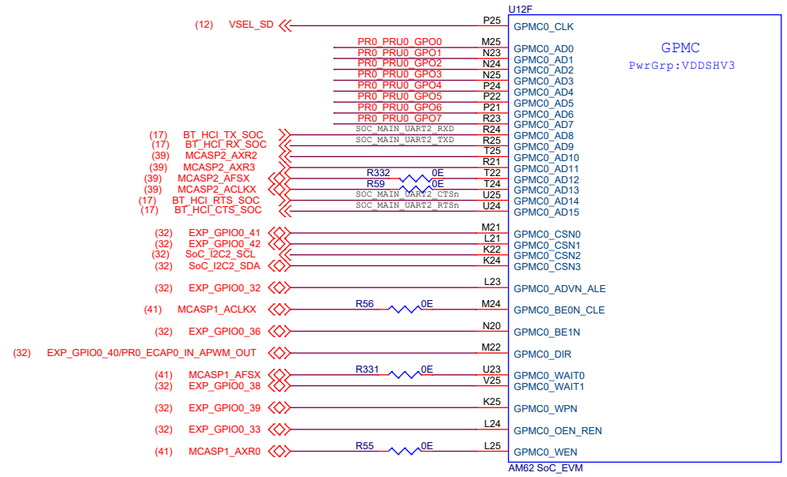
Designed for TI by Mistral Solutions Pvt Ltd

Title	FT4232 UART TO USB BRIDGE	
Size C	PROC114E1	Rev E1
Date: Tuesday, November 02, 2021	Sheet 30 of 44	

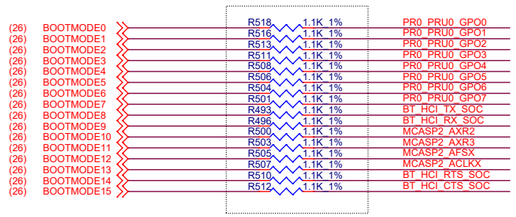
SOC WKUP DOMAIN



SOC GPMC

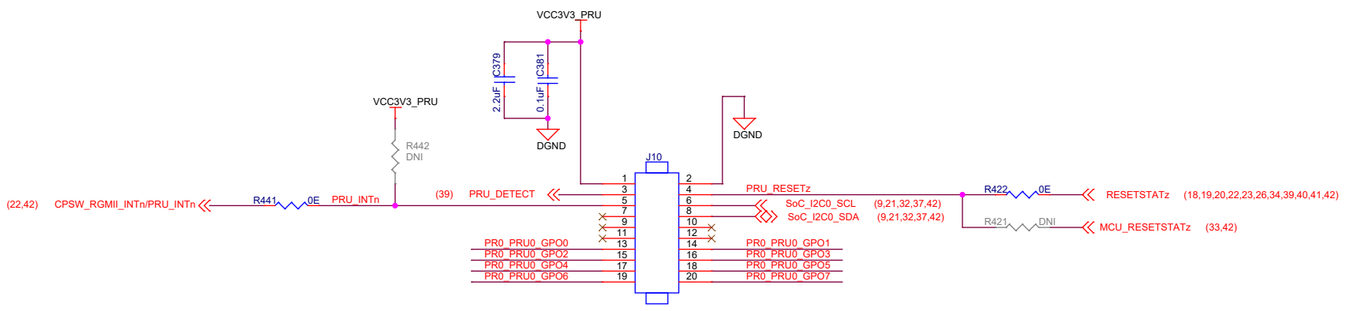


BOOTMODE PINS



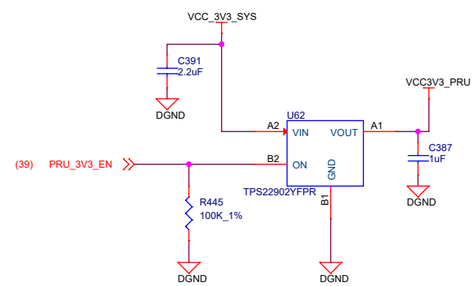
NOTE: 1.1K Resistors are used to isolate the BOOTMODE control logic after the value is latched

PRU HEADER



Silk: PRU HDR

POWER SWITCH FOR PRU HEADER



3V3 supply of PRU Header is limited to sourcing 500mA max.

NOTE: PRU Header I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

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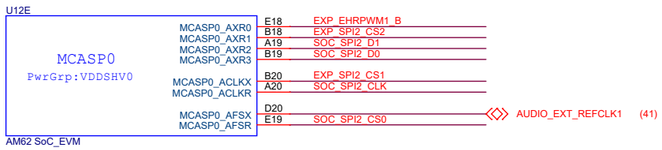
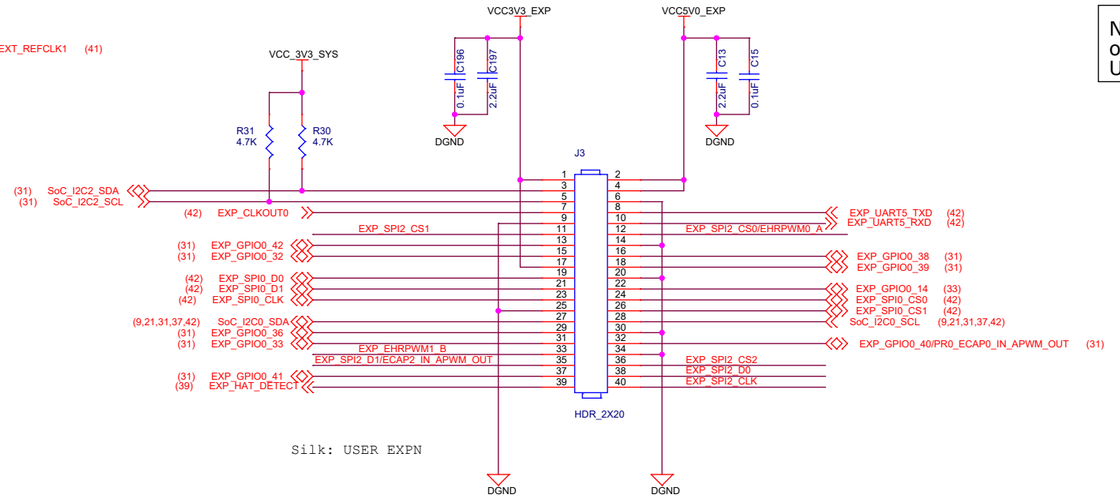
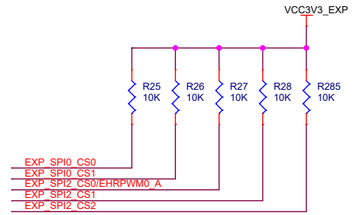
Title	PRU HEADER		
Size C	PROC114E1		Rev E1
Date:	Thursday, October 28, 2021	Sheet 31 of 44	

USER EXPANSION CONNECTOR

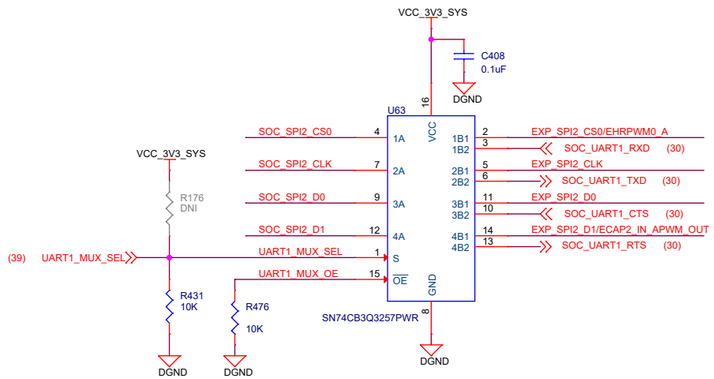




Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)

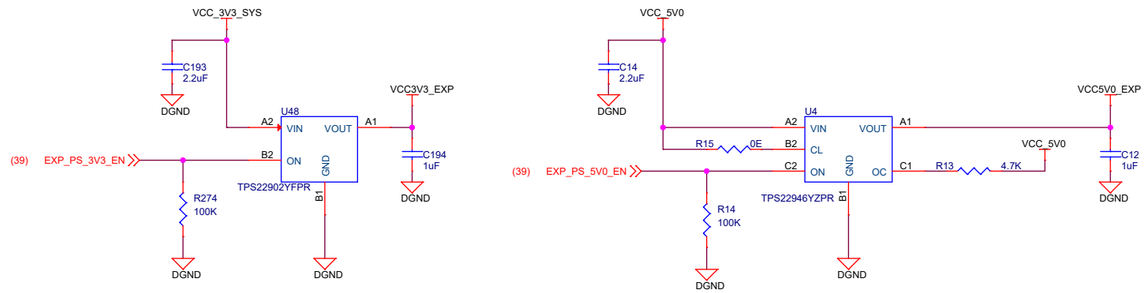


SOC_UART1 MUX



OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	SOC - EXP CONN
L	H	An=nB2	SOC - FT4232

POWER SWITCHES FOR USER EXPANSION CONNECTOR



NOTE:

AM62x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

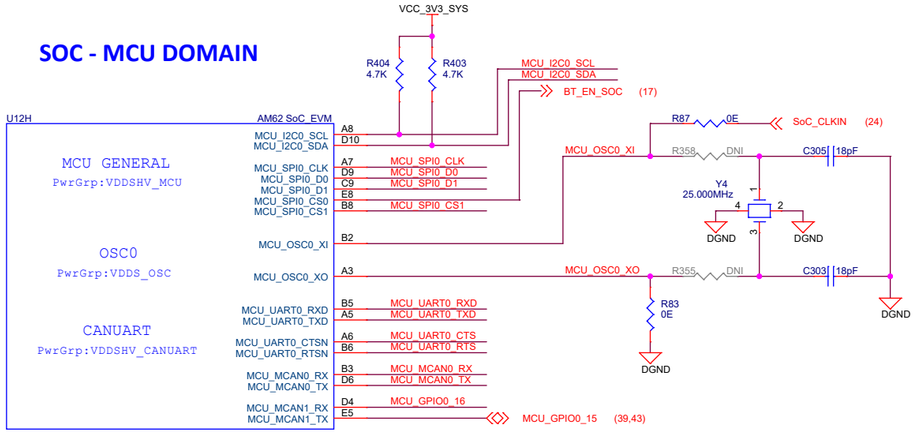
5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

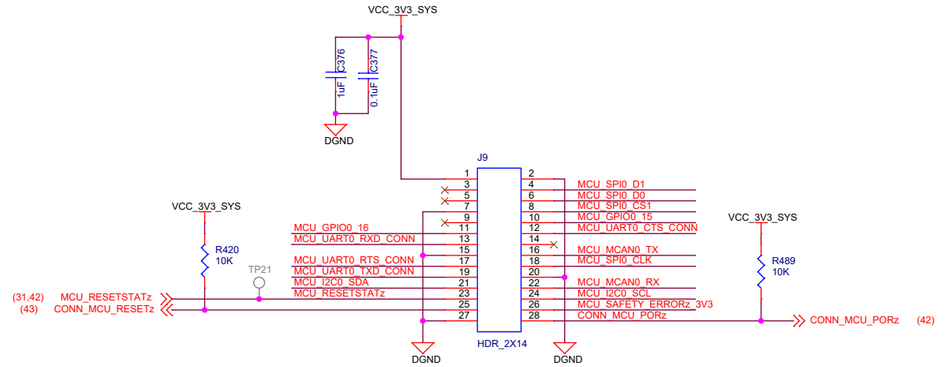
Designed for TI by Mistral Solutions Pvt Ltd

Title	USER EXPANSION CONNECTOR	
Size	PROC114E1	Rev E1
Date:	Thursday, October 28, 2021	Sheet 32 of 44

SOC - MCU DOMAIN

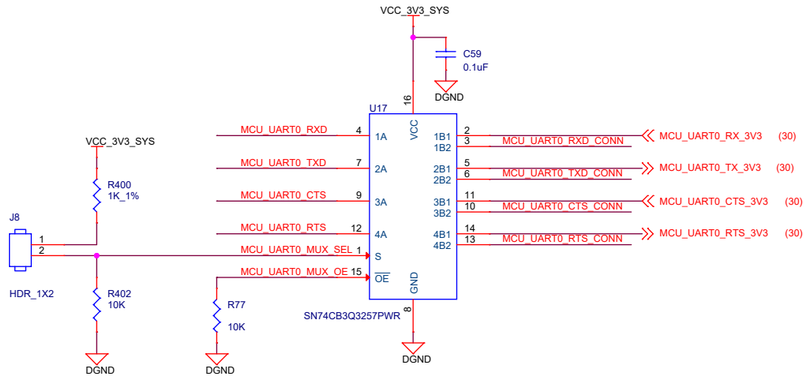


MCU HEADER

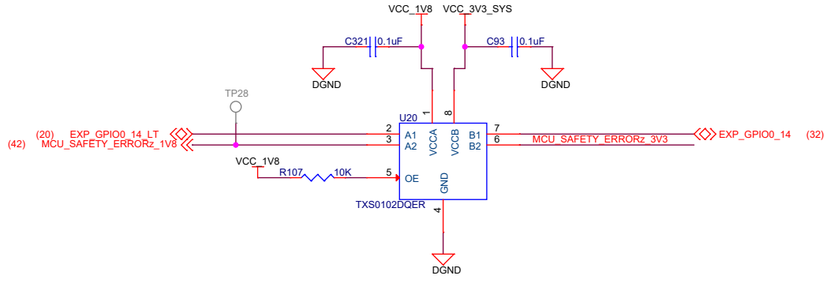


Silk: MCU HDR

MCU_UART0 MUX



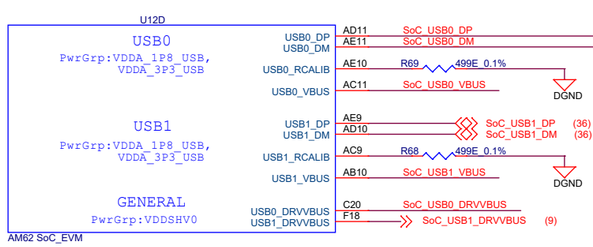
OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER



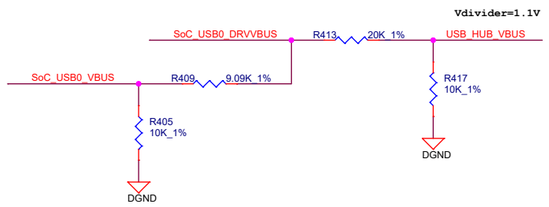
Designed for TI by Mistral Solutions Pvt Ltd

Title	MCU HEADER	
Size C	PROC114E1	Rev E1
Date: Tuesday, November 09, 2021	Sheet 33 of 44	

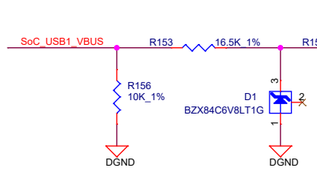
USB 2.0 HUB

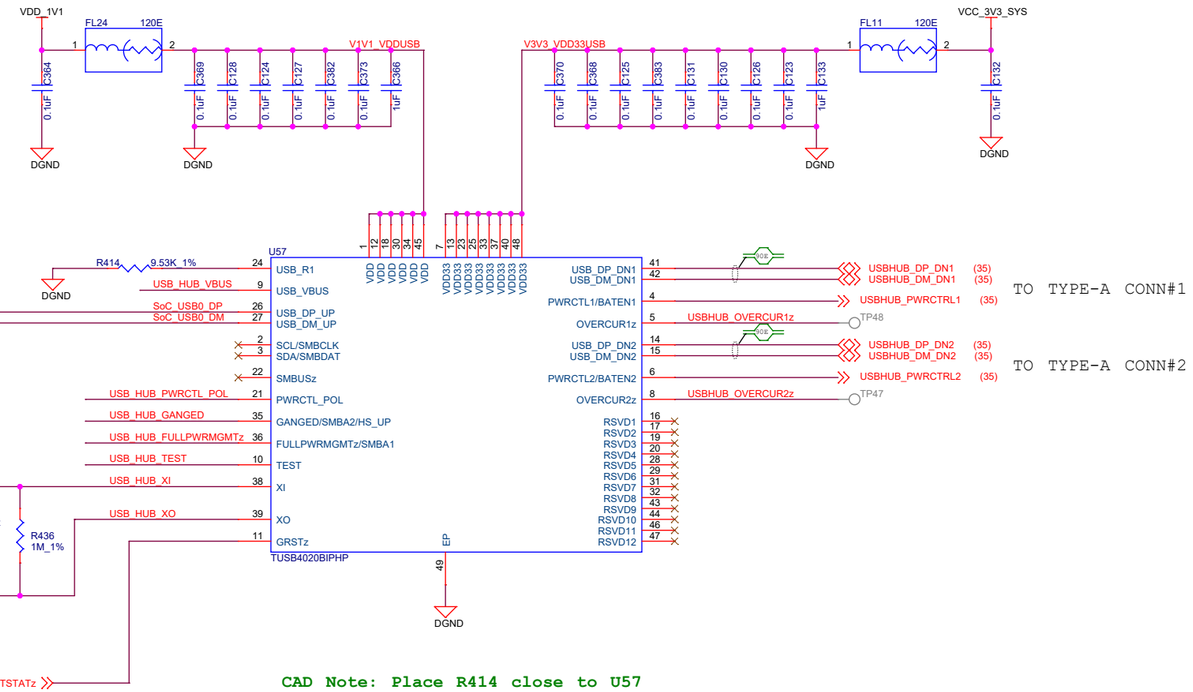


VBUS circuit for Embedded Hub

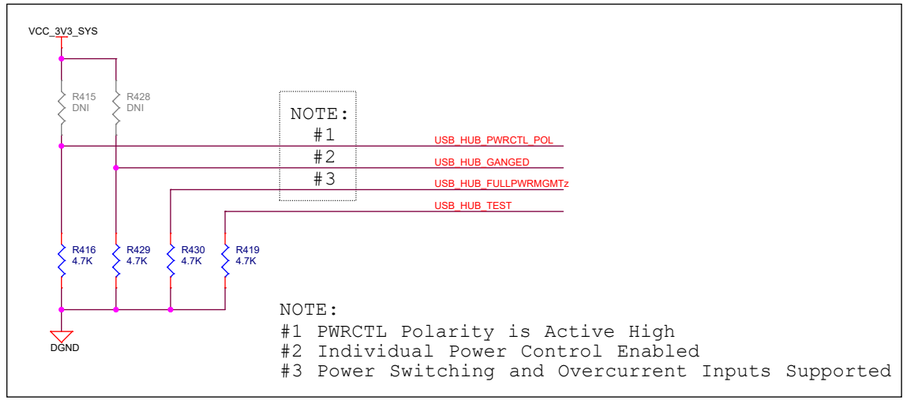


Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS





CAD Note: Place R414 close to U57

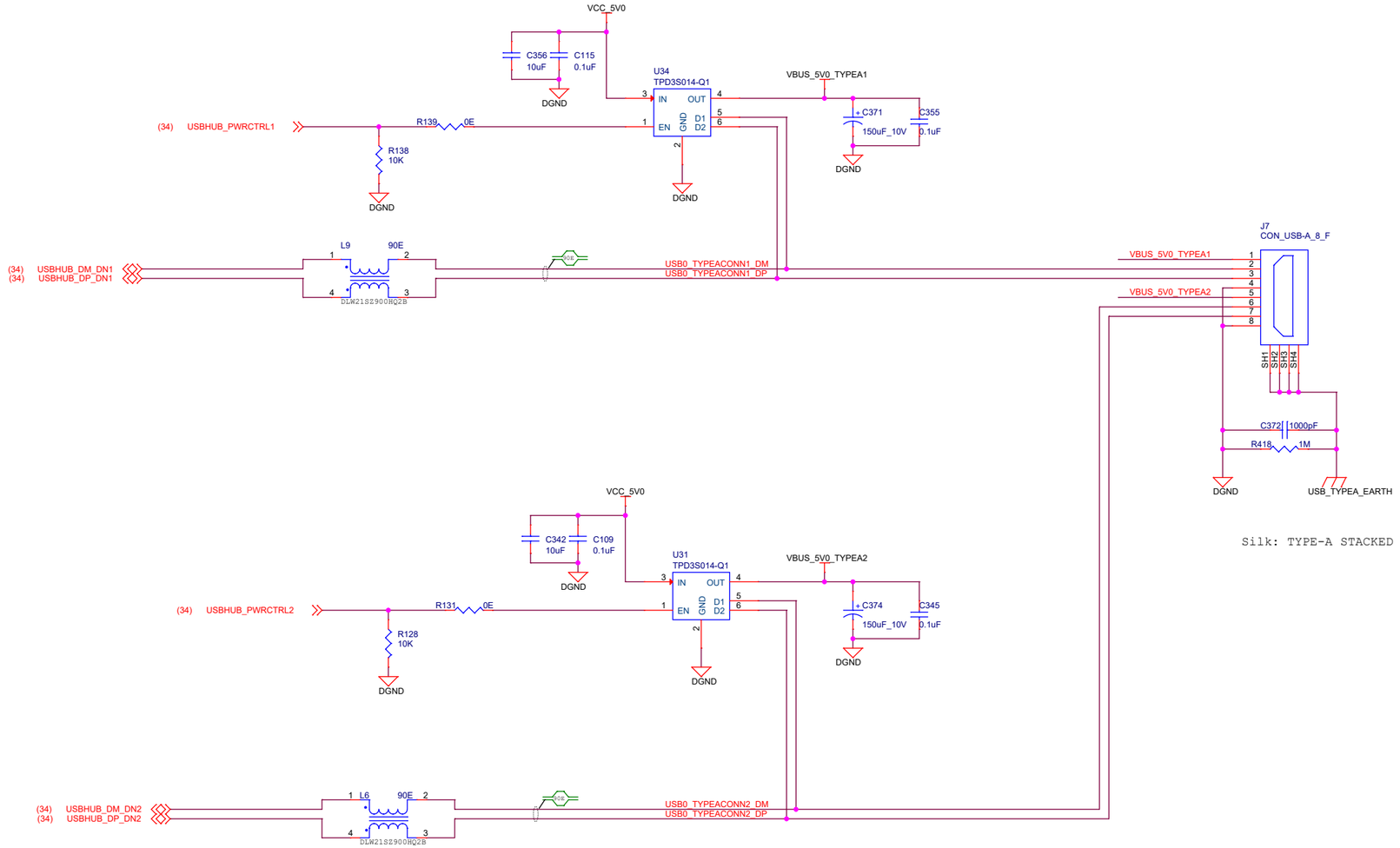


NOTE:
#1 PWRCTL Polarity is Active High
#2 Individual Power Control Enabled
#3 Power Switching and Overcurrent Inputs Supported

Designed for TI by Mistral Solutions Pvt Ltd

Title	USB 2.0 HUB	
Size C	PROC114E1	Rev E1
Date: Thursday, October 28, 2021	Sheet 34 of 44	

USB 2.0 TYPE A CONNECTORS

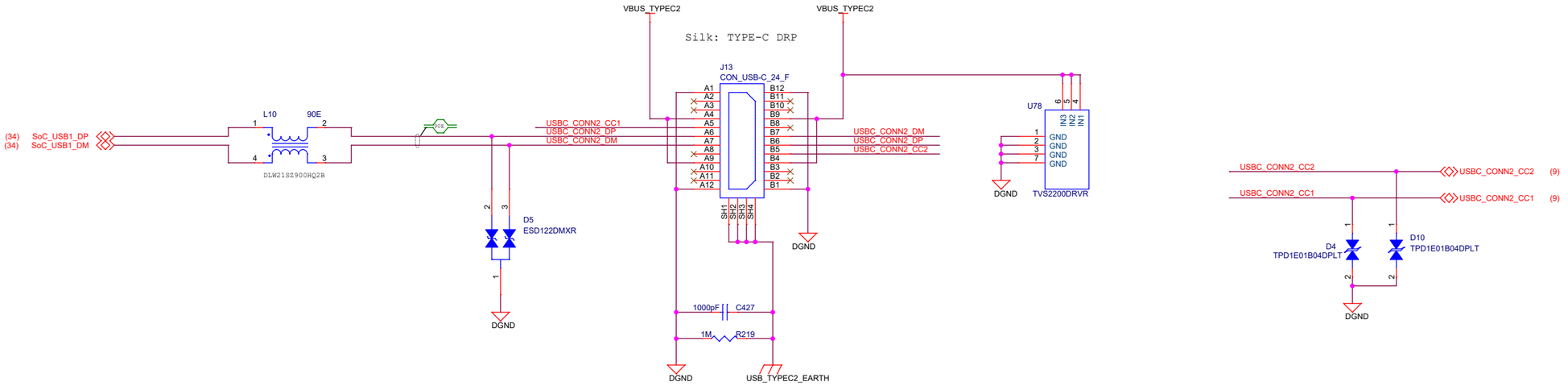


Silk: TYPE-A STACKED

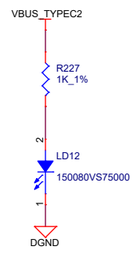
Designed for TI by Mistral Solutions Pvt Ltd

Title	USB 2.0 TYPE A CONNECTORS		
Size	PROC114E1		Rev
C			E1
Date:	Tuesday, November 02, 2021	Sheet 35 of 44	

USB 2.0 TYPE-C DRP



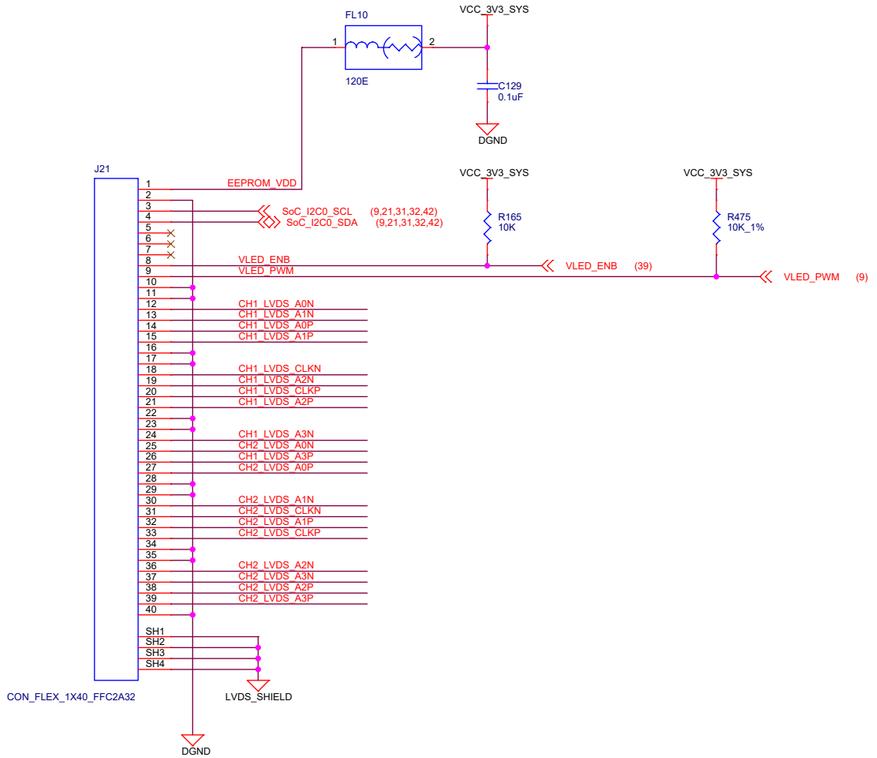
POWER INDICATION LED: VBUS_TYPEC2

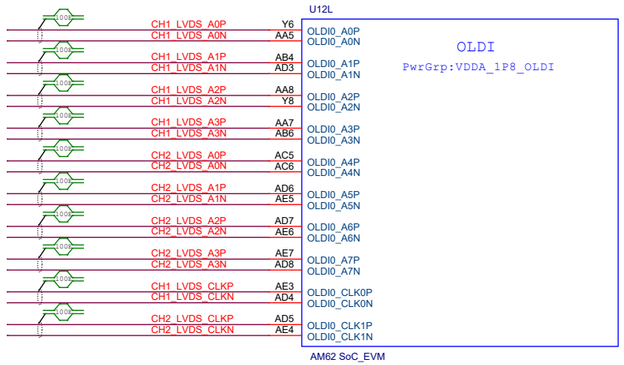


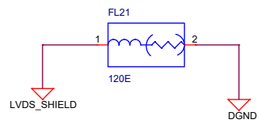
Designed for TI by Mistral Solutions Pvt Ltd

Title	USB TYPE-C DRP	
Size: C	PROC114E1	Rev: E1
Date: Thursday, October 28, 2021	Sheet 36 of 44	

OLDI DISPLAY INTERFACE







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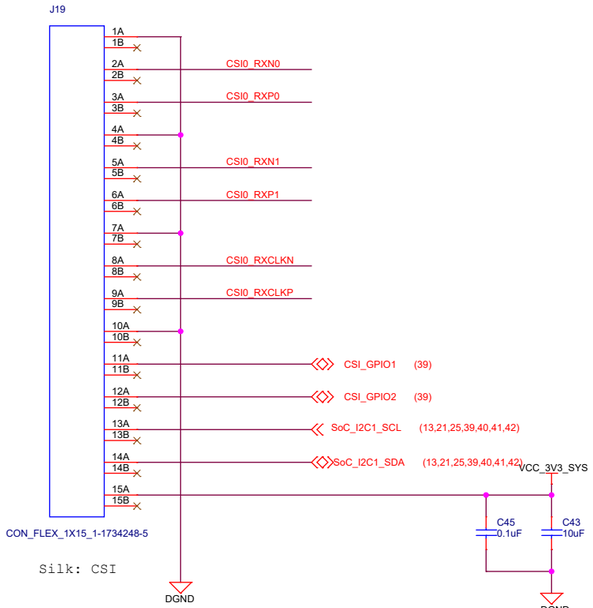
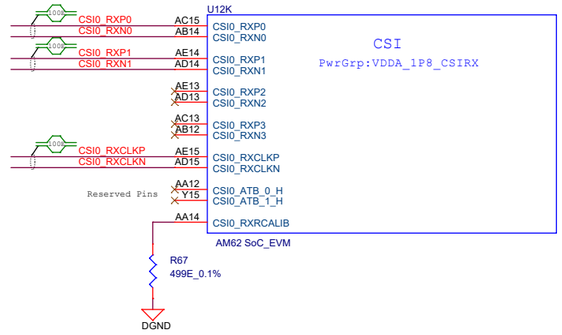
Title	OLDI DISPLAY INTERFACE	
Size C	PROC114E1	Rev E1
Date: Thursday, October 28, 2021	Sheet 37 of 44	

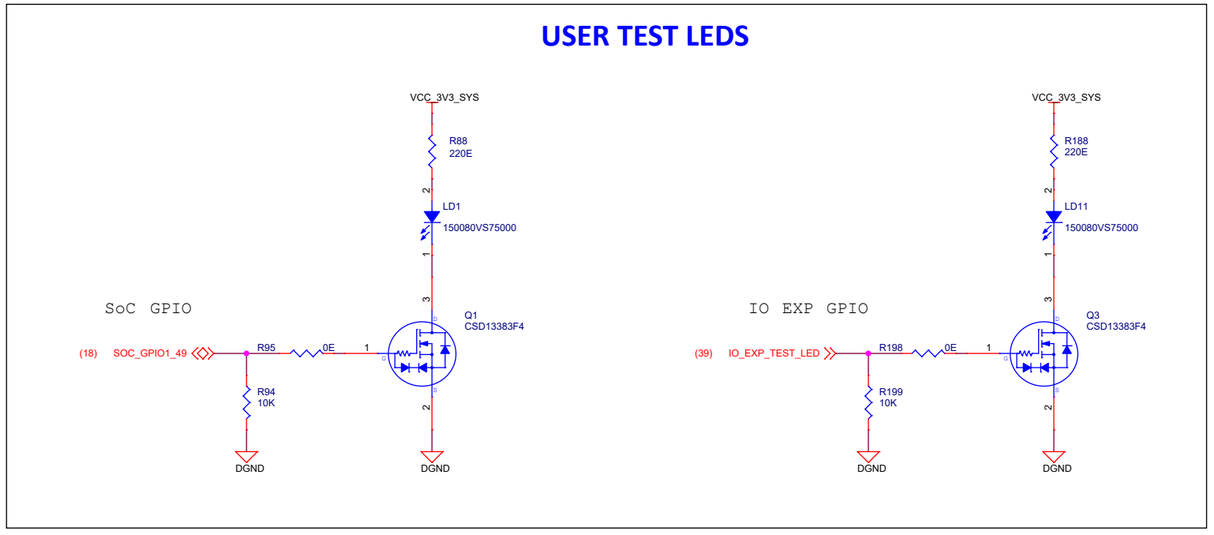
CSI INTERFACE

CSI CAMERA HEADER





USER TEST LEDS



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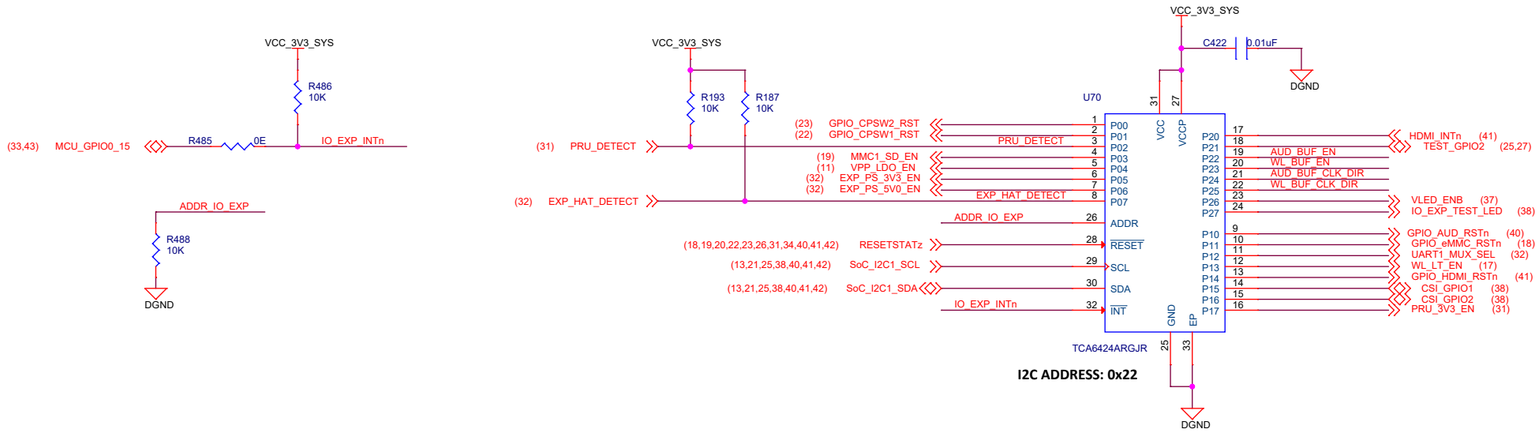
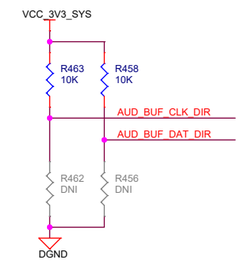
Title	CSI INTERFACE & USER TEST LEDS		
Size	PROC114E1		Rev
C			E1
Date:	Tuesday, November 02, 2021	Sheet 38 of 44	

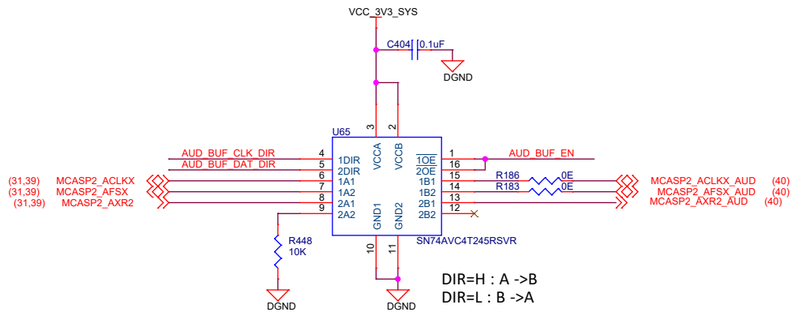
IO EXPANDER

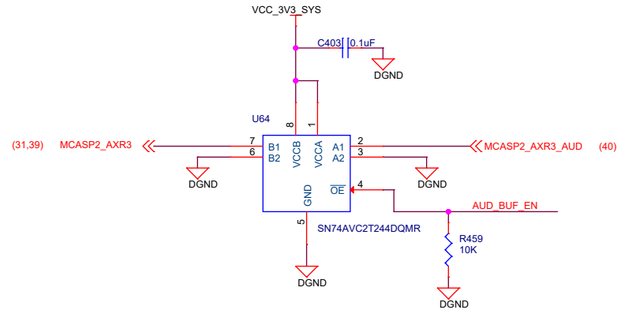


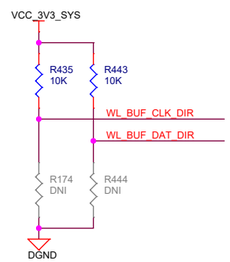
AUD_BUF_EN	WL_BUF_EN	MCASP2
LOW(DEFAULT)	HIGH(DEFAULT)	AUDIO CODEC
HIGH	LOW	WILINK BT

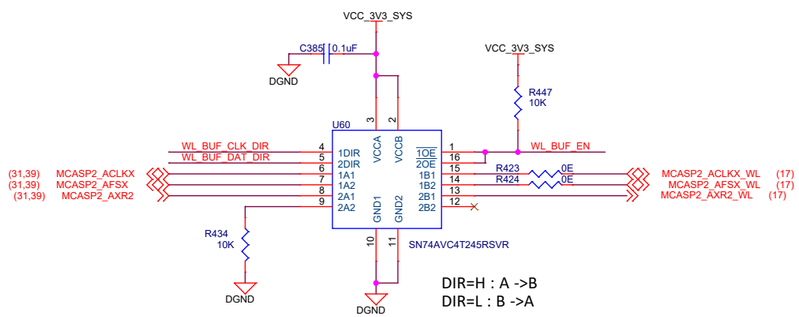
MCASP2 BUFFERS

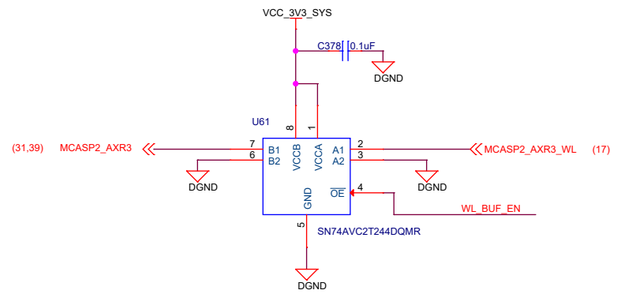








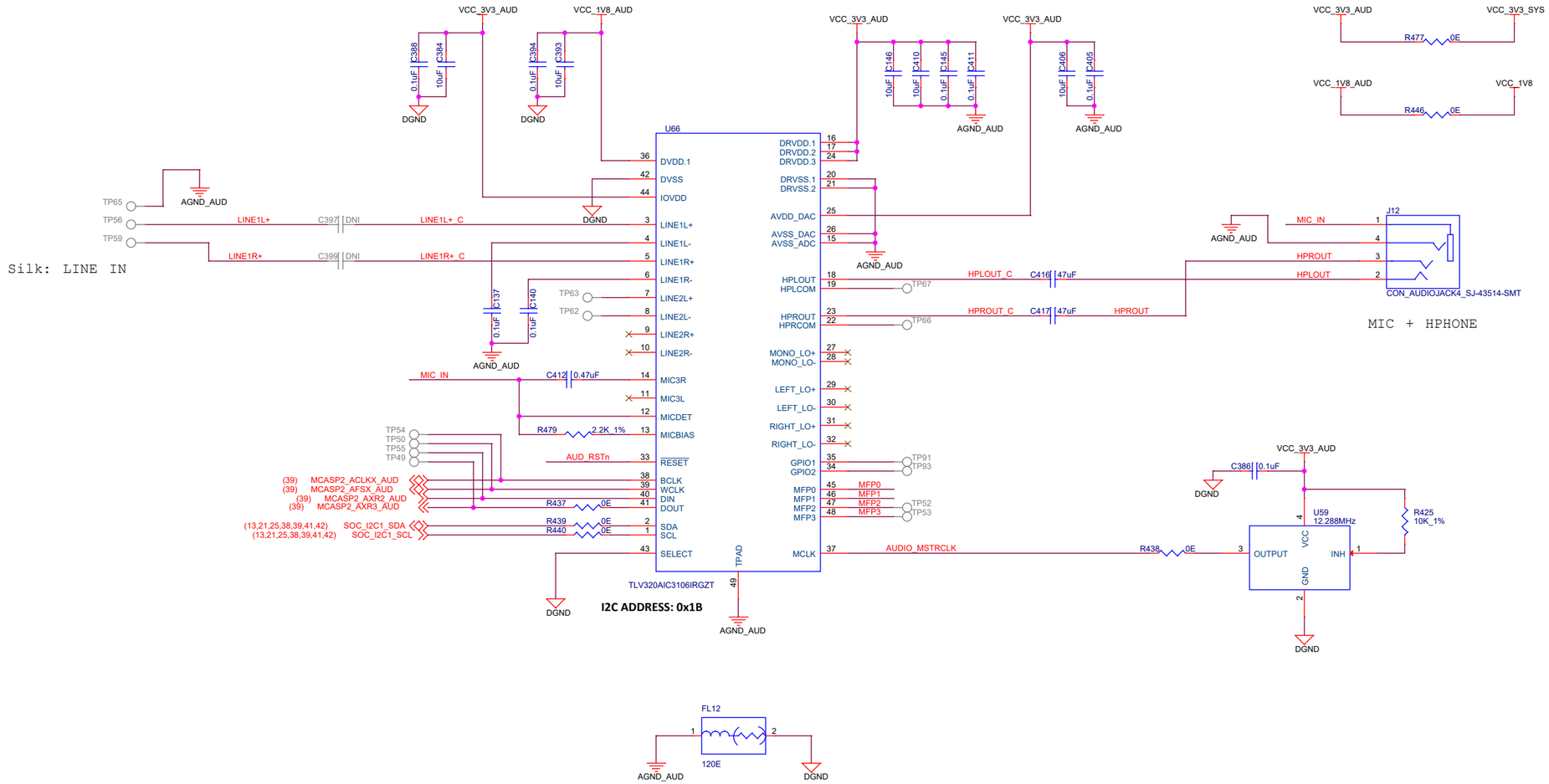




Designed for TI by Mistral Solutions Pvt Ltd

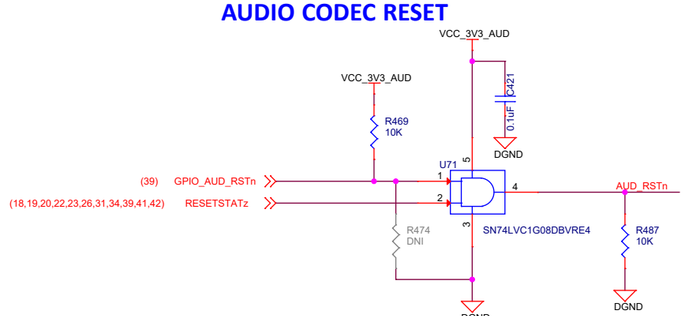
Title	IO EXPANDER	
Size: C	PROC114E1	Rev: E1
Date: Thursday, October 28, 2021	Sheet 39 of 44	

AUDIO CODEC



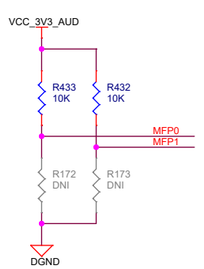
Silk: LINE IN

AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

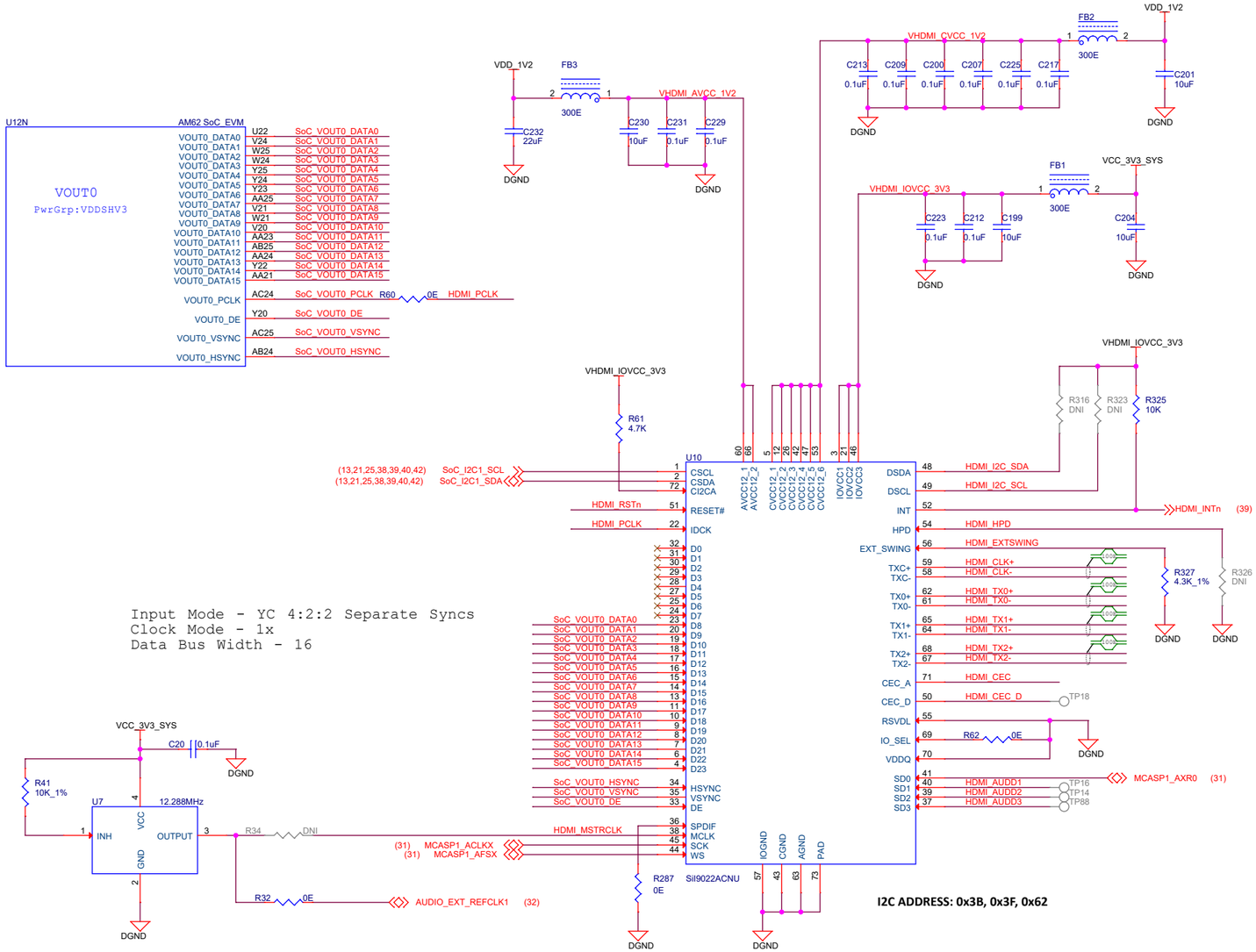
MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUDIO CODEC		
Size C	PROC114E1		Rev E1
Date:	Tuesday, November 02, 2021	Sheet 40 of 44	

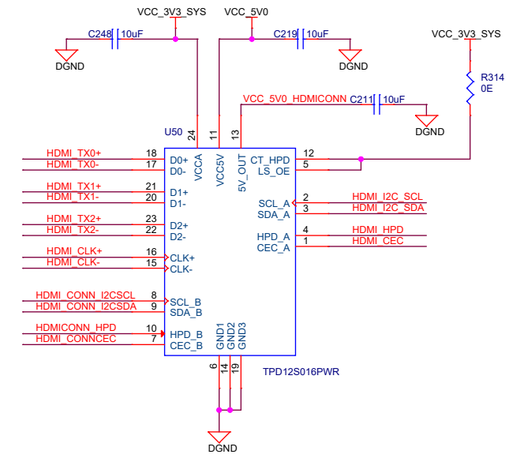
HDMI INTERFACE



Input Mode - YC 4:2:2 Separate Syncs
Clock Mode - 1x
Data Bus Width - 16

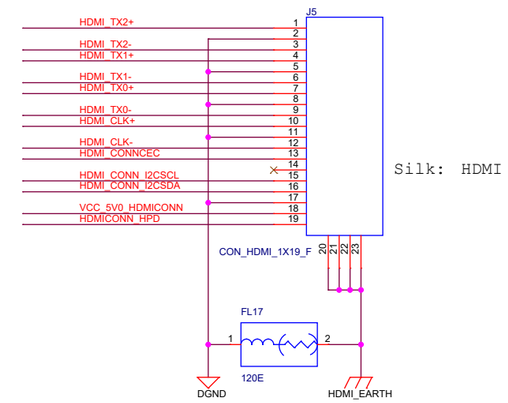
I2C ADDRESS: 0x3B, 0x3F, 0x62

HDMI ESD DEVICE



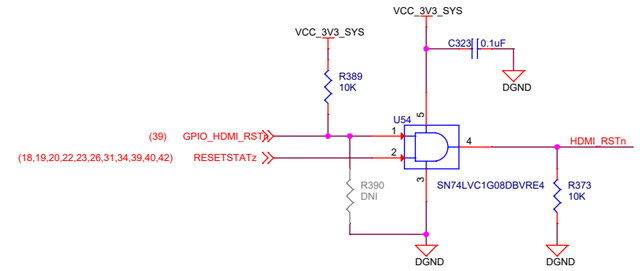
NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR



Silk: HDMI

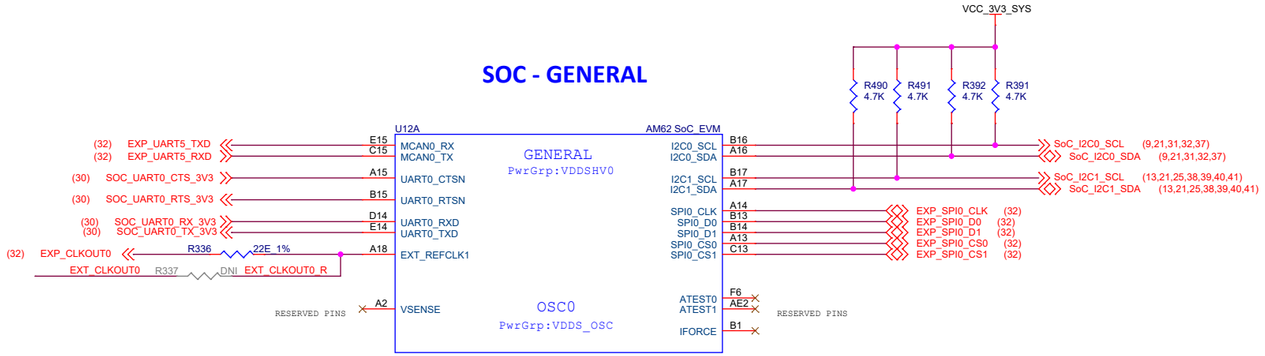
HDMI RESET



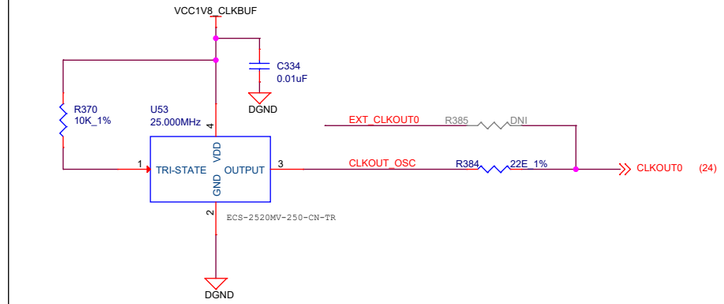
Designed for TI by Mistral Solutions Pvt Ltd

Title	HDMI INTERFACE		
Size	PROC114E1		Rev
C			E1
Date:	Thursday, October 28, 2021	Sheet 41 of 44	

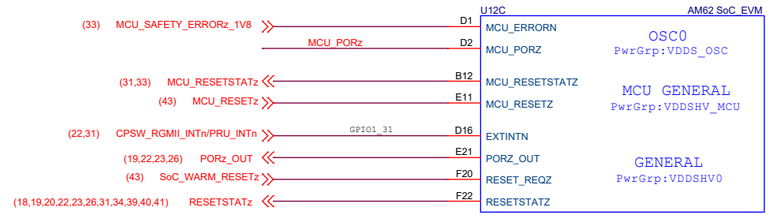
SOC - GENERAL

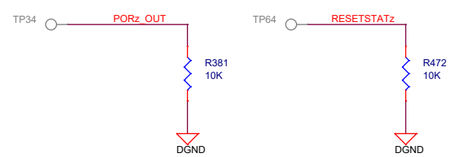


OSCILLATOR

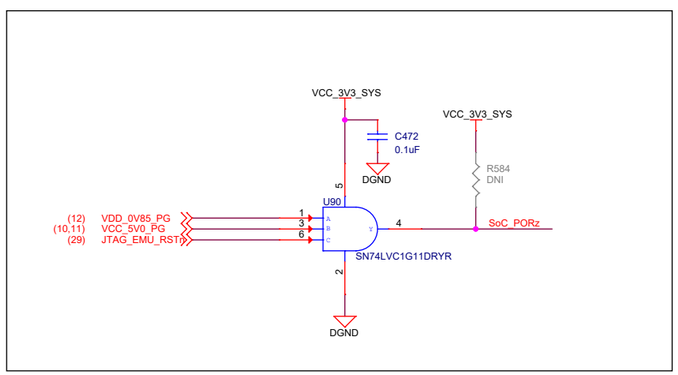


SOC - RESET

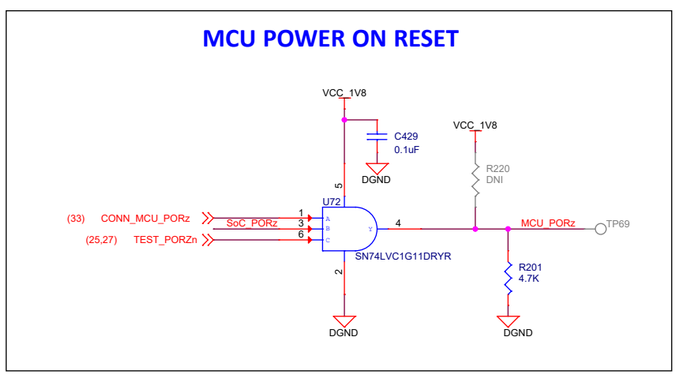




Pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up seqence



MCU POWER ON RESET



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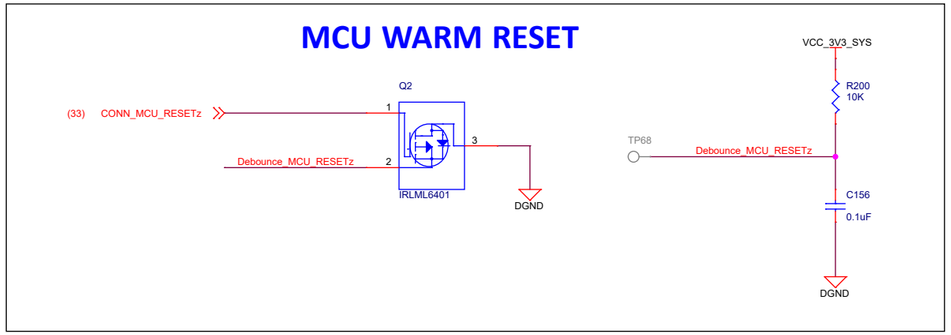
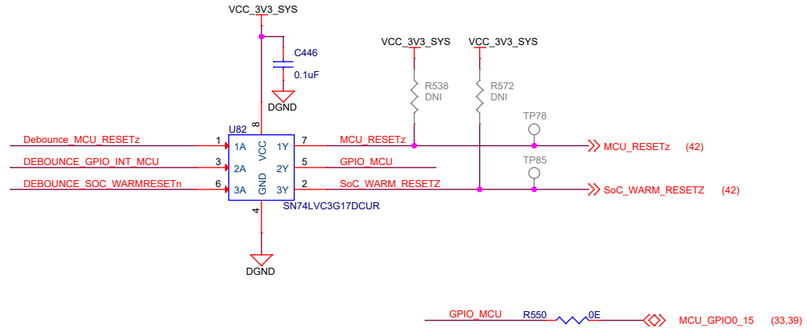
Title	OSCILLATOR		
Size C	PROC114E1		Rev E1
Date: Thursday, October 28, 2021		Sheet 42 of 44	

RESET

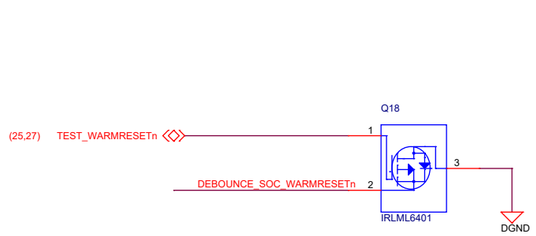
MCU WARM RESET

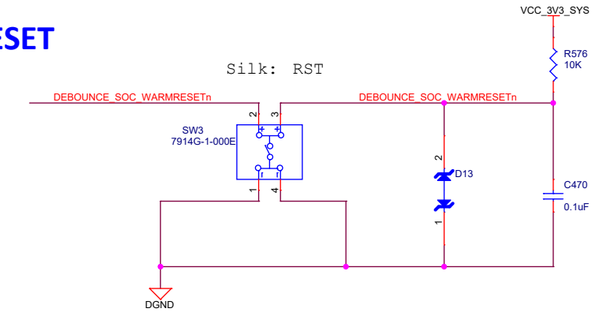


DEBOUNCE CIRCUIT

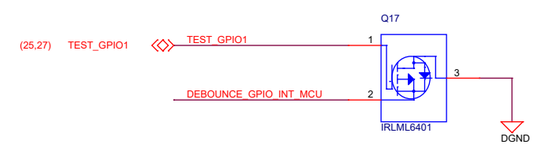


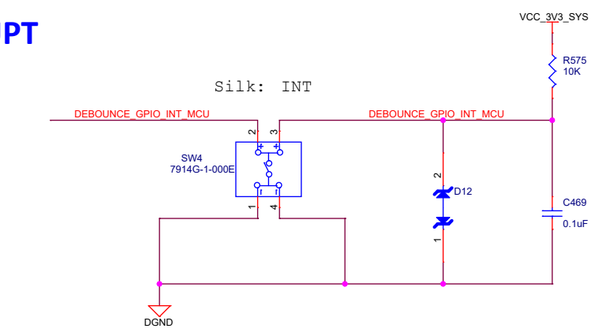
SOC WARM RESET





USER INTERRUPT





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Title	RESET		
Size: C	PROC114E1		Rev: E1
Date: Thursday, October 28, 2021		Sheet 43 of 44	

HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB

PROC114

PROC114E1

JUMPERS

ACC2

SPC02SYAN

LOGOs

PCB LOGO DNI — Texas Intruments

PCB LOGO DNI — For Evaluation only; not FCC approved for resale

PCB LOGO DNI — WEEE Mark

PCB LOGO DNI — CE Mark

AM62x SOCKET

ACC1

DNI

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

LABELS

Board Serial No.

LBL1

PCB LABEL

DNI

Assembly Revision

LBL2

PCB LABEL

DNI

Designed for TI by Mistral Solutions Pvt Ltd

Title	HARDWARE SCHEMATICS	
Size: C	PROC114E1	Rev: E1
Date: Monday, November 08, 2021	Sheet 44 of 44	