AM62x STARTER KIT EVM

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VER	0.03

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TEXAS INSTRUMENTS

MISTRAL

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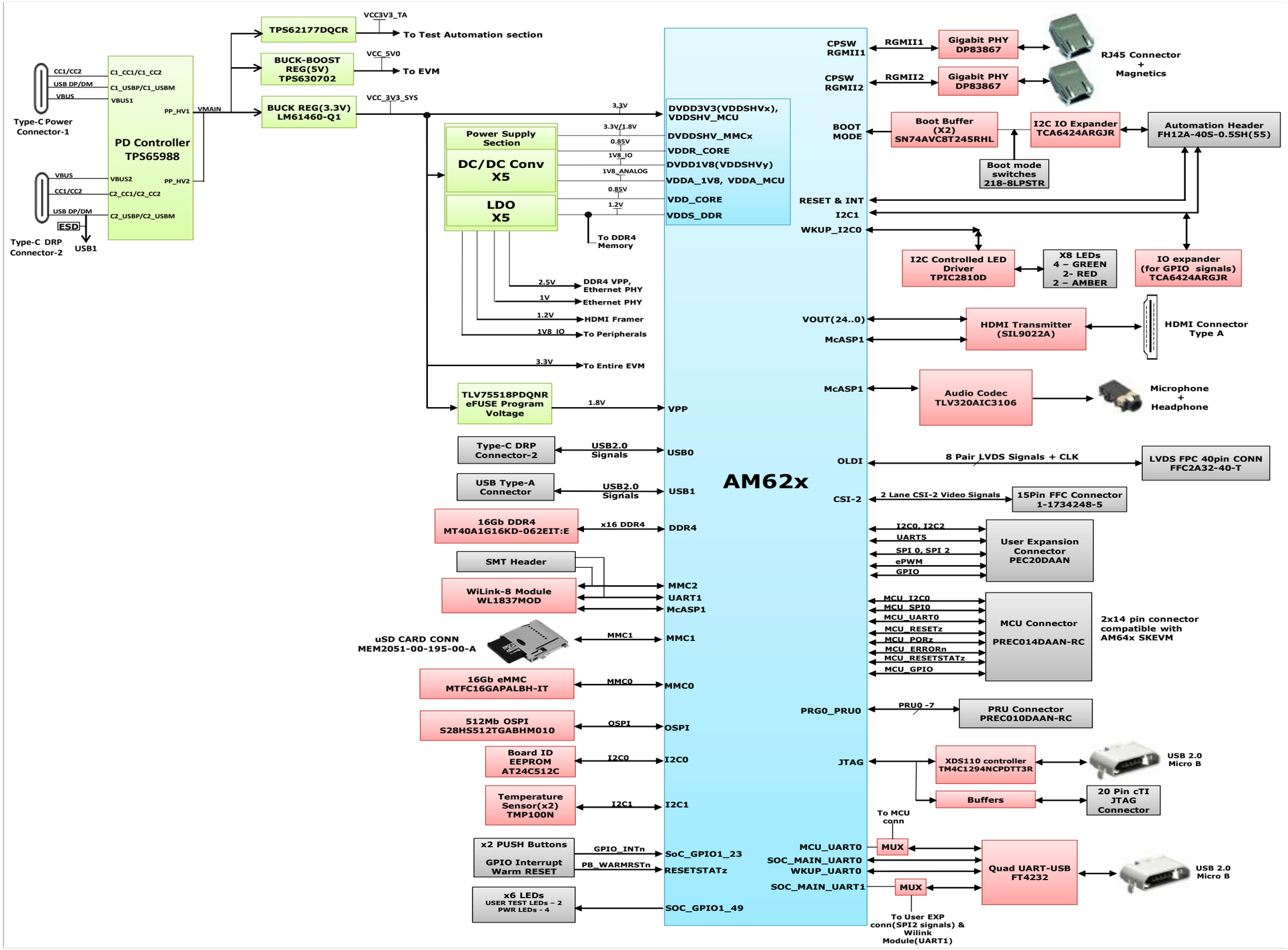
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	21 JAN 2022	Drafted from E1 Schematics	Mistral Design Team		
0.02	18 FEB 2022	Changes and Review comments are updated as mentioned in the Change list spreadsheet.	Mistral Design Team		
0.03	21 FEB 2022	Baselined and Released	Mistral Design Team		

BLOCK DIAGRAM AM62x SKEVM



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Title	BLOCK DIAGRAM AM62x SKEVM		
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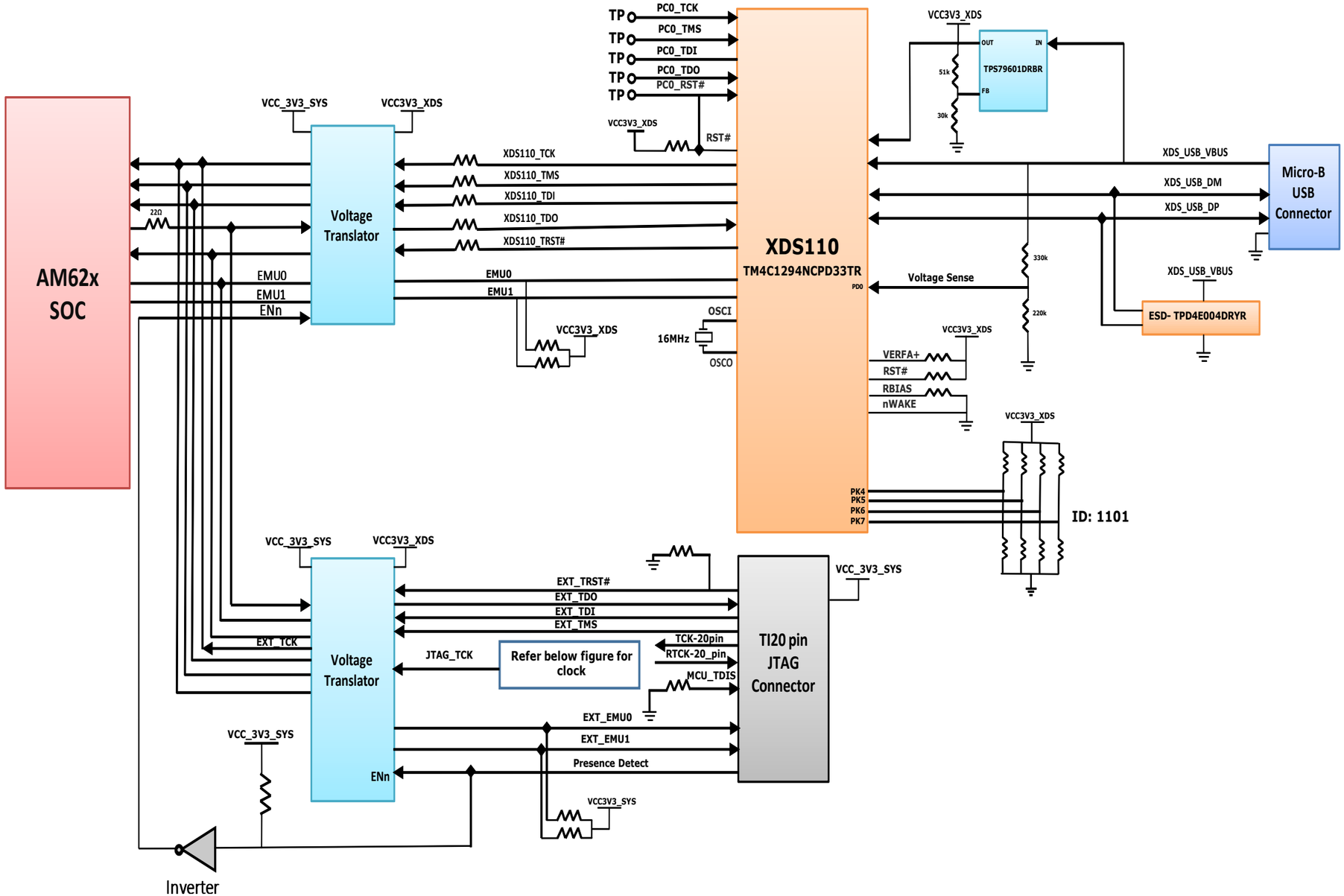
BLOCK DIAGRAM_XDS110



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Title	BLOCK DIAGRAM_XDS110	
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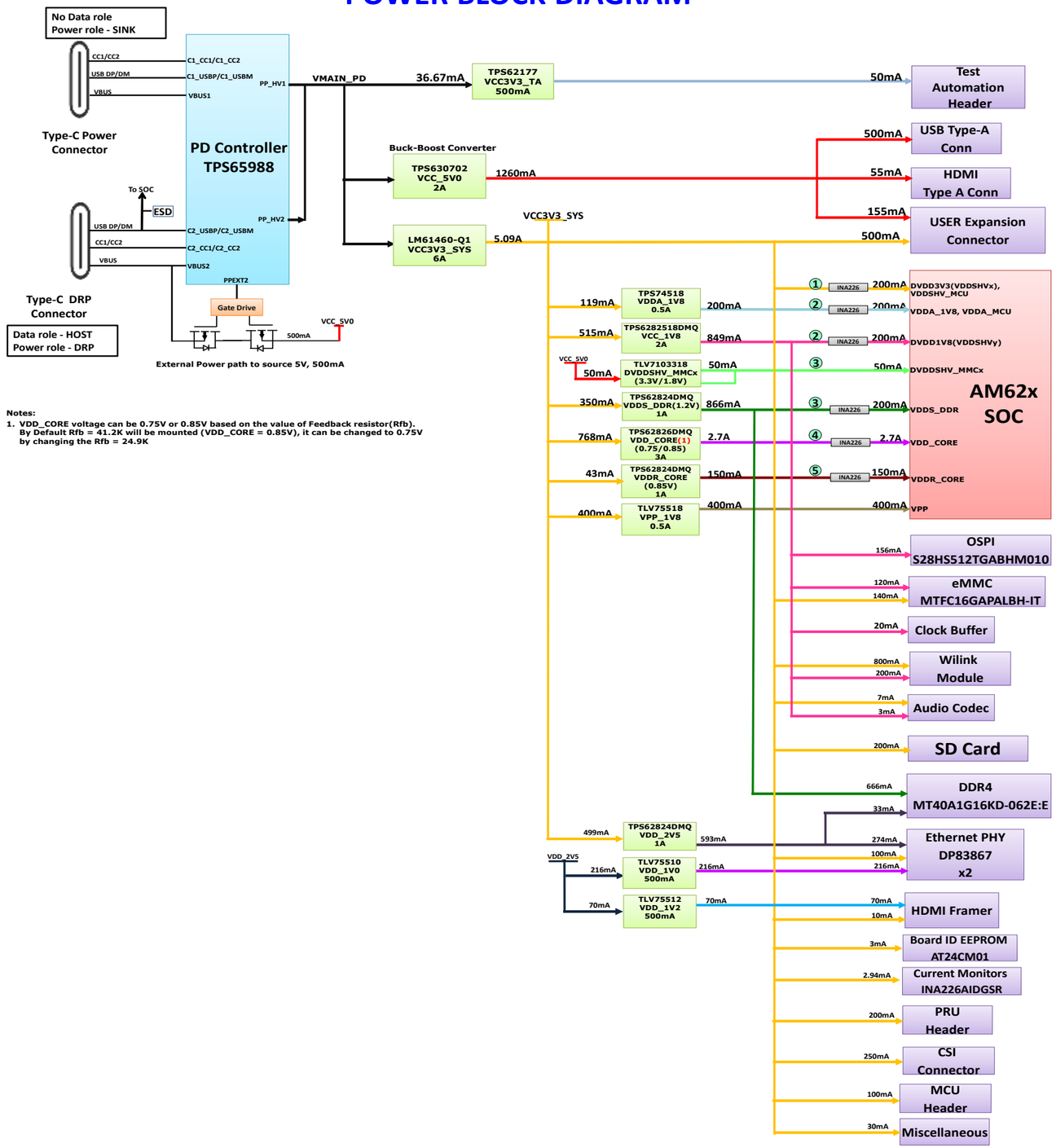
POWER BLOCK DIAGRAM



Notes:

1. VDD_CORE voltage can be 0.75V or 0.85V based on the value of Feedback resistor(Rfb). By Default Rfb = 41.2K will be mounted (VDD_CORE = 0.85V), it can be changed to 0.75V by changing the Rfb = 24.9K

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Title	POWER BLOCK DIAGRAM		
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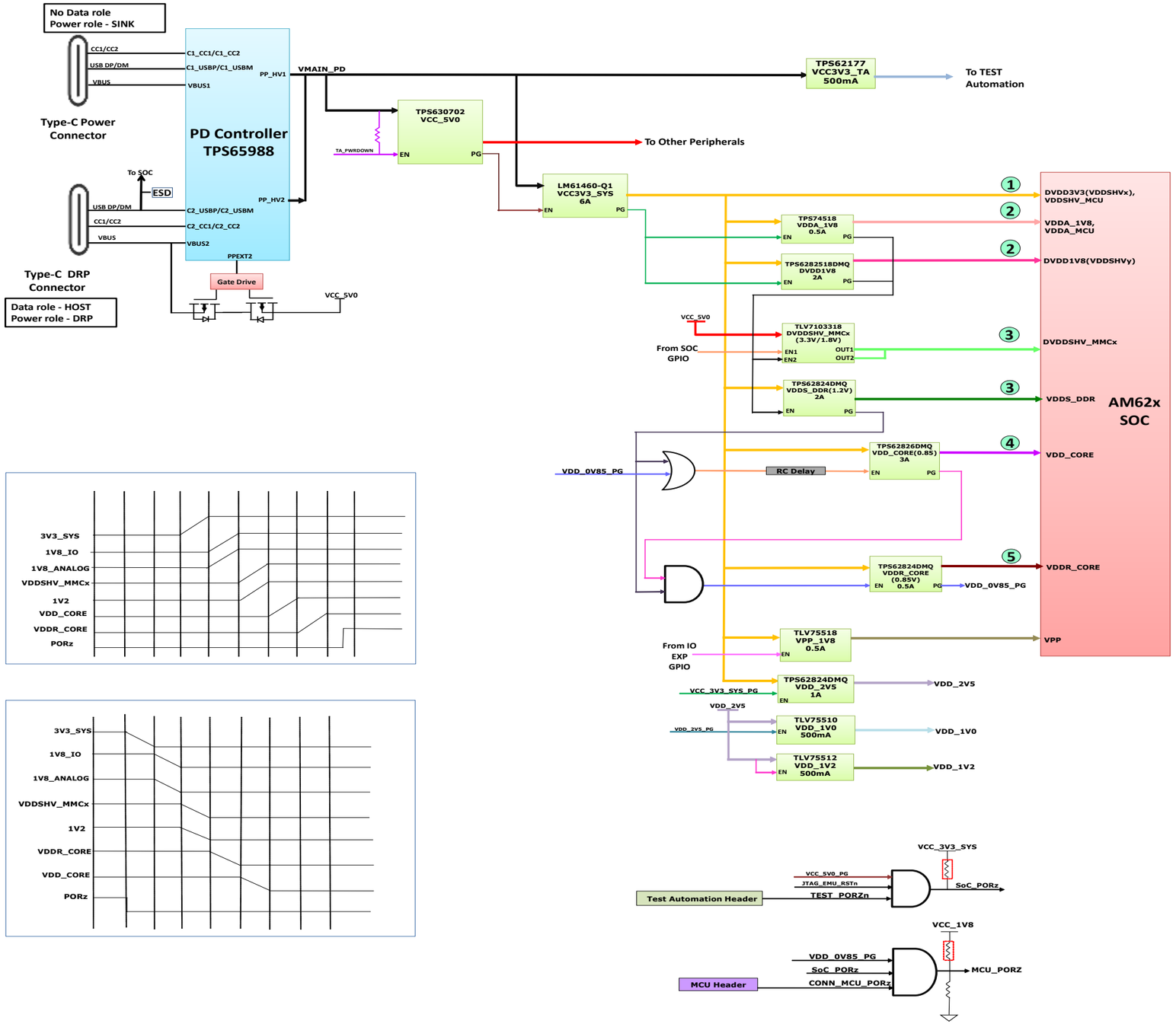
POWER SEQUENCE



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Title	POWER SEQUENCE		
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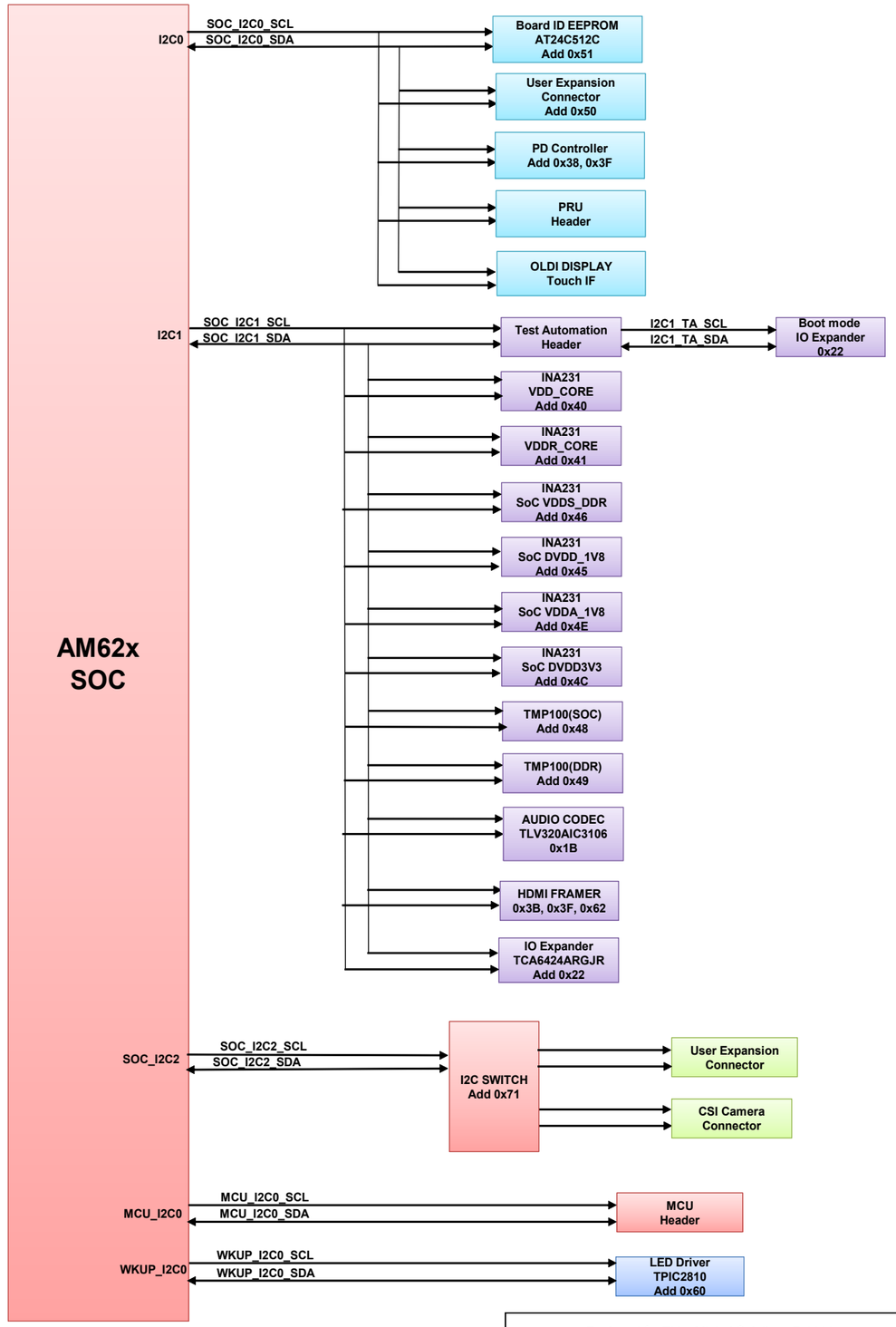
I2C TREE



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Title	I2C TREE		
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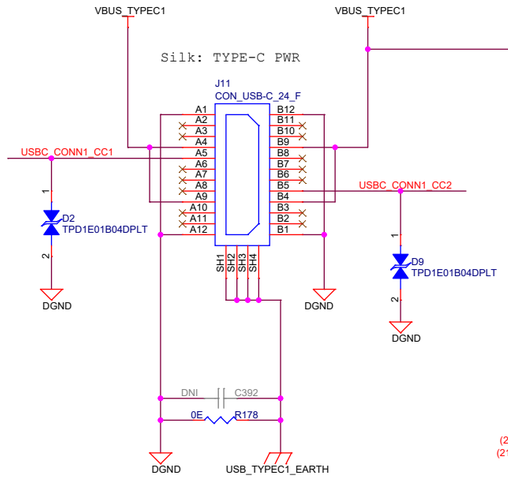
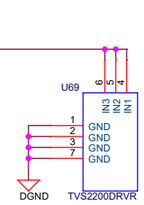
GPIO MAPPING TABLE

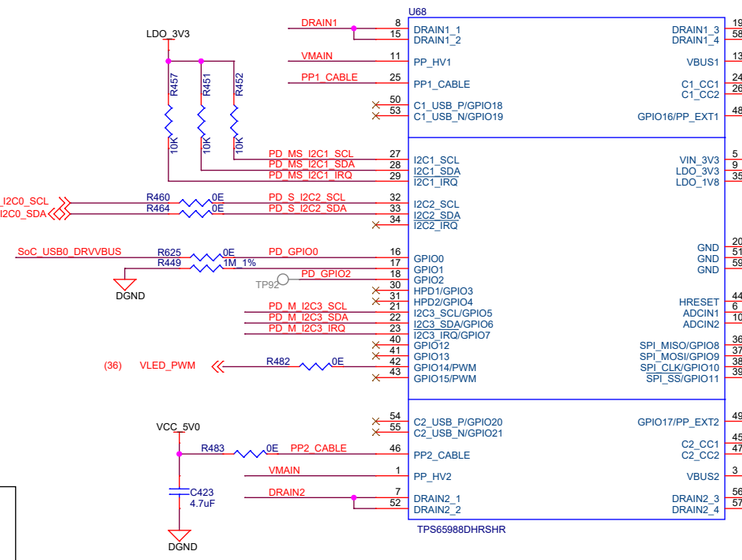
SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	PRU Connector Interrupt									
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	SoC_GPIO1_23	UART0_RTSN	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	User Interrupt Push Button/ TEST GPIO1 from Test Automation Connector									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P00		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER -P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER - P10		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER - P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	UART1 FET Switch and Buffer Enable signal	UART1_FET_BUF_EN	ENABLE	IO EXPANDER - P12		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP1 FET Switch Enable	MCASP1_FET_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20	MCASP1 Level Translator buffer for BT Enable	MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER - P23		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
21	MCASP1 FET Switch select pin status	MCASP1_FET_SEL	GPIO	IO EXPANDER - P24		INPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
22	SOC UART1 FET Switch Select	UART1_FET_SEL	SELECT	IO EXPANDER - P25		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3

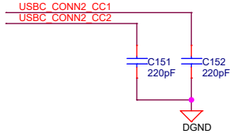
USB TYPE-C POWER

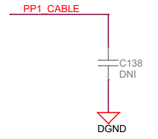


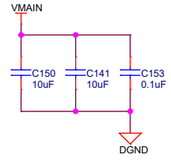


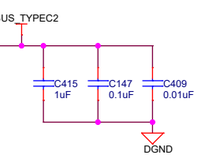
TYPE-C DUAL PD CONTROLLER



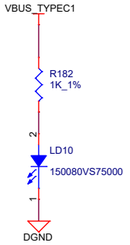




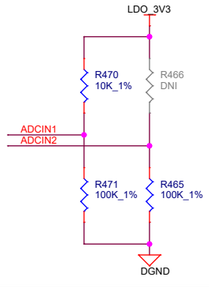




POWER INDICATION LED: VBUS_TYPEC1

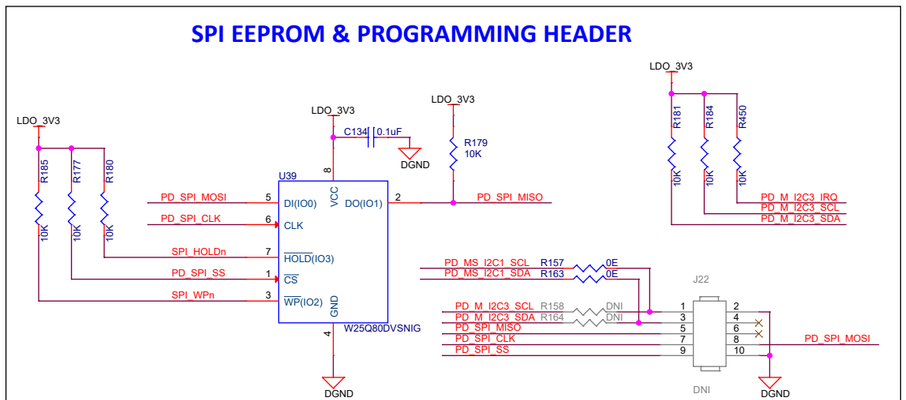


BP_NoWait
Safe Configuration

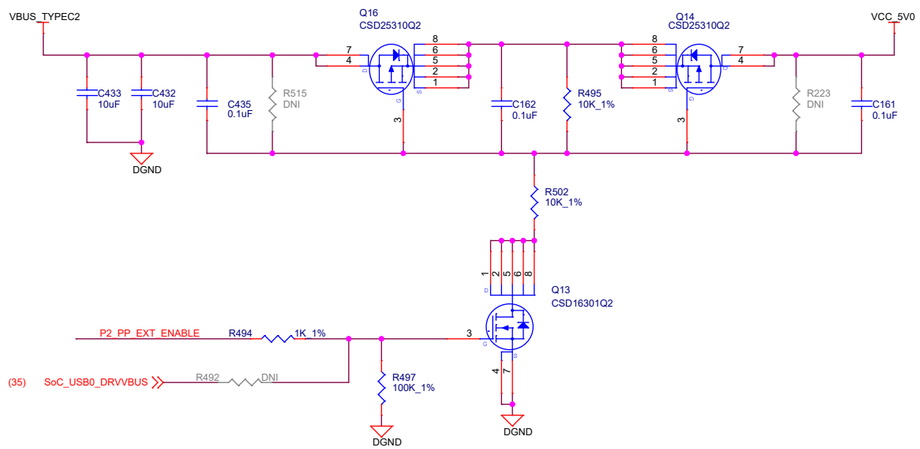


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

SPI EEPROM & PROGRAMMING HEADER



EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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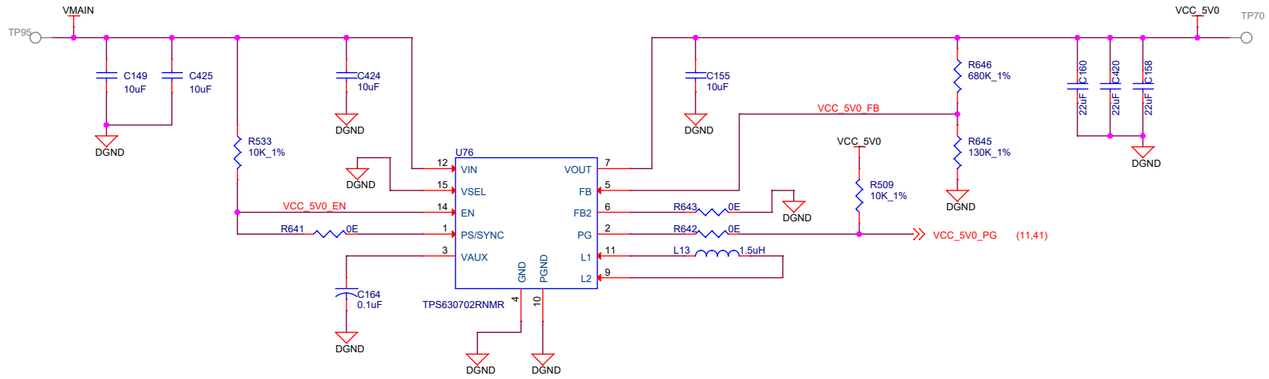
PERIPHERAL POWER SUPPLY-1



Power Cycle control from Test Automation

GROUND TEST POINTS

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Title	PERIPHERAL POWER SUPPLY -1	
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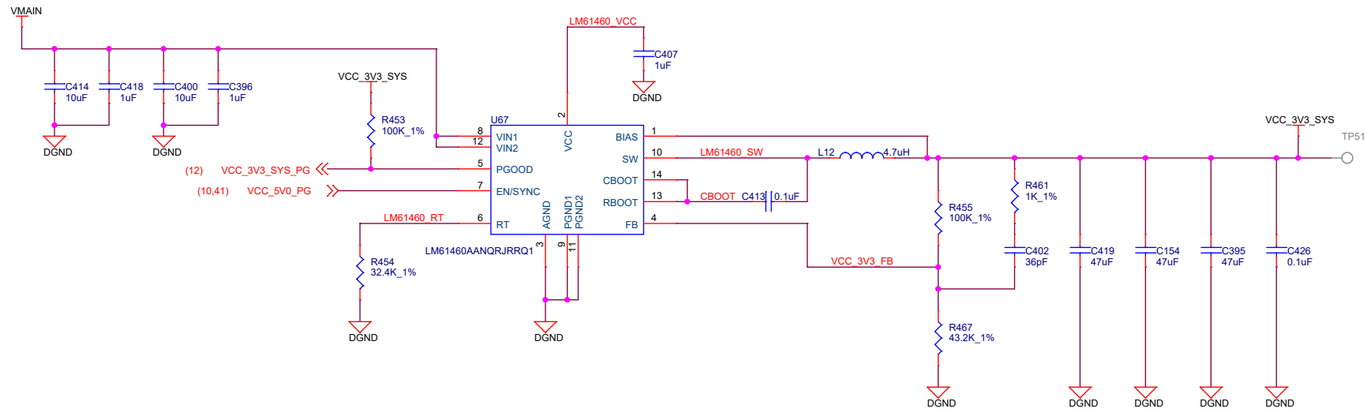
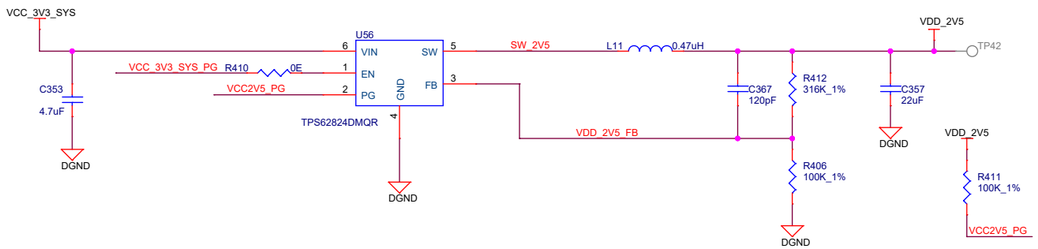
PERIPHERAL POWER SUPPLY-2

3.3V, 6.0AMPS SUPPLY

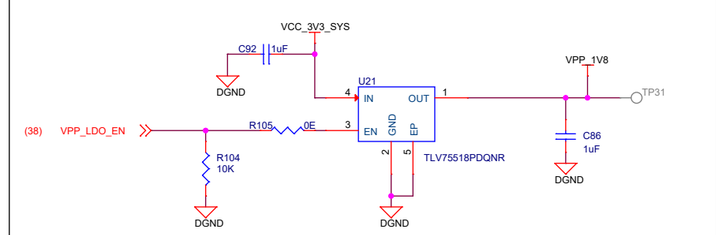
VinMin = 4.5V
VinMax = 24V
Vout = 3.3V @ 6A



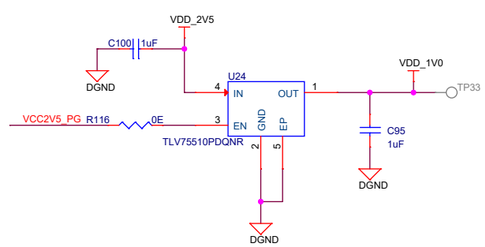
2.5V, 1.0AMPS SUPPLY



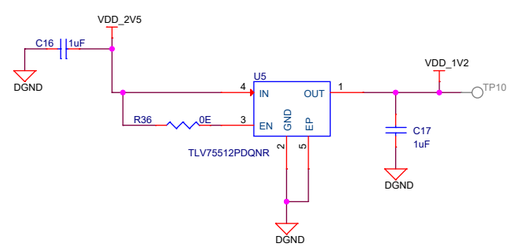
1.8V VPP, 0.5AMPS SUPPLY



1.0V, 0.5AMPS SUPPLY



1.2V, 0.5AMPS SUPPLY



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Title	PERIPHERAL POWER SUPPLY-2		
Size	PROC114E2		Rev
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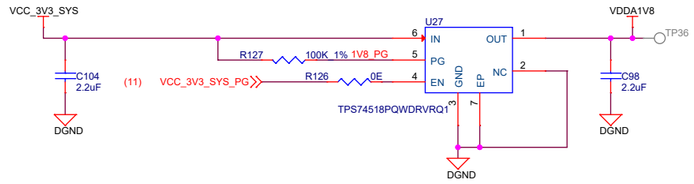
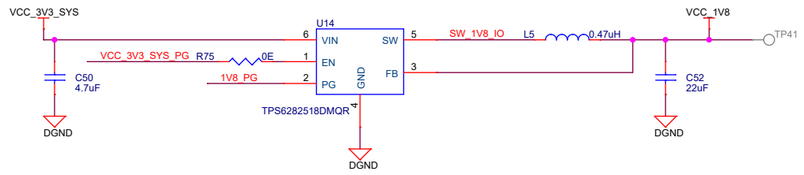
SOC POWER SUPPLY

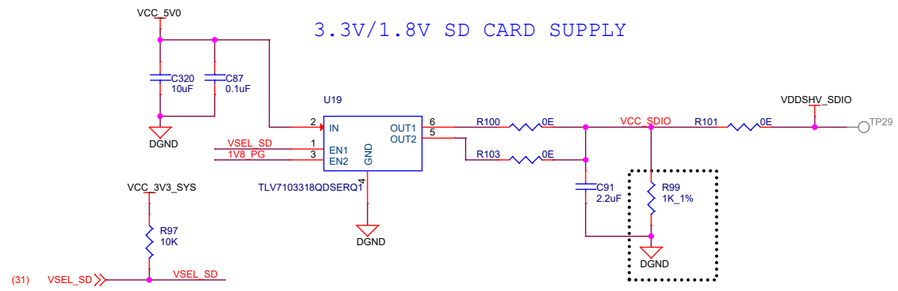
1.8V ANALOG, 0.5 AMPS SUPPLY



1.8V IO, 2.0 AMPS SUPPLY



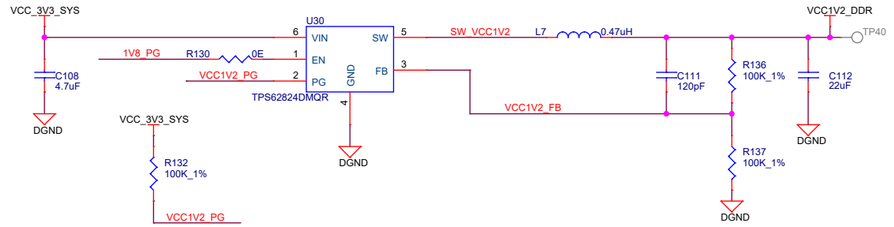
3.3V/1.8V SD CARD SUPPLY



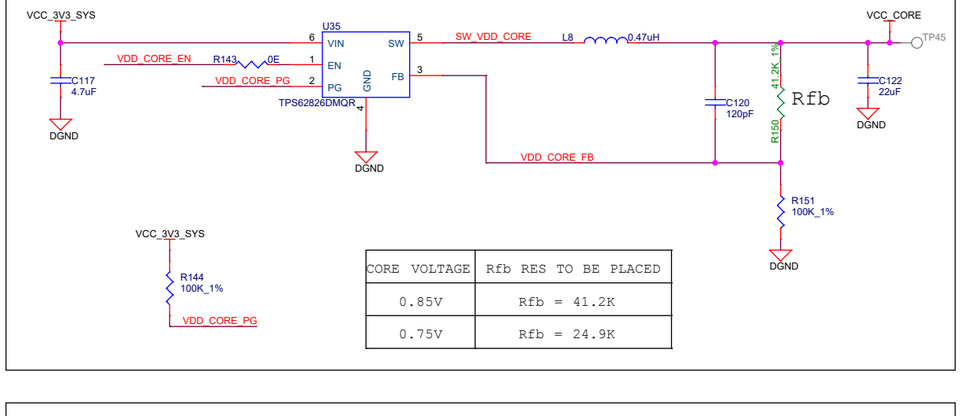
Note: Resistor is to 'bleed' off voltage.

VSEL_SD	SD VOLTAGE
HIGH(DEFAULT)	3.3V
LOW	1.8V

1.2V , 1.0 AMPS SUPPLY

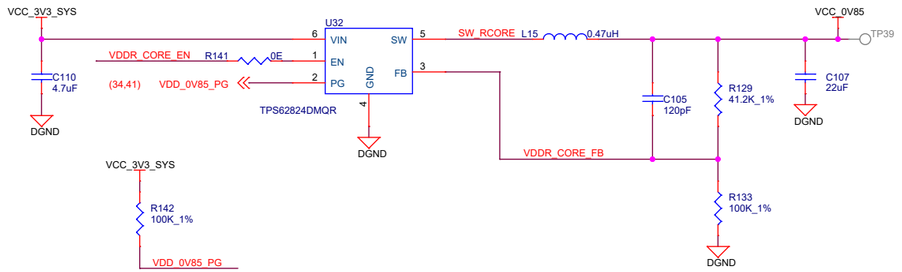


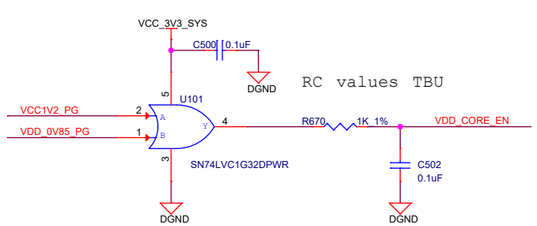
0.75V/0.85V , 3.0 AMPS SUPPLY

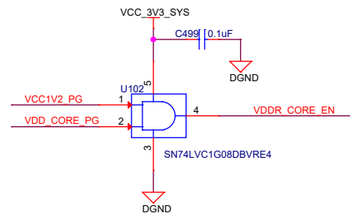


CORE VOLTAGE	Rfb RES TO BE PLACED
0.85V	Rfb = 41.2K
0.75V	Rfb = 24.9K

0.85V, 0.5 AMPS SUPPLY







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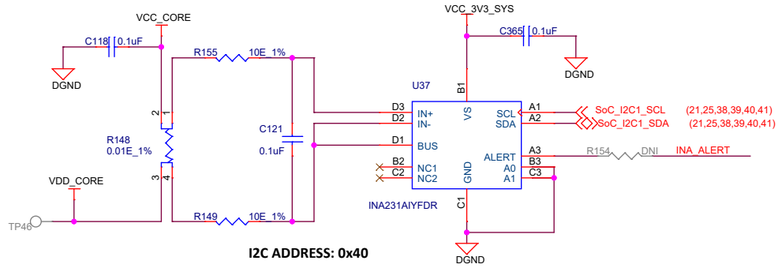
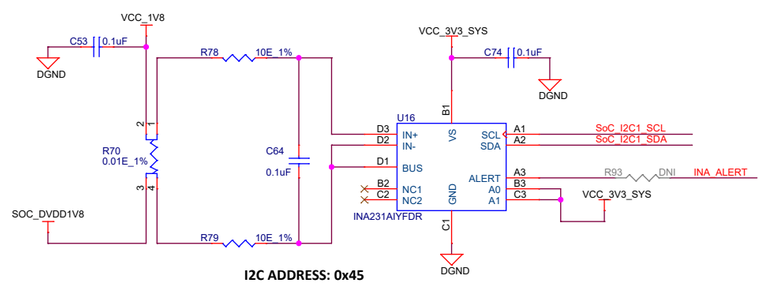
CURRENT MONITORING DEVICES

VDD_CORE



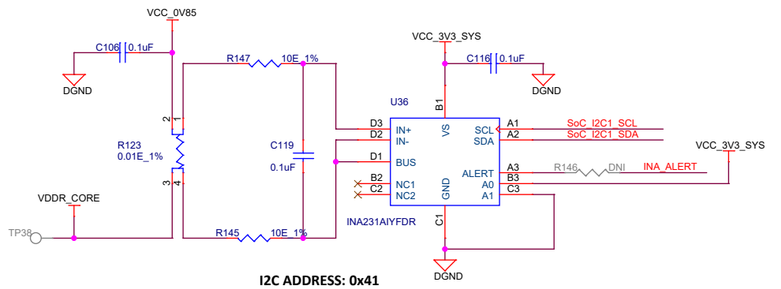
I2C ADDRESS: 0x40

SoC_DVDD1V8



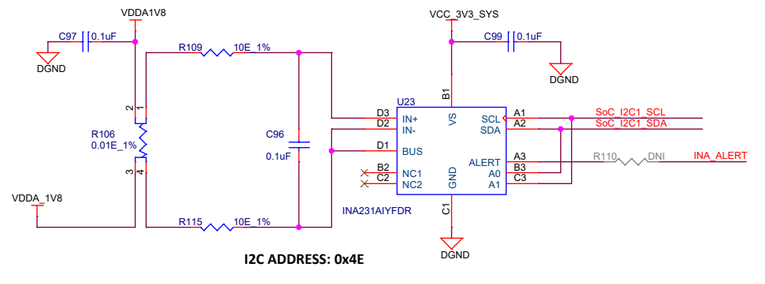
I2C ADDRESS: 0x45

VDDR_CORE



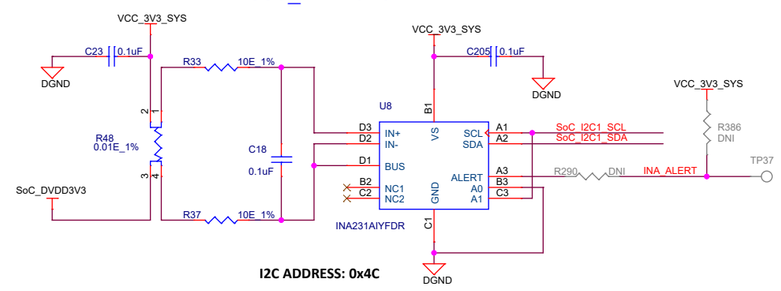
I2C ADDRESS: 0x41

VDDA_1V8



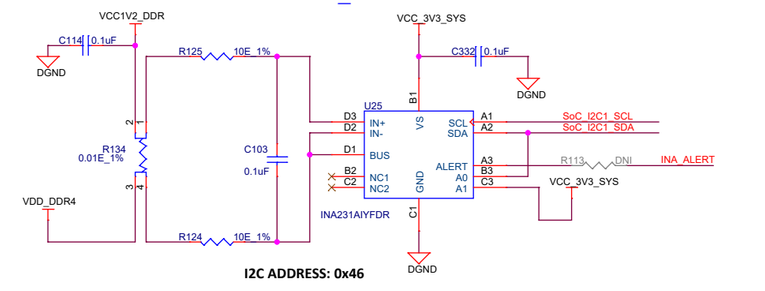
I2C ADDRESS: 0x4E

SoC_DVDD3V3



I2C ADDRESS: 0x4C

VDD_DDR4



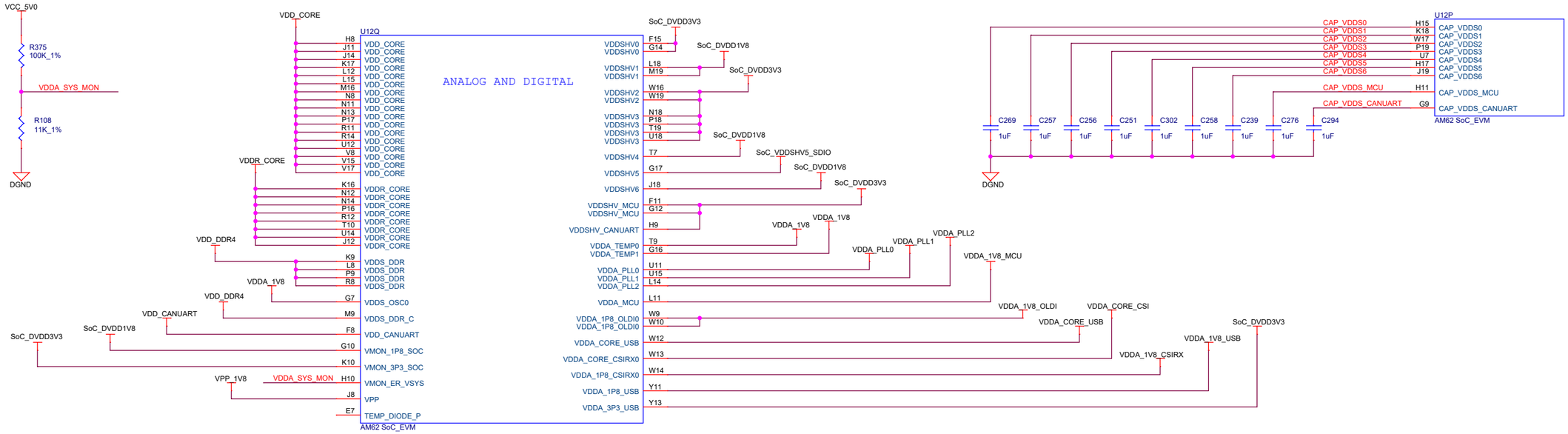
I2C ADDRESS: 0x46

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46

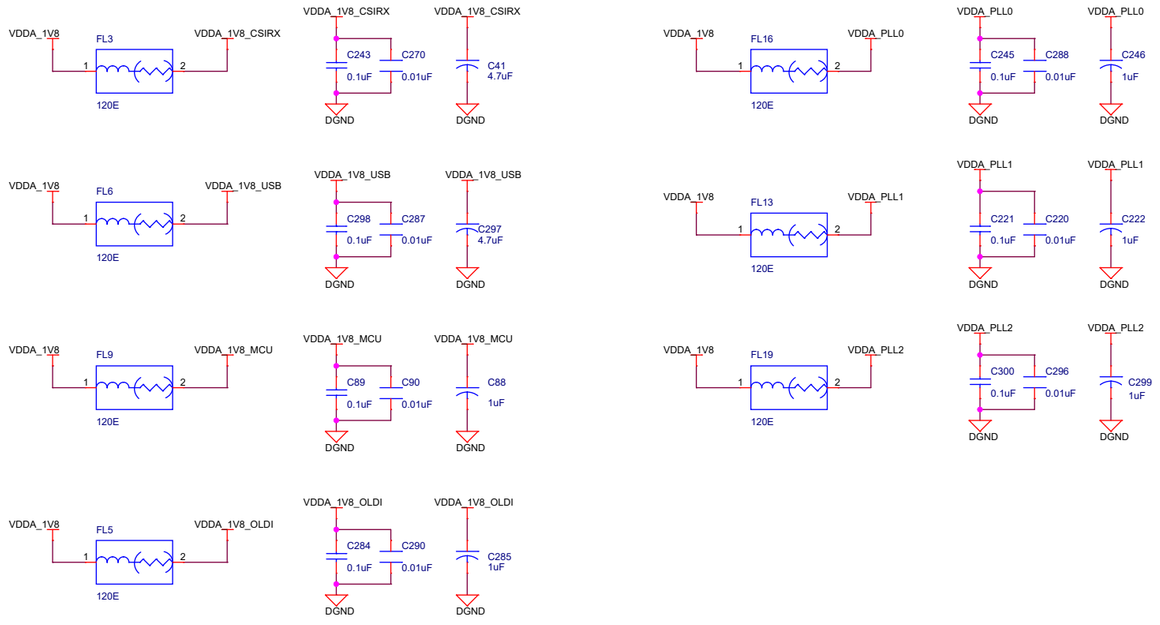
Designed for TI by Mistral Solutions Pvt Ltd

Title	CURRENT MONITORING DEVICES		
Size	PROC114E2		Rev
C			E2
Date:	Tuesday, February 22, 2022	Sheet 13 of 43	

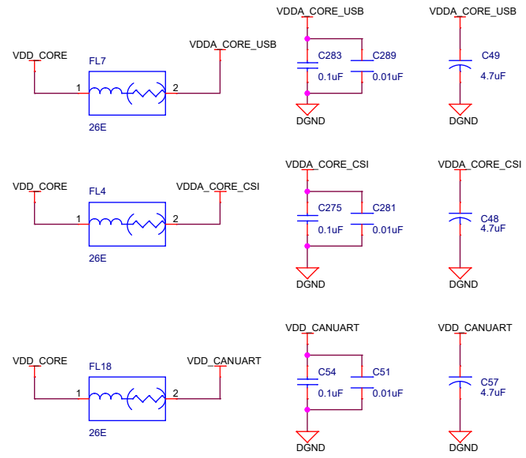
SOC POWER



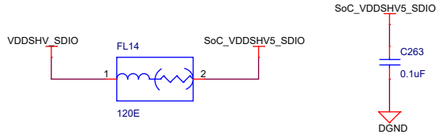
1.8V Analog SUPPLY



CORE SUPPLY



3.3V/1.8V MMC1 SUPPLY



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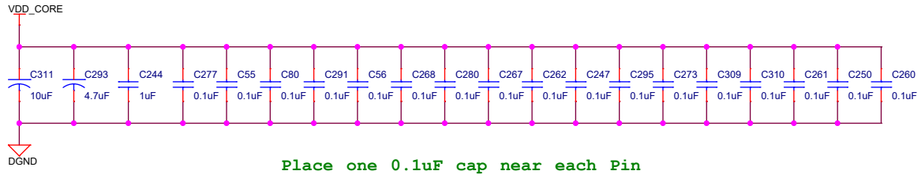
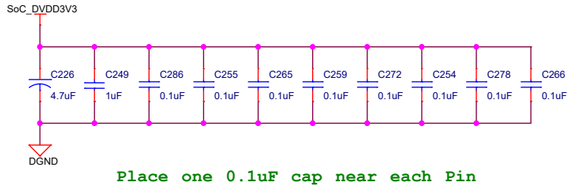
Title	SOC POWER	
Size: C	Variant Name = PROC114E2	Rev: E2
Date: Tuesday, February 22, 2022	Sheet 14 of 43	

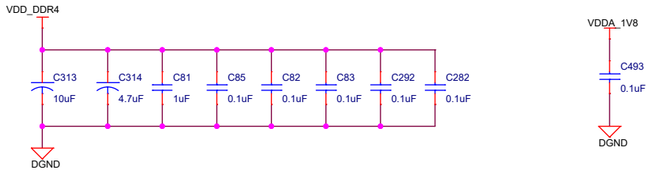
SOC POWER DECAPS



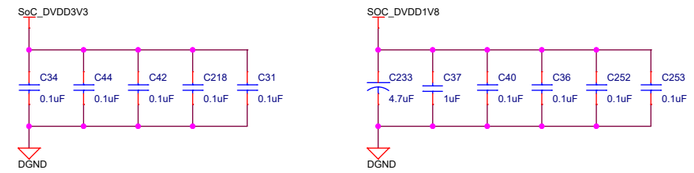
Place one 0.1uF cap near each Pin



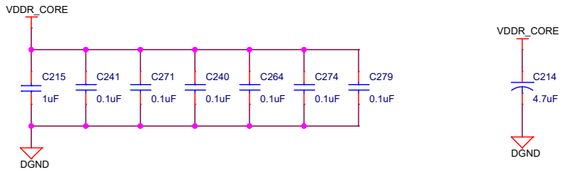
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin

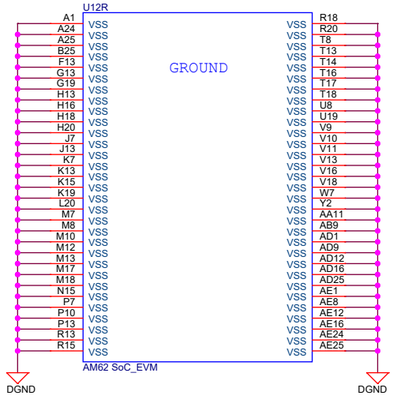


Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin

SOC VSS



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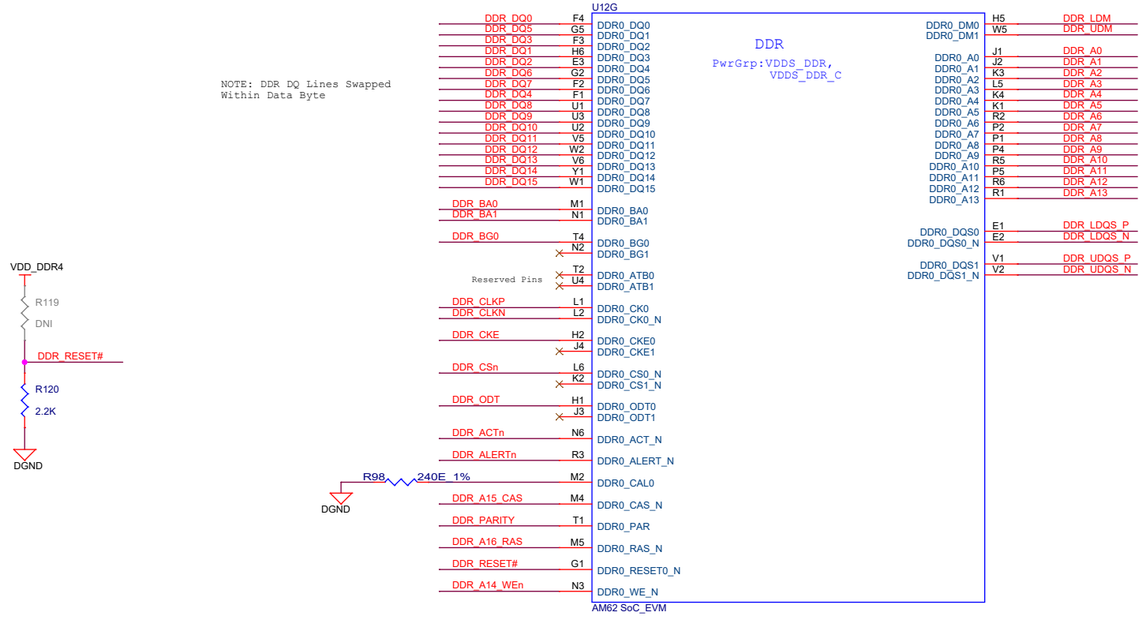
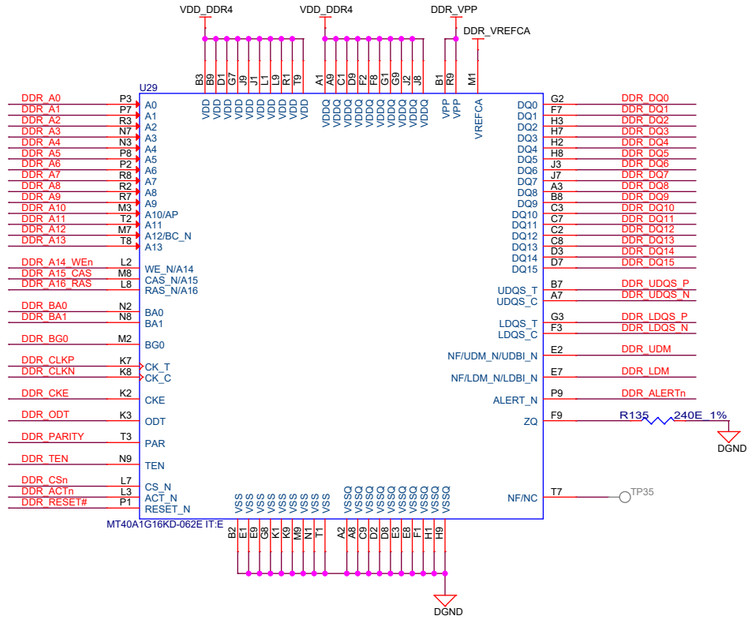
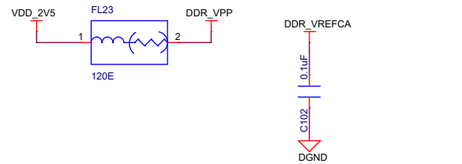
Title	SOC POWER CAPS & SOC VSS	
Size C	Variant Name = PROC114E2	Rev
Date: Tuesday, February 22, 2022	Sheet 15 of 43	

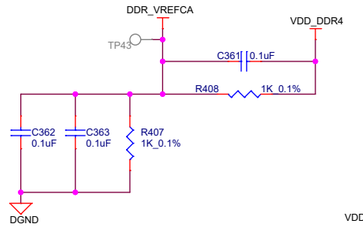
SOC DDR INTERFACE

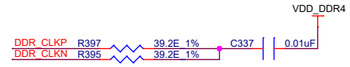


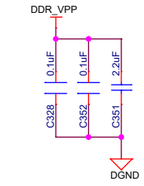
DDR4 DEVICE

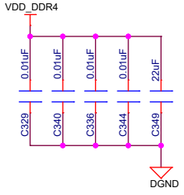


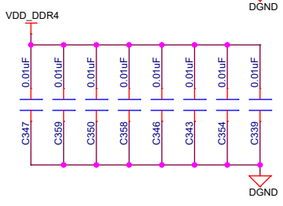


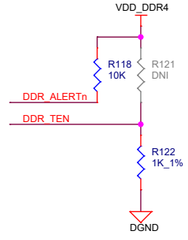


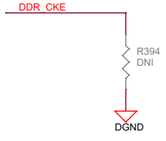












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Title	DDR4 Interface	
Size C	Variant Name = PROC114E2	Rev E2
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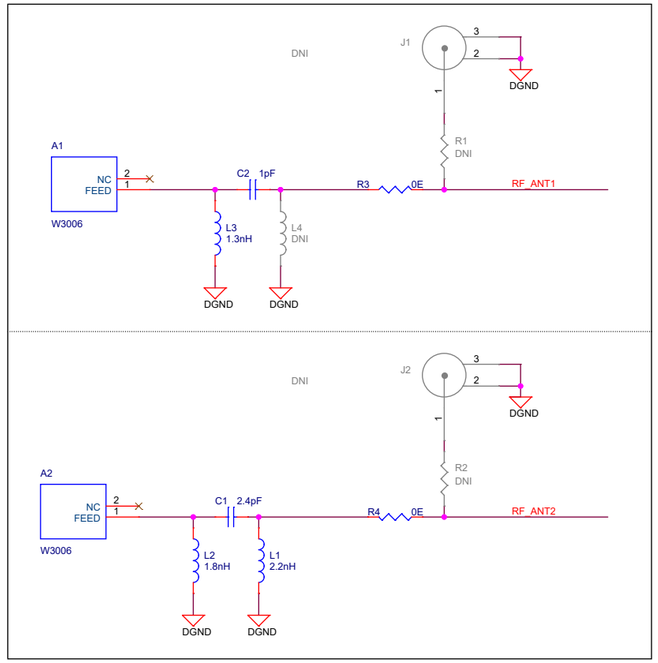
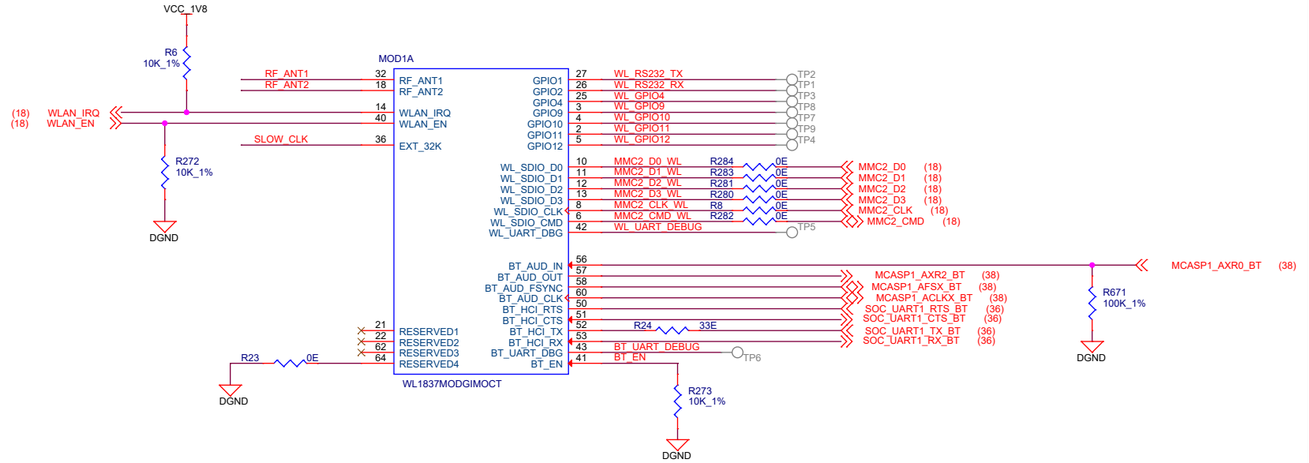
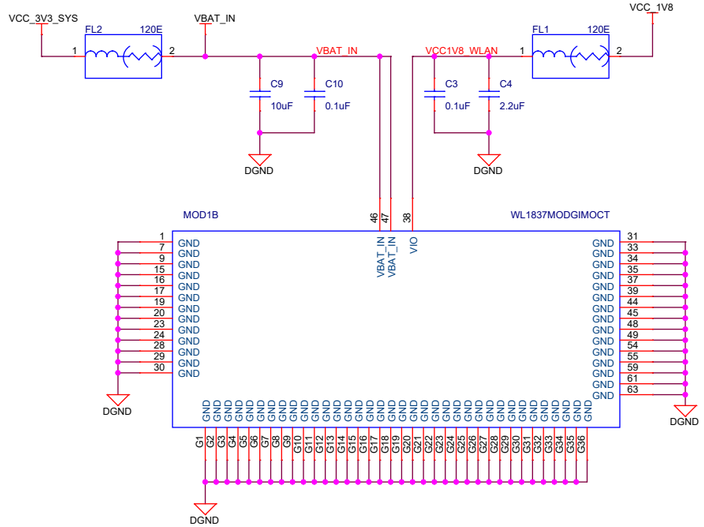
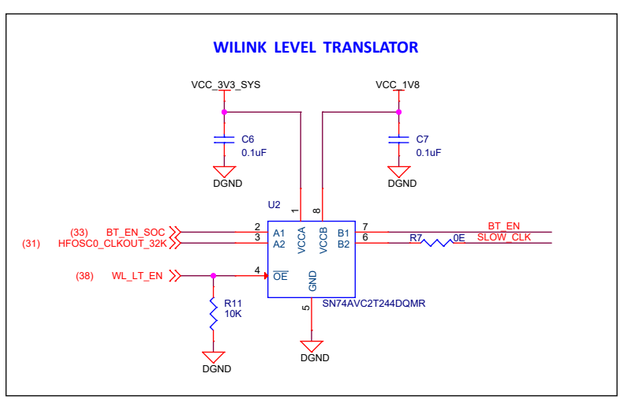
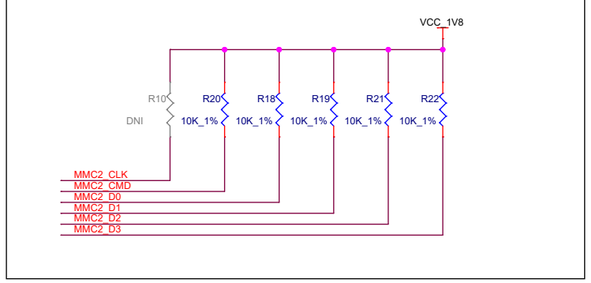
WL1837 MODULE











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Title	WL1837 MODULE		
Size	PROC114E2		Rev
C			E2
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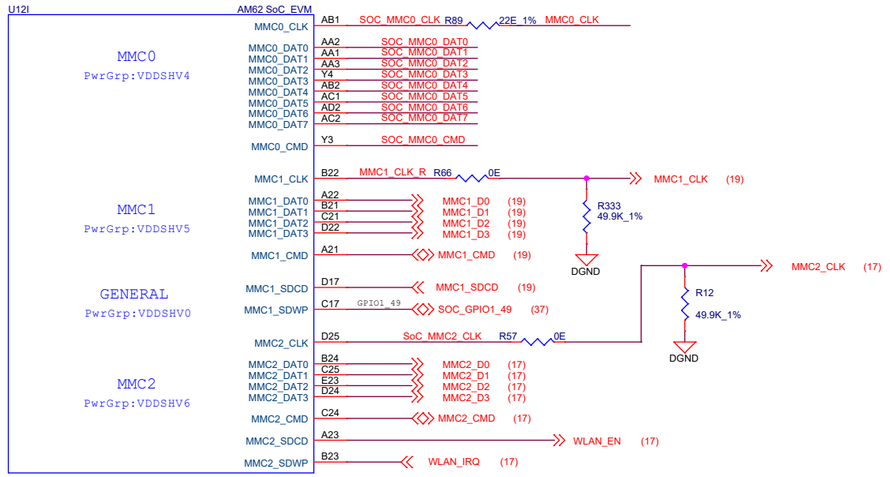
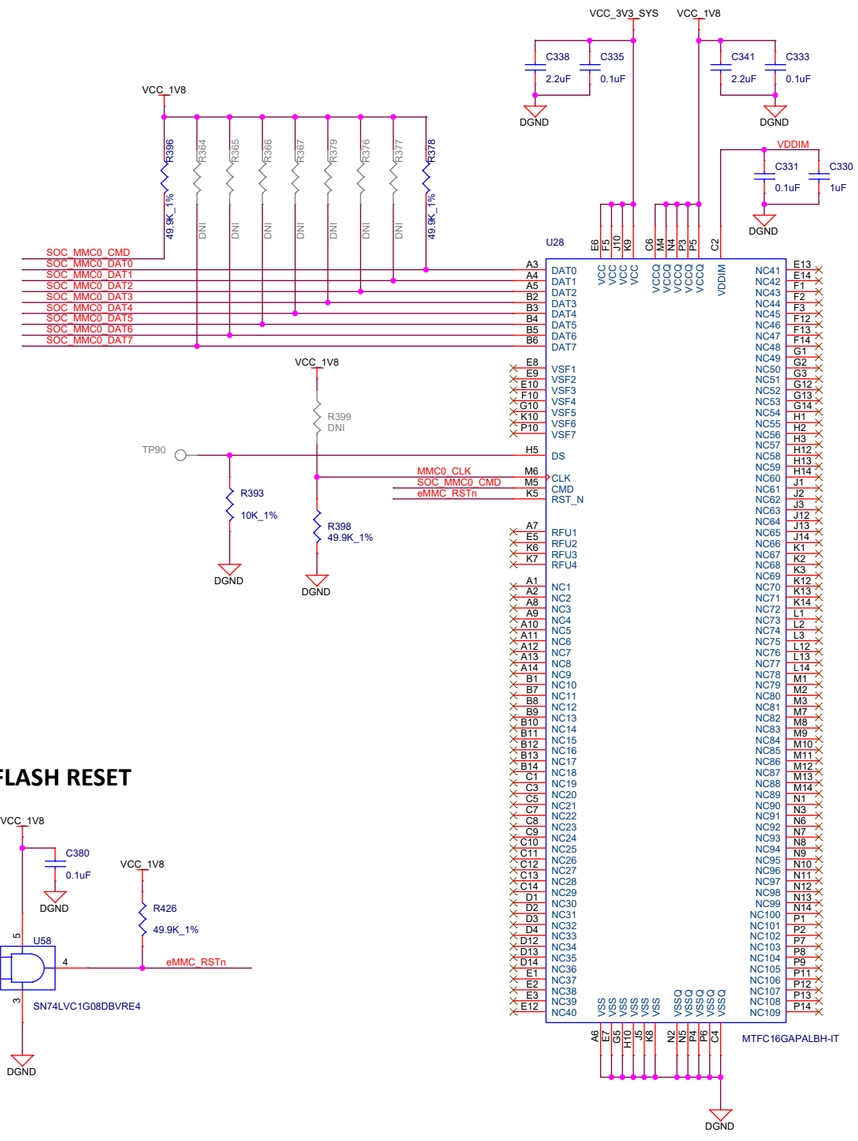
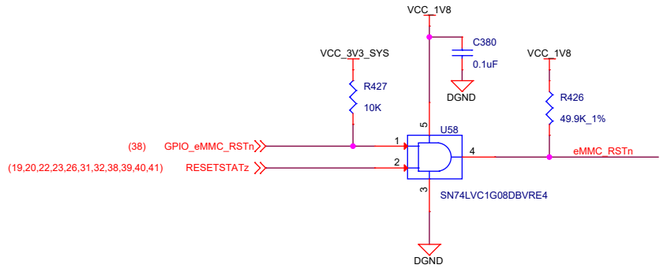
SOC - MMC Interface



eMMC FLASH



eMMC FLASH RESET



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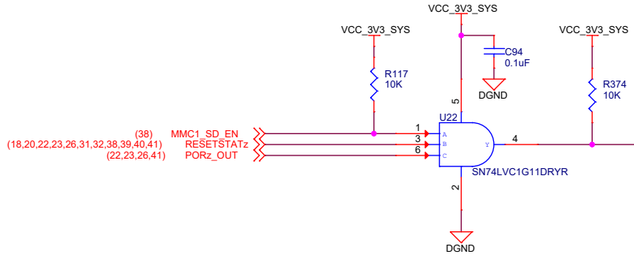
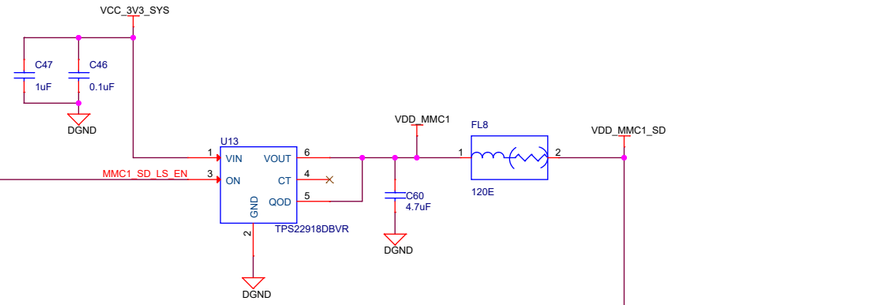
Title	eMMC FLASH INTERFACE	
Size: C	PROC114E2	Rev: E2
Date: Tuesday, February 22, 2022	Sheet 18 of 43	

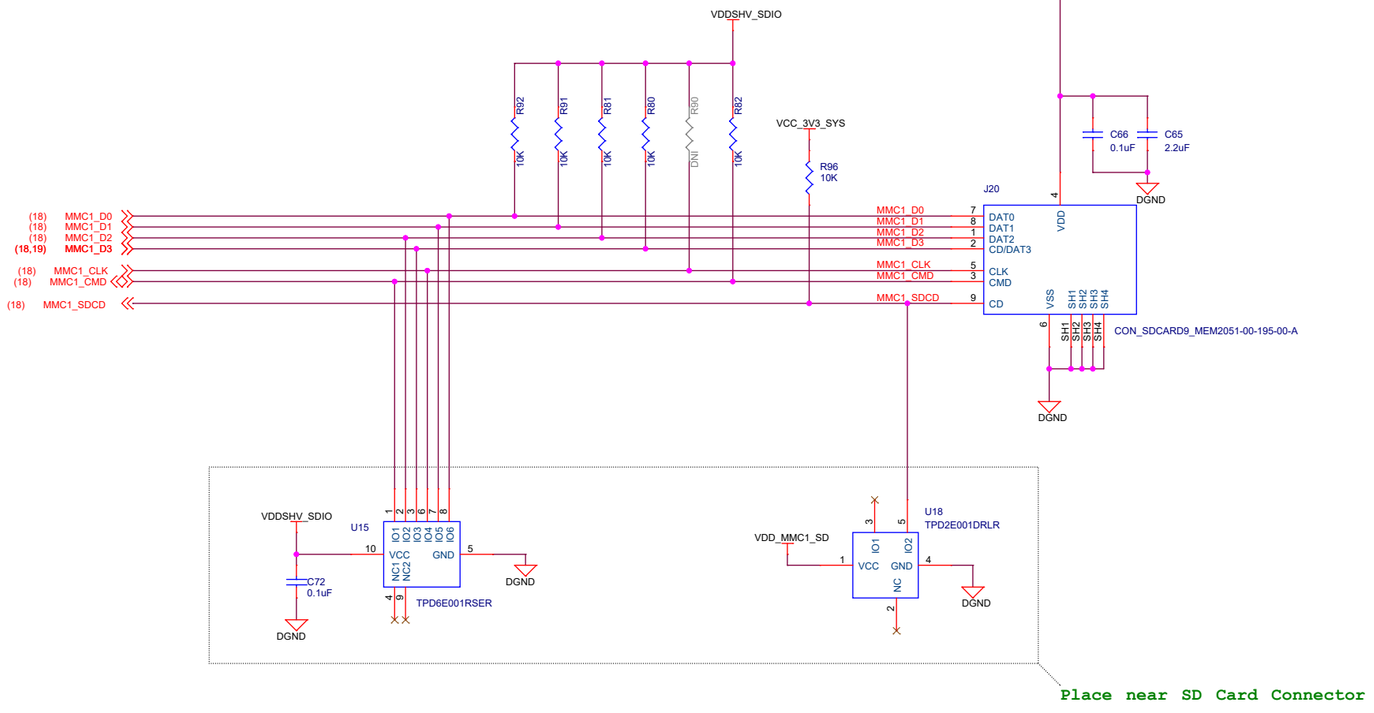
SD CARD INTERFACE

SD CARD RESET



LOAD SWITCH





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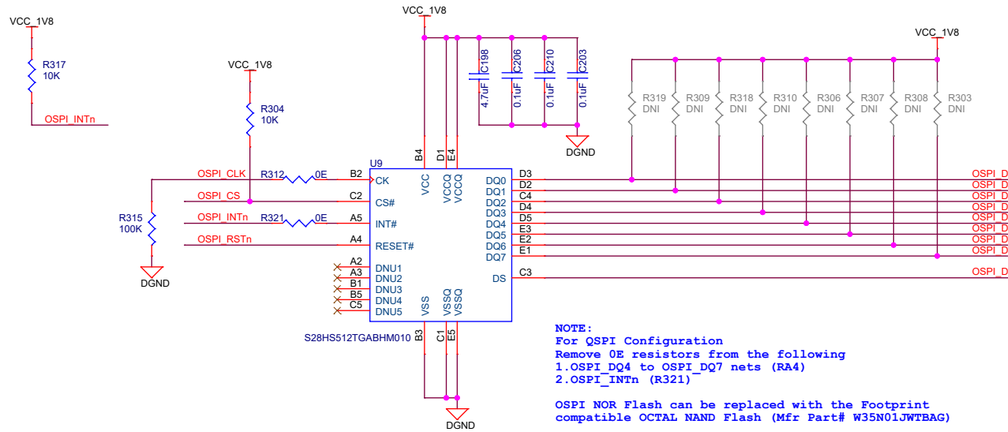
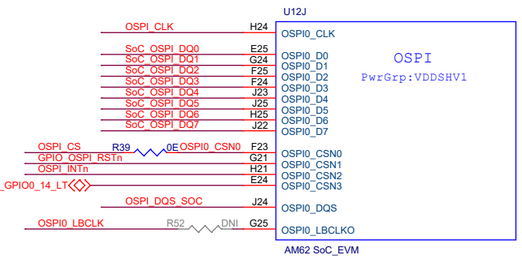
Title	SD CARD INTERFACE		
Size	PROC114E2		Rev
C			E2
Date:	Tuesday, February 22, 2022	Sheet 19 of 43	

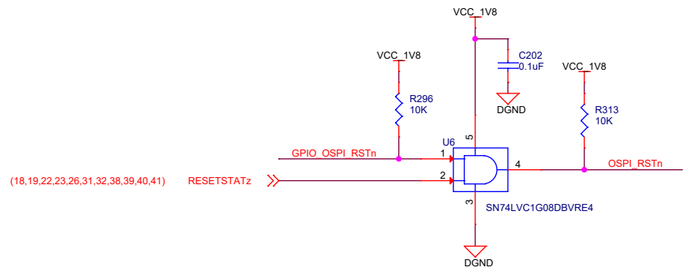
OSPI FLASH



SOC OSPI INTERFACE



OSPI FLASH RESET



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Title	OSPI INTERFACE	
Size: C	PROC114E2	Rev: E2
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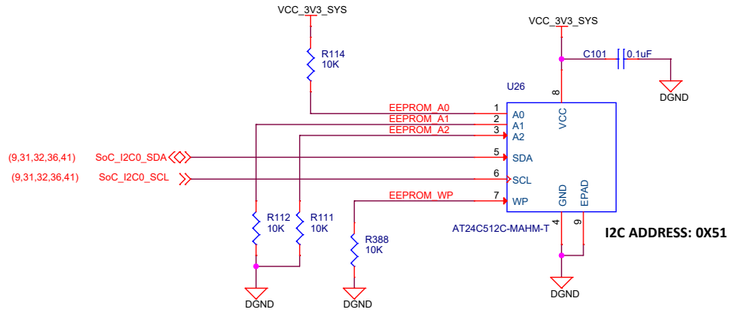
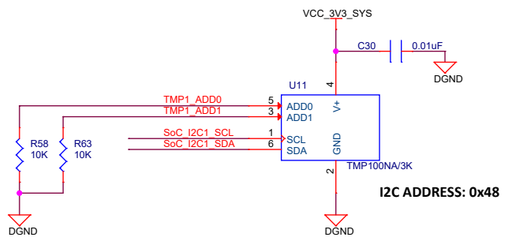
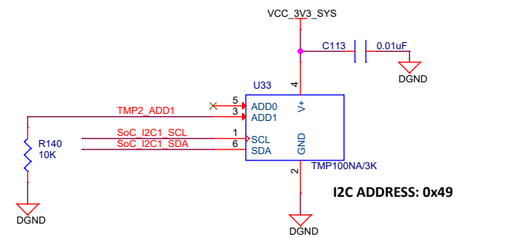
BOARD ID EEPROM



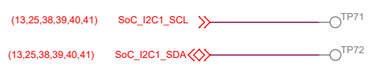
TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR U11 CLOSE TO SoC



CAD NOTE: PLACE TEMP SENSOR U33 CLOSE TO DDR4



Silk: SOC_I2C1

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOARD ID EEPROM & TEMPERATURE SENSORS	
Size: C	PROC114E2	Rev: E2
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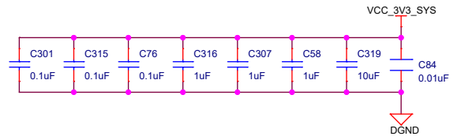
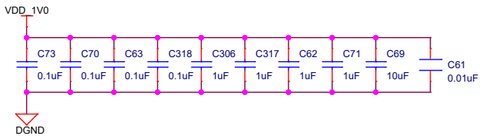
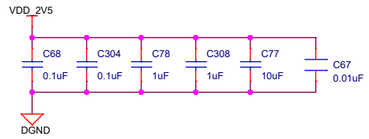
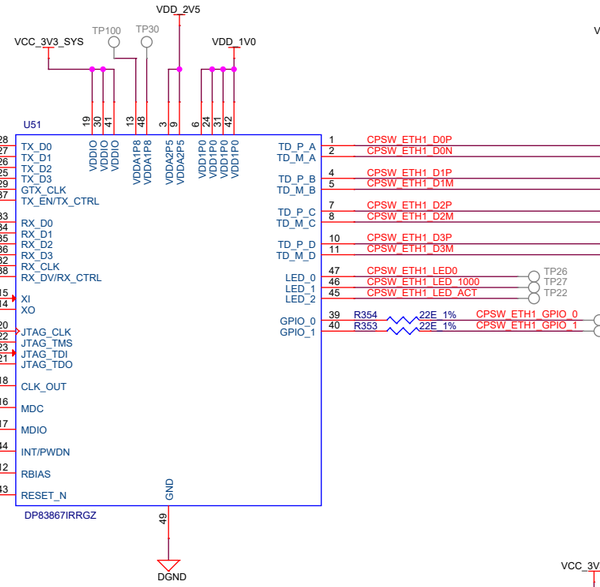
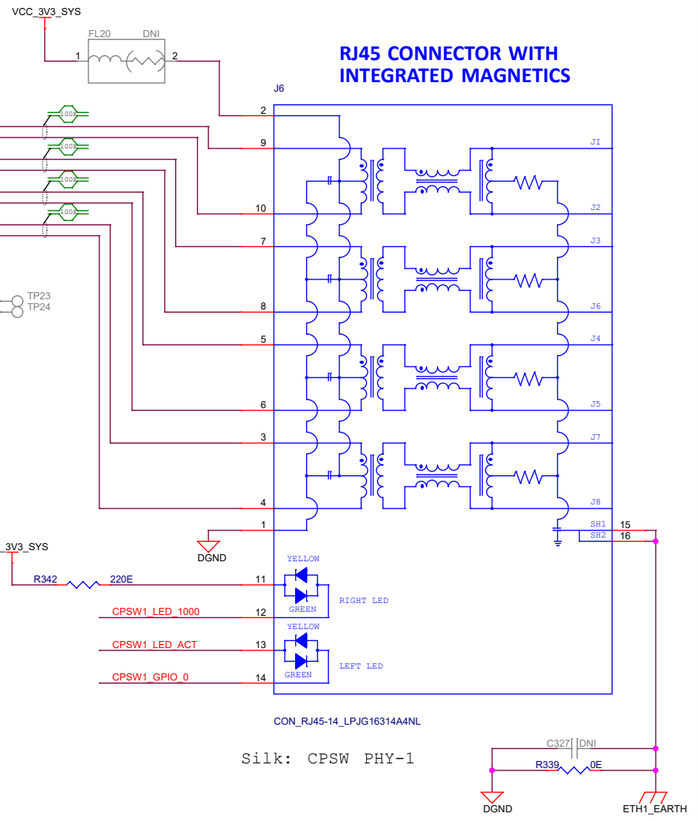
CPSW RGMII 1 - PHY

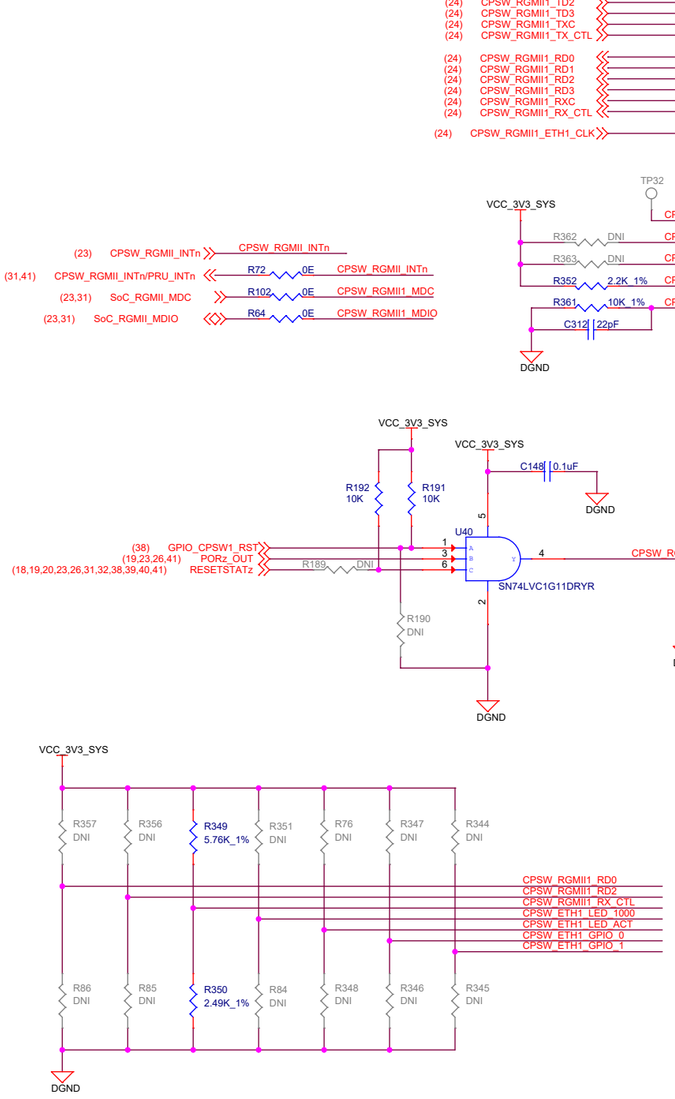


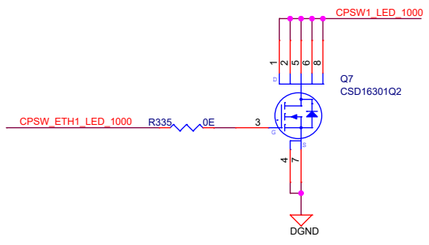


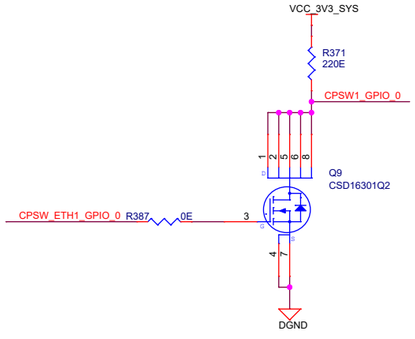


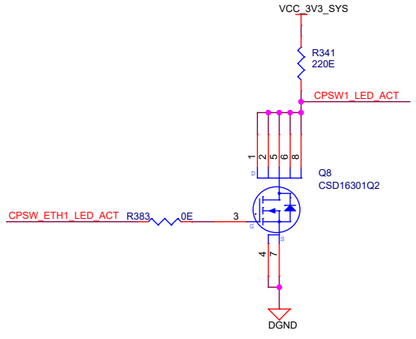













```
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 2ns
Rx Clock Skew = 2ns
```

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_1 ETHERNET PHY	
Size C	PROC114E2	Rev E2
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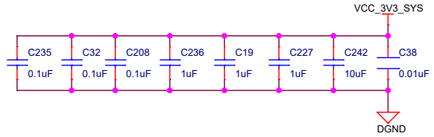
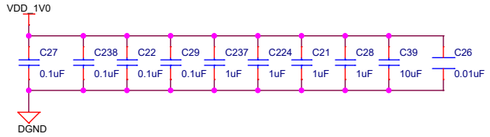
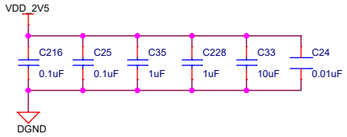
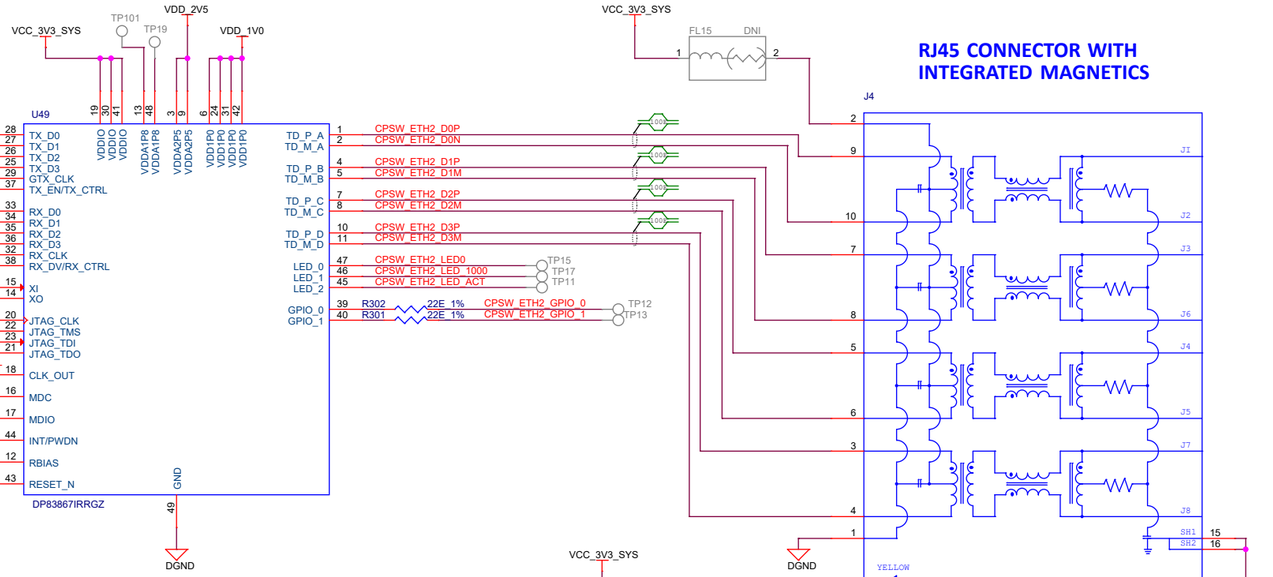
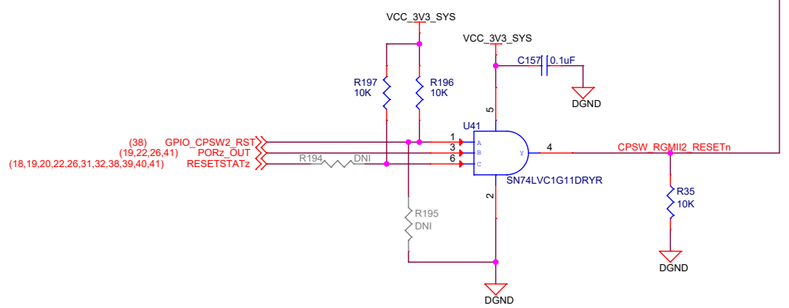
CPSW RGMII 2 - PHY



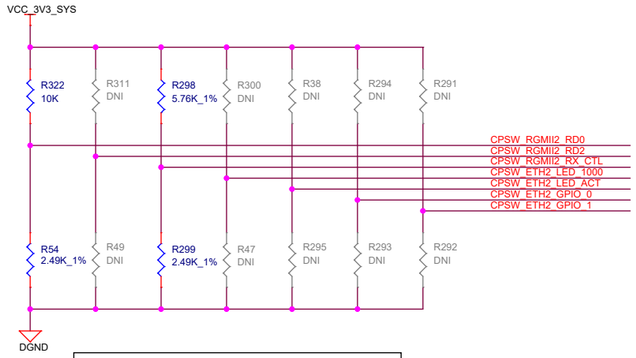


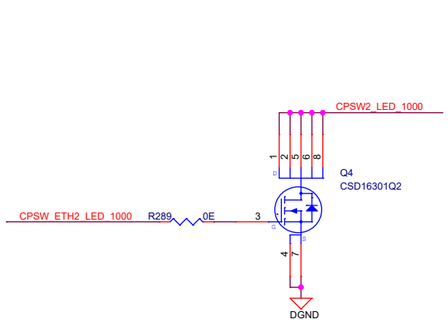


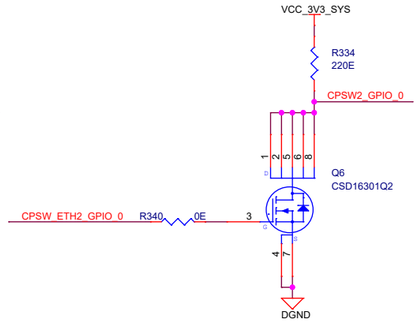


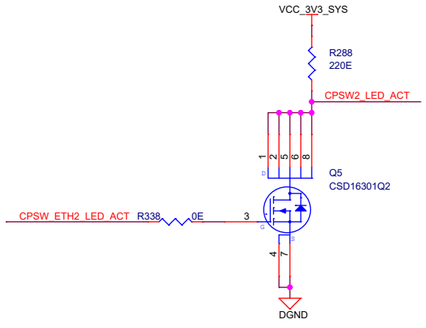


Silk: CPSW PHY-2







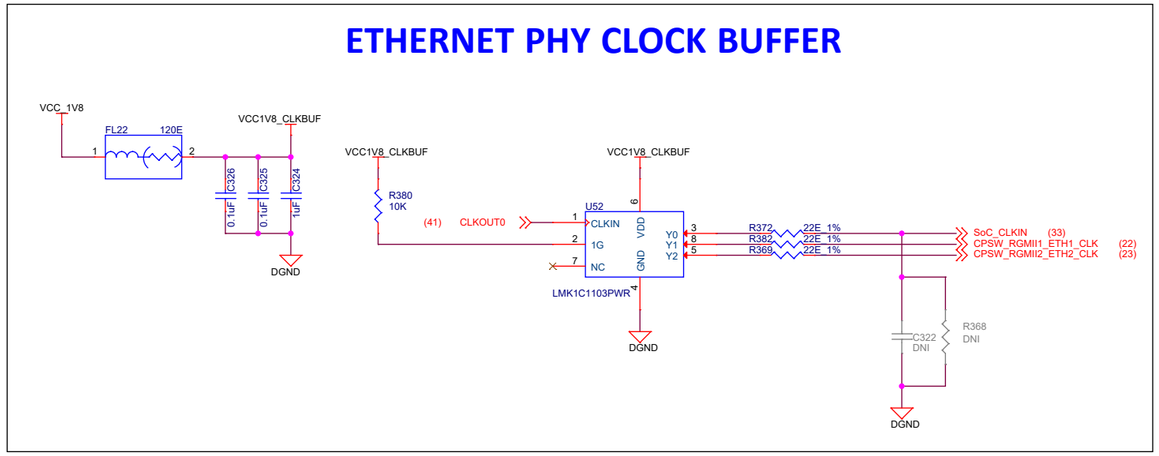



```
PHY ADDRESS = 00001
Auto-negotiation  Enabled
10/100/1000 advertised,  Auto-MDI-X
Tx Clock Skew = 2ns
Rx Clock Skew = 2ns
```

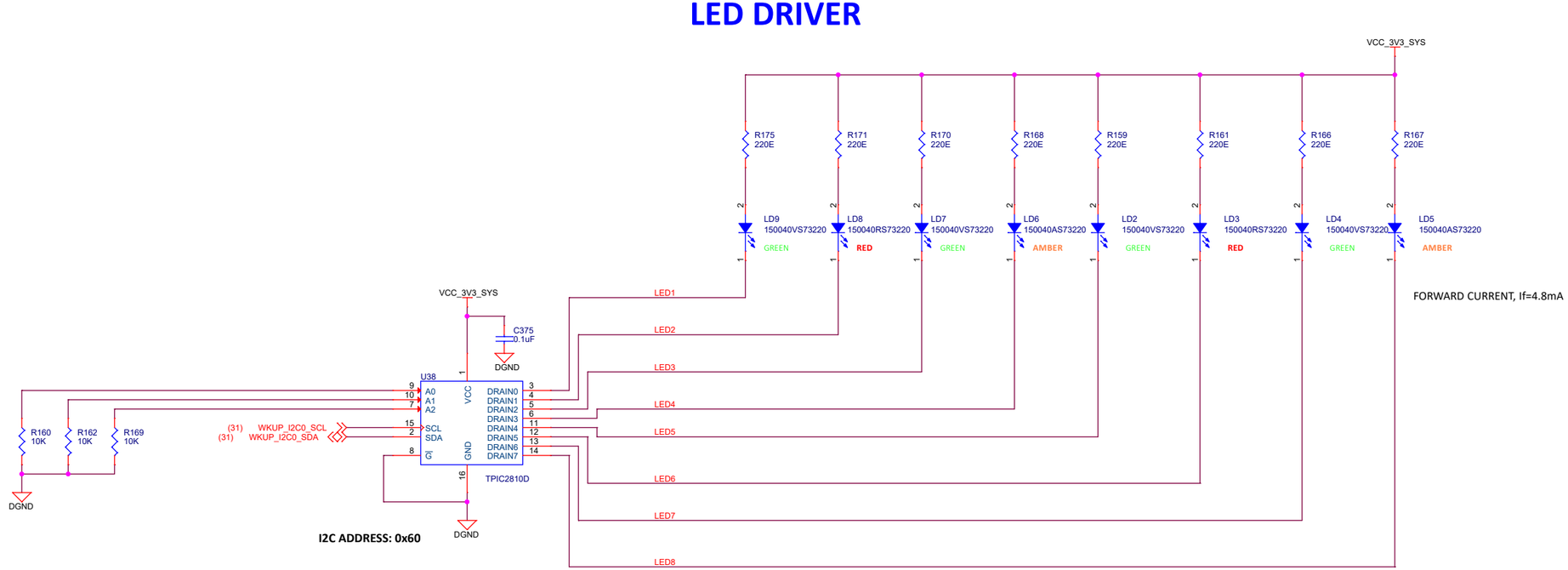
Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_2 ETHERNET PHY	
Size C	PROC114E2	Rev E2
Date: Tuesday, February 22, 2022	Sheet 23 of 43	

ETHERNET PHY CLOCK BUFFER



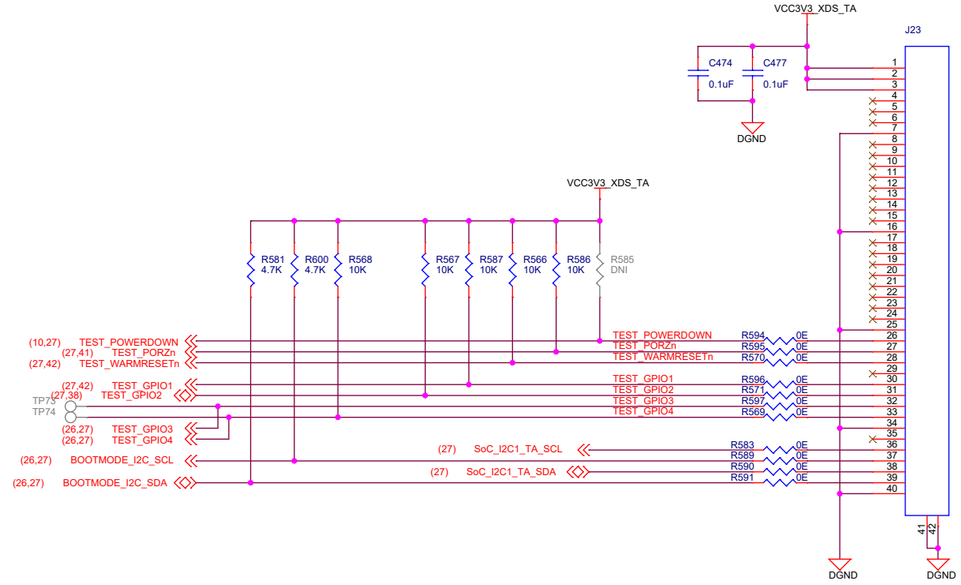
LED DRIVER



Designed for TI by Mistral Solutions Pvt Ltd

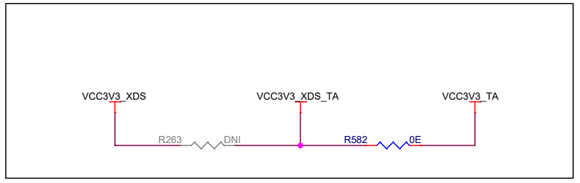
Title	ETHERNET PHY CLOCK BUFFER & LED DRIVER	
Size C	PROC114E2	Rev E2
Date: Tuesday, February 22, 2022	Sheet 24 of 43	

40-PIN TEST AUTOMATION HEADER

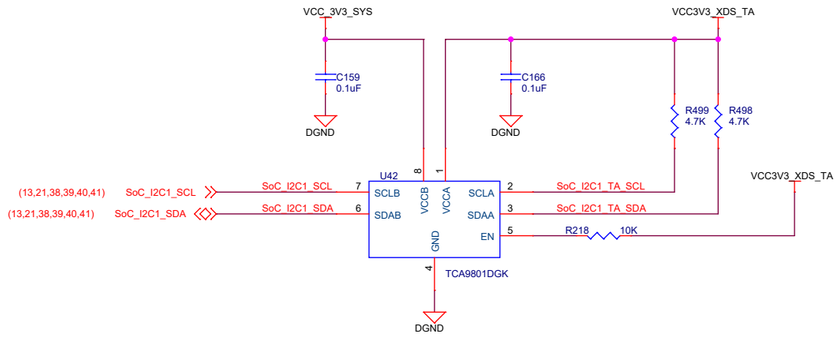


CON_FLEX_40X1_FH12A-40S-0.5SH

Silk: AUTOMATION HDR

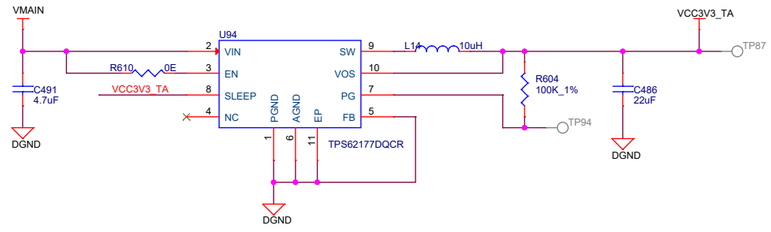


I2C BUS BUFFER



TEST AUTOMATION BOARD POWER

VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A



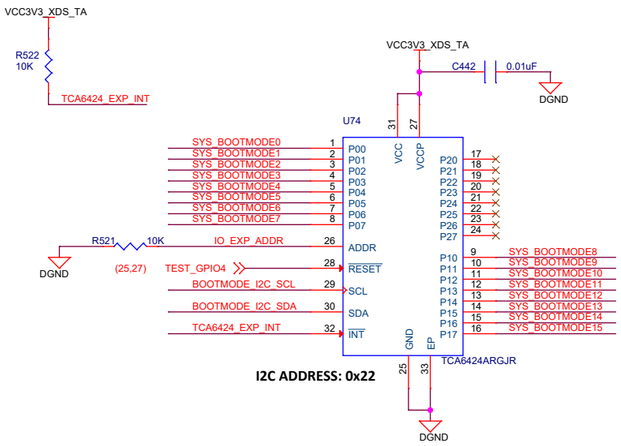
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SoC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

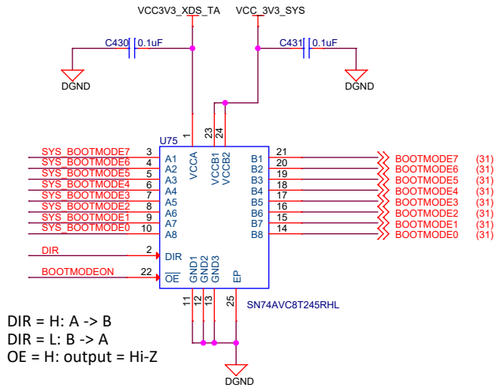
Designed for TI by Mistral Solutions Pvt Ltd

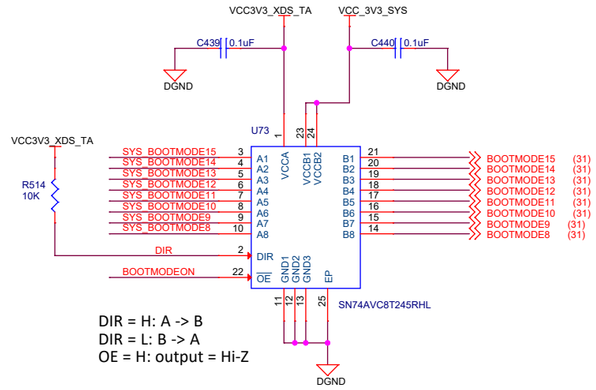
Title	TEST AUTOMATION	
Size C	PROC114E2	Rev E2
Date: Tuesday, February 22, 2022	Sheet 25 of 43	

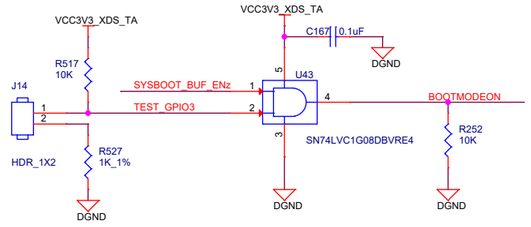
BOOTMODE IO EXPANDER



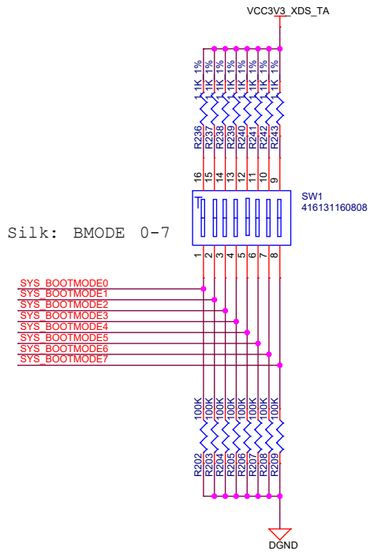
BOOT MODE BUFFERS



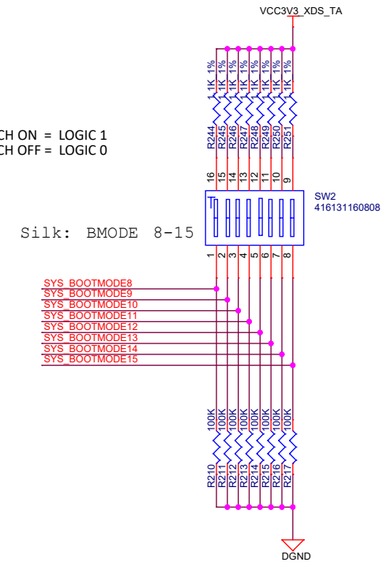




BOOT MODE SWITCHES



SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. BACKUP BOOT OPTION

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOOT MODE BUFFER & SWITCHES	
Size C	PROC114E2	Rev E2
Date: Tuesday, February 22, 2022	Sheet 26 of 43	

XDS110 DEBUGGER

TP86
XDS_USB_VBUS
C180 4.7uF
D8 TPD1E10B06DPYR
DGND
C455 2.2uF
R540 0E
U79
IN1 IN2 EN GND PAD OUT1 OUT2 NR/FB NC
TPS79601DRBR
R520 51K
C441 15pF
R519 30K
C443 1uF
VCC3V3_XDS
TP77
C454 1uF
C468 0.1uF
C173 0.1uF
C181 0.01uF
C176 0.01uF
C191 0.01uF
U45B
VDD GNDA GND VDDA VDDC VBAT
TM4C1294NCPDTT3R
C192 1uF
C189 0.01uF
VDDC_1V2
C179 2.2uF
C178 1uF
C449 0.1uF
R228 49.9E_1%
C169 0.1uF

Silk: JTAG

J16
VBUS D- D+ ID GND SH1 SH2 SH3 SH4
CON_MUSB-B_5_F
XDS_USB_DM
XDS_USB_DP
XDS_USB_ID
R256 0E
C185 DNI
XDS_SHIELD
U89
IO1 IO2 IO3 IO4 VCC GND
TPD4E004DRYR

U45A
PA0/U0RX PA1/U0TX PA2/SSI0CLK PA3/SSI0FSS PA4/SSI0XDAT0 PA5/SSI0XDAT1 PA6 PA7
PC0/TCK/SWCLK PC1/TMS/SWDIO PC2/TDI PC3/TDO/SWO PC4/C1- PC5/C1+ PC6/C0+ PC7/C0-
PE0/AIN3 PE1/AIN2 PE2/AIN1 PE3/AIN0 PE4/AIN9 PE5/AIN8
PG0 PG1
PJ0 PJ1
PL0 PL1 PL2 PL3 PL4 PL5 PL6/USB0DP PL7/USB0DM
PN0 PN1 PN2 PN3 PN4 PN5
PQ0 PQ1 PQ2 PQ3 PQ4
TM4C1294NCPDTT3R
XDS110_TCK XDS110_TMS XDS110_TDO XDS110_TDI XDS110_TRST#
TM4C129_TCK TM4C129_TMS TM4C129_TDI TM4C129_TDO
BOOTMODE_I2C_SCL BOOTMODE_I2C_SDA
SoC_I2C1_TA_SDA SoC_I2C1_TA_SCL
PB0/USB0ID PB1/USB0VBUS PB2/I2C0SCL PB3/I2C0SDA PB4/AIN10 PB5/AIN11
PD0/AIN15 PD1/AIN14 PD2/AIN13 PD3/AIN12 PD4/AIN7 PD5/AIN6 PD6/AIN5 PD7/AIN4
PF0 PF1 PF2 PF3 PF4
PH0 PH1 PH2 PH3
PK0/AIN16 PK1/AIN17 PK2/AIN18 PK3/AIN19 PK4 PK5 PK6 PK7
PM0 PM1 PM2 PM3 PM4 PM5 PM6 PM7
PP0/C2+ PP1/C2- PP2 PP3 PP4 PP5
R530 100E_1%
R235 DNI
C170 0.1uF
XDS_USB_ID
XDS_USB_VBUS
R268 30K
R269 20K_1%
R267 220E
R271 220E
LD14 150080VS75000 GREEN
LD15 150040RS73220 RED
XDS110_EMU0
XDS110_EMU1
R598 R580 DNI
R525 R544 DNI
R229 R224 R230 R225 R231 R226 R232 DNI
TEST_POWERDOWN (10,25)
TEST_PORZn (25,41)
TEST_WARMRESETn (25,42)
TEST_GPIO1 (25,42)
TEST_GPIO2 (25,38)
TEST_GPIO3 (25,26)
TEST_GPIO4 (25,26)
TP76
R563 R560 R556 R552 1K_1%
R260 R259 R258 R255 DNI

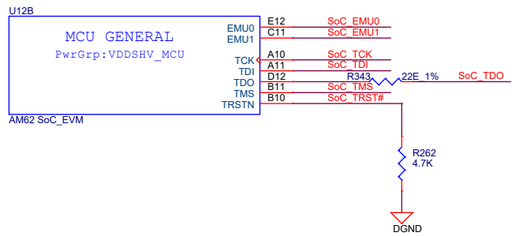
Sets the unique ID of the Debugger

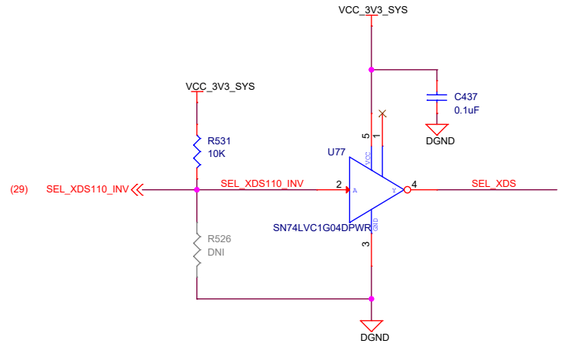
VCC3V3_XDS
R539 10K
TP75
R546 DNI
U45C
RST WAKE OSC0 OSC1 XOSC0 XOSC1 RBAIS VREFA+ HIB EN0RXIP EN0RXIN EN0RX0P EN0RX0N
TM4C1294NCPDTT3R
XDS_RSTn
R270 4.7K
XDS_VREF
C172 12pF
C171 12pF
Y2 16.000MHz
R261 4.87K_1%
C186 0.01uF
C190 0.1uF
U47
LM4040B25IDCKR
R264 4.7K
R265 4.7K

Designed for TI by Mistral Solutions Pvt Ltd

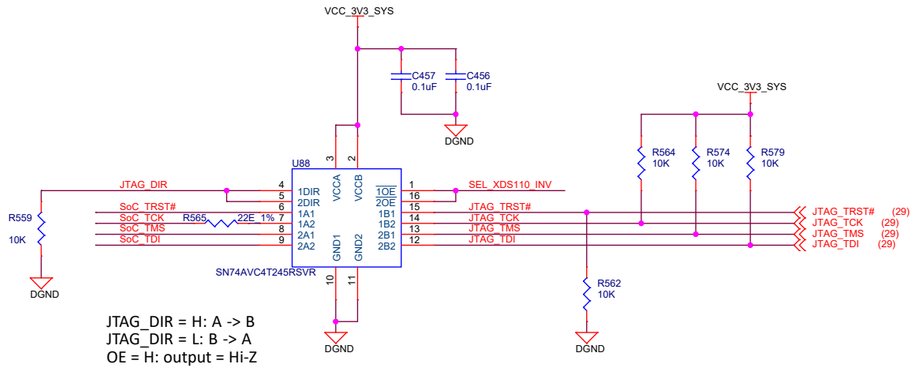
Title	XDS110 DEBUGGER	
Size	PROC114E2	Rev
C		E2
Date:	Tuesday, February 22, 2022	Sheet 27 of 43

JTAG SOC SECTION



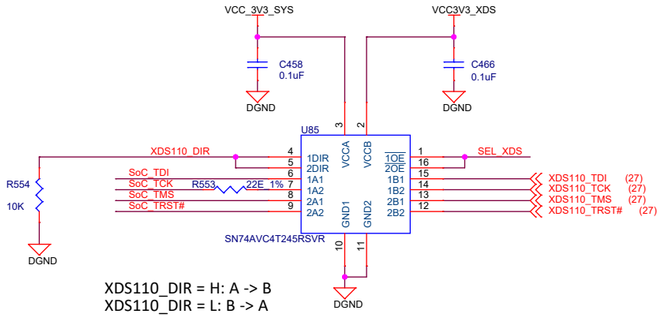


cTI20 JTAG BUFFERS



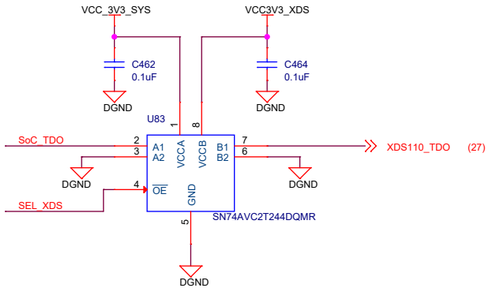
JTAG_DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z

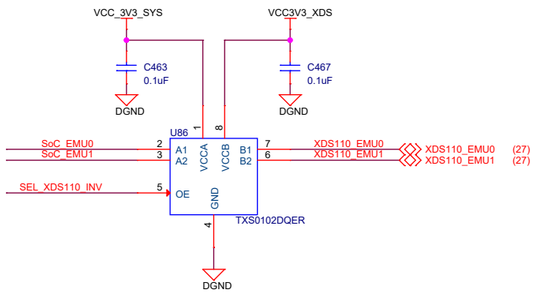
BUFFER XDS110

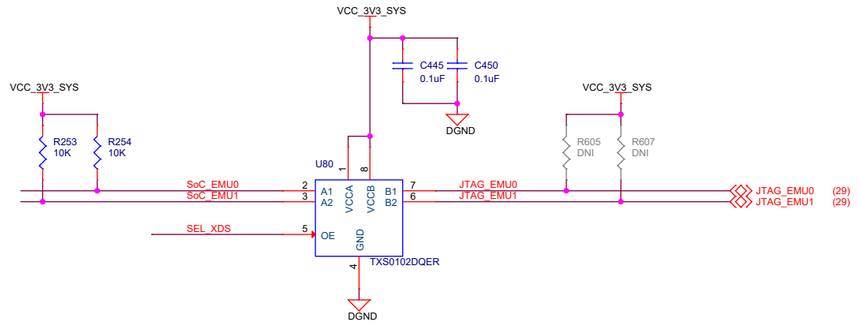


XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z

CAD NOTE: Buffers U88 and U96
need to be placed closer to the
cTI-20pin connector J17 to reduce Stub length of the JTAG signals.







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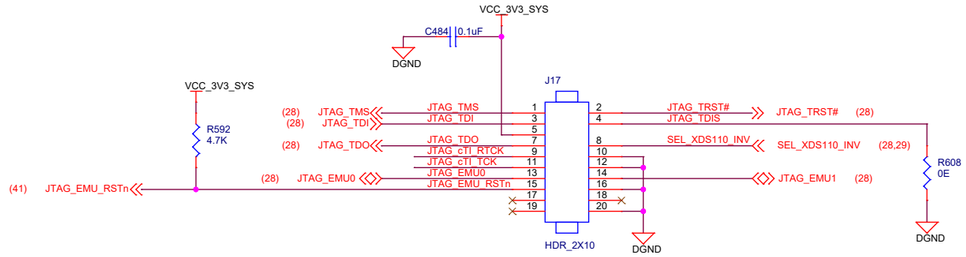
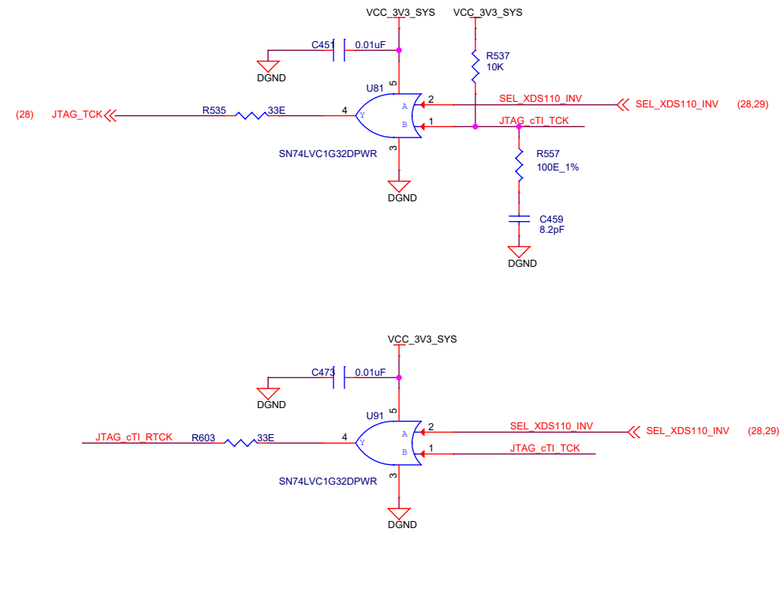
Title	JTAG BUFFER	
Size: C	PROC114E2	Rev: E2
Date: Tuesday, February 22, 2022	Sheet 28 of 43	

JTAG 20 PIN cTI CONNECTOR



Silk: cTI

JTAG CLOCK BUFFER

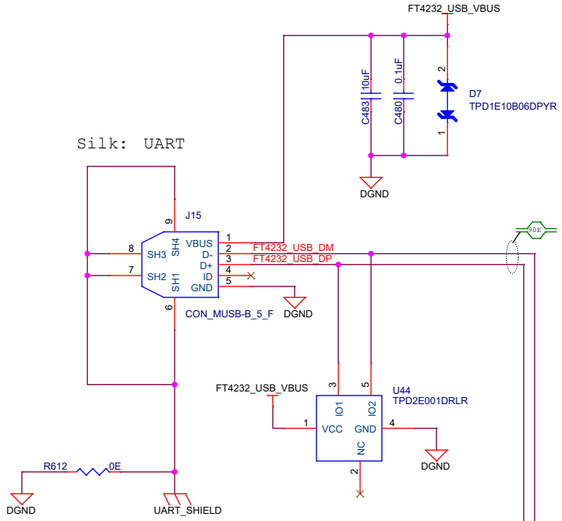


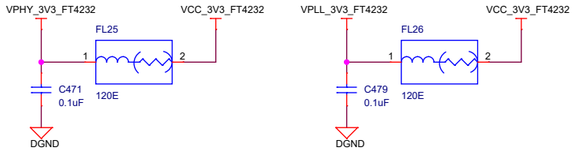
Designed for TI by Mistral Solutions Pvt Ltd

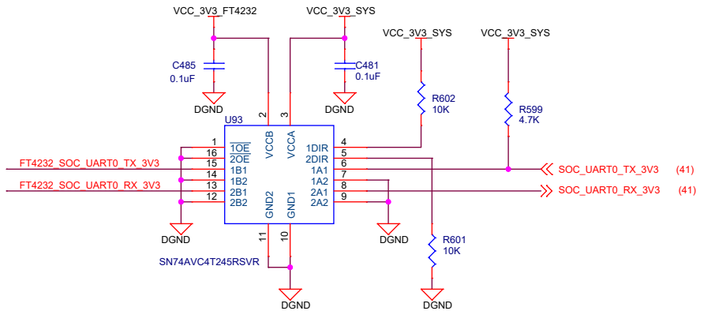
Title	JTAG 20 PIN cTI CONNECTOR	
Size C	PROC114E2	Rev E2
Date: Tuesday, February 22, 2022	Sheet 29 of 43	

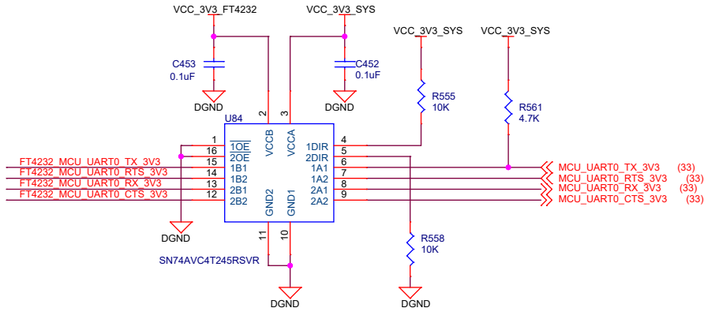
FT4232 UART

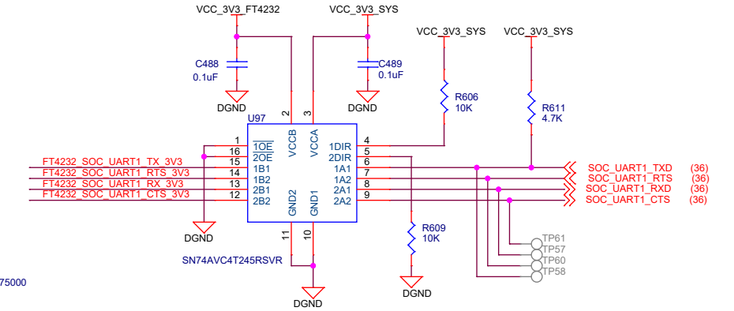
Silk: UART

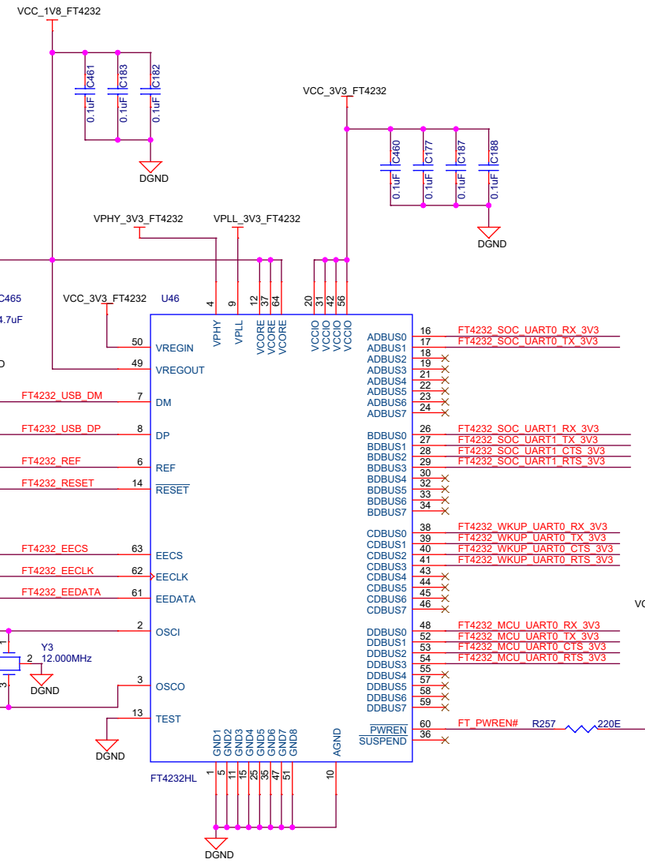


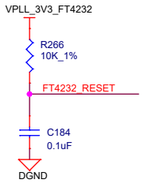


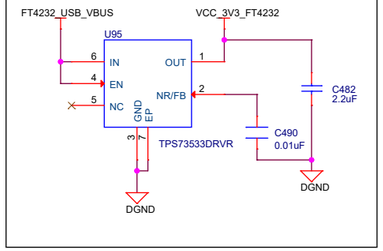


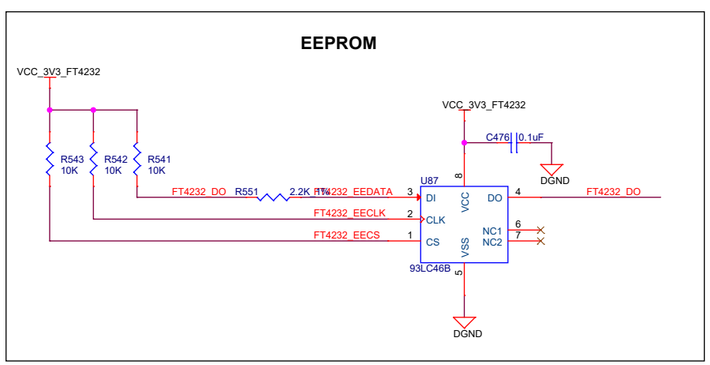


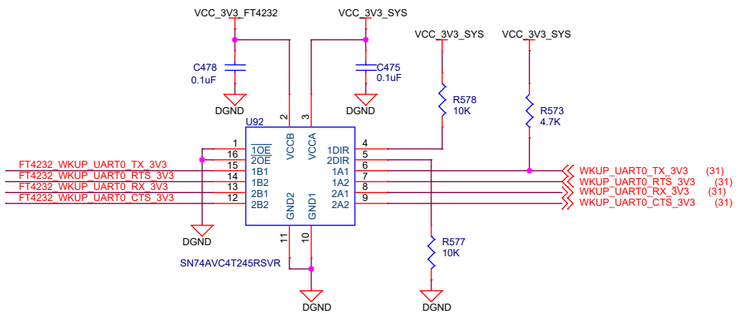












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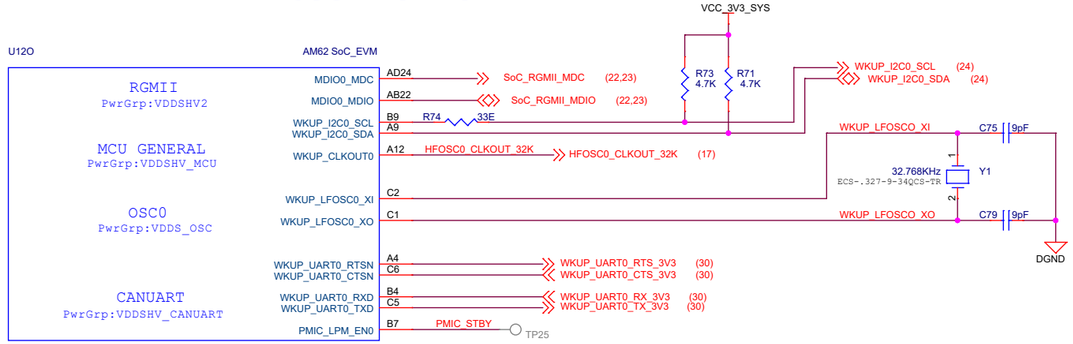
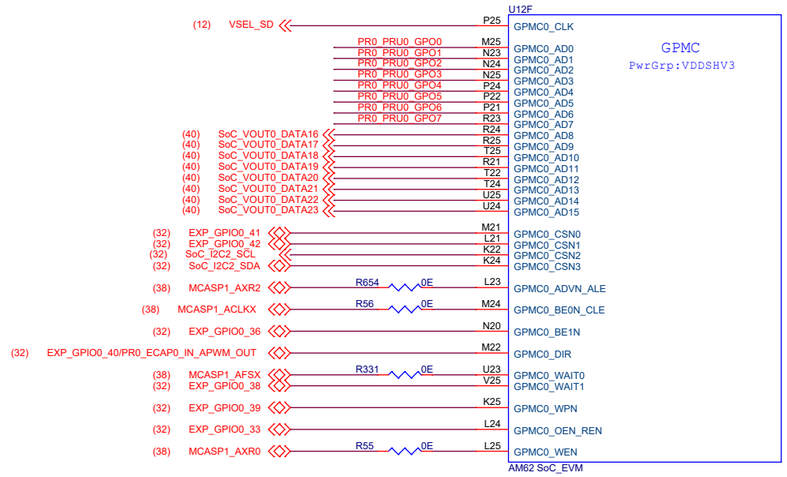
Title	FT4232 UART TO USB BRIDGE	
Size C	PROC114E2	Rev E2
Date: Tuesday, February 22, 2022	Sheet 30 of 43	

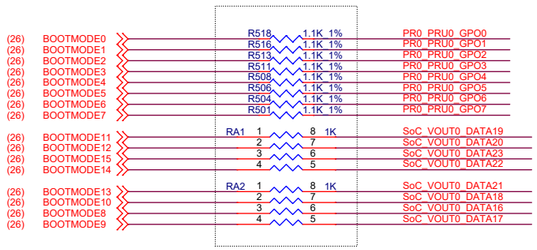
SOC WKUP DOMAIN



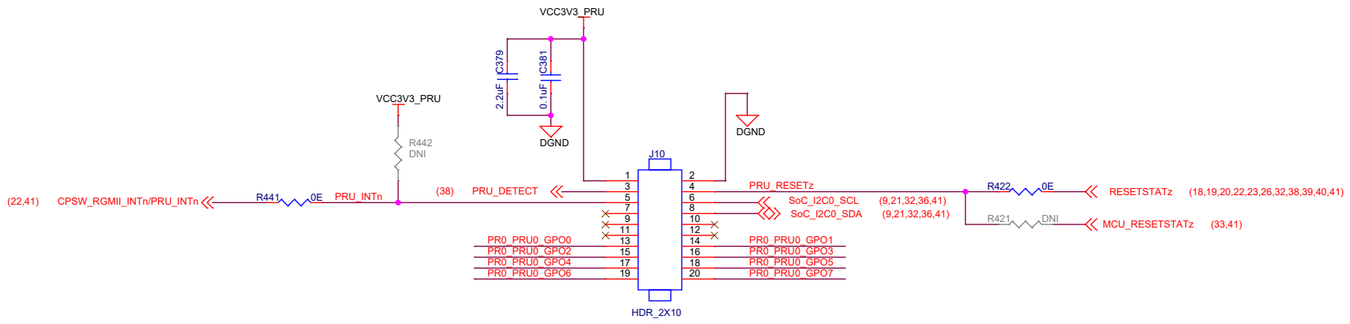
SOC GPMC



BOOTMODE PINS



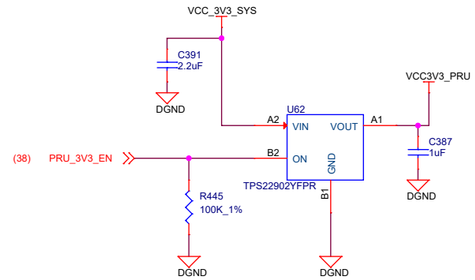
PRU HEADER



Silk: PRU HDR

NOTE: PRU Header I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

POWER SWITCH FOR PRU HEADER



3V3 supply of PRU Header is limited to sourcing 500mA max.

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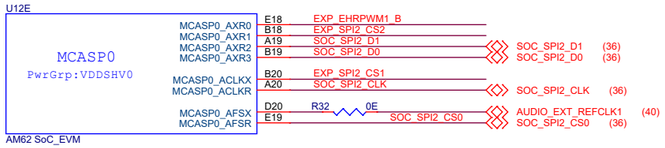
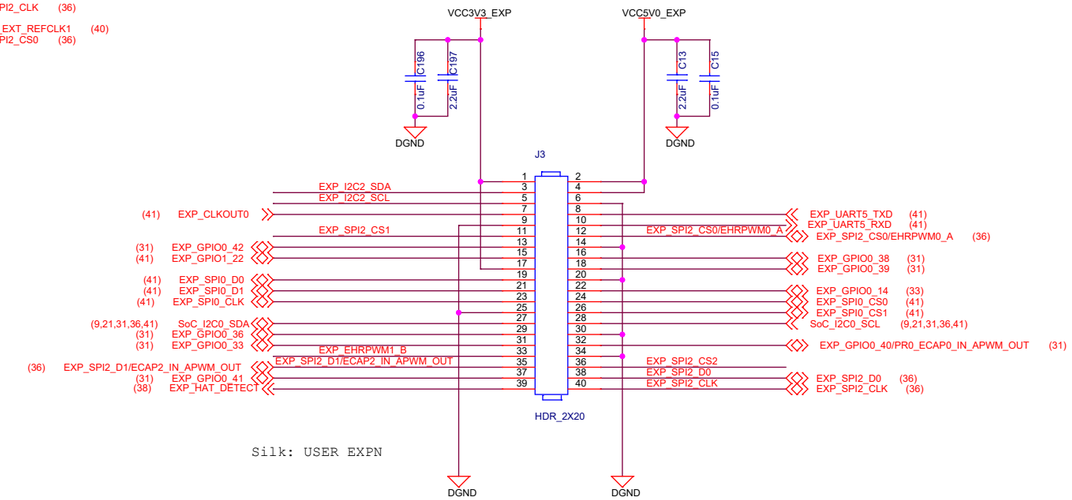
Title	PRU HEADER		
Size	PROC114E2		Rev E2
Date:	Tuesday, February 22, 2022	Sheet 31 of 43	

USER EXPANSION CONNECTOR

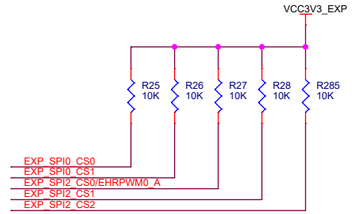


R32(Series damping resistor) should be placed close to SoC

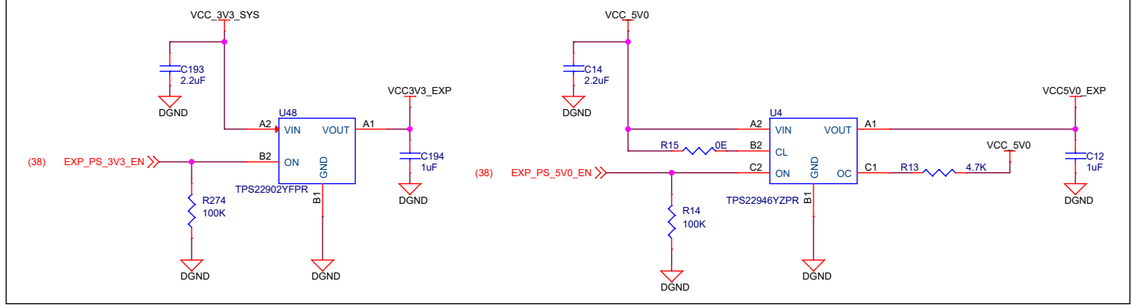


Silk: USER EXPN

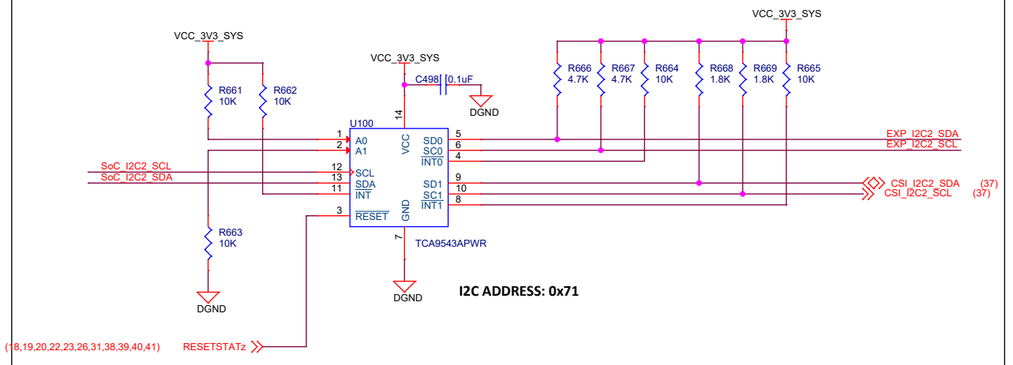
Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



POWER SWITCHES FOR USER EXPANSION CONNECTOR



I2C SWITCH FOR SoC_I2C2



NOTE:

AM62x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

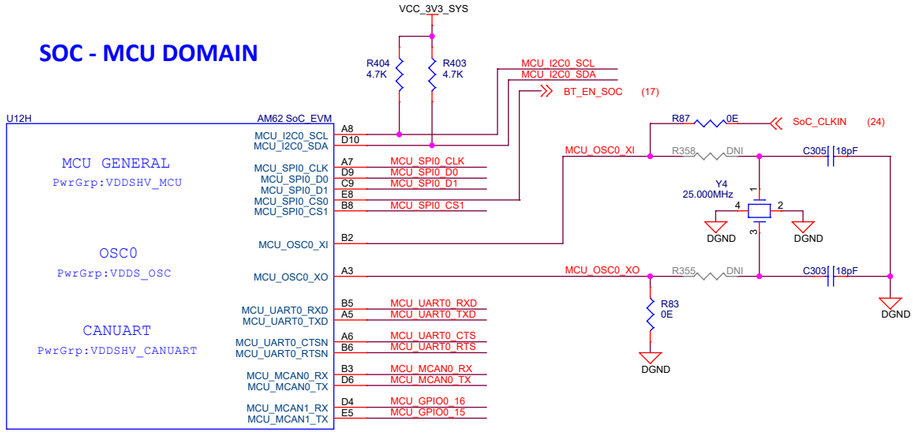
5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

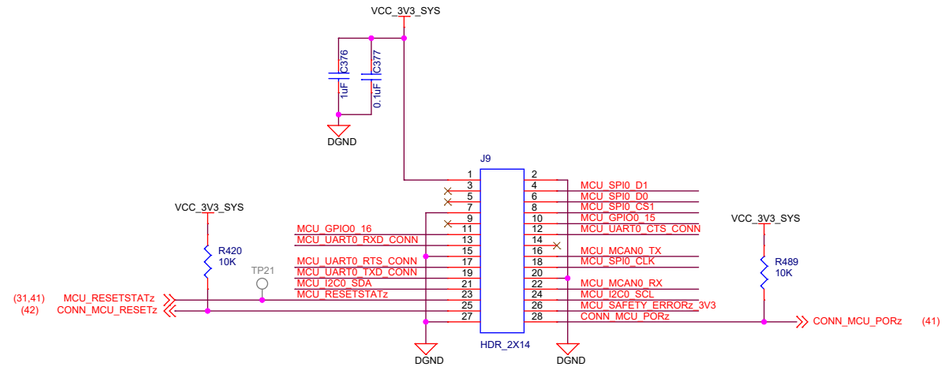
Designed for TI by Mistral Solutions Pvt Ltd

Title	USER EXPANSION CONNECTOR	
Size C	PROC114E2	Rev E2
Date: Tuesday, February 22, 2022	Sheet 32 of 43	

SOC - MCU DOMAIN

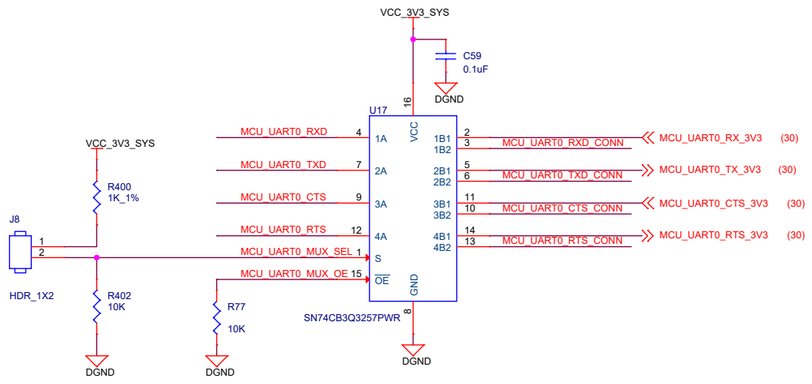


MCU HEADER

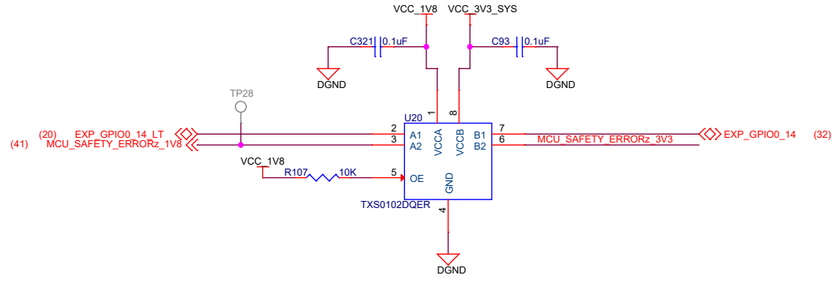


Silk: MCU HDR

MCU_UART0 MUX



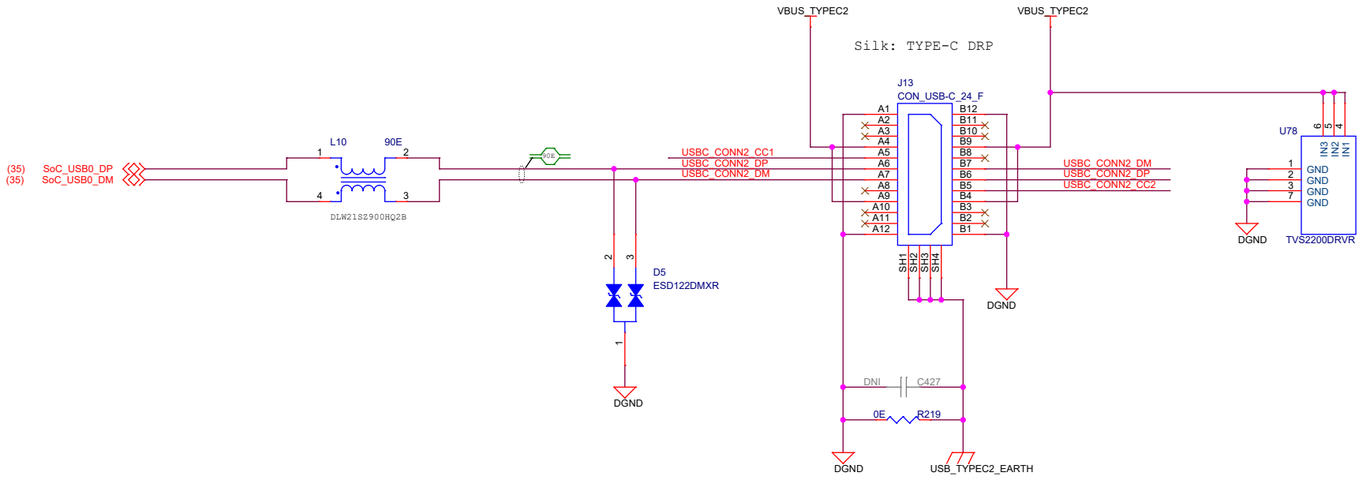
OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

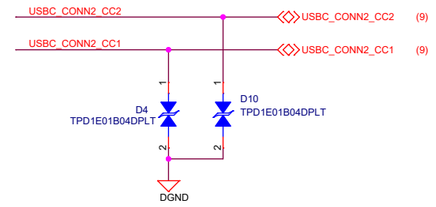


Designed for TI by Mistral Solutions Pvt Ltd

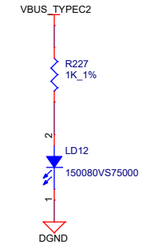
Title	MCU HEADER	
Size C	PROC114E2	Rev E2
Date: Tuesday, February 22, 2022	Sheet 33 of 43	

USB0 TYPE-C DRP

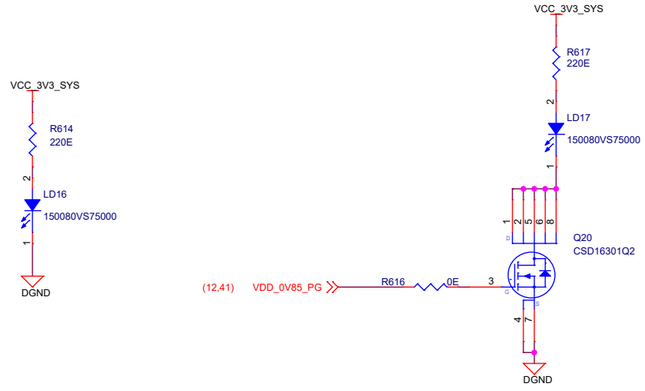




POWER INDICATION LED: VBUS_TYPEC2



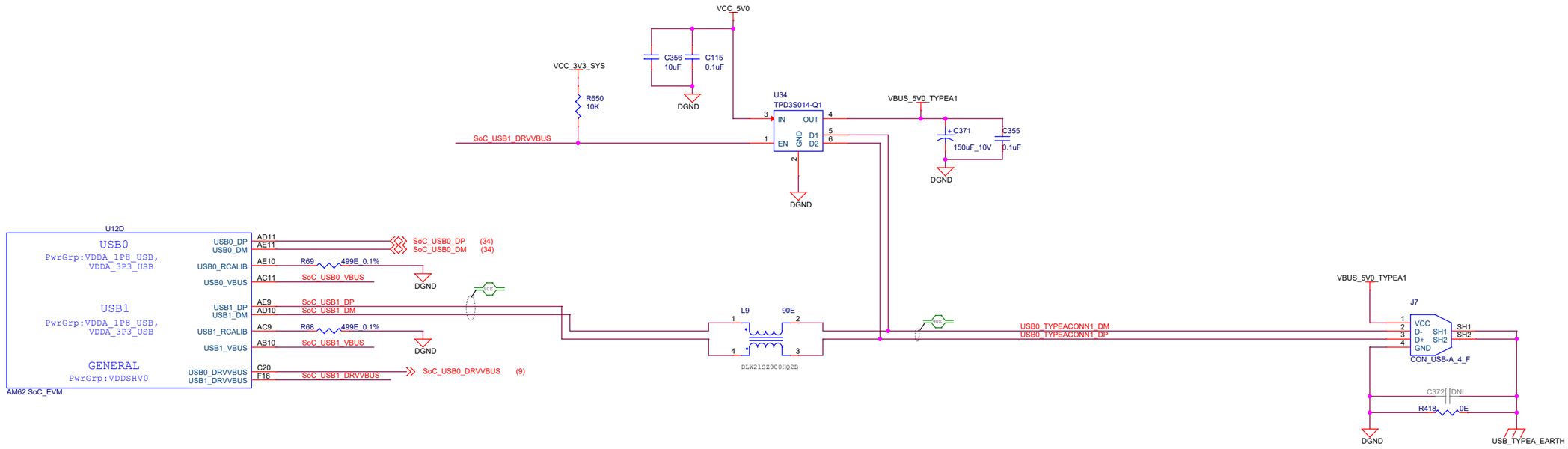
POWER RAIL LEDS



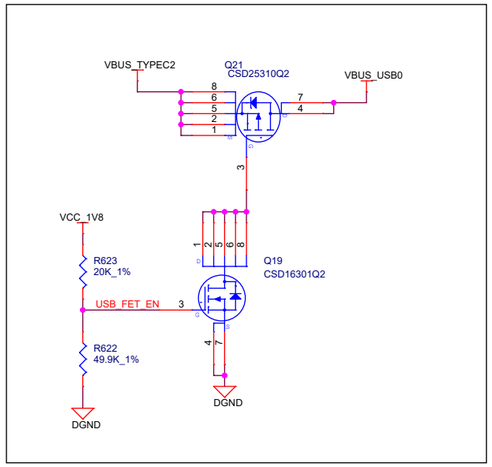
Designed for TI by Mistral Solutions Pvt Ltd

Title	USB0 TYPE-C DRP	
Size: C	PROC114E2	Rev: E2
Date: Tuesday, February 22, 2022	Sheet 34 of 43	

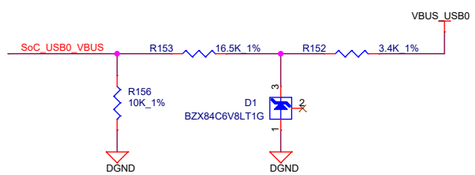
USB1 TYPE-A



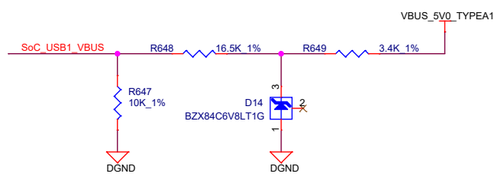
Silk: TYPE-A



Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



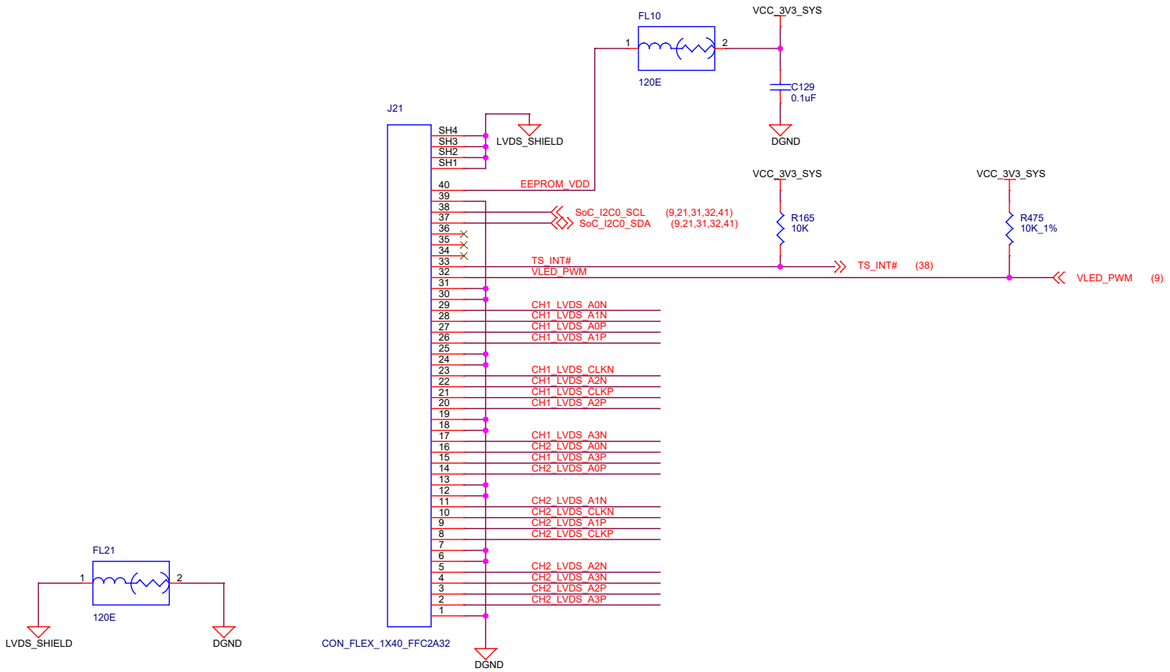
Note: Recommended VBUS circuit for SoC_USB1_VBUS

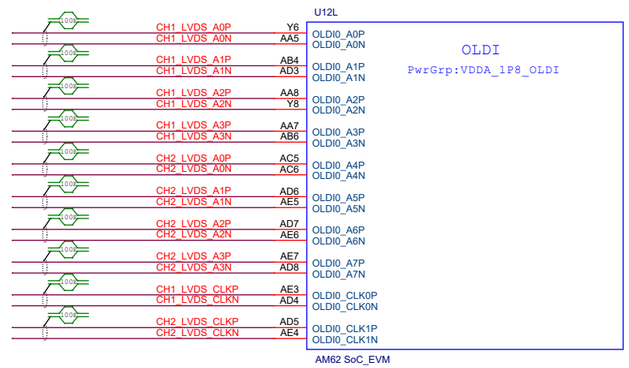


Designed for TI by Mistral Solutions Pvt Ltd

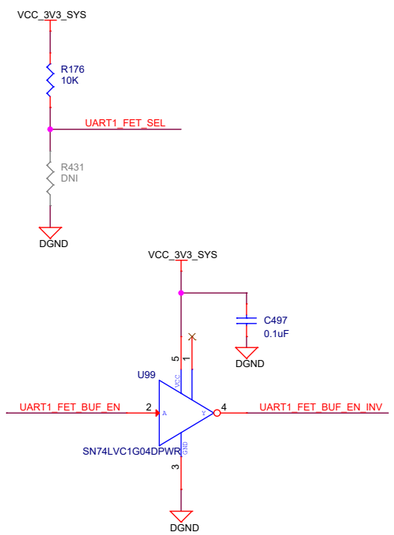
Title	USB1 TYPE-A		
Size	PROC114E2		Rev
C			E2
Date:	Tuesday, February 22, 2022	Sheet 35 of 43	

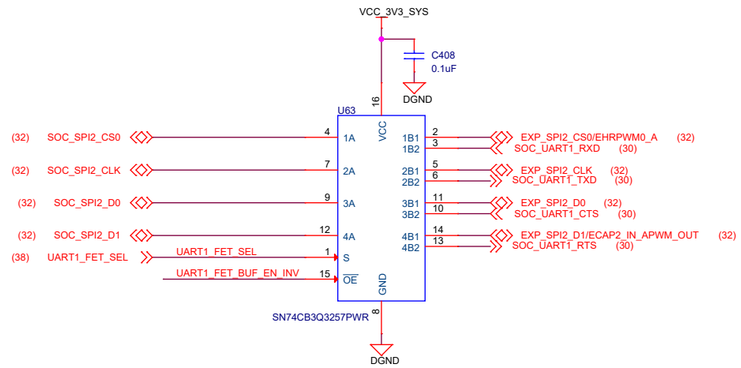
OLDI DISPLAY INTERFACE

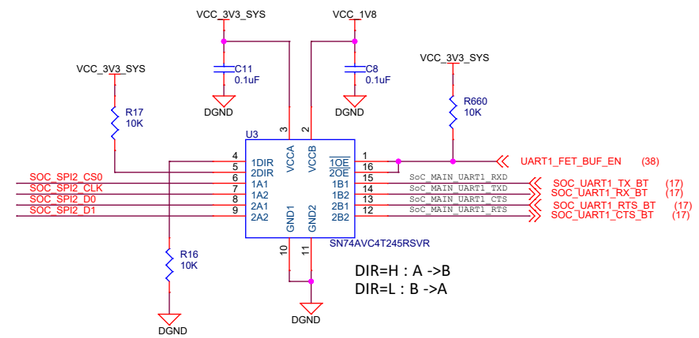




SoC UART1 FET SWITCH & BUFFER







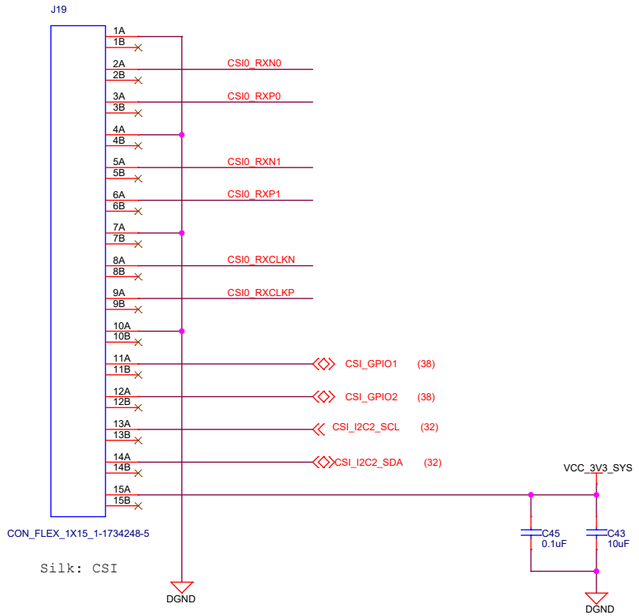
OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	FT4232
L	L	An=nB1	EXP CONN

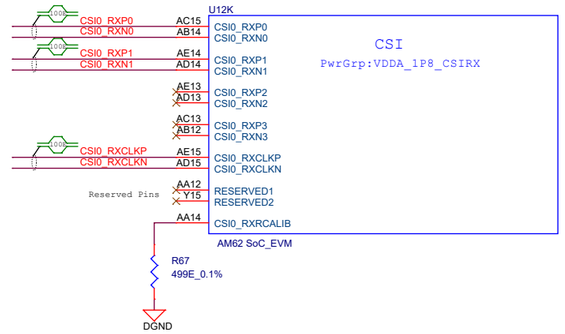
Designed for TI by Mistral Solutions Pvt Ltd

Title	OLDI DISPLAY INTERFACE	
Size C	PROC114E2	Rev E2
Date: Tuesday, February 22, 2022	Sheet 36 of 43	

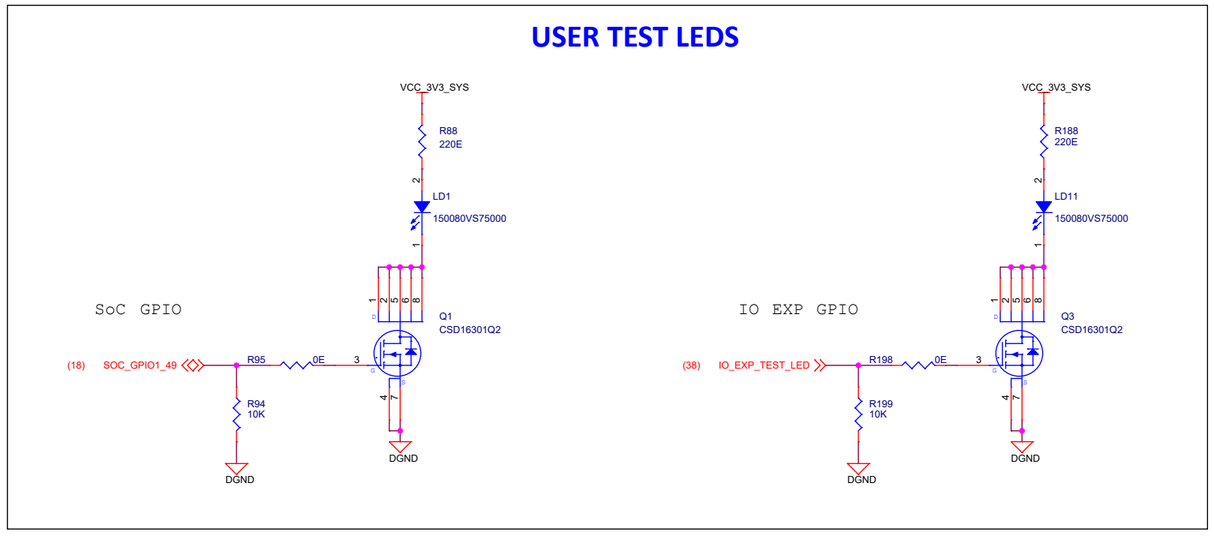
CSI INTERFACE

CSI CAMERA HEADER





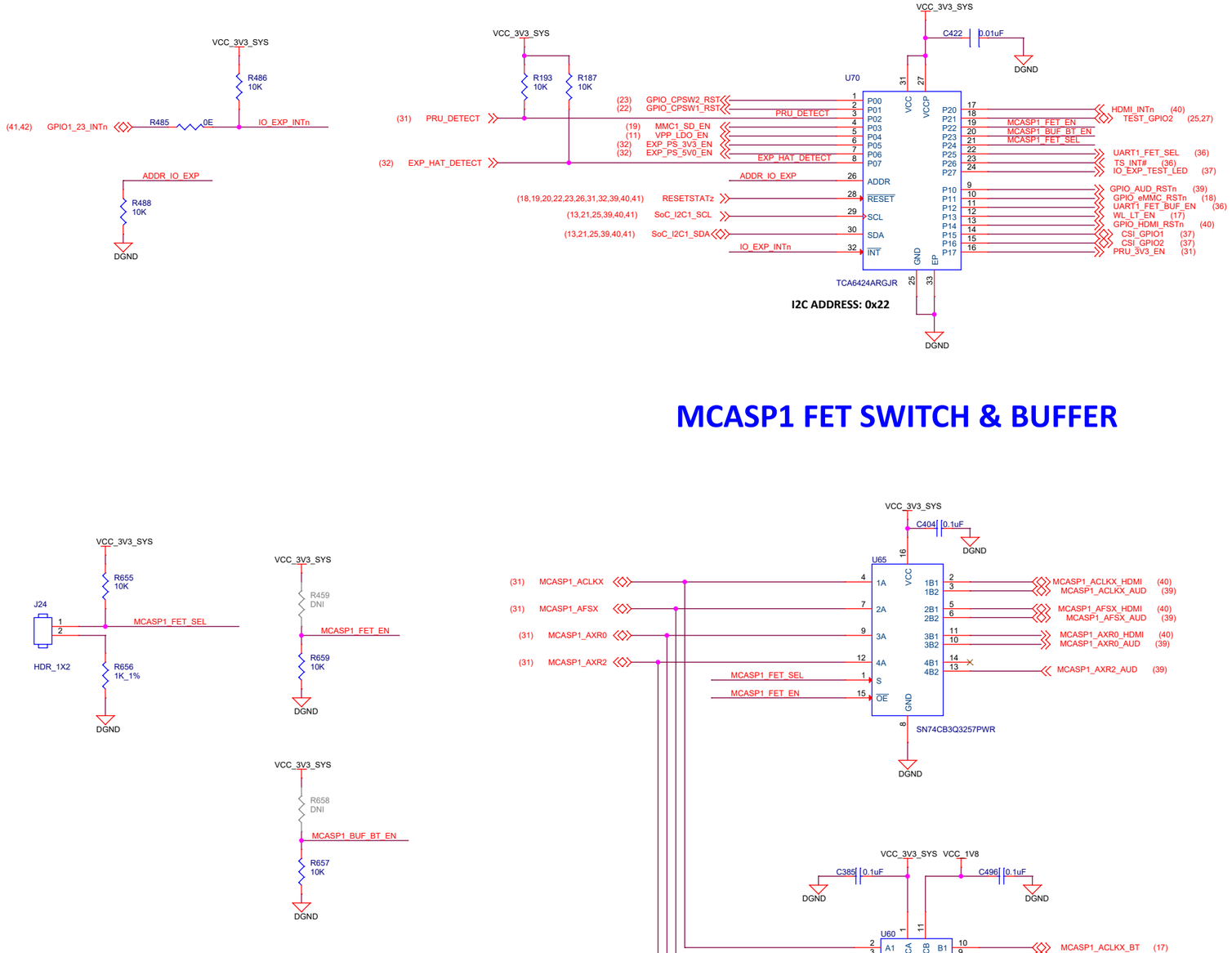
USER TEST LEDS



Designed for TI by Mistral Solutions Pvt Ltd

Title	CSI INTERFACE & USER TEST LEDS		
Size	PROC114E2		Rev
C			E2
Date:	Tuesday, February 22, 2022	Sheet 37 of 43	

IO EXPANDER



MCASP1 FET SWITCH & BUFFER

OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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Title	IO EXPANDER		
Size: C	PROC114E2		Rev: E2
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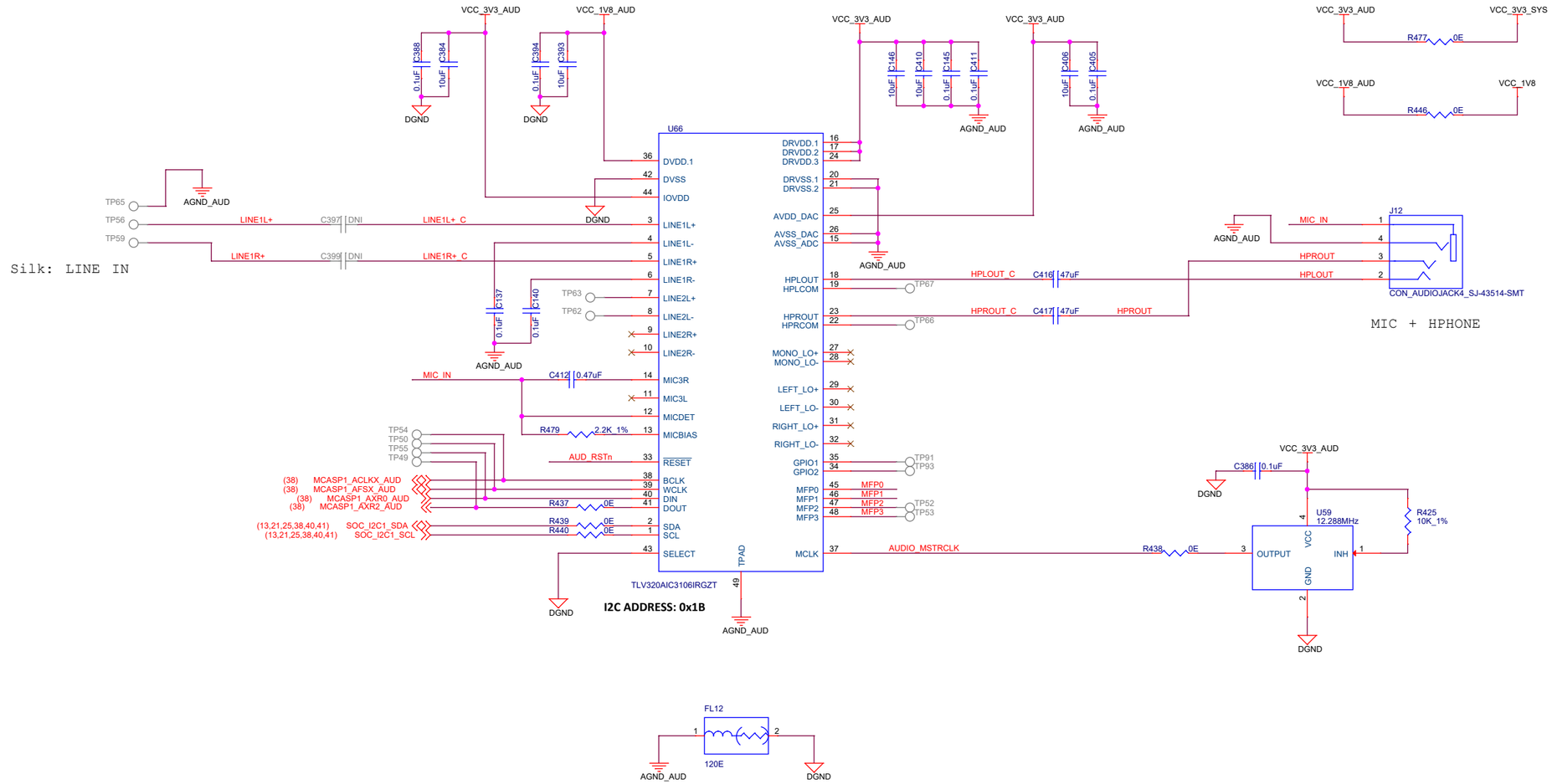
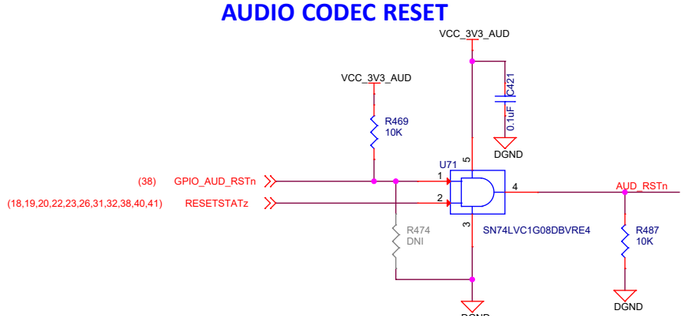
AUDIO CODEC

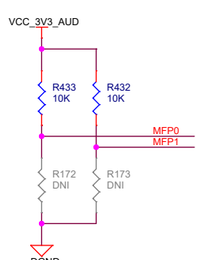


AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUDIO CODEC		
Size C	PROC114E2		Rev E2
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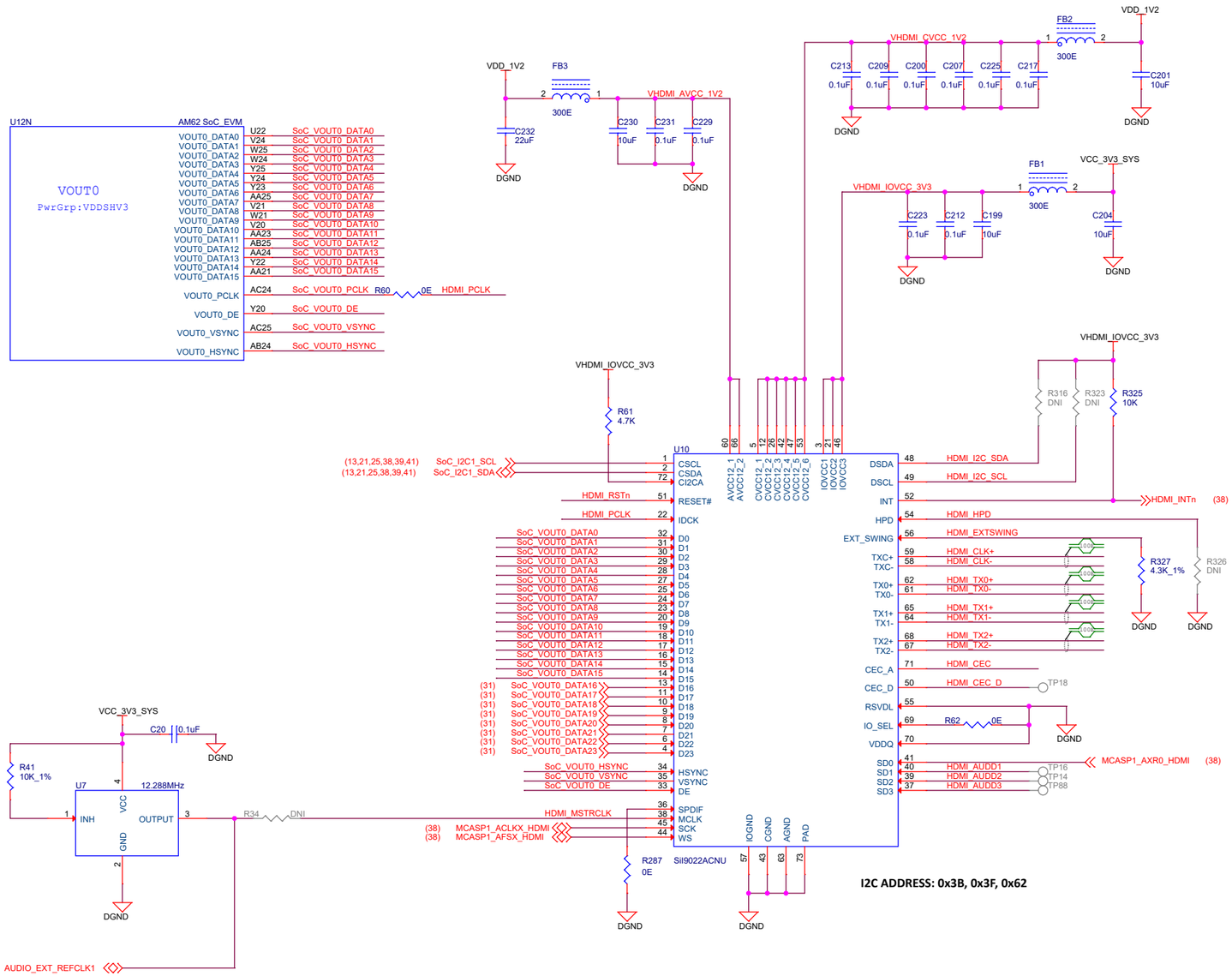
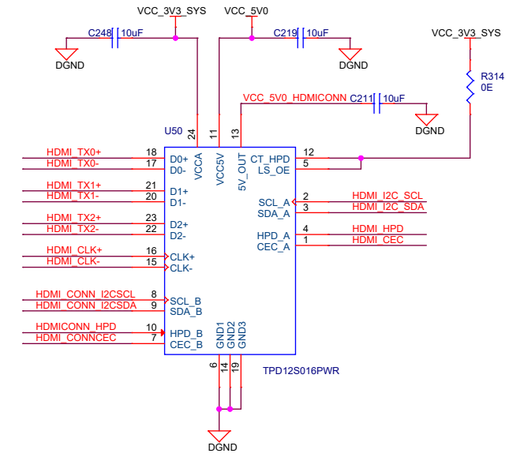
HDMI INTERFACE



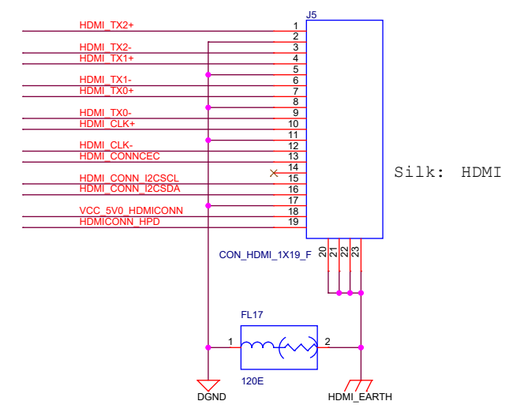
I2C ADDRESS: 0x3B, 0x3F, 0x62

HDMI ESD DEVICE

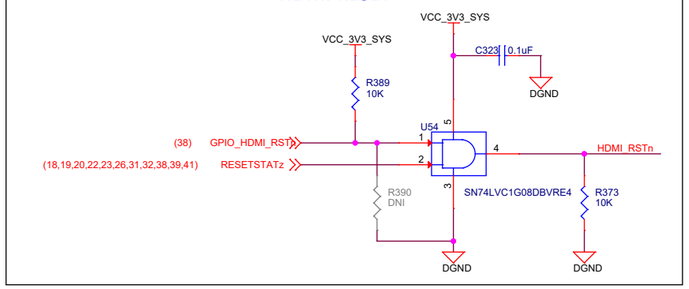


NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR



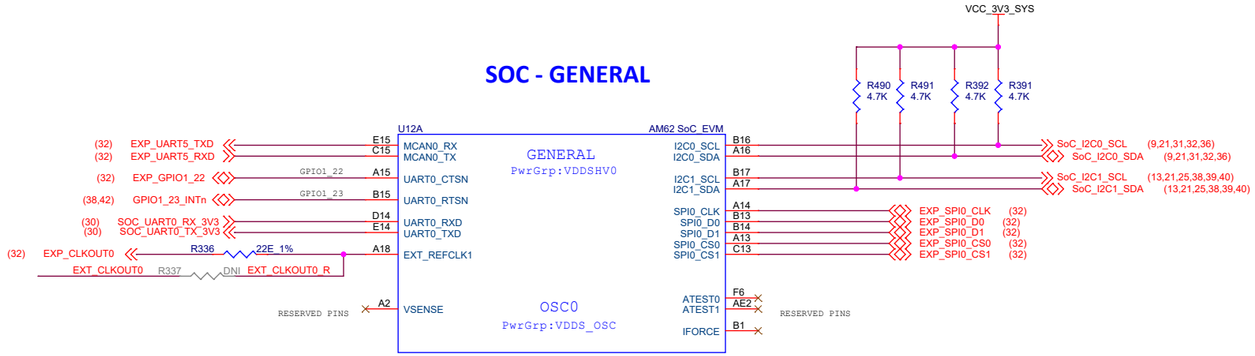
HDMI RESET



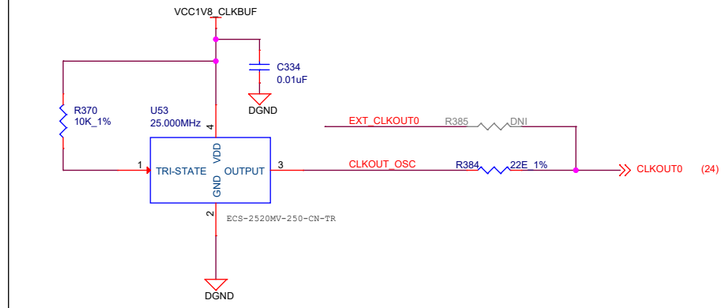
Designed for TI by Mistral Solutions Pvt Ltd

Title	HDMI INTERFACE		
Size	PROC114E2		Rev
C			E2
Date:	Tuesday, February 22, 2022	Sheet 40 of 43	

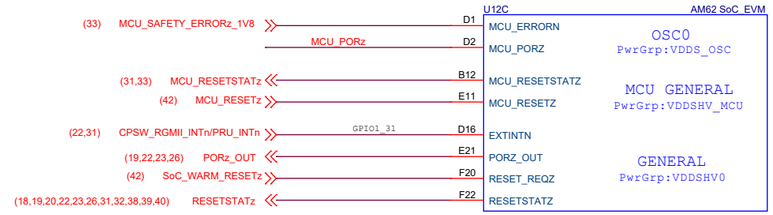
SOC - GENERAL



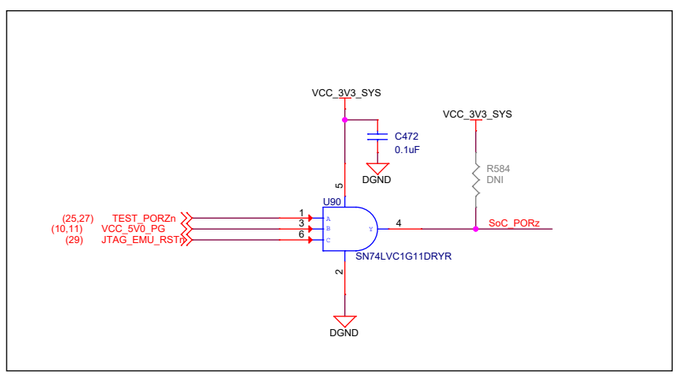
OSCILLATOR



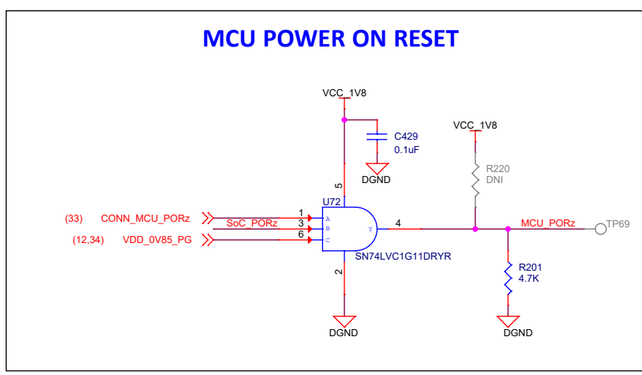
SOC - RESET



Pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up seqence



MCU POWER ON RESET



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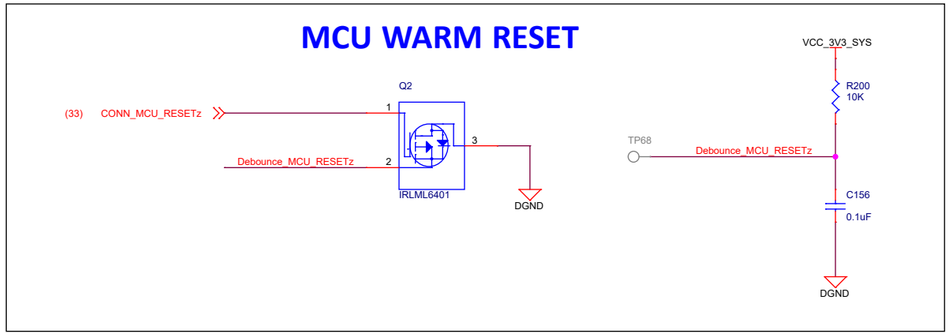
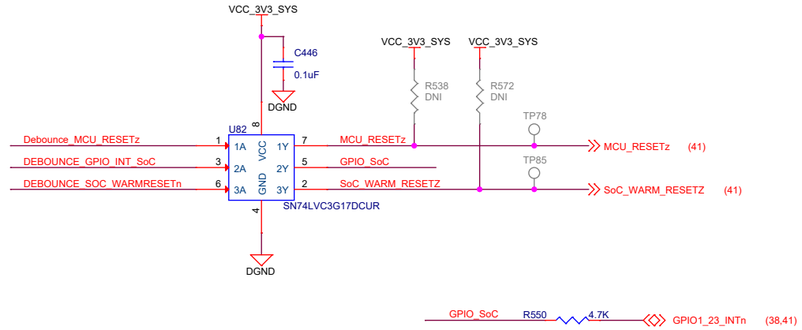
Title	OSCILLATOR		
Size C	PROC114E2		Rev E2
Date: Tuesday, February 22, 2022		Sheet 41 of 43	

RESET

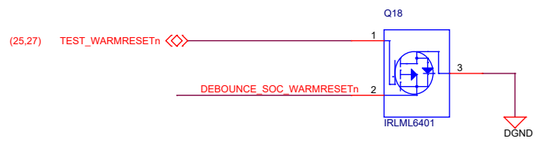
MCU WARM RESET

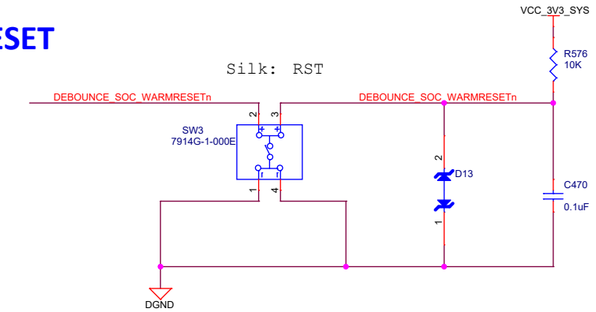


DEBOUNCE CIRCUIT

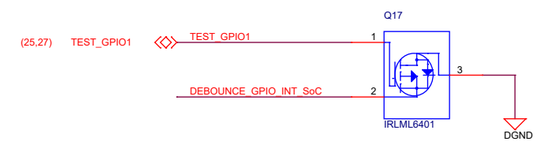


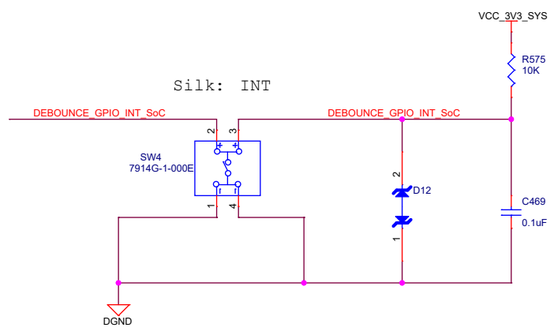
SOC WARM RESET





USER INTERRUPT





Designed for TI by Mistral Solutions Pvt Ltd

Title	RESET		
Size	PROC114E2		Rev
C			E2
Date:	Tuesday, February 22, 2022	Sheet 42 of 43	

HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB

PROC114

PROC114E1

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

LABELS

Board Serial No.

LBL1
PCB LABEL
DNI

Assembly Revision

LBL2
PCB LABEL
DNI

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

Designed for TI by Mistral Solutions Pvt Ltd

Title	HARDWARE SCHEMATICS	
Size: C	PROC114E2	Rev: E2
Date: Tuesday, February 22, 2022	Sheet 43 of 43	