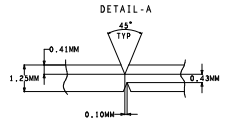
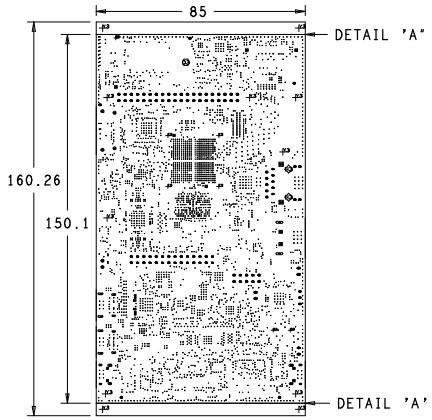
REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

FABRICATION NOTES:

1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012D, CLASS 2$_B$ PER IPC-6011. PCB SHALL BE MANUFACTURED USING ITEQ IT 180A OR EQUIVALENT
2. MATERIALS:
   1. LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/126. (MIN.TG 170)
   2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150. UNLESS OTHERWISE SPECIFIED. THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. BOARD FINISHED SHALL BE ACCORDING TO IPC-6012D CLASS 2.
7. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
8. FINISH:
   1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL/IMMERSION GOLD. ELECTROLESS NICKEL SHALL BE 3-6 MICRONS. TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
   2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES SHALL BE RESIN FILLED AND COVERED WITH SOLDER MASK. ONLY SOLDER MASK IMAGES THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE GREEN.
   3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
   4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM [0.00079"], INCASE OF LASER VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 12UM [0.00047"] AND BURIED VIA'S SHALL NOT BE LESS THAN 15UM [0.0006"].
   5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLIANCE TO IPC6012, CLASS 2.
9. MARKING:
   1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
10. TEST REQUIREMENTS:
    1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
11. THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
12. TEAR DROPS SHALL BE ADDED ON VIA'S AND THROUGH HOLE PADS IN ALL INTERNAL AND OUTER LAYERS.
13. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IF REQUIRED.
14. FINISHED PCB THICKNESS SHALL BE 0.049" +/-10%.
15. MIN TRACE WIDTH/SPACING ON BOARD IS 0.0032"/0.0033".
16. ENSURE UL REGISTERED E-FILE NUMBER SHALL BE PRINTED ON THE PCB SILKSCREEN.
17. VIA ON PAD SHALL BE RESIN FILLED AND CAP-PLATED.
18. FOR STACKUP DETAIL PROC135E1_STACKUP.PDF SHALL BE REFERRED.



DETAIL-A(V-GROOVE DETAILS)
SCALE:NTS



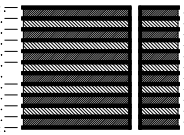
DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	7.99	+3.0/-3.0	PLATED	20
·	8.0	+3.0/-3.0	PLATED	3834
•	36.0	+3.0/-3.0	PLATED	38
•	40.0	+3.0/-2.0	PLATED	6
•	40.0	+3.0/-3.0	PLATED	62
•	44.0	+2.0/-2.0	PLATED	2
•	52.0	+1.0/-1.0	PLATED	4
■	66.0	+3.0/-3.0	PLATED	2
◆	118.0	+3.0/-3.0	PLATED	1
•	32.0	+3.0/-3.0	NON-PLATED	4
•	34.0	+2.0/-2.0	NON-PLATED	2
•	40.0	+3.0/-3.0	NON-PLATED	2
•	44.0	+2.0/-2.0	NON-PLATED	1
■	48.0	+3.0/-3.0	NON-PLATED	2
■	62.0	+2.0/-2.0	NON-PLATED	1
■	66.0	+3.0/-3.0	NON-PLATED	2
■	68.0	+3.0/-3.0	NON-PLATED	4
■	108.0	+3.0/-3.0	NON-PLATED	11
◆	126.0	+3.0/-3.0	NON-PLATED	2
-	48.0x22.0	+3.0/-3.0	PLATED	4
-	62.0x24.0	+2.0/-2.0	PLATED	4
-	68.0x34.0	+3.0/-3.0	PLATED	4
-	82.0x24.0	+2.0/-2.0	PLATED	4
-	118.0x28.0	+3.0/-3.0	PLATED	2

LAYER STACKUP

LAYER NAME	FINISHED Cu	DIELECTRIC THICKNESS [INCHES]
PRIMARY SIDE SILKSCREEN		
PRIMARY SIDE SOLDERMASK		
L01 PRIMARY SIDE	1.47oz.	0.0030
L02 GROUND-PLANE-1	0.5oz.	0.0030
L03 INNER-SIGNAL-1	0.5oz.	0.0044
L04 GROUND-PLANE-2	0.5oz.	0.0030
L05 INNER-SIGNAL-2	0.5oz.	0.0044
L06 POWER-PLANE-1	0.5oz.	0.0030
L07 POWER-PLANE-2	0.5oz.	0.0045
L08 POWER-PLANE-2	0.5oz.	0.0030
L09 GROUND-PLANE-3	0.5oz.	0.0044
L10 INNER-SIGNAL-3	0.5oz.	0.0030
L11 GROUND-PLANE-4	0.5oz.	0.0030
L12 SECONDARY SIDE	1.47oz.	
SECONDARY SIDE SOLDERMASK		
SECONDARY SIDE SILKSCREEN		



IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	EDGE COUPLED MICROSTRIP	L1, L12	3.5	5.5	100	L2, L11
02	EDGE COUPLED MICROSTRIP	L1, L12	4	4.3	90	L2, L11
03	MICROSTRIP	L1, L12	5.5	NA	50	L2, L11
04	EDGE COUPLED STRIPLINE	L3, L10	3.5	5	100	L2/L4, L9/L11
05	EDGE COUPLED STRIPLINE	L05	3.5	5	100	L4/L6
06	EDGE COUPLED STRIPLINE	L3, L10	4	4	90	L2/L4, L9/L11
07	EDGE COUPLED STRIPLINE	L5	4	4	90	L4/L6
08	EDGE COUPLED STRIPLINE	L3, L5	5	4	80	L2/L4, L4/L6
09	EDGE COUPLED STRIPLINE	L10	7.4	4.4	66	L9/L11
10	EDGE COUPLED STRIPLINE	L3	3	6.5	133	L2/L4
11	STRIPLINE	L3, L10	4	NA	50	L2/L4, L9/L11
12	STRIPLINE	L5	4	NA	50	L4/L6
13	STRIPLINE	L3, L5	5.5	NA	40	L2/L4, L4/L6

SIGNATURES		DATE
LAYOUT BY	SM	060622
REVIEWED BY	ZA	060622
APPROVED BY	AMB	060622

TEXAS INSTRUMENTS

PROC135E1

AM62A EVM BOARD

SIZE D | Rev E1

SCALE:NONE | SHEET 1 OF 19