AM64x STARTER KIT EVM BOARD

SK-AM64B

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REV	A
VER	1.3
BOM Variant	002

Note: Raspberry Pi is the trademark / wordmark of Raspberry Pi Foundation

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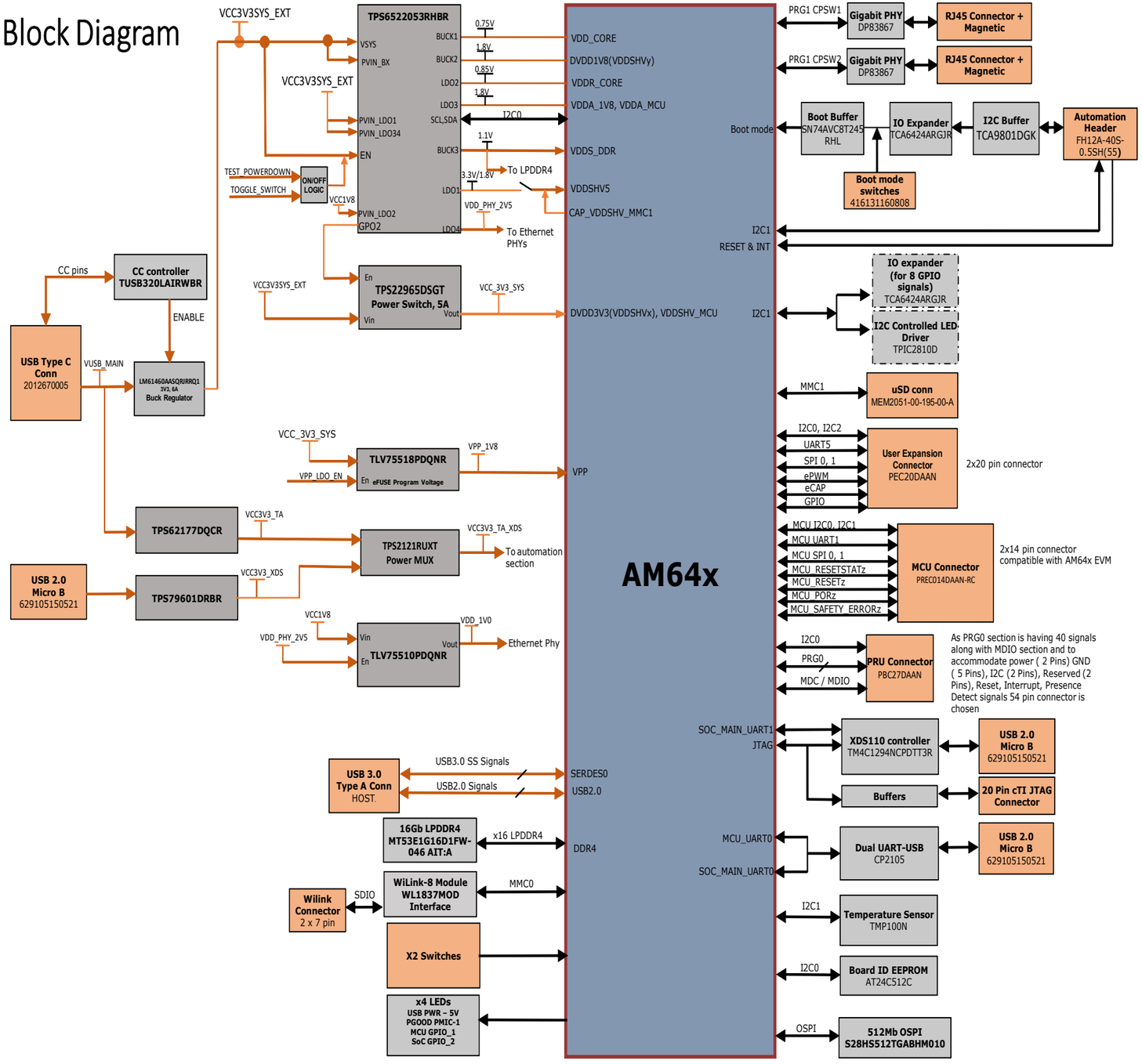
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
1.0	20th APR 2022	Drafted from "PROC100E4_SCH" Document and updated PG2.0 changes.	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.1	21st APR 2022	Power Mux added, R375 added, R138 is replaced to 0E from 1M ohm, R469 & R470 are removed, C343 is made as DNI.	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.2	21st APR 2022	Antenna Tuning Network C2, L2 and L4 values updated	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.3	12th SEPT 2022	PMIC Buck Capacitors replaced with 47uF (C373, C374, C376), RSVD ball names updated in SoC and Replaced obsolete components with alternate components.	Mistral Design Team	Krishna Prasad	Krishna Prasad

BLOCK DIAGRAM_AM64x_SKEVM

Functional Block Diagram



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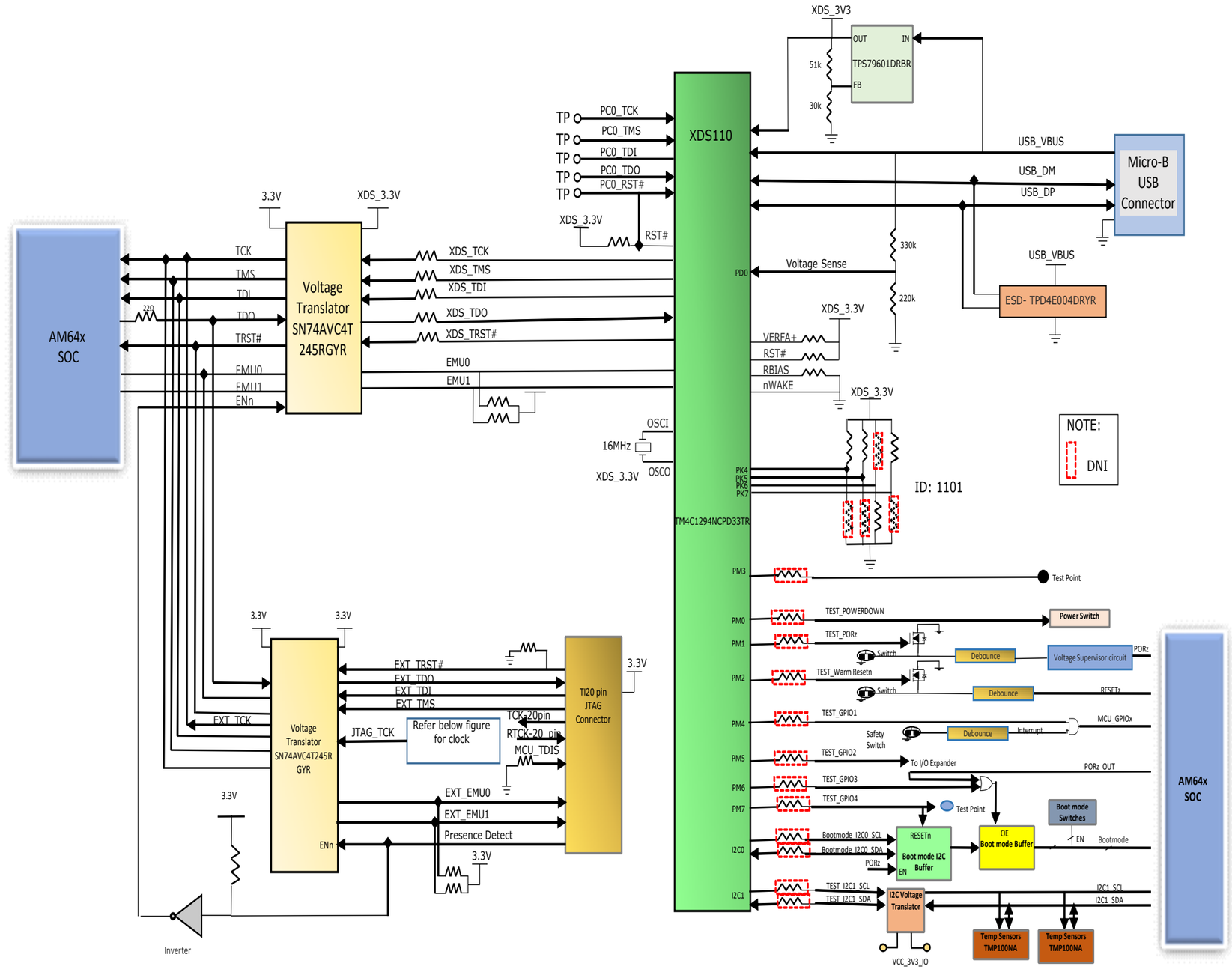
BLOCK DIAGRAM_XDS110



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Title	BLOCK DIAGRAM_XDS110	
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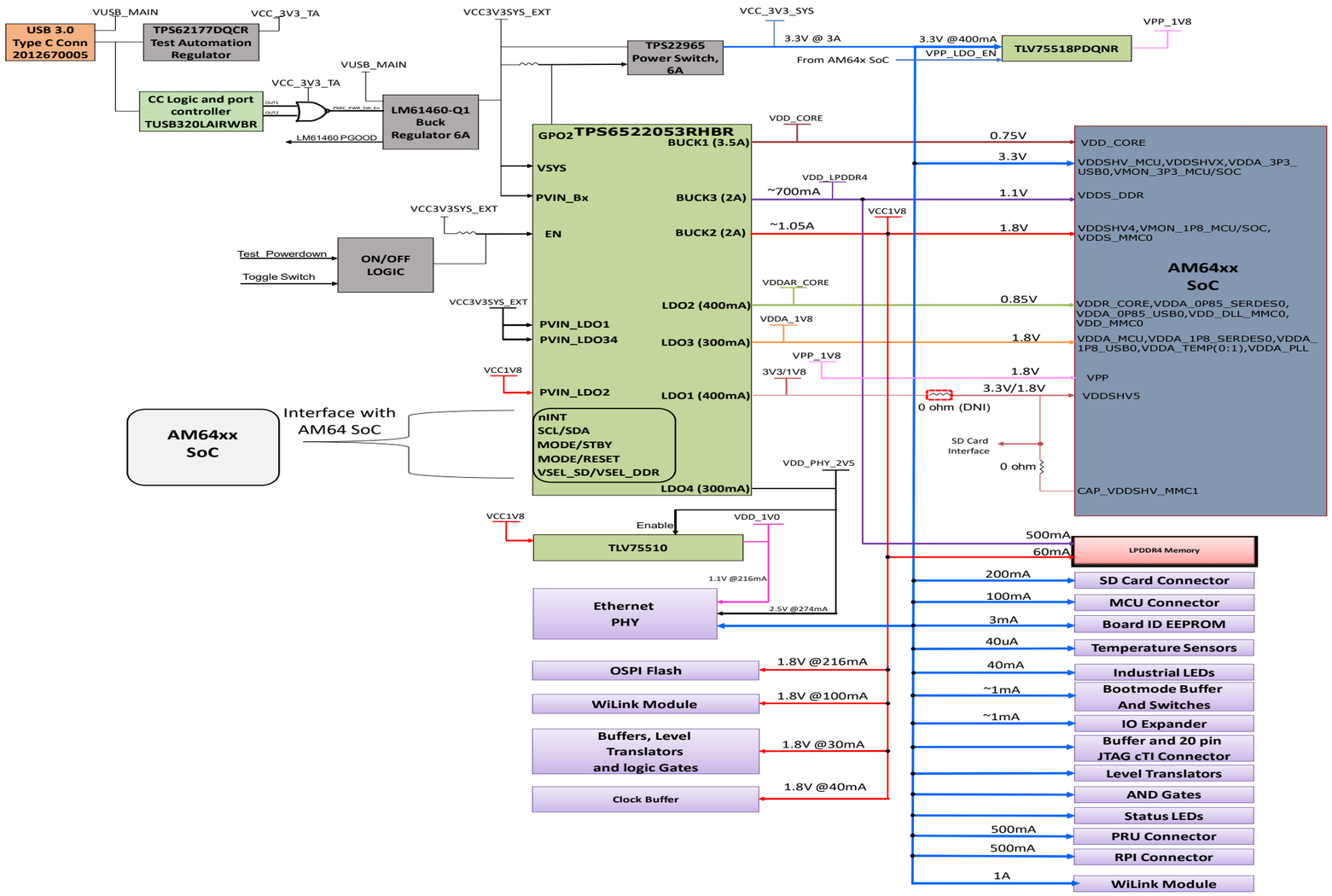
POWER BLOCK DIAGRAM



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Title	POWER BLOCK DIAGRAM	
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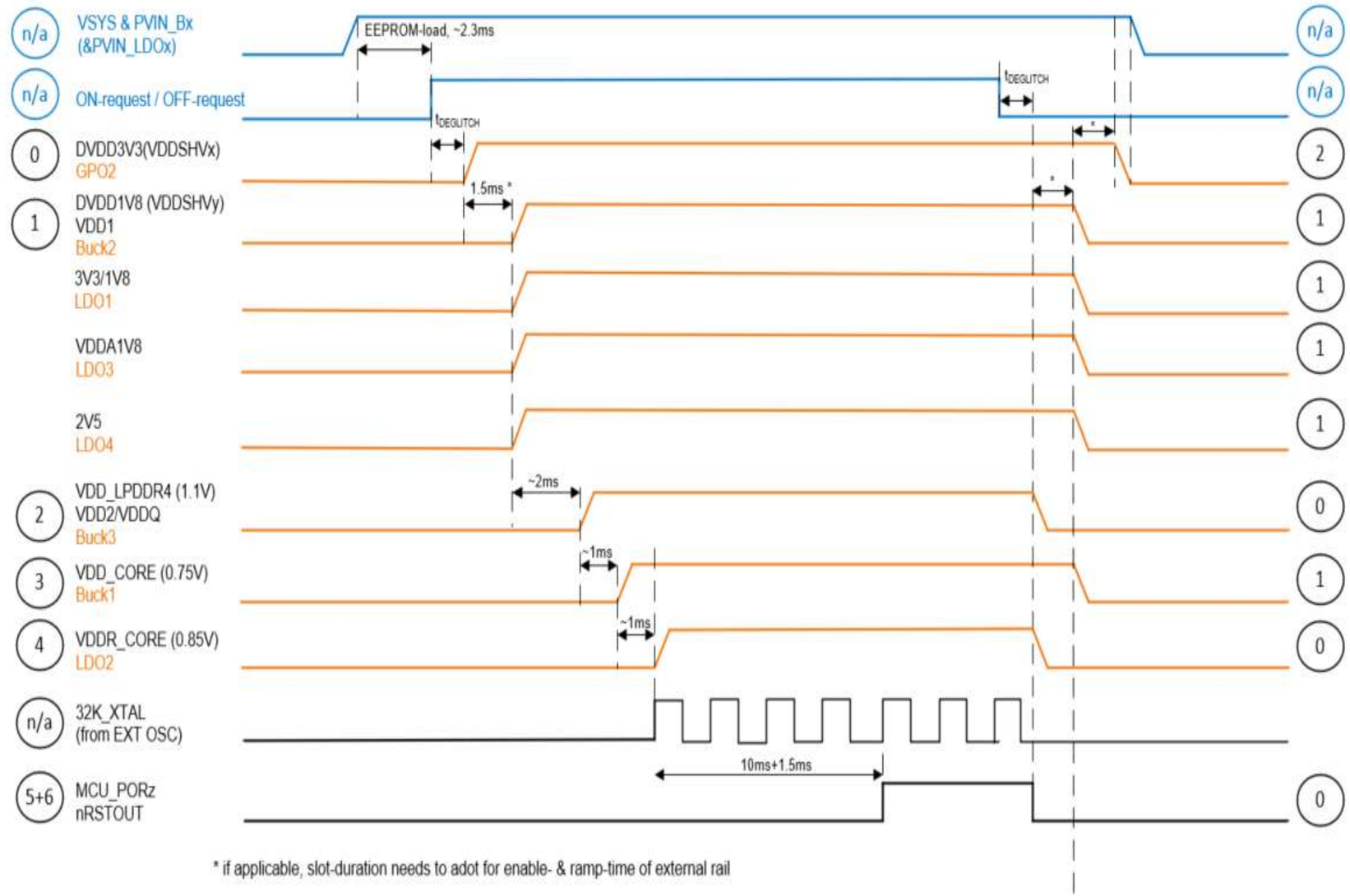
POWER SEQUENCE



* if applicable, slot-duration needs to adot for enable- & ramp-time of external rail

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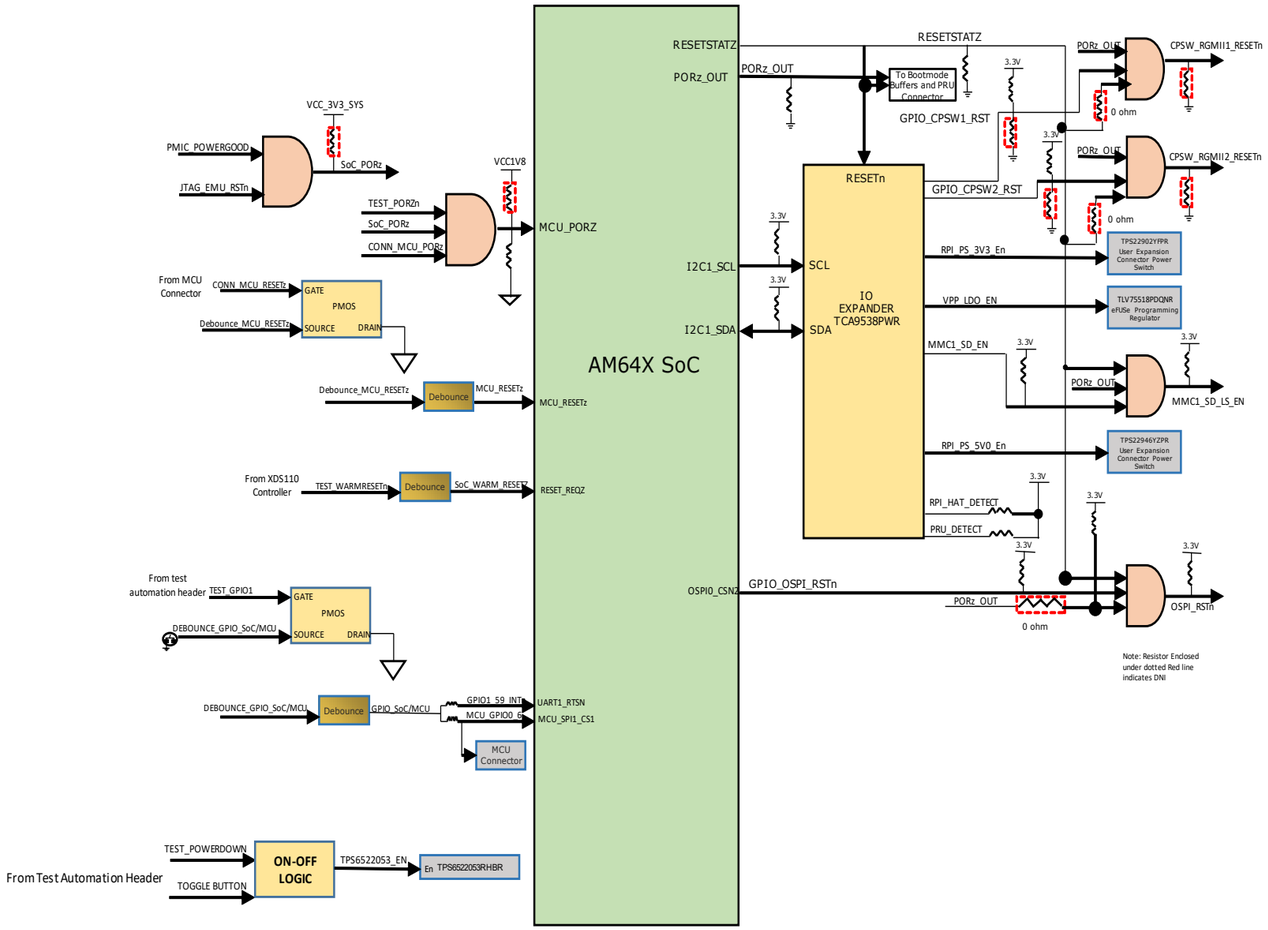
RESET ARCHITECTURE



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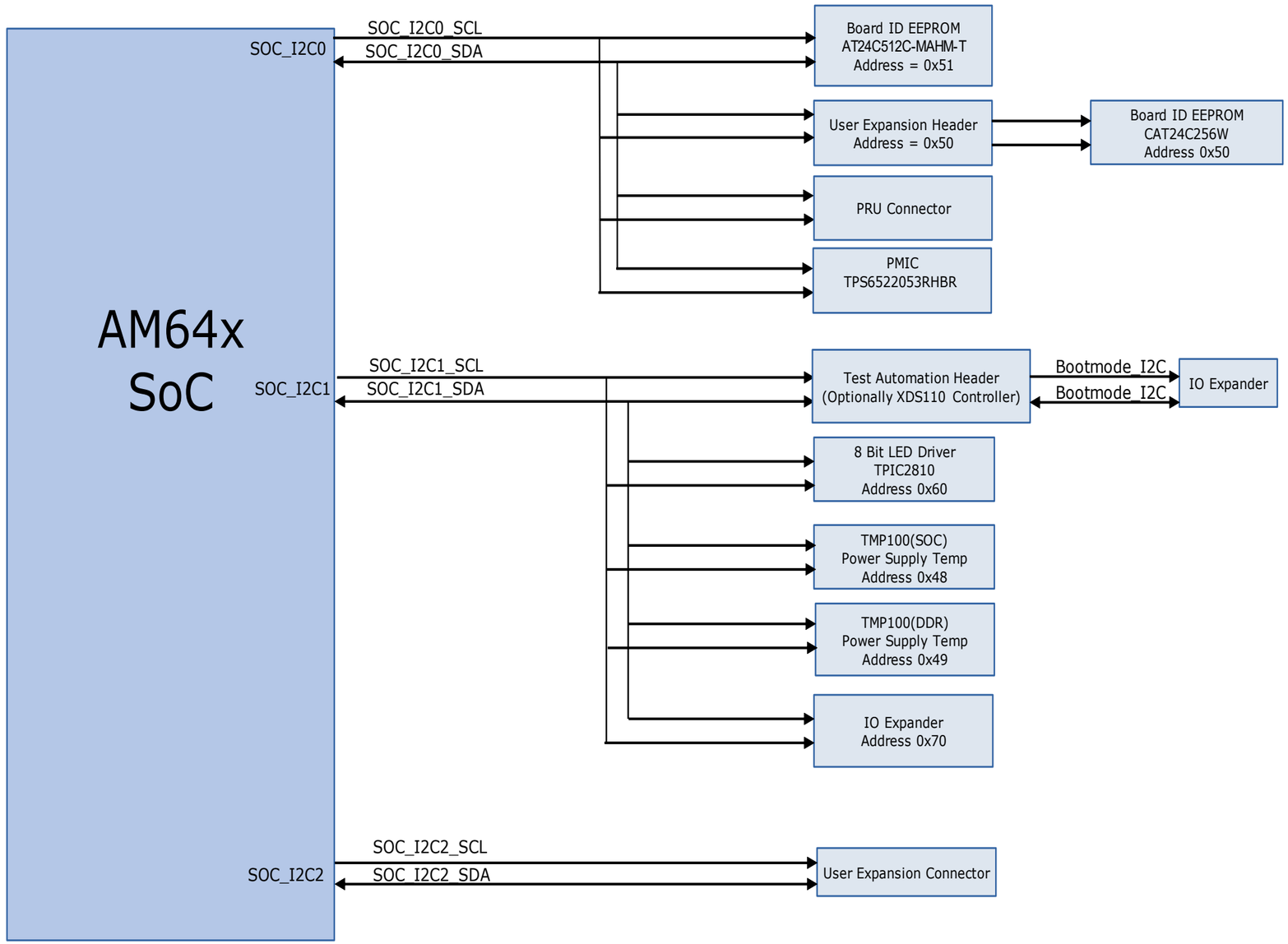
GPIO MAPPING TABLE

AM64x GPIO MAPPING TABLE										
Sl.NO	GPIO Description	GPIO Netname	Functionality	GPIO Used	SoC Muxed Signal Name	Direction with respect to SoC	Default State	Active State	Voltage Domain On Processor Side	Voltage Connected on SKEVM
1	IO Expander Interrupt	IO_EXP_INTn_SDIO	Interrupt	GPIO1_78	MMC1_SDWP	Input	High	Low	VDDSHV0	SoC_DVDD3V3
2	Enable for COM8 Level Translator	COM8_LS_EN	Enable	GPIO0_62	PRG1_PRU0_GPO17	Output	High	Low	VDDSHV2	SoC_DVDD3V3
3	Enable for WLAN Interface in COM8 Connector	WLAN_EN_SoC_LS	Enable	GPIO0_48	PRG1_PRU0_GPO3	Output	Low	High	VDDSHV2	SoC_DVDD3V3
4	Enable for BT Interface in COM8 Connector	BT_EN_SOC_LS	Enable	GPIO0_49	PRG1_PRU0_GPO4	Output	Low	High	VDDSHV2	SoC_DVDD3V3
5	WLAN SDIO out-of band interrupt line	WLAN_IRQ_LS	Interrupt	GPIO0_46	PRG1_PRU0_GPO1	Input	High	Low	VDDSHV2	SoC_DVDD3V3
6	OSPI Interrupt	OSPI_INTn	Interrupt	GPIO0_14	OSPI0_CSN3	Input	High	Low	VDDSHV4	SOC_DVDD1V8
7	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	Reset	GPIO0_13	OSPI0_CSN2	Output	High	Low	VDDSHV4	SOC_DVDD1V8
8	User LED	TEST_LED1	Test	GPIO0_60	PRG1_PRU0_GPO15	Output	Low	High	VDDSHV2	SoC_DVDD3V3
9	User LED	TEST_LED2	Test	MCU_GPIO0_5	MCU_SPI1_CS0	Output	Low	High	VDDSHV_MCU	SoC_DVDD3V3
10	SD card load switch enable control	MMC1_SD_EN	Enable	IO Expander-P3		Output	High	High	VDDSHV0	SoC_DVDD3V3
11	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn								
12	PRU Connector Interrupt	PRU_INTn	Interrupt	GPIO1_70	EXTINTn	Input	High	Low	VDDSHV0	SoC_DVDD3V3
13	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	Reset	IO Expander-P1		Output	High	Low	VDDSHV0	SoC_DVDD3V3
14	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	Reset	IO Expander-P0		Output	High	Low	VDDSHV0	SoC_DVDD3V3
15	TEST GPIO1 from Test Automation	TEST_GPIO1	GPIO for communication with AM64x	GPIO1_59 MCU_GPIO0_6	UART1_RTSN MCU_SPI1_CS1	Input Input	High High	Low Low	VDDSHV0 VDDSHV_MCU	SoC_DVDD3V3 SoC_DVDD3V3
16	BTUART_RTS or Bootmode10 switch select	BTUART_RTS_SEL	Switch Selection	GPIO0_63	PRG1_PRU0_GPO18	Output	Low	High	VDDSHV2	SoC_DVDD3V3
17	VPP 1.8V regulator Enable	VPP_LDO_EN	Enable	IO Expander-P4		Output	Low	High	VDDSHV0	SoC_DVDD3V3
18	MODE/STBY	PMIC_STBY	Standby Mode	GPIO0_51	PRG1_PRU0_GPO6	Output	High	Low	VDDSHV2	SoC_DVDD3V3
19	VSEL_SD/VSEL_DDR	VSEL_SD_SWITCH	SD Selection	GPIO0_45	PRG1_PRU0_GPO2	Output	High	High	VDDSHV2	SoC_DVDD3V3
20	Power Switch Enable for USB device	USB0_DRVBUS	Enable	GPIO1_79	USB0_DRVVBUS	Output	Low	High	VDDSHV0	SoC_DVDD3V3
21	RPI-HAT Detection	RPI_HAT_DETECT	Detection	IO Expander-P7		Input	High	Low	VDDSHV0	SoC_DVDD3V3
22	PRU Detection	PRU_DETECT	Detection	IO Expander-P2		Input	High	Low	VDDSHV0	SoC_DVDD3V3
23	PRU Power Switch Enable	PRU_3V3_En	Enable	GPIO0_64	PRG1_PRU0_GPO19	Output	Low	High	VDDSHV2	SoC_DVDD3V3
24	Rpi Power Switch Enable	RPI_PS_5V0_En	Enable	IO Expander-P6		Output	Low	High	VDDSHV0	SoC_DVDD3V3
25	Rpi Power Switch Enable	RPI_PS_3V3_En	Enable	IO Expander-P5		Output	Low	High	VDDSHV0	SoC_DVDD3V3

I2C TREE



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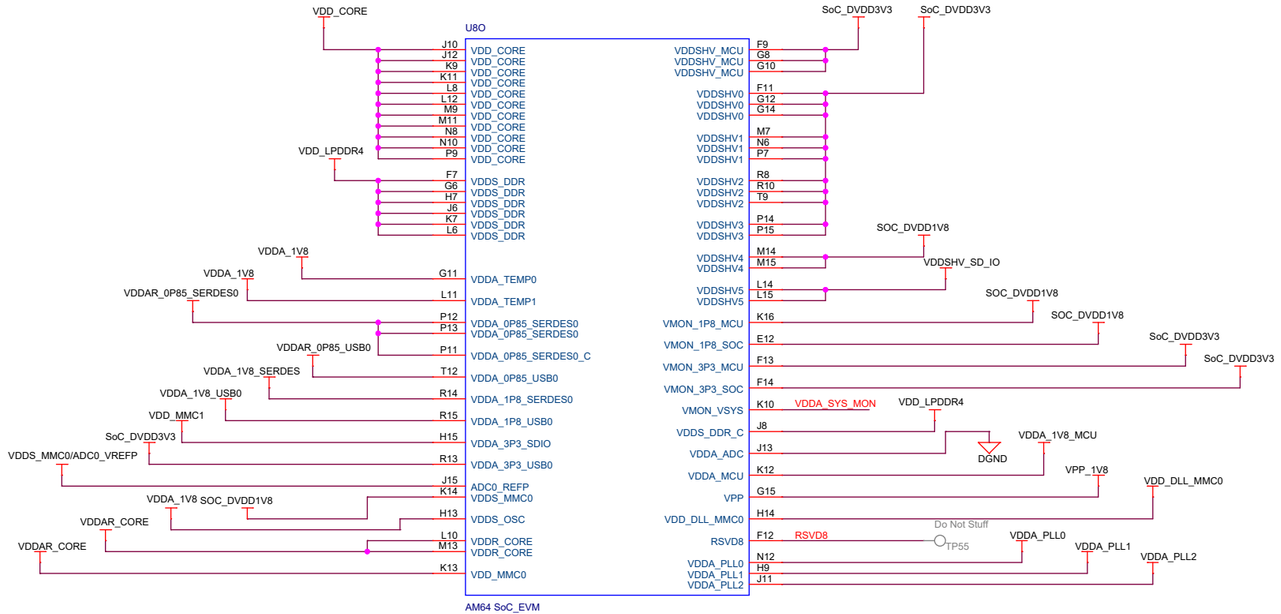
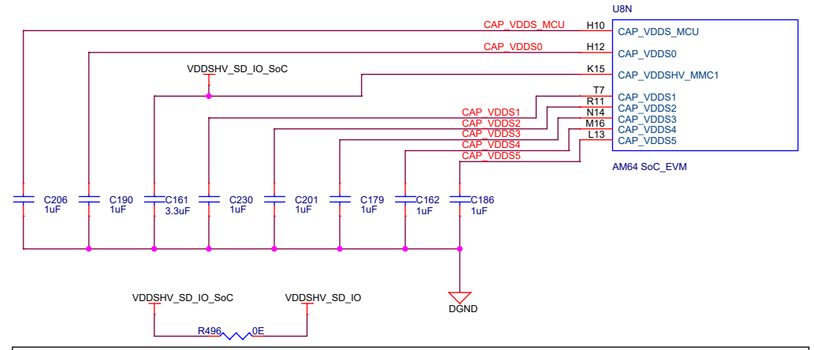
SOC POWER

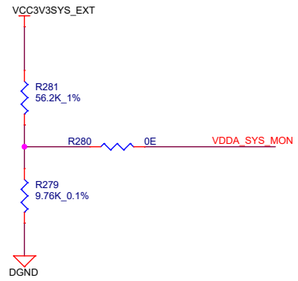




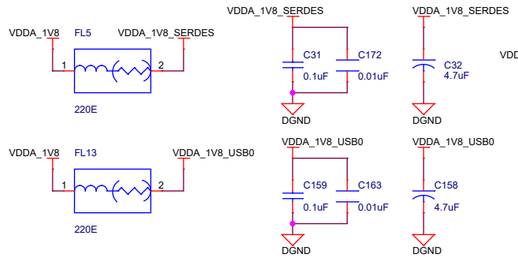
RESISTOR DIVIDER TBV

Vth : (0.45V+(+/-3% Tolerance))
Vth max: 0.4635
Vth min: 0.4365

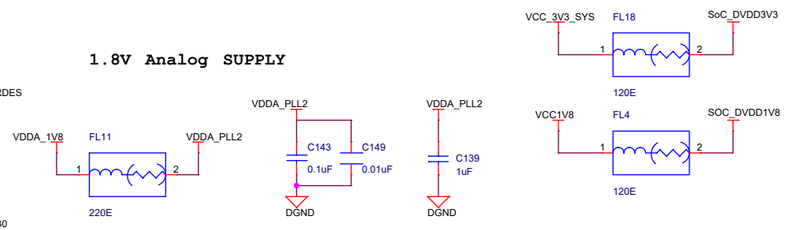
AM64x Recommended Operating Conditions:
Vmin: 3.135V
Vnom: 3.3V
Vmax: 3.465V



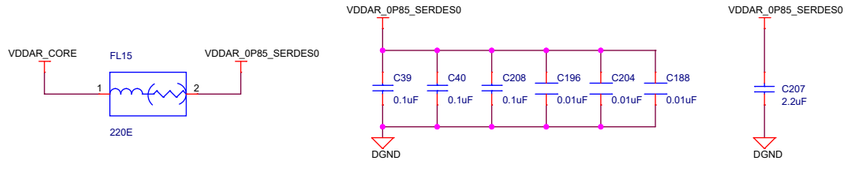
1.8V Analog SUPPLY



1.8V Analog SUPPLY

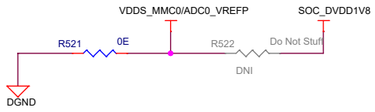


CORE SUPPLY



PG2.0 Changes

If SR1.0 is installed, mount R522 and make R521 as DNI
If SR2.0 is installed, mount R521 and make R522 as DNI



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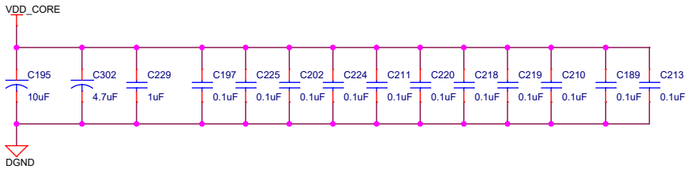
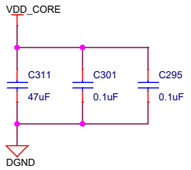
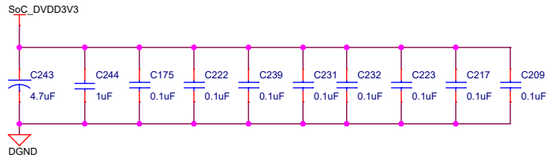
SOC POWER DECAPS



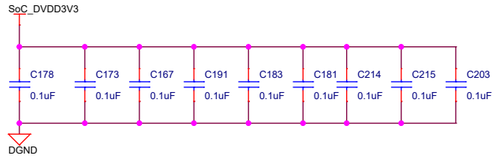
Place one 0.1uF cap near each Pin

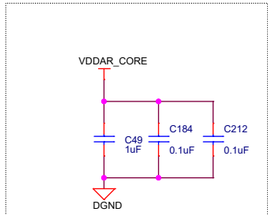


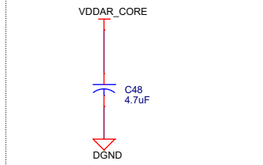
To place after current sense resitor on VDD_CORE plane

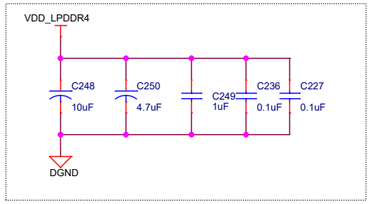


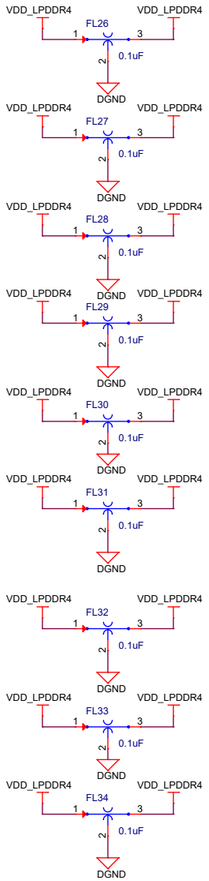
Place one 0.1uF cap near each Pin

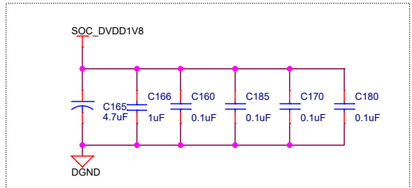


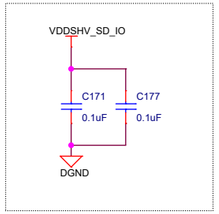








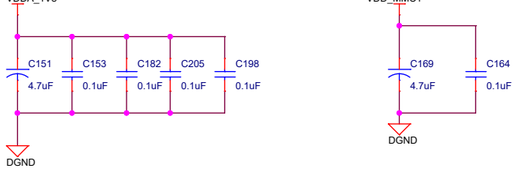




Place one 0.1uF cap near each Pin

VDD ARRAY CORE

VDDA_3P3_SDIO



Place one 0.1uF cap near each Pin

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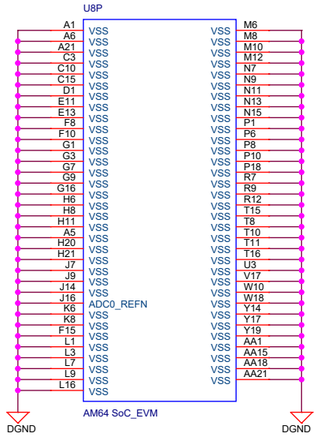
SOC POWER - VSS



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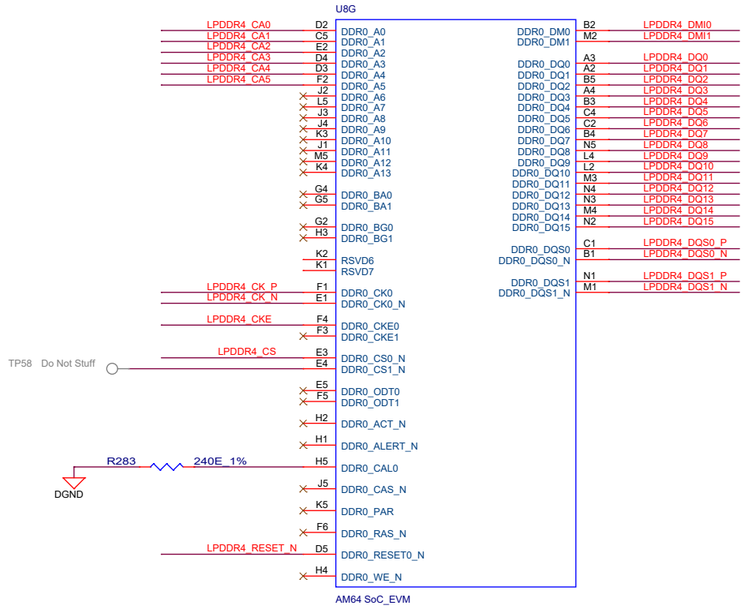
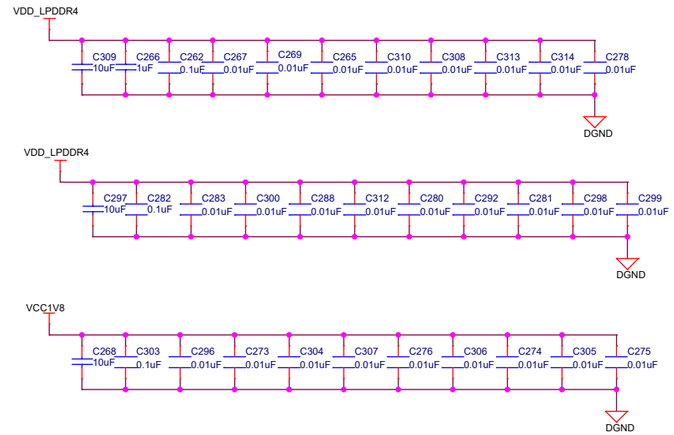
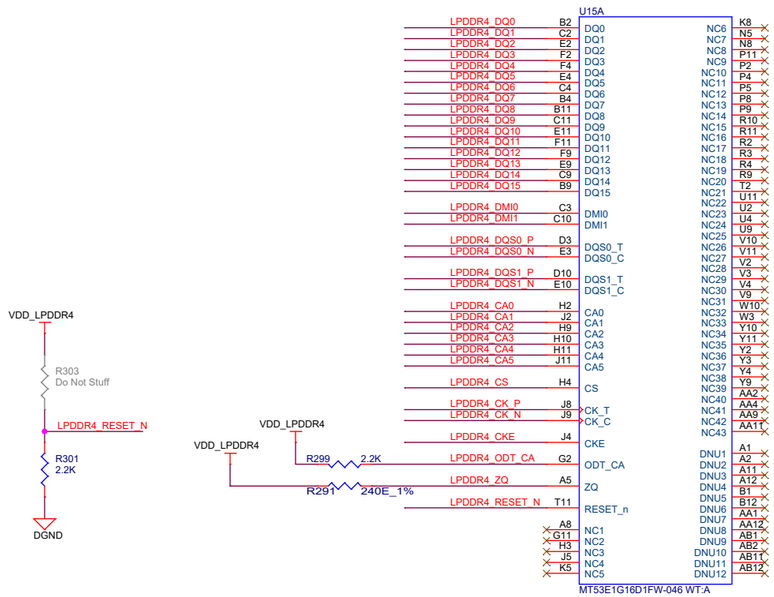
SOC LPDDR4 INTERFACE

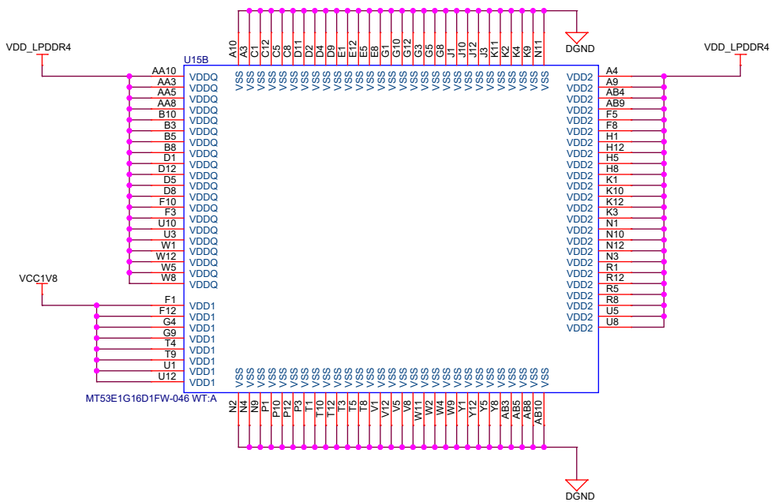


LPDDR4 POWER DECAPS



LPDDR4 DEVICE





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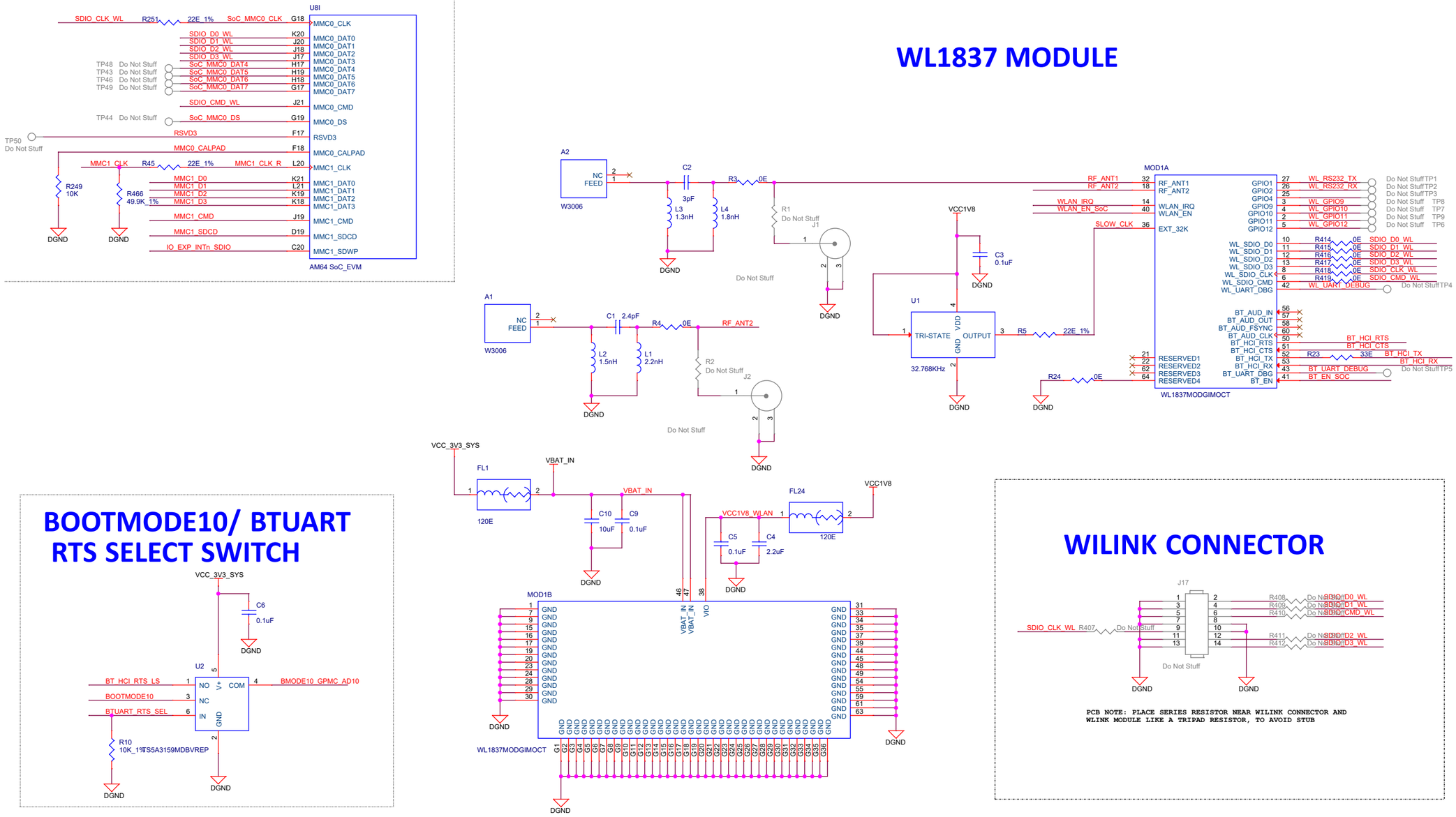
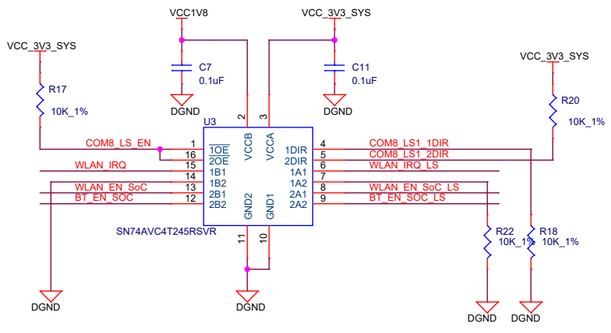
WL1837 MODULE



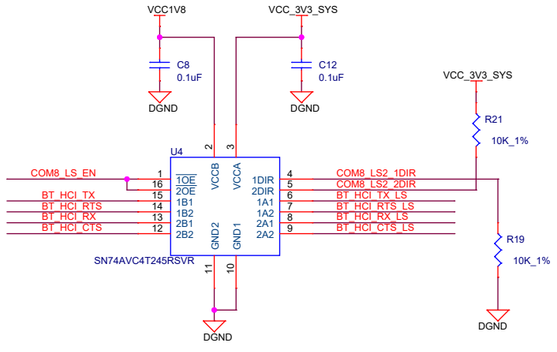
BOOTMODE10/ BTUART RTS SELECT SWITCH

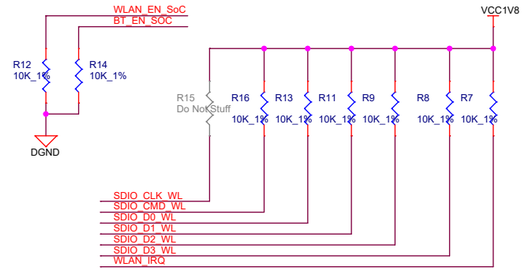
WILINK CONNECTOR

COM8 LEVEL TRANSLATOR-1



COM8 LEVEL TRANSLATOR-2





OFF PAGE CONNECTIONS

25	WLAN_IRQ_LS	WLAN_IRQ_LS	
25	WLAN_EN_SoC_LS	WLAN_EN_SoC_LS	
25	BT_EN_SOC_LS	BT_EN_SOC_LS	
31	BT_HCI_TX_LS	BT_HCI_TX_LS	
31	BT_HCI_RX_LS	BT_HCI_RX_LS	
26	BT_HCI_CTS_LS	BT_HCI_CTS_LS	
25	COM8_LS_EN	COM8_LS_EN	
36	IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO	
16	MMC1_D0	MMC1_D0	
16	MMC1_D1	MMC1_D1	
16	MMC1_D2	MMC1_D2	
14,16	**MMC1_D3**	MMC1_D3	
16	MMC1_CMD	MMC1_CMD	
16	MMC1_SDCD	MMC1_SDCD	
16	MMC1_CLK	MMC1_CLK	
26	BMODE10_GPMC_AD10	BMODE10_GPMC_AD10	
20	BOOTMODE10	BOOTMODE10	
25	BTUART_RTS_SEL	BTUART_RTS_SEL	

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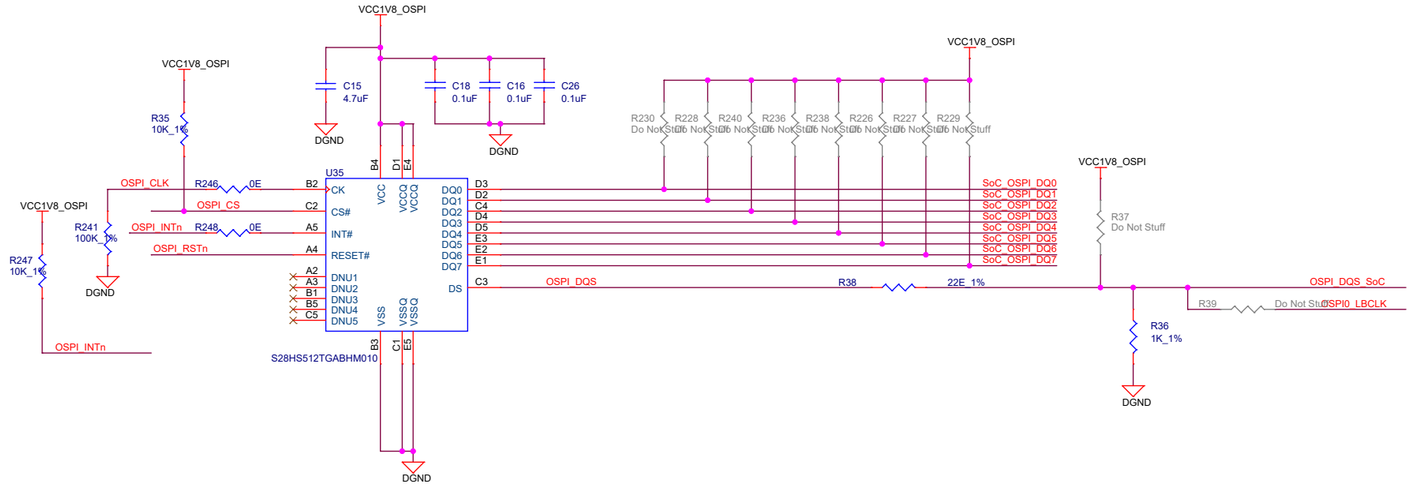
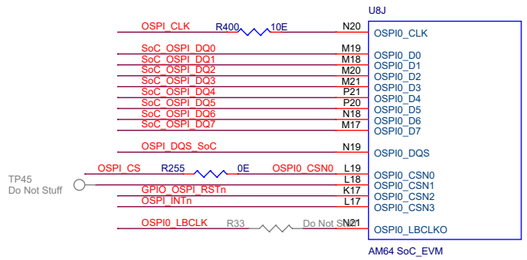
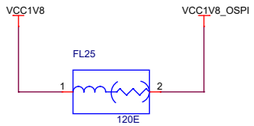
OSPI FLASH

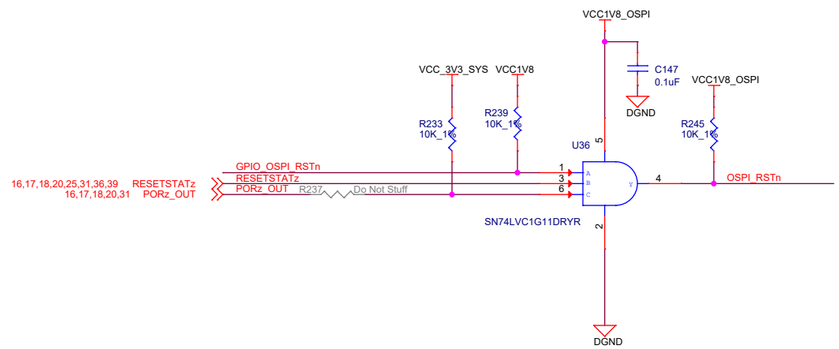


SOC OSPI INTERFACE





OSPI FLASH RESET



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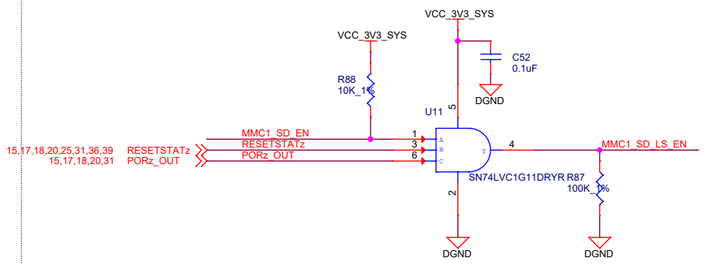
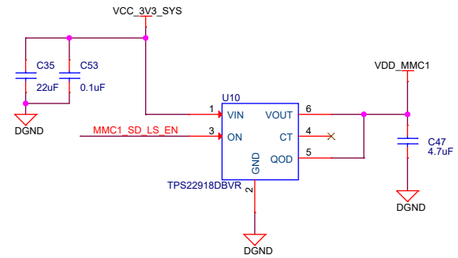
SD CARD INTERFACE

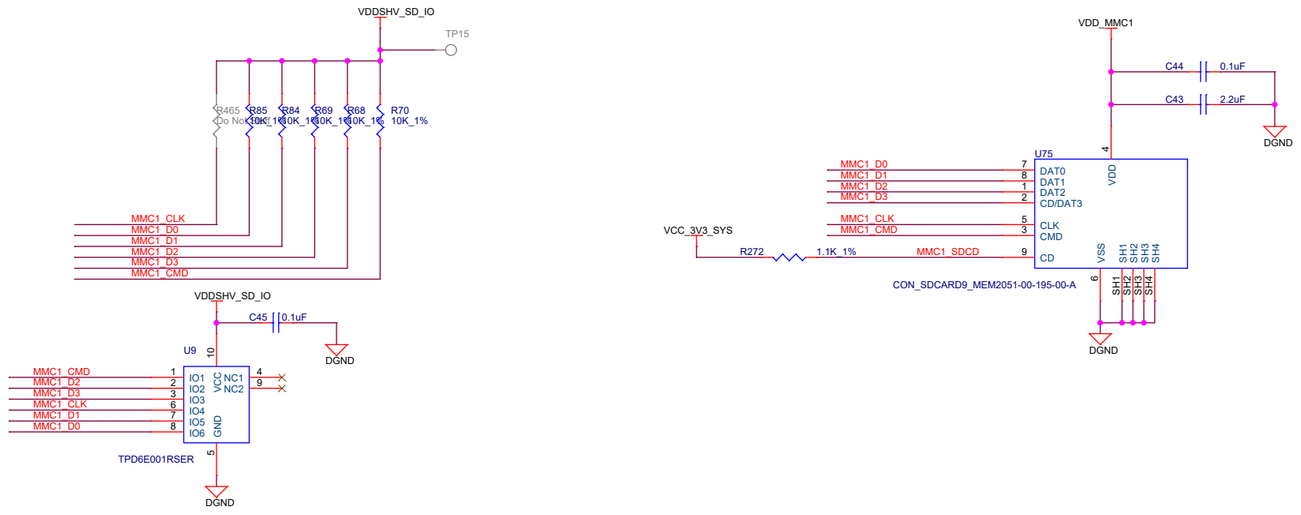
SD CARD RESET



POWER SWITCH



SD CARD CONNECTOR



OFF PAGE CONNECTIONS

14	MMC1_CLK	MMC1_CLK
36	MMC1_SD_EN	MMC1_SD_EN
14	MMC1_D0	MMC1_D0
14	MMC1_D1	MMC1_D1
14	MMC1_D2	MMC1_D2
14,16	MMC1_D3	MMC1_D3
14	MMC1_CMD	MMC1_CMD
14	MMC1_SDCD	MMC1_SDCD

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Title	SDCARD INTERFACE		
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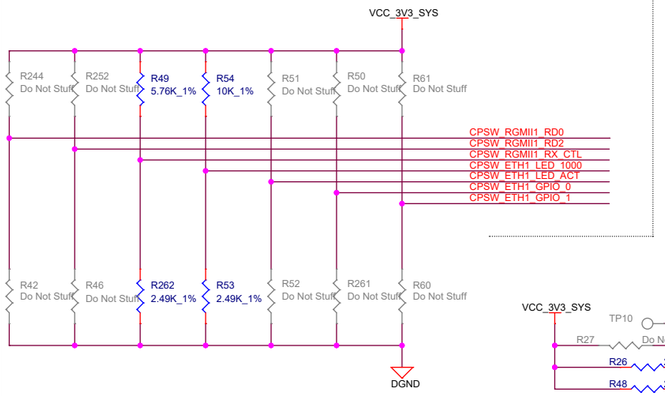
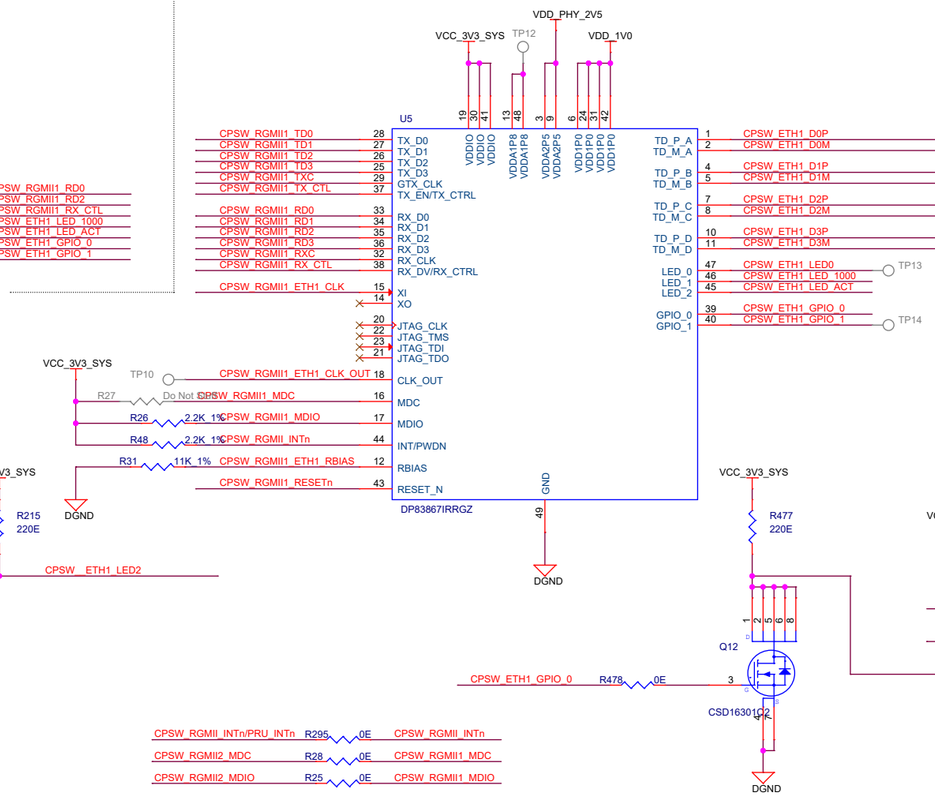
CPSW RGMII 1 - PHY

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

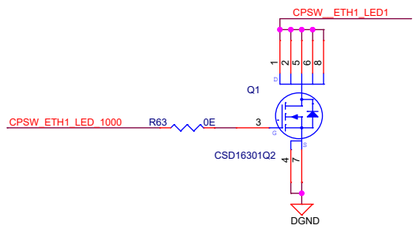
STRAPPING RESISTORS



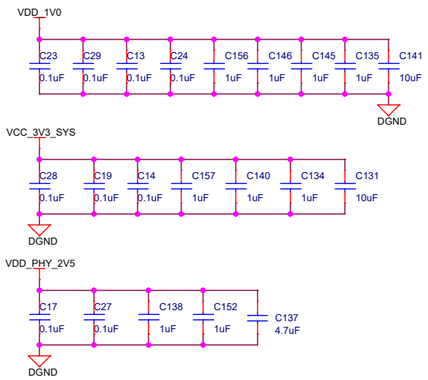
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
Refer 44 page for strap configuration



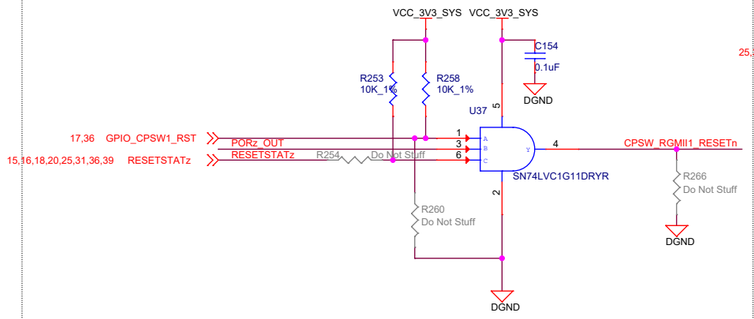
LED STATUS



DECAPS



CPSW PHY-1 RESET



OFF PAGE CONNECTIONS

25	CPSW_RGMII1_RD0	CPSW_RGMII1_RD0
25	CPSW_RGMII1_RD1	CPSW_RGMII1_RD1
25	CPSW_RGMII1_RD2	CPSW_RGMII1_RD2
25	CPSW_RGMII1_RD3	CPSW_RGMII1_RD3
25	CPSW_RGMII1_RXC	CPSW_RGMII1_RXC
25	CPSW_RGMII1_RX_CTL	CPSW_RGMII1_RX_CTL
25	CPSW_RGMII1_TD0	CPSW_RGMII1_TD0
25	CPSW_RGMII1_TD1	CPSW_RGMII1_TD1
25	CPSW_RGMII1_TD2	CPSW_RGMII1_TD2
25	CPSW_RGMII1_TD3	CPSW_RGMII1_TD3
25	CPSW_RGMII1_TX_CTL	CPSW_RGMII1_TX_CTL
25	CPSW_RGMII1_TXC	CPSW_RGMII1_TXC
15,16,18,20,31	PORz_OUT	PORz_OUT
25,31,39	CPSW_RGMII_INTn/PRU_INTn	CPSW_RGMII_INTn/PRU_INTn
17,36	GPIO_CPSW1_RST	GPIO_CPSW1_RST
29	CPSW_RGMII1_ETH1_CLK	CPSW_RGMII1_ETH1_CLK
18,25	CPSW_RGMII2_MDC	CPSW_RGMII2_MDC
18,25	CPSW_RGMII2_MDIO	CPSW_RGMII2_MDIO
18	CPSW_RGMII_INTn	CPSW_RGMII_INTn

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Title	CPSW RGMII_1 ETHERNET PHY		
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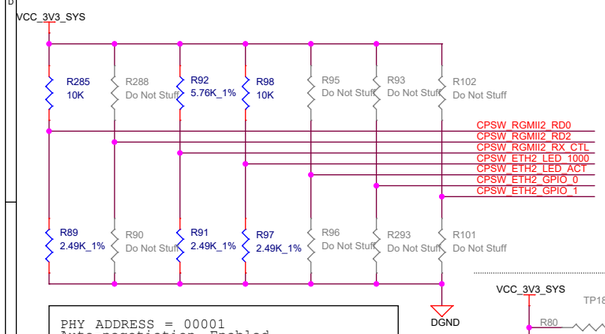
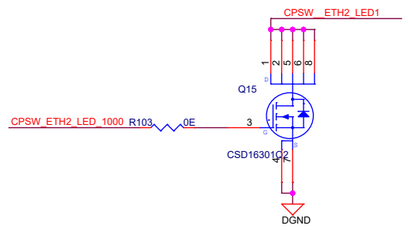
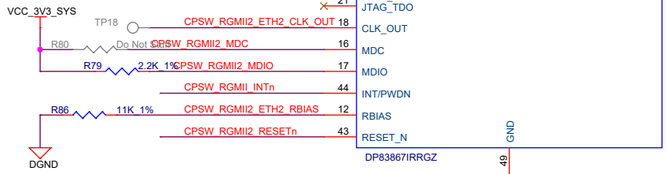
CPSW RGMII 2 - PHY

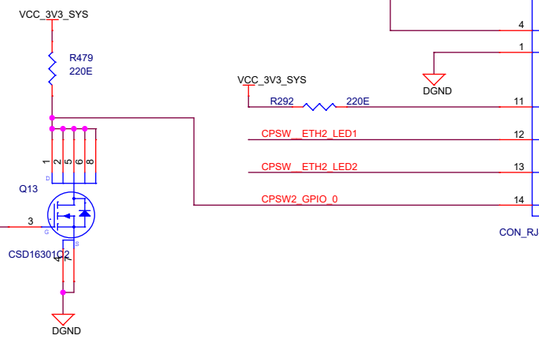
STRAPPING RESISTORS



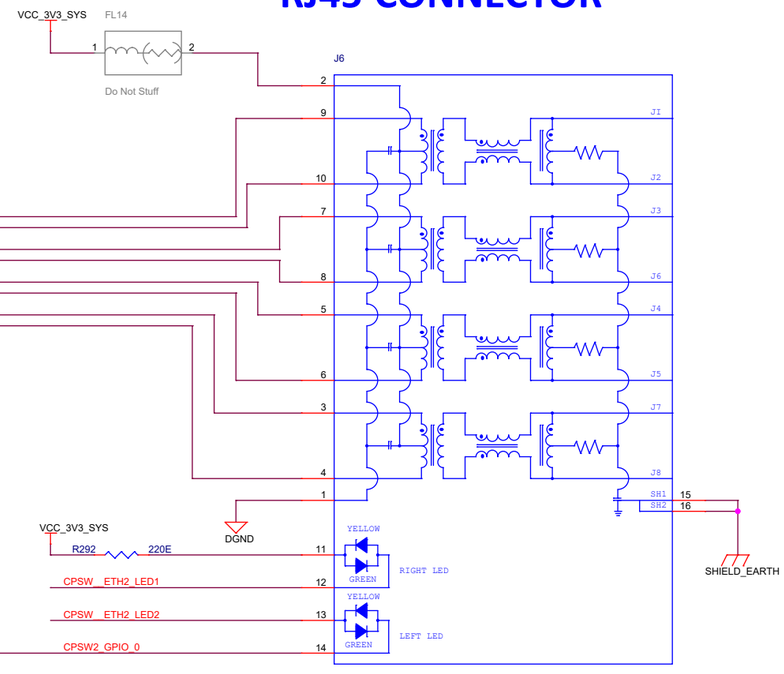
PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
Refer 44 page for strap configuration



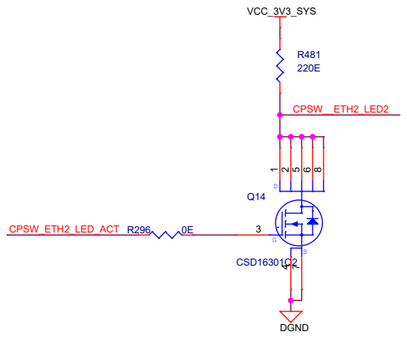




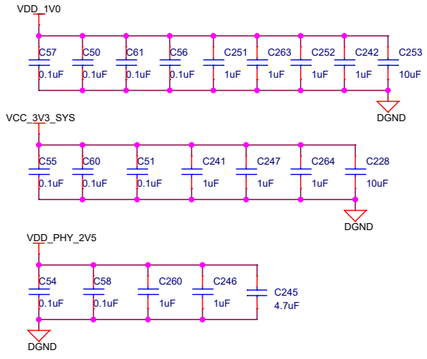
RJ45 CONNECTOR



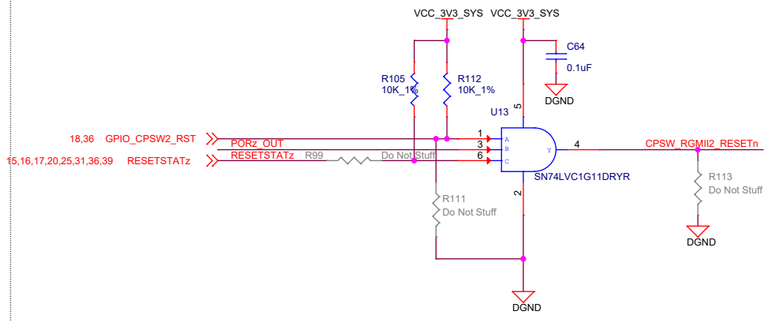
CPSW PHY-2 SPEED AND ACTIVITY LED's DRIVERS



DECAPS



CPSW PHY-2 RESET



OFF PAGE CONNECTIONS

25	CPSW_RGMII2_RD0	CPSW_RGMII2_RD0
25	CPSW_RGMII2_RD1	CPSW_RGMII2_RD1
25	CPSW_RGMII2_RD2	CPSW_RGMII2_RD2
25	CPSW_RGMII2_RD3	CPSW_RGMII2_RD3
25	CPSW_RGMII2_RXC	CPSW_RGMII2_RXC
25	CPSW_RGMII2_RX_CTL	CPSW_RGMII2_RX_CTL
25	CPSW_RGMII2_TD0	CPSW_RGMII2_TD0
25	CPSW_RGMII2_TD1	CPSW_RGMII2_TD1
25	CPSW_RGMII2_TD2	CPSW_RGMII2_TD2
25	CPSW_RGMII2_TD3	CPSW_RGMII2_TD3
25	CPSW_RGMII2_TXC	CPSW_RGMII2_TXC
25	CPSW_RGMII2_TX_CTL	CPSW_RGMII2_TX_CTL
		PORz_OUT
15,16,17,20,31	PORz_OUT	GPIO_CPSW2_RST
18,36	GPIO_CPSW2_RST	CPSW_RGMII2_ETH2_CLK
29	CPSW_RGMII2_ETH2_CLK	CPSW_RGMII2_MDC
17,25	CPSW_RGMII2_MDC	CPSW_RGMII2_MDIO
17,25	CPSW_RGMII2_MDIO	CPSW_RGMII_INTn
17	CPSW_RGMII_INTn	

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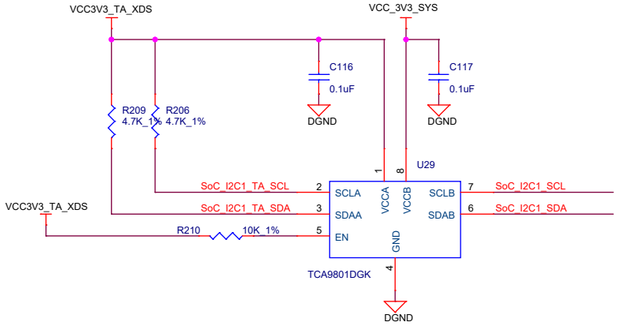
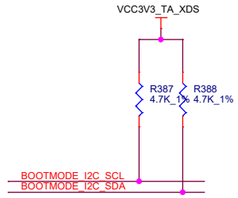
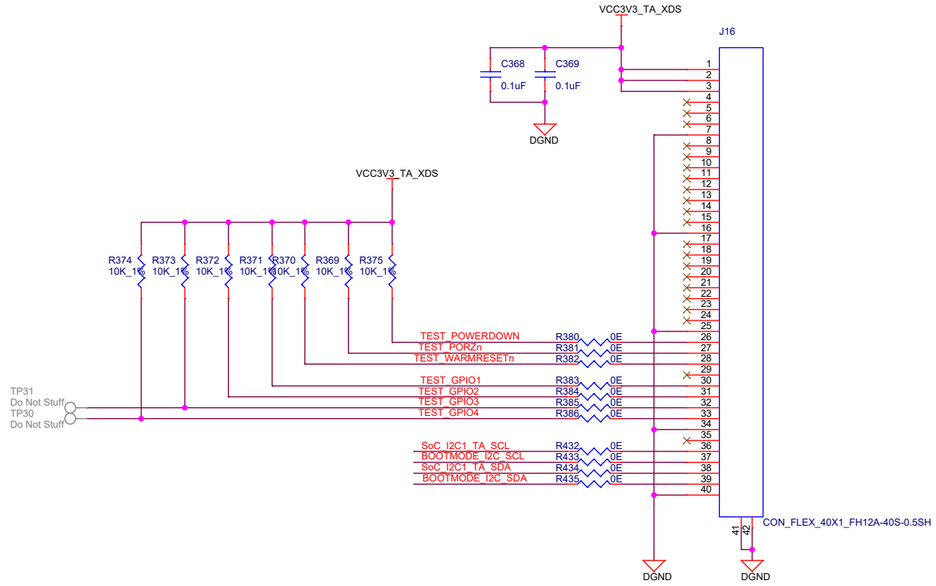
I2C BUS BUFFER

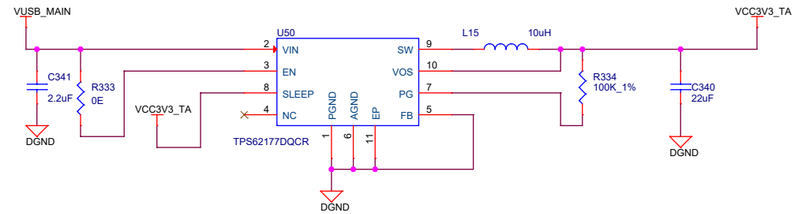




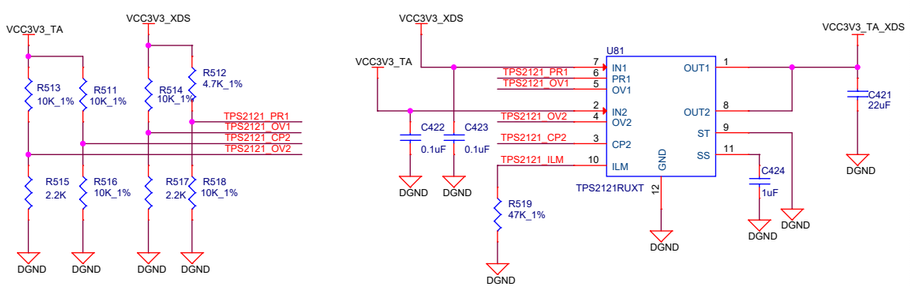
40-PIN AUTOMATION HEADER



TEST AUTOMATION BOARD POWER



POWER MUX



Note: When IN1 drops below 2.425V, then IN2 is used.
Over voltage protection: OV1 & OV2 : 5.878V

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO1_59_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to SoC GPIO to Communicate	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Design	Specifications
VPR1	2.2V
VCP2	1.65V
VOV1	0.3V
VOV2	0.3V

OFF PAGE CONNECTIONS

30,31,34,36 SoC_I2C1_SCL	SoC_I2C1_SCL
30,31,34,36 SoC_I2C1_SDA	SoC_I2C1_SDA
20,21 BOOTMODE_I2C_SCL	BOOTMODE_I2C_SCL
20,21 BOOTMODE_I2C_SDA	BOOTMODE_I2C_SDA
21,32 TEST_PORZn	TEST_PORZn
21,39 TEST_POWERDOWN	TEST_POWERDOWN
21,32 TEST_WARMRESETn	TEST_WARMRESETn
21 TEST_GPIO2	TEST_GPIO2
20,21 TEST_GPIO3	TEST_GPIO3
20,21 TEST_GPIO4	TEST_GPIO4
21,32 TEST_GPIO1	TEST_GPIO1
21 SoC_I2C1_TA_SDA	SoC_I2C1_TA_SDA
21 SoC_I2C1_TA_SCL	SoC_I2C1_TA_SCL

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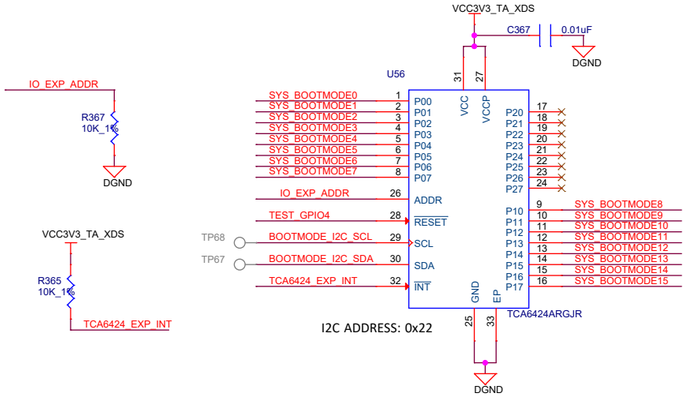
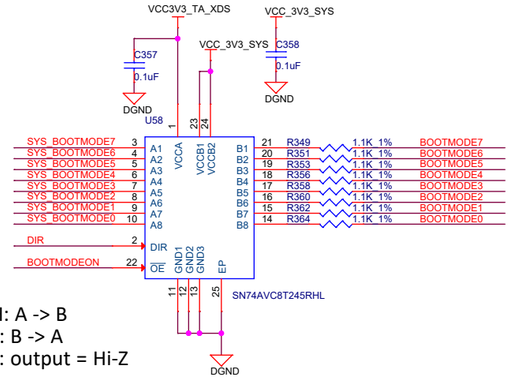
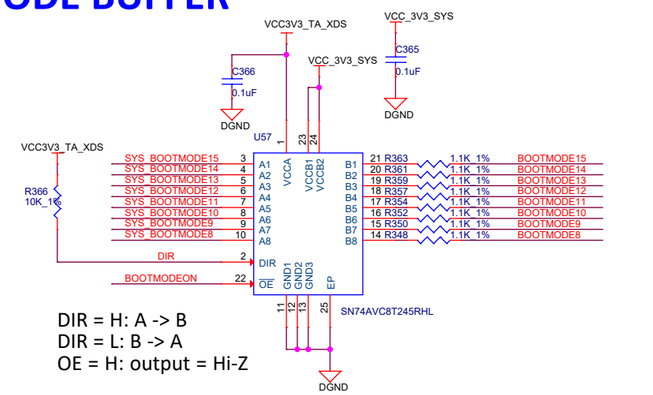
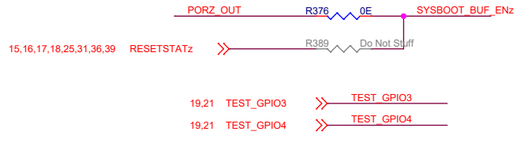
IO EXPANDER

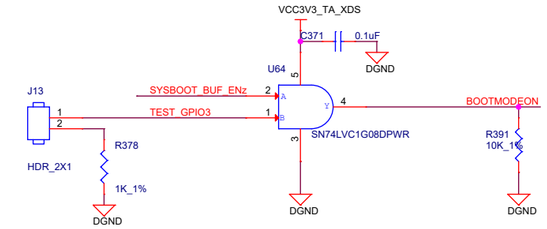


BOOT MODE BUFFER







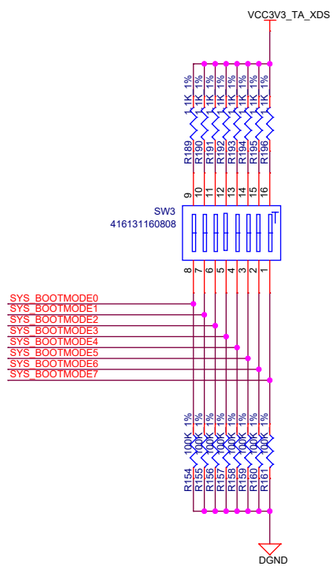


BOOT MODES SUPPORTED

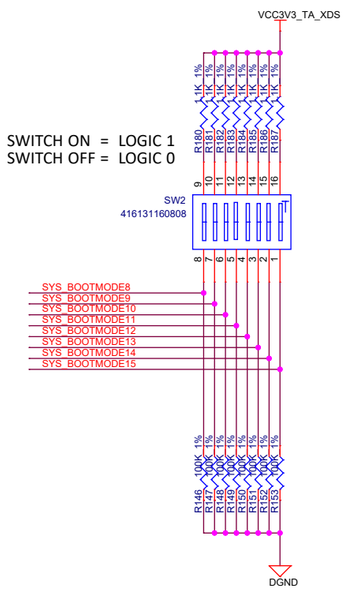
1. OSPI
2. MMC1 - SD CARD
3. CPSW Ethernet
4. USB Device
5. Ethernet

MCU Boot Mode Pins to be Finalized

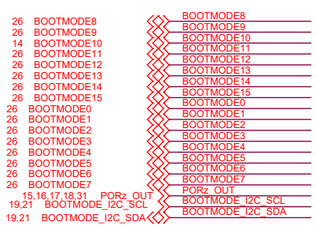
BOOT MODE SWITCHES



SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0



OFF PAGE CONNECTIONS



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Title	BOOT MODE BUFFER & SWITCHES		
Size	PROC100A 002		Rev
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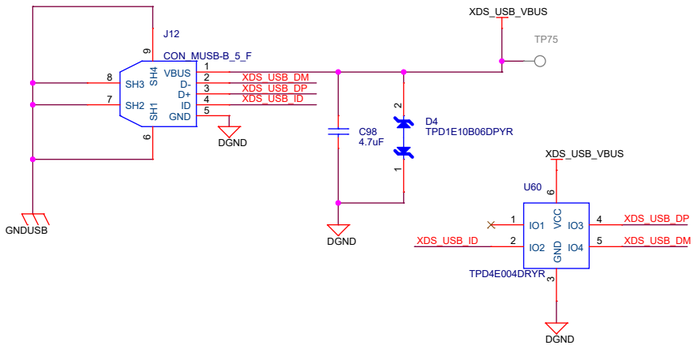
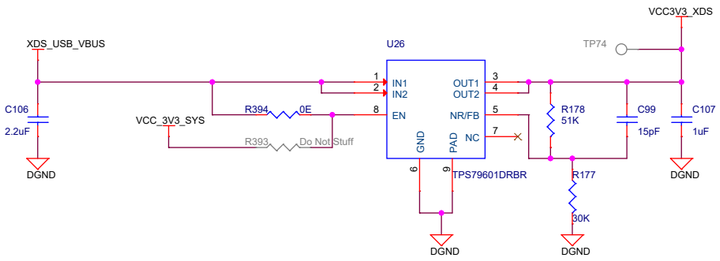
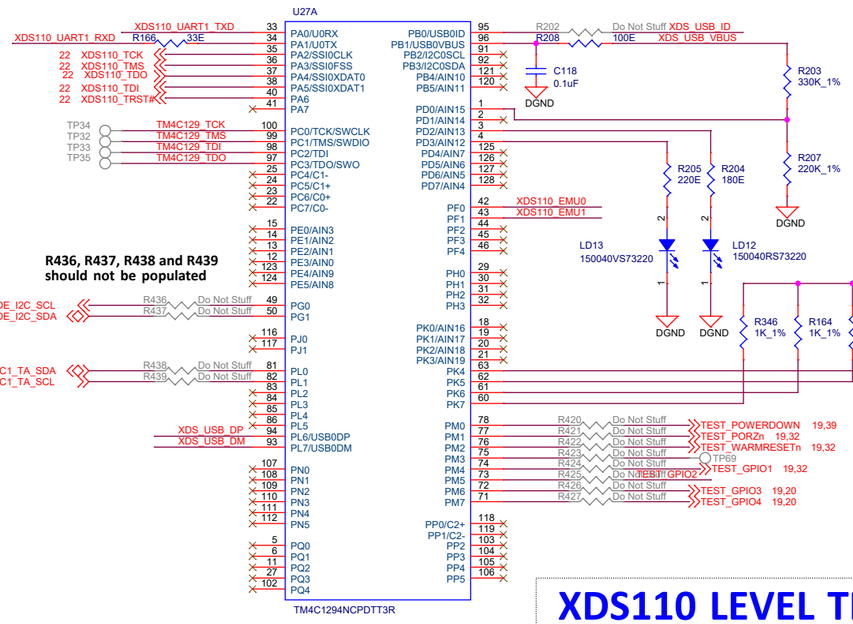
XDS110 POWER

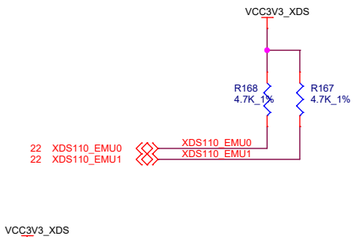
USB Connector

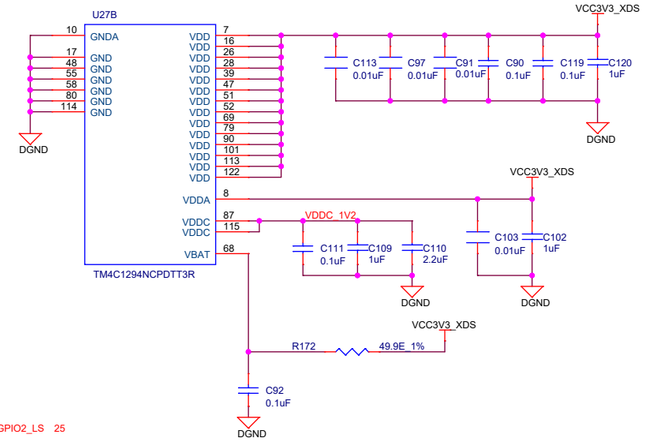


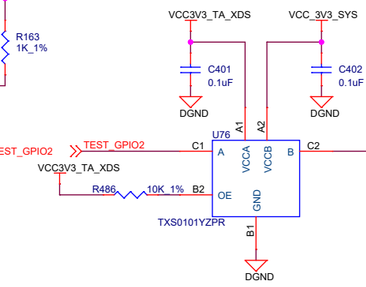


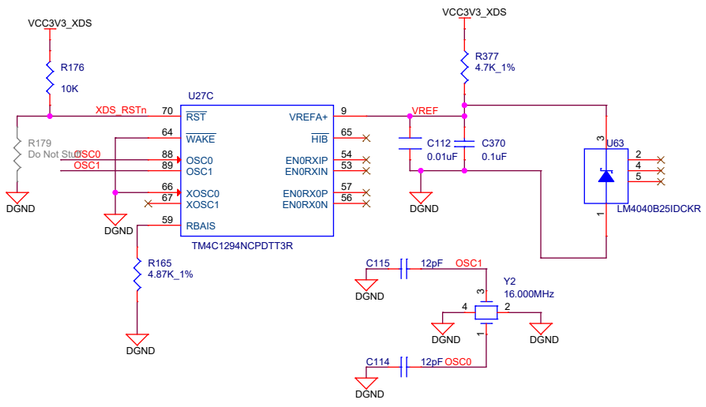
XDS110 DEBUGGER



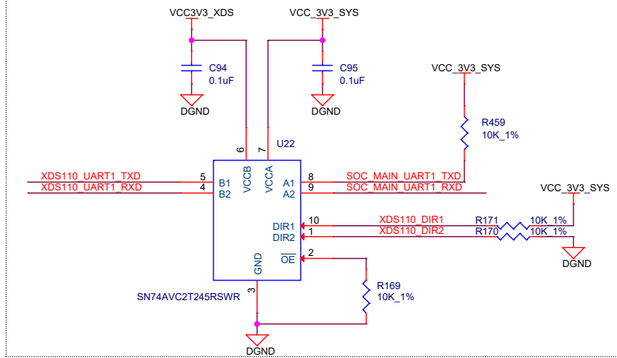








XDS110 LEVEL TRANSLATOR



OFF PAGE CONNECTIONS

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Title	XDS110 DEBUGGER	
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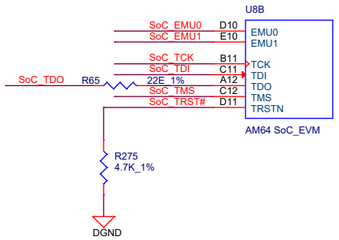
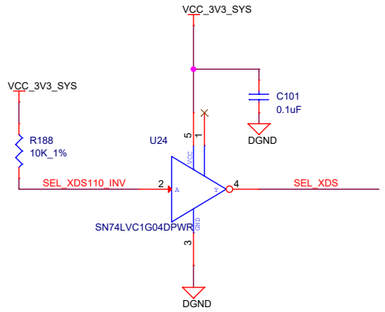
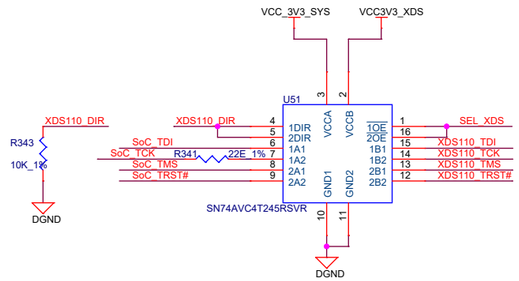
JTAG SoC SECTION

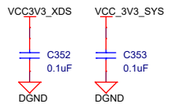


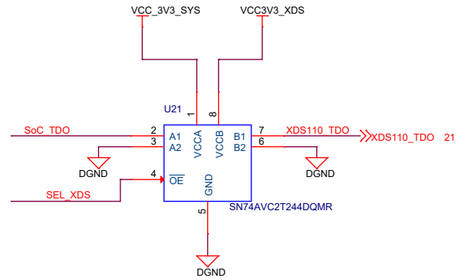
INVERTER

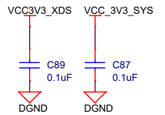


BUFFER XDS110









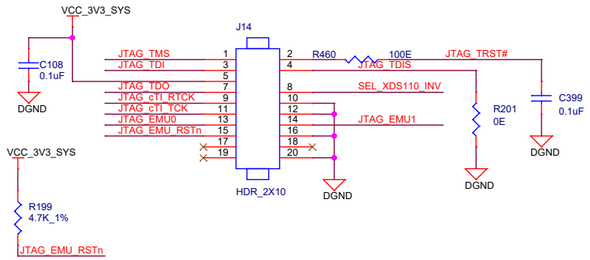
OFF PAGE CONNECTIONS

23 SEL_XDS110_INV	SEL_XDS110_INV
21 XDS110_TDI	XDS110_TDI
21 XDS110_TCK	XDS110_TCK
21 XDS110_TMS	XDS110_TMS
21 XDS110_TRST#	XDS110_TRST#
23 SoC_TDO	SoC_TDO
23 SoC_TDI	SoC_TDI
23 SoC_TCK	SoC_TCK
23 SoC_TMS	SoC_TMS
21 XDS110_EMU0	XDS110_EMU0
21 XDS110_EMU1	XDS110_EMU1
23 SEL_XDS	SEL_XDS
23 SoC_EMU0	SoC_EMU0
23 SoC_EMU1	SoC_EMU1
23 SoC_TRST#	SoC_TRST#

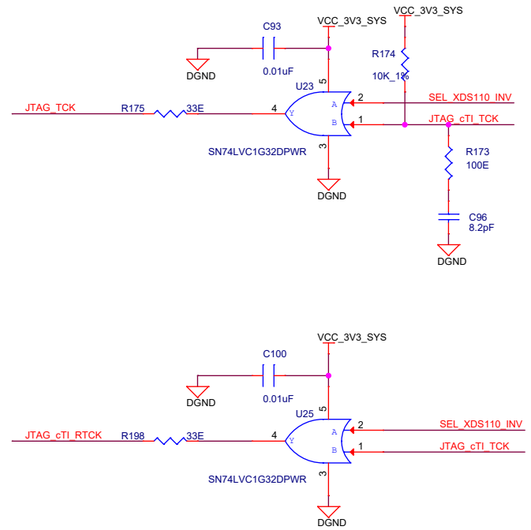
Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG BUFFER	
Size C	PROC100A 002	Rev A
Date: Thursday, September 15, 2022	Sheet 22 of 43	

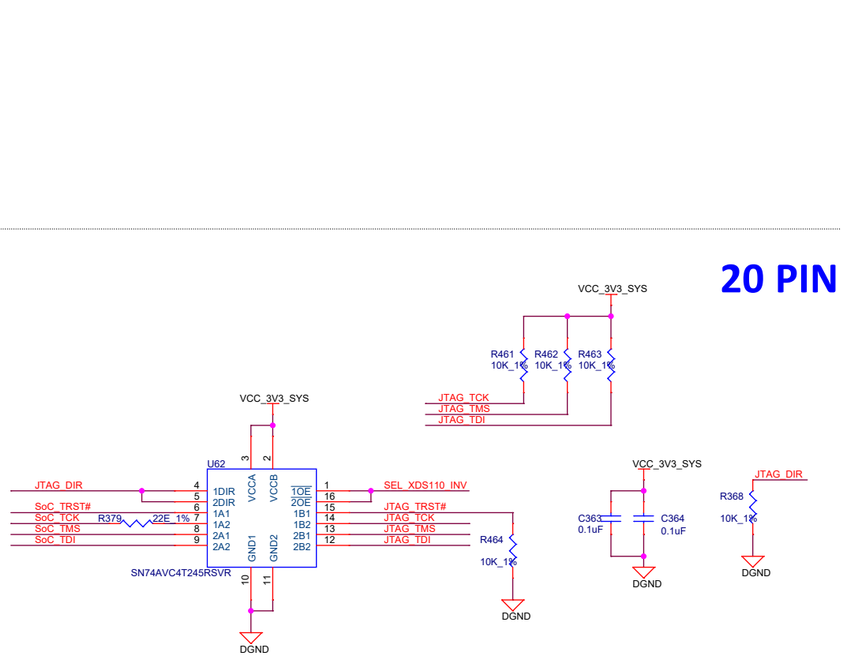
JTAG 20 PIN cTI CONNECTOR



JTAG CLOCK BUFFER



20 PIN JTAG BUFFERS



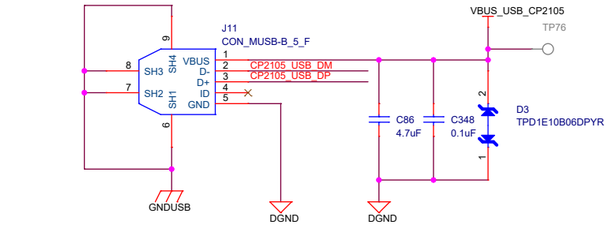
OFF PAGE CONNECTIONS

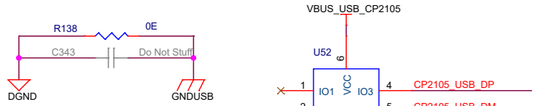
22	SEL_XDS110_INV	SEL_XDS110_INV
22	SoC_TDO	SoC_TDO
22	SoC_TDI	SoC_TDI
22	SoC_TCK	SoC_TCK
22	SoC_TMS	SoC_TMS
22	SoC_TRST#	SoC_TRST#
32	JTAG_EMU_RSTn	JTAG_EMU_RSTn
22	SEL_XDS	SEL_XDS
22	SoC_EMU0	SoC_EMU0
22	SoC_EMU1	SoC_EMU1

Designed for TI by Mistral Solutions Pvt Ltd

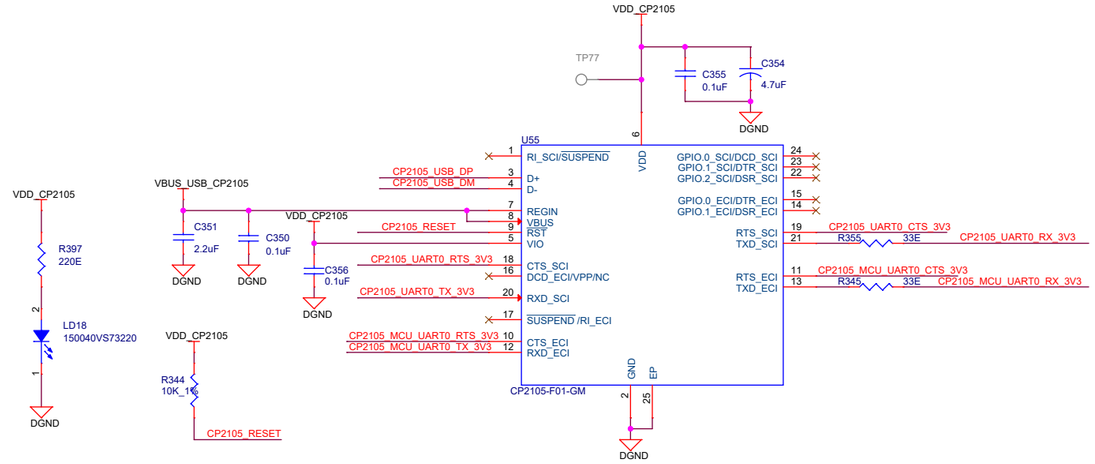
Title	JTAG 20 PIN cTI CONNECTOR		
Size	PROC100A 002		Rev
C			A
Date:	Thursday, September 15, 2022	Sheet 23 of 43	

USB Micro B CONNECTOR

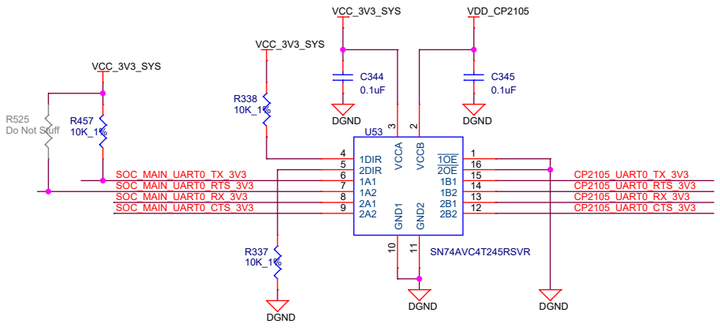


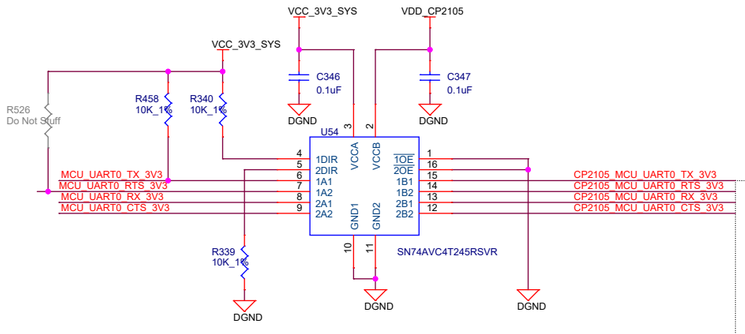


USB TO DUAL UART BRIDGE



CP2105 LEVEL TRANSLATOR





OFF PAGE CONNECTIONS

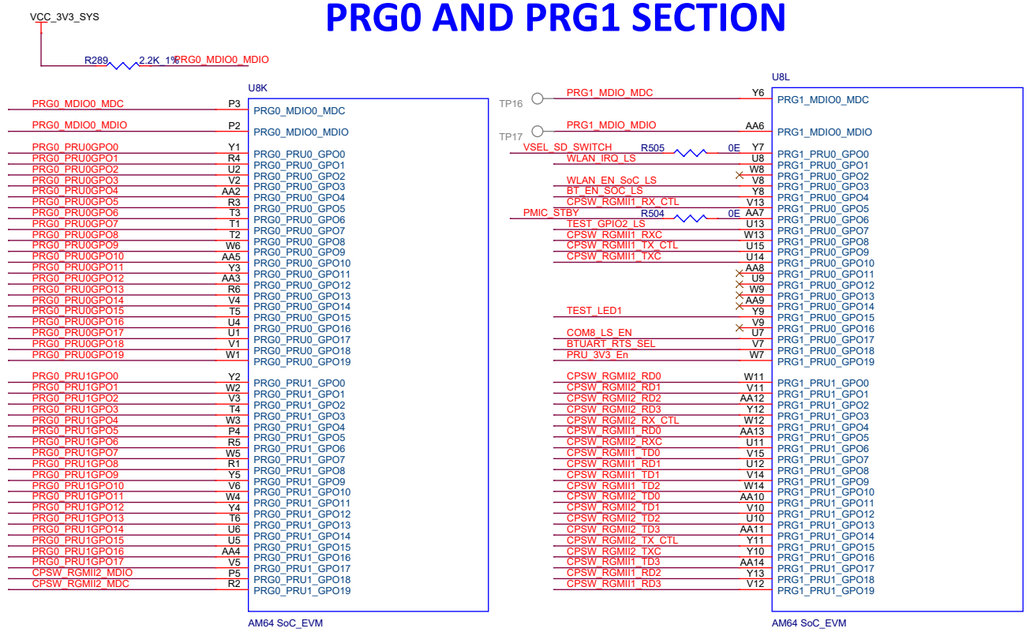
SOC_MAIN_UART0_RX_3V3 → SOC_MAIN_UART0_RX_3V3 31
SOC_MAIN_UART0_TX_3V3 → SOC_MAIN_UART0_TX_3V3 31
SOC_MAIN_UART0_RTS_3V3 → SOC_MAIN_UART0_RTS_3V3 31
SOC_MAIN_UART0_CTS_3V3 → SOC_MAIN_UART0_CTS_3V3 31

MCU_UART0_RX_3V3 → MCU_UART0_RX_3V3 31
MCU_UART0_TX_3V3 → MCU_UART0_TX_3V3 31
MCU_UART0_RTS_3V3 → MCU_UART0_RTS_3V3 31
MCU_UART0_CTS_3V3 → MCU_UART0_CTS_3V3 31

Designed for TI by Mistral Solutions Pvt Ltd

Title	CP2105 UART TO USB BRIDGE	
Size: C	PROC100A 002	Rev: A
Date: Thursday, September 15, 2022	Sheet 24 of 43	

PRG0 AND PRG1 SECTION



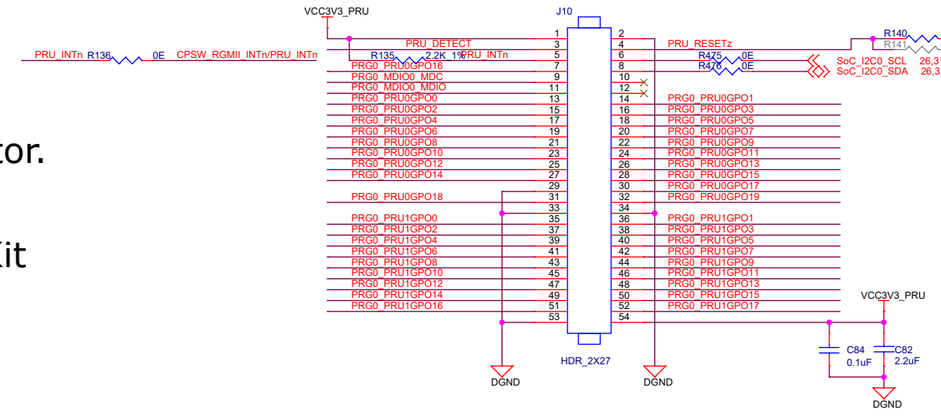
PRU CONNECTOR

NOTE:

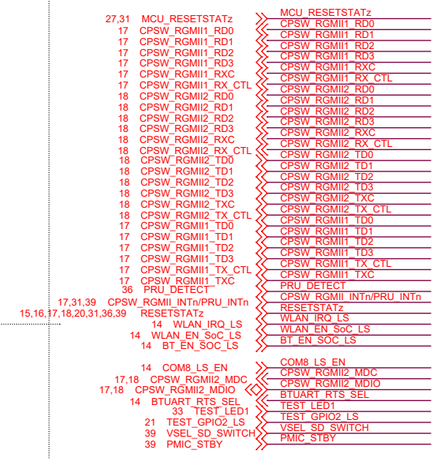
AM64x Starter Kit shall not be powered through the 3V3 pins on the PRU Connector.

PRU Connector I/O are not fail-safe and shall not be driven when AM64x Starter Kit is not powered.

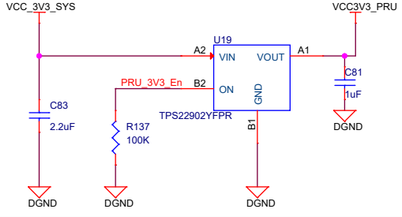
3V3 supply of User Expansion Connector is limited to sourcing 500mA max.



OFF PAGE CONNECTIONS



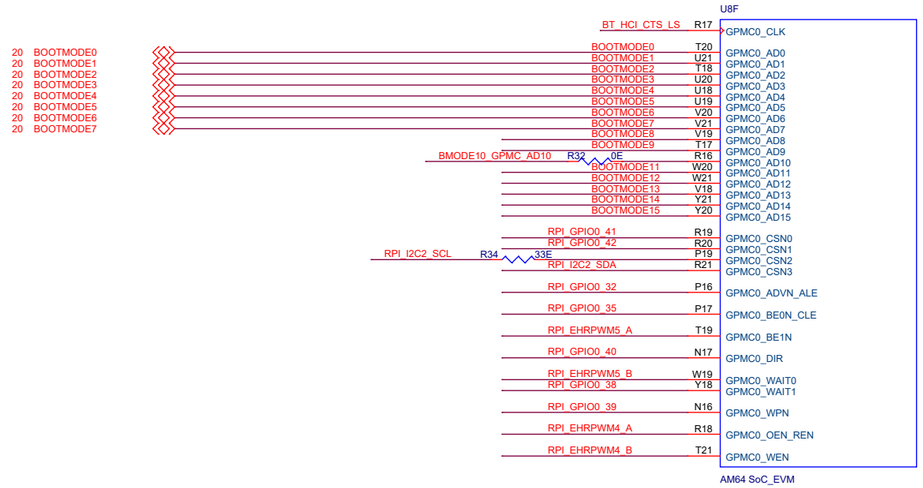
POWER SWITCH FOR 3.3V TO PRU CONNECTOR



Designed for TI by Mistral Solutions Pvt Ltd

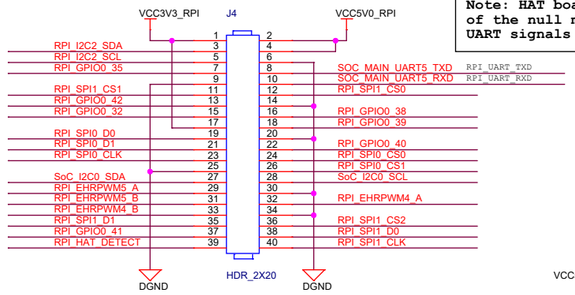
Title	PRU CONNECTOR	
Size C	PROC100A 002	Rev A
Date: Thursday, September 15, 2022	Sheet 25 of 43	

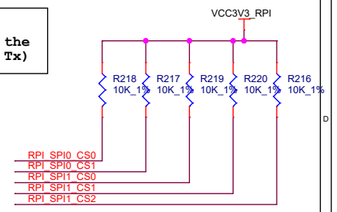
GPMC SECTION

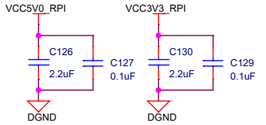


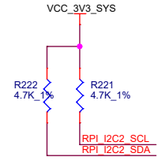
USER EXPANSION CONNECTOR

Note: HAT boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)





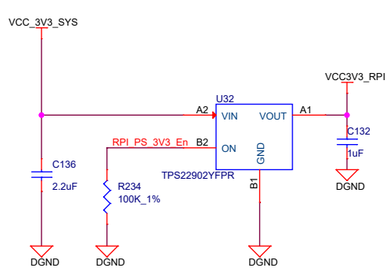


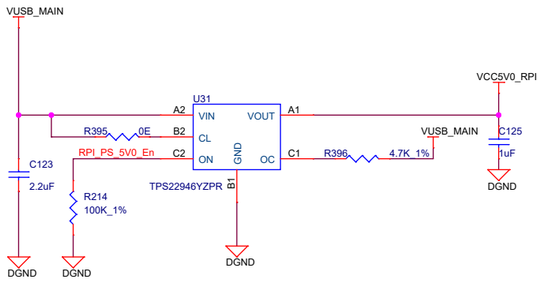


Note: This connector is compatible to GPIO Expansion Header (J8) found on the Raspberry Pi Boards

Note: Raspberry Pi is the trademark / wordmark of Raspberry Pi Foundation

POWER SWITCH FOR USER EXPANSION CONNECTOR





NOTE:

AM64x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM64x Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

OFF PAGE CONNECTIONS

RPI_HAT_DETECT	RPI_HAT_DETECT 36
RPI_SPI1_CLK	RPI_SPI1_CLK 31
RPI_SPI1_D0	RPI_SPI1_D0 31
RPI_SPI1_D1	RPI_SPI1_D1 31
RPI_SPI1_CS0	RPI_SPI1_CS0 31
RPI_SPI1_CS1	RPI_SPI1_CS1 31
RPI_SPI1_CS2	RPI_SPI1_CS2 31
RPI_SPI0_CLK	RPI_SPI0_CLK 31
RPI_SPI0_D0	RPI_SPI0_D0 31
RPI_SPI0_D1	RPI_SPI0_D1 31
RPI_SPI0_CS0	RPI_SPI0_CS0 31
RPI_SPI0_CS1	RPI_SPI0_CS1 31
SoC_I2C0_SCL	SoC_I2C0_SCL 25,31,35,39
SoC_I2C0_SDA	SoC_I2C0_SDA 25,31,35,39
BT_HCI_CTS_LS	BT_HCI_CTS_LS 14
BOOTMODE8	BOOTMODE8 20
BOOTMODE9	BOOTMODE9 20
BOOTMODE11	BOOTMODE11 20
BOOTMODE12	BOOTMODE12 20
BOOTMODE13	BOOTMODE13 20
BOOTMODE14	BOOTMODE14 20
BOOTMODE15	BOOTMODE15 20
SOC_MAIN_UART5_RXD	SOC_MAIN_UART5_RXD 31
SOC_MAIN_UART5_TXD	SOC_MAIN_UART5_TXD 31
RPI_PS_3V3_En	RPI_PS_3V3_En 36
RPI_PS_5V0_En	RPI_PS_5V0_En 36
BMODE10_GPMC_AD10	BMODE10_GPMC_AD10 14

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Title	USER EXPANSION CONNECTOR	
Size C	PROC100A 002	Rev A
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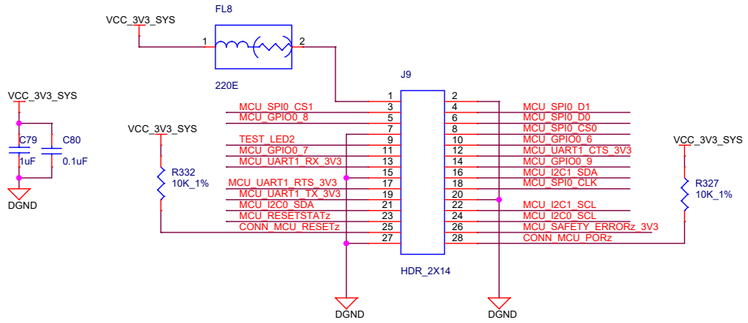
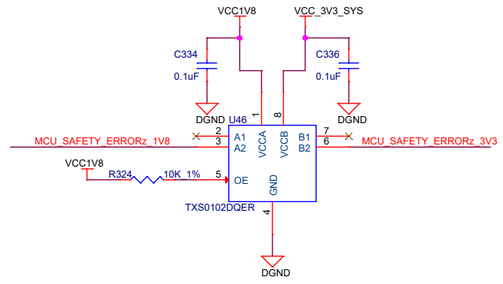
MCU CONNECTOR

Only 100mA supported on this pin



LEVEL TRANSLATOR



OFF PAGE CONNECTIONS

32	CONN_MCU_RESETz	CONN_MCU_RESETz
32	CONN_MCU_PORz	CONN_MCU_PORz
31	MCU_SPI0_CS1	MCU_SPI0_CS1
31	MCU_GPIO0_8	MCU_GPIO0_8
31,33	TEST_LED2	TEST_LED2
31	MCU_GPIO0_7	MCU_GPIO0_7
31	MCU_UART1_RX_3V3	MCU_UART1_RX_3V3
31	MCU_UART1_RTS_3V3	MCU_UART1_RTS_3V3
31	MCU_UART1_TX_3V3	MCU_UART1_TX_3V3
31	MCU_I2C0_SDA	MCU_I2C0_SDA
25,31	MCU_RESETSTATz	MCU_RESETSTATz
31	MCU_SPI0_D1	MCU_SPI0_D1
31	MCU_SPI0_D0	MCU_SPI0_D0
31	MCU_SPI0_CS0	MCU_SPI0_CS0
31,32	MCU_GPIO0_6	MCU_GPIO0_6
31	MCU_UART1_CTS_3V3	MCU_UART1_CTS_3V3
31	MCU_GPIO0_9	MCU_GPIO0_9
31	MCU_I2C1_SDA	MCU_I2C1_SDA
31	MCU_SPI0_CLK	MCU_SPI0_CLK
31	MCU_I2C1_SCL	MCU_I2C1_SCL
31	MCU_I2C0_SCL	MCU_I2C0_SCL
31	MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8

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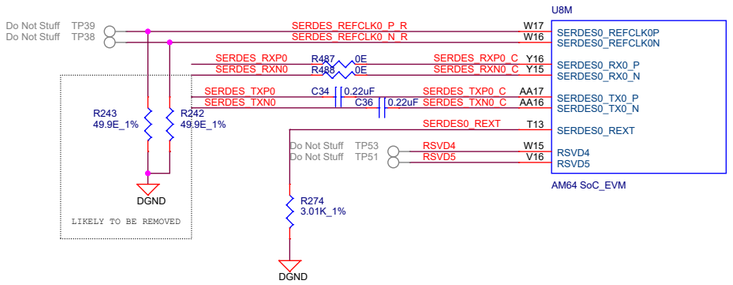
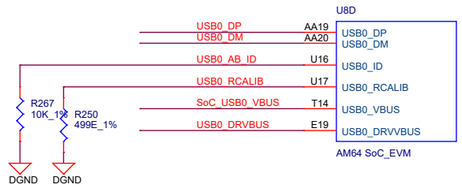
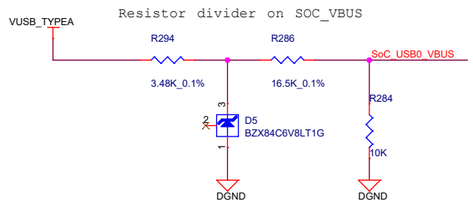
Title	MCU CONNECTOR	
Size C	PROC100A 002	Rev A
Date: Thursday, September 15, 2022	Sheet 27 of 43	

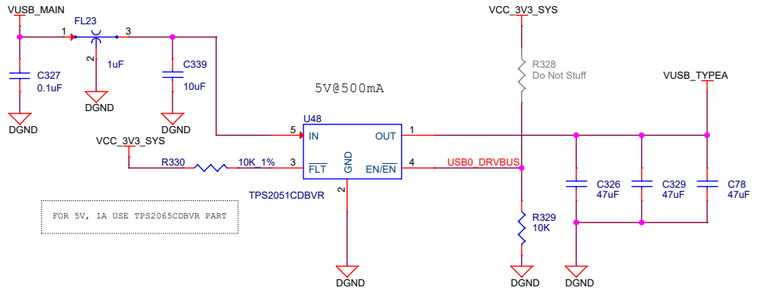
USB 3.0 INTERFACE



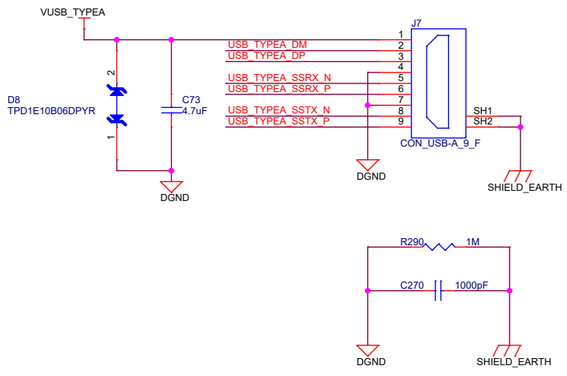




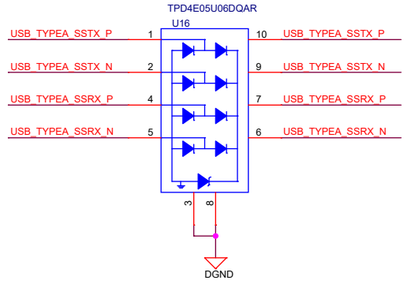
5V Power switch for USB 3.0 Device

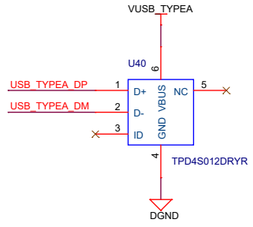


Type-A Connector

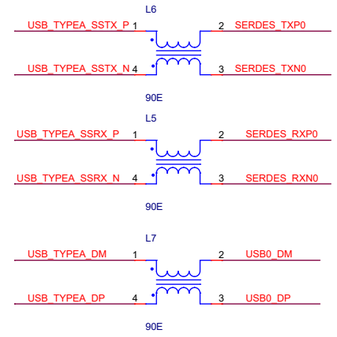


ESD DIODES





CHOKE



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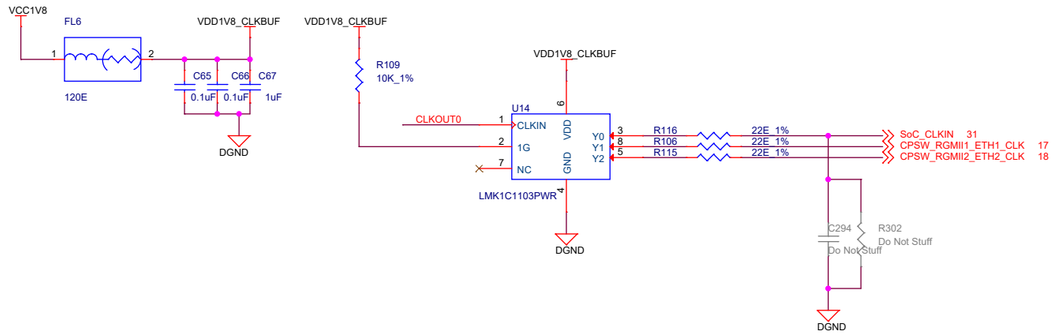
Title	USB 3.0 INTERFACE		
Size	PROC100A 002		Rev
C			A
Date:	Thursday, September 15, 2022	Sheet 28 of 43	

ETHERNET PHY CLOCK BUFFER



OFF PAGE CONNECTIONS

31,37 CLKOUT0 <<< CLKOUT0

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Title	ETHERNET PHY CLOCK BUFFER	
Size	PROC100A 002	Rev
C		A
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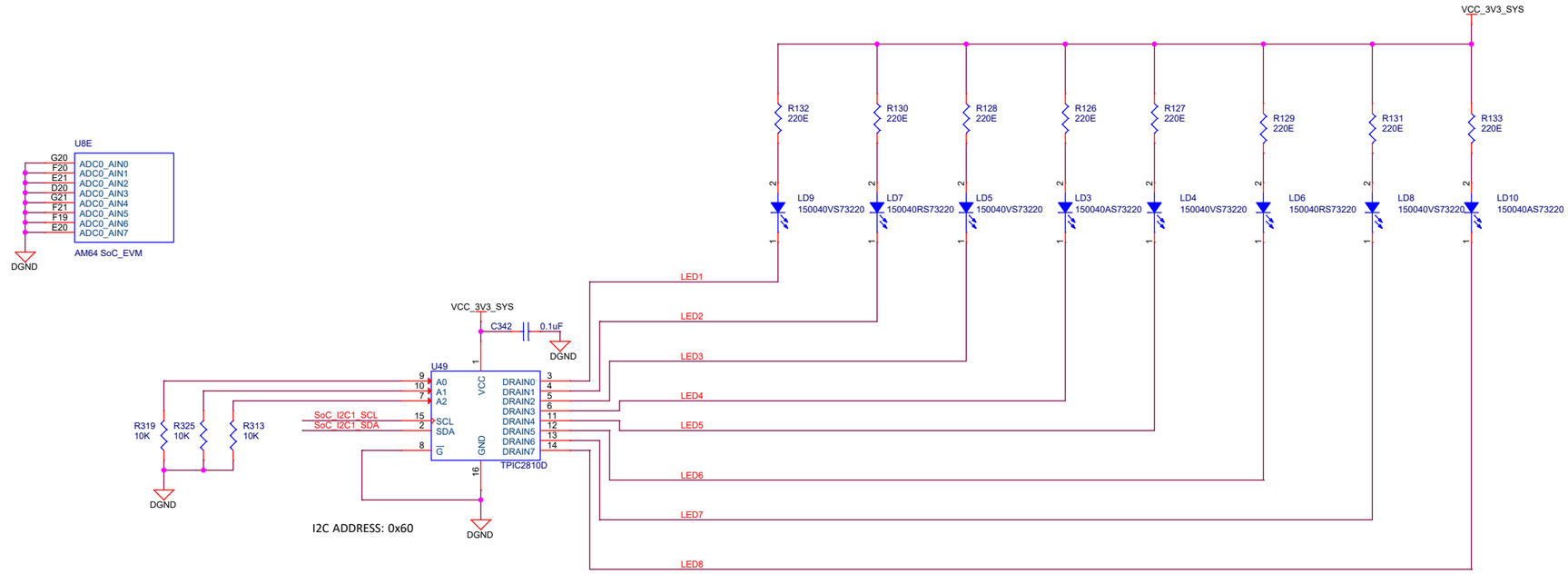
INDUSTRIAL COMMUNICATION LED's



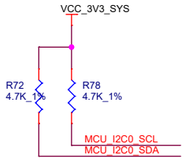
OFF PAGE CONNECTIONS

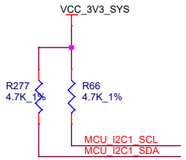
SoC_I2C1_SCL — SoC_I2C1_SCL 19,31,34,36
SoC_I2C1_SDA — SoC_I2C1_SDA 19,31,34,36

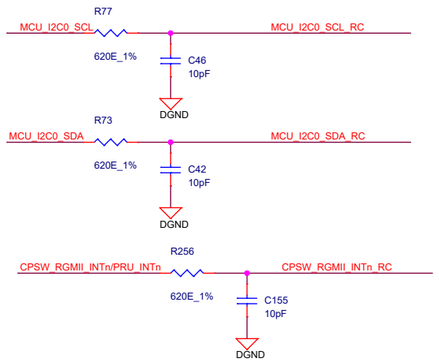
Designed for TI by Mistral Solutions Pvt Ltd

Title	INDUSTRIAL COMMUNICATION LED's		
Size	PROC100A 002		Rev
C			A
Date:	Thursday, September 15, 2022	Sheet 30 of 43	

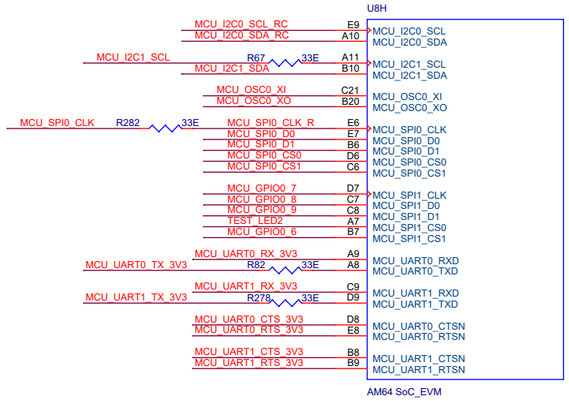
MCU_GENERAL

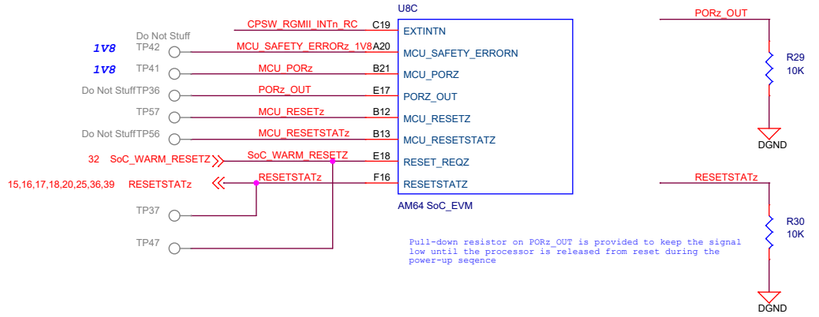






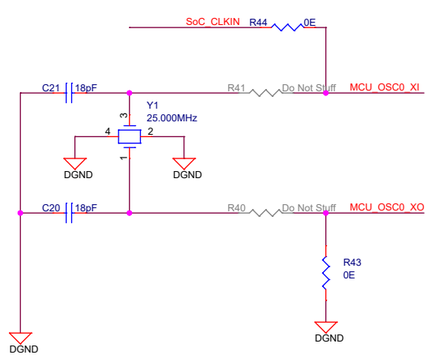
LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly



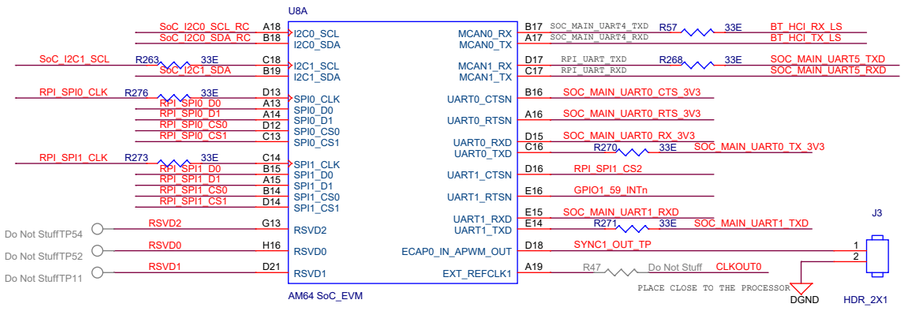


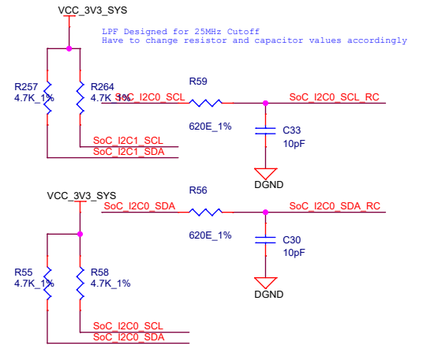
CRYSTAL

Only Footprint option to mount the Oscillator is provided.
By default the part is not mounted on the board.



SoC MAIN DOMAIN





OFF PAGE CONNECTIONS

32 MCU_RESETz — MCU_RESETz
32 MCU_PORz — MCU_PORz
25,27,31 MCU_RESETSTATz — MCU_RESETSTATz
15,16,17,18,20 PORz_OUT — PORz_OUT
17,25,39 CPSW_RGMII_INTn/PRU_INTn — CPSW_RGMII_INTn/PRU_INTn
27,31,33 TEST_LED2 — TEST_LED2
27,31,32 MCU_GPIO0_6 — MCU_GPIO0_6
29 SoC_CLKIN — SoC_CLKIN
24 MCU_UART0_RX_3V3 — MCU_UART0_RX_3V3
24 MCU_UART0_TX_3V3 — MCU_UART0_TX_3V3
24 MCU_UART0_RTS_3V3 — MCU_UART0_RTS_3V3
24 MCU_UART0_CTS_3V3 — MCU_UART0_CTS_3V3

27 MCU_SPI0_CS1 — MCU_SPI0_CS1
27 MCU_GPIO0_8 — MCU_GPIO0_8
27,31,33 TEST_LED2 — TEST_LED2
27 MCU_GPIO0_7 — MCU_GPIO0_7
27 MCU_UART1_RX_3V3 — MCU_UART1_RX_3V3
27 MCU_UART1_RTS_3V3 — MCU_UART1_RTS_3V3
27 MCU_UART1_TX_3V3 — MCU_UART1_TX_3V3
27 MCU_I2C0_SDA — MCU_I2C0_SDA
25,27,31 MCU_RESETSTATz — MCU_RESETSTATz
27 MCU_SPI0_D1 — MCU_SPI0_D1
27 MCU_SPI0_D0 — MCU_SPI0_D0
27 MCU_SPI0_CS0 — MCU_SPI0_CS0
27,31,32 MCU_GPIO0_6 — MCU_GPIO0_6
27 MCU_UART1_CTS_3V3 — MCU_UART1_CTS_3V3
27 MCU_GPIO0_9 — MCU_GPIO0_9
27 MCU_I2C1_SDA — MCU_I2C1_SDA
27 MCU_SPI0_CLK — MCU_SPI0_CLK
27 MCU_I2C1_SCL — MCU_I2C1_SCL
27 MCU_I2C0_SCL — MCU_I2C0_SCL
27 MCU_SAFETY_ERRORz_1V8 — MCU_SAFETY_ERRORz_1V8

BT_HCI_TX_LS — BT_HCI_TX_LS 14
BT_HCI_RX_LS — BT_HCI_RX_LS 14
SOC_MAIN_UART5_RXD — SOC_MAIN_UART5_RXD 26
SOC_MAIN_UART5_TXD — SOC_MAIN_UART5_TXD 26
RPI_SPI1_CLK — RPI_SPI1_CLK 26
RPI_SPI1_D0 — RPI_SPI1_D0 26
RPI_SPI1_D1 — RPI_SPI1_D1 26
RPI_SPI1_CS0 — RPI_SPI1_CS0 26
RPI_SPI1_CS1 — RPI_SPI1_CS1 26
RPI_SPI1_CS2 — RPI_SPI1_CS2 26
SOC_MAIN_UART0_RX_3V3 — SOC_MAIN_UART0_RX_3V3 24
SOC_MAIN_UART0_TX_3V3 — SOC_MAIN_UART0_TX_3V3 24
SOC_MAIN_UART0_RTS_3V3 — SOC_MAIN_UART0_RTS_3V3 24
SOC_MAIN_UART0_CTS_3V3 — SOC_MAIN_UART0_CTS_3V3 24
SoC_I2C0_SCL — SoC_I2C0_SCL 25,26,35,39
SoC_I2C0_SDA — SoC_I2C0_SDA 25,26,35,39
SoC_I2C1_SCL — SoC_I2C1_SCL 19,30,34,36
SoC_I2C1_SDA — SoC_I2C1_SDA 19,30,34,36
CLKOUT0 — CLKOUT0 29,37
RPI_SPI0_CLK — RPI_SPI0_CLK 26
RPI_SPI0_D0 — RPI_SPI0_D0 26
RPI_SPI0_D1 — RPI_SPI0_D1 26
RPI_SPI0_CS0 — RPI_SPI0_CS0 26
RPI_SPI0_CS1 — RPI_SPI0_CS1 26
GPIO1_59_INTn — GPIO1_59_INTn 32
SOC_MAIN_UART1_RXD — SOC_MAIN_UART1_RXD 21
SOC_MAIN_UART1_TXD — SOC_MAIN_UART1_TXD 21

Designed for TI by Mistral Solutions Pvt Ltd

Title	SoC MAIN AND MCU DOMAIN		
Size	PROC100A 002		Rev
C			A
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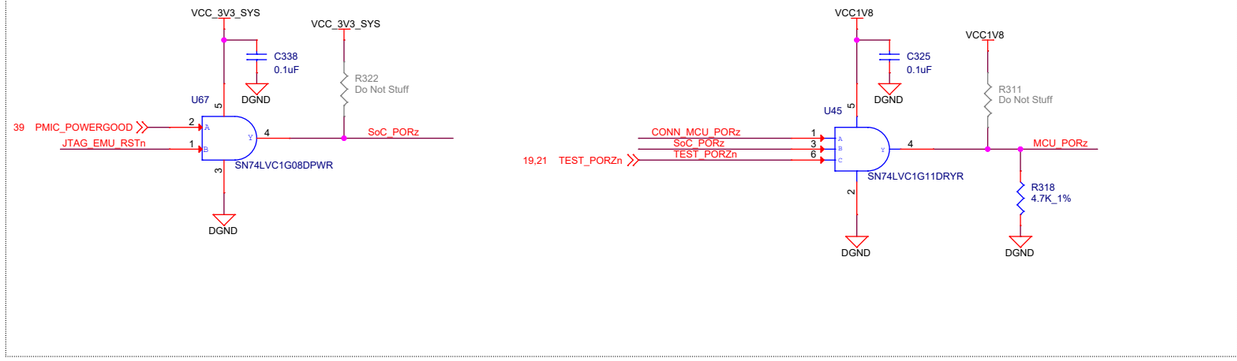
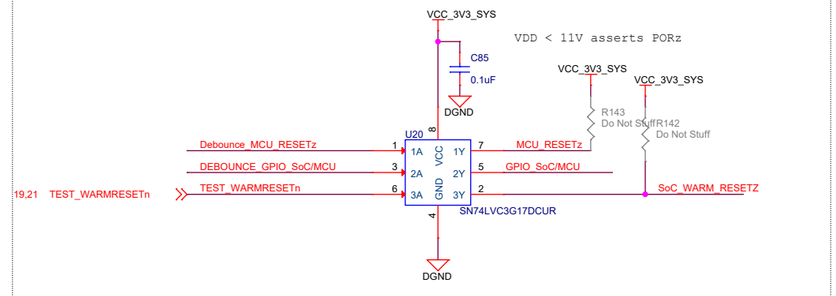
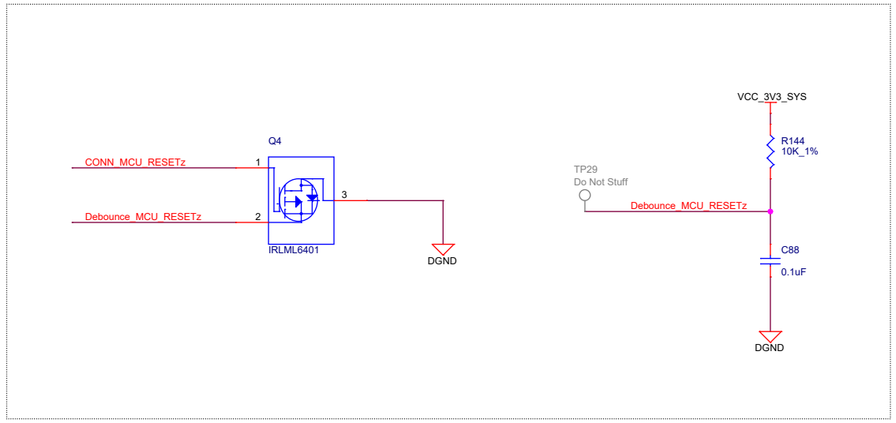
POR

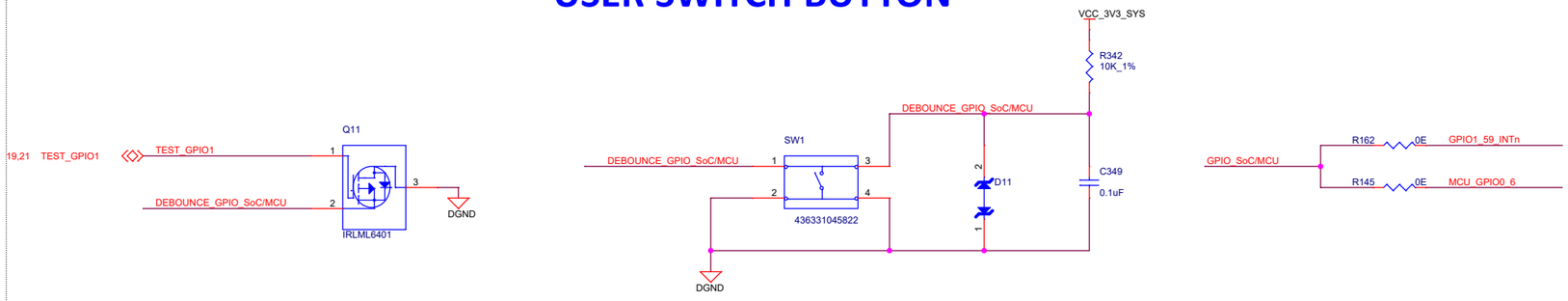


DEBOUNCE CIRCUIT





USER SWITCH BUTTON



OFF PAGE CONNECTIONS

31 SoC_WARM_RESETZ	SoC_WARM_RESETZ
31 MCU_RESETz	MCU_RESETz
23 JTAG_EMU_RSTn	JTAG_EMU_RSTn
27 CONN_MCU_RESETz	CONN_MCU_RESETz
31 MCU_PORz	MCU_PORz
27,31 MCU_GPIO0_6	MCU_GPIO0_6
31 GPIO1_59_INTn	GPIO1_59_INTn
27 CONN_MCU_PORz	CONN_MCU_PORz

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Title	RESET CIRCUIT		
Size	PROC100A 002		Rev
C			A
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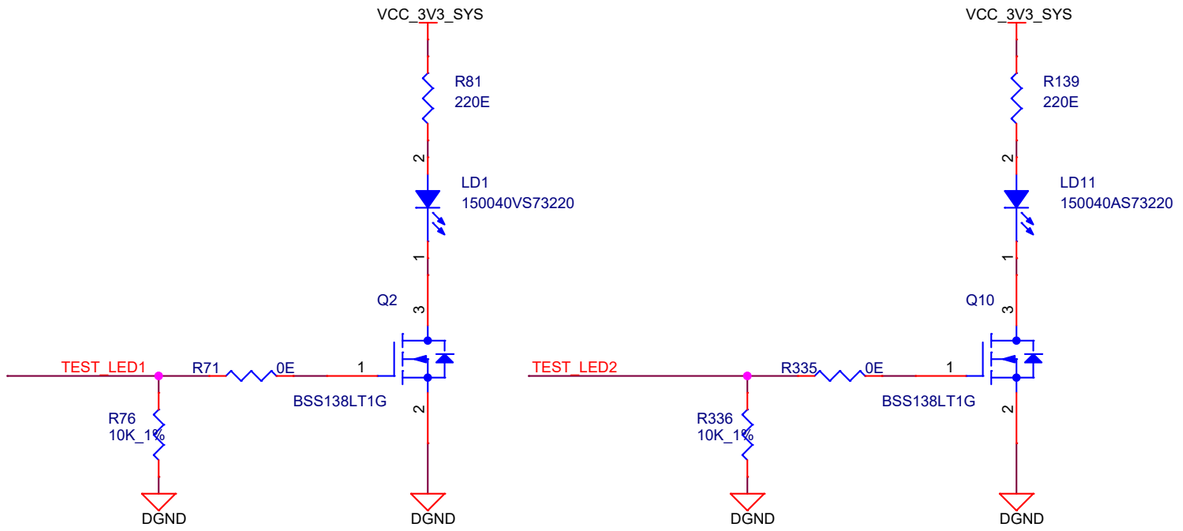
USER TEST LED's



OFF PAGE CONNECTIONS

TEST_LED1	TEST_LED1	25
TEST_LED2	TEST_LED2	27,31

Designed for TI by Mistral Solutions Pvt Ltd

Title	USER TEST LED's		
Size	PROC100A 002		Rev
B			A
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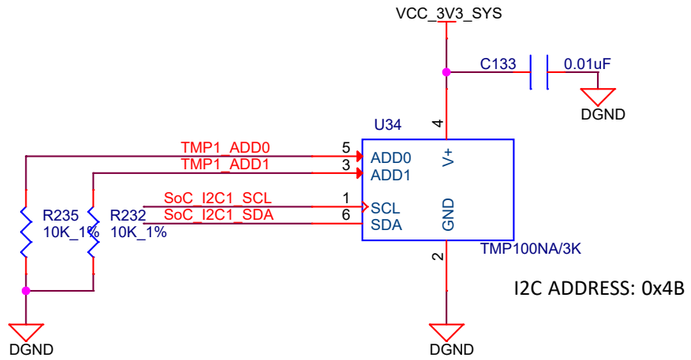
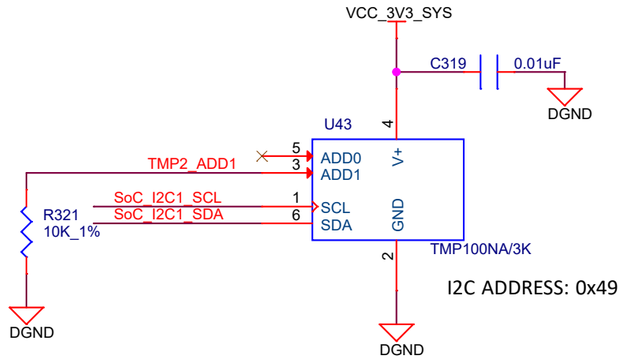
TEMPERATURE SENSORS



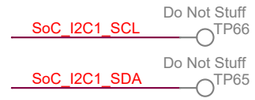
I2C ADDRESS: 0x4B

NOTE: PLACE TEMP SENSOR CLOSE TO SoC



I2C ADDRESS: 0x49

NOTE: PLACE TEMP SENSOR CLOSE TO LPDDR4



OFF PAGE CONNECTIONS

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Title	TEMPERATURE SENSORS	
Size B	PROC100A 002	Rev A
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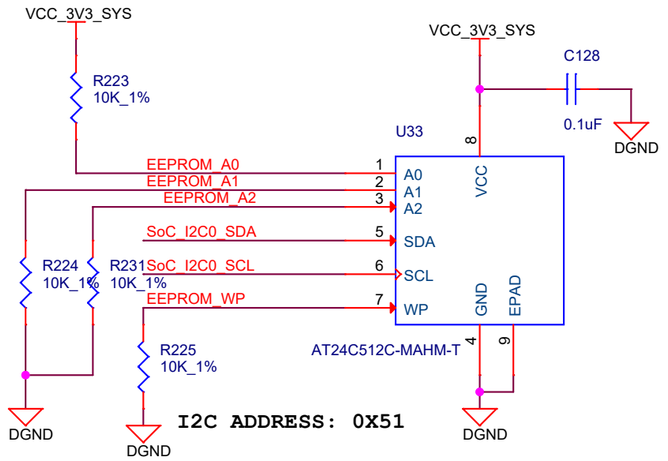
BOARD ID EEPROM



OFF PAGE CONNECTIONS

SoC_I2C0_SDA
SoC_I2C0_SCL

SoC_I2C0_SDA 25,26,31,39
SoC_I2C0_SCL 25,26,31,39

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Title	BOARD ID EEPROM	
Size B	PROC100A 002	Rev A
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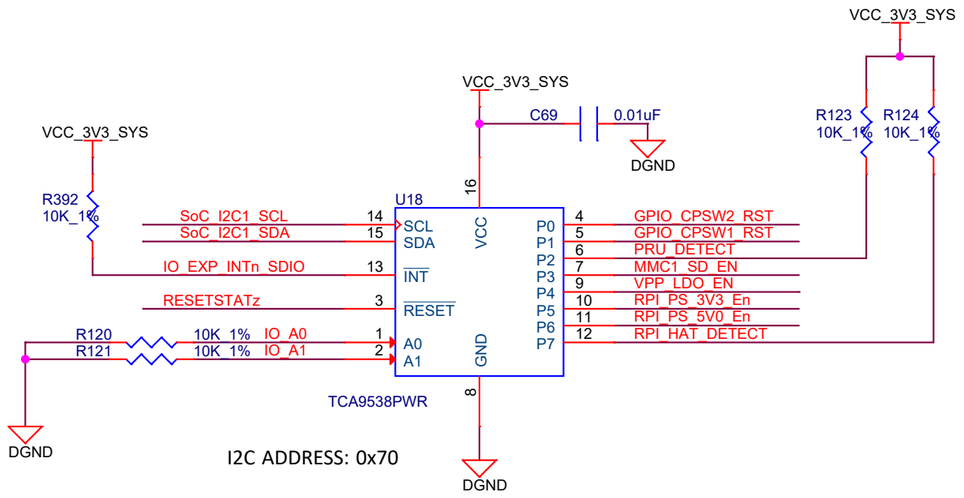
IO EXPANDER



OFF PAGE CONNECTIONS

RPI_PS_3V3_En	RPI_PS_3V3_En 26
RPI_PS_5V0_En	RPI_PS_5V0_En 26
GPIO_CPSW2_RST	GPIO_CPSW2_RST 18
GPIO_CPSW1_RST	GPIO_CPSW1_RST 17
MMC1_SD_EN	MMC1_SD_EN 16
VPP_LDO_EN	VPP_LDO_EN 40
RESETSTATz	RESETSTATz 15,16,17,18,20,25,31,39
IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO 14
SoC_I2C1_SCL	SoC_I2C1_SCL 19,30,31,34
SoC_I2C1_SDA	SoC_I2C1_SDA 19,30,31,34
RPI_HAT_DETECT	RPI_HAT_DETECT 26
PRU_DETECT	PRU_DETECT 25

Designed for TI by Mistral Solutions Pvt Ltd

Title	IO EXPANDER	
Size	PROC100A 002	Rev
B		A
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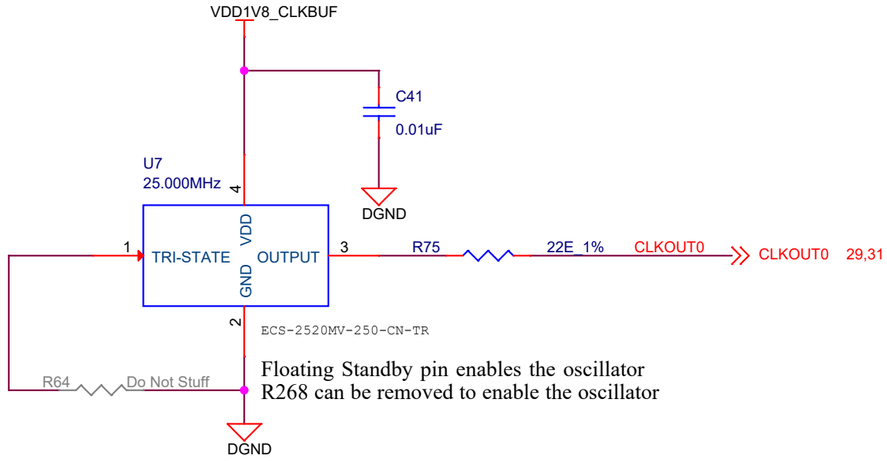
OSCILLATOR



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Title	OSCILLATOR	
Size: B	PROC100A 002	Rev: A
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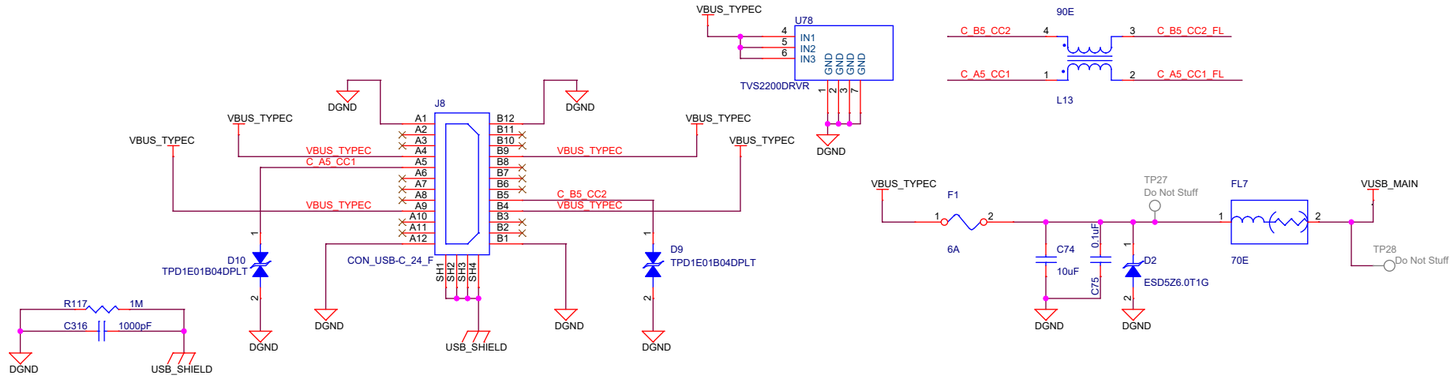
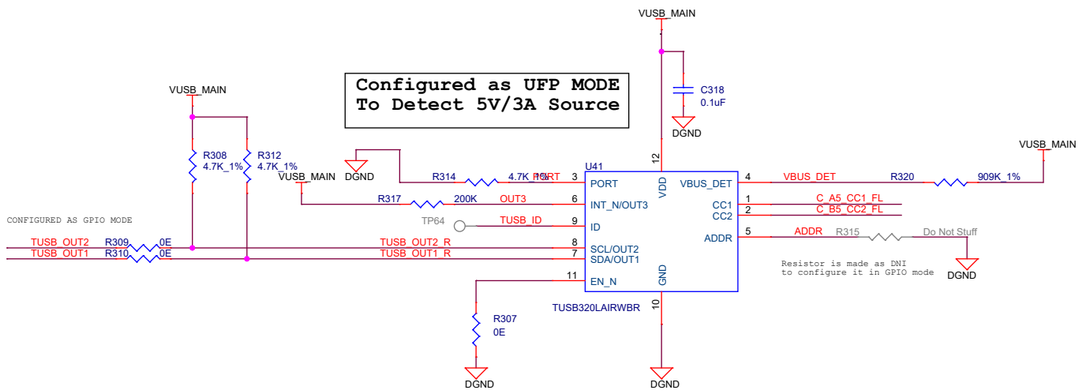
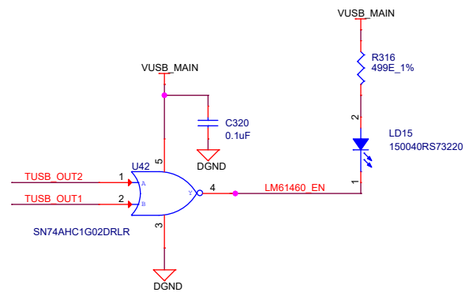
USB TYPE-C CONNECTOR



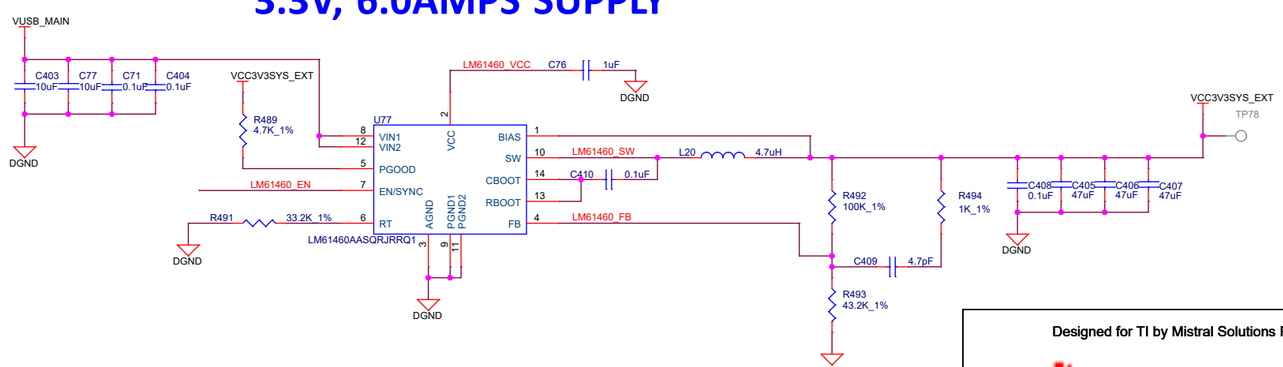
USB TYPE C CONFIGURATION CHANNEL LOGIC AND PORT CONTROLLER



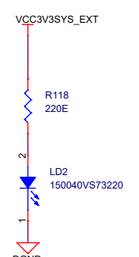
Enable Logic for 3V3 Regulator



3.3V, 6.0AMPS SUPPLY



POWER INDICATION LED



Designed for TI by Mistral Solutions Pvt Ltd

Title	USB MAIN 5V POWER SUPPLY		
Size	PROC100A 002		Rev
C			A
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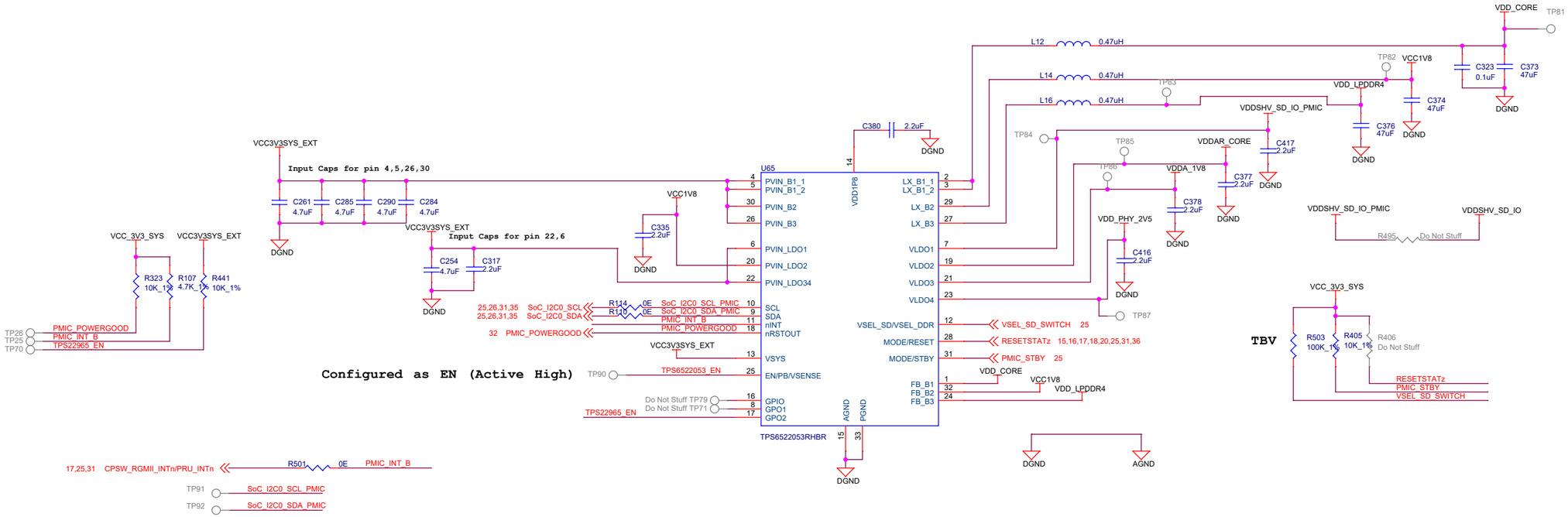
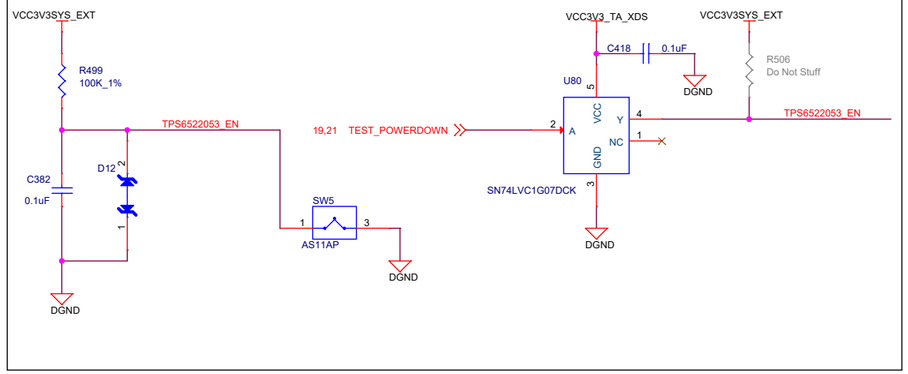
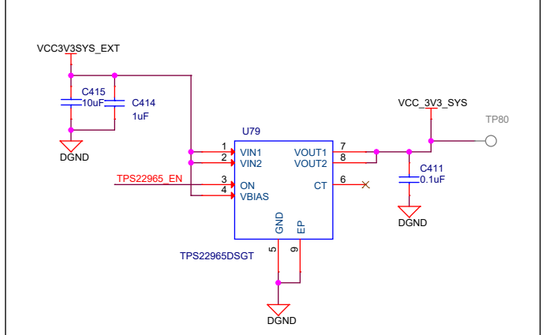
TPS6522053 PMIC



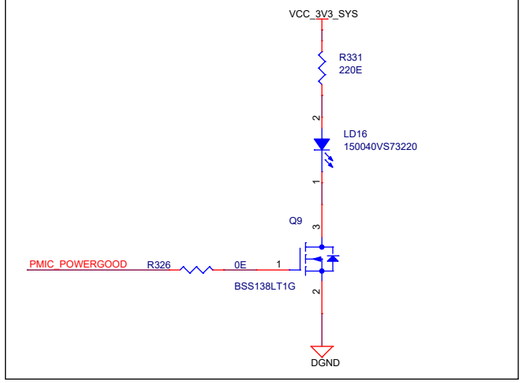
ON/OFF LOGIC



3V3 POWER SWITCH



POWER INDICATION LED



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Title	TPS6522053RHBR PMIC		
Size C	PROC100A 002		Rev A
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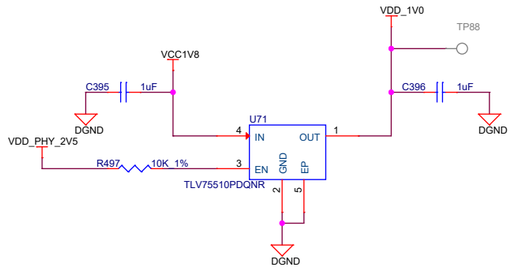
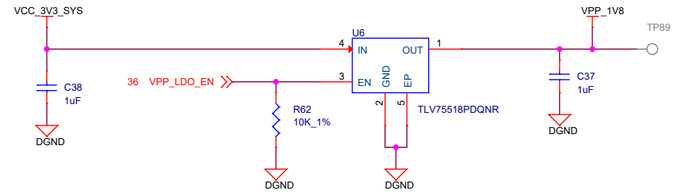
1.0V, 500mA SUPPLY



eFUSE PROGRAMMING VOLTAGE TO SoC



1.8V VPP, 0.15AMPS SUPPLY

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Title	DISCRETE POWER REGULATORS	
Size C	PROC100A 002	Rev A
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STRAP CONFIGURATION OF ETHERNET PHYS

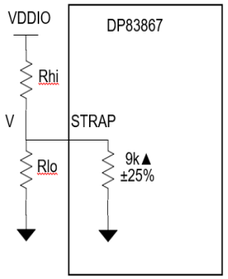

Figure 25. Strap Circuit

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
1	0	0	0.098 × VDDIO	OPEN	OPEN
2	0.140 × VDDIO	0.165 × VDDIO	0.191 × VDDIO	10	2.49
3	0.225 × VDDIO	0.255 × VDDIO	0.284 × VDDIO	5.76	2.49
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

Level Strap Resistor Ratios

PIN NAME	64 HTQFP PIN #	48 QFN PIN #	DEFAULT	STRAP FUNCTION		
RX_D0	44	33	[00]	**MODE**	PHY_ADD1	PHY_ADD0
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D2	46	35	[00]	**MODE**	PHY_ADD3	PHY_ADD2
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D4	48		[00]	**MODE**	ANEG_SEL1	PHY_ADD4
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D5	49		[00]	**MODE**	Force MDI/X	Half-Duplex Enable (FD/HD)
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D6	50		[00]	**MODE**	RGMII Disable	AMDIX Disable
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D7	51		[00]	**MODE**	Speed Optimization Enable	Clock Out Disable
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_DV/RX_CTRL (1) (Straps Required)	53	38	[0]	**MODE**		Autoneg Disable
				1		N/A
				2		N/A
				3		0
				4		1
CRS(2)	56		[0]	**MODE**		Fast Link Drop (FLD)
				1		0
				2		1
				3		N/A

Level Strap Pins

PIN NAME	64 HTQFP PIN #	48 QFN PIN #	DEFAULT	STRAP FUNCTION		
LED_2(3)		45	[00]	**MODE**	RGMII Clock Skew TX[1]	RGMII Clock Skew TX[0]
				1	0	0
				2	0	1
				3	1	0
				4	1	1
LED_1 (RGZ)		46	[00]	**MODE**	ANEG_SEL	RGMII Clock Skew TX[2]
				1	0	0
				2	0	1
				3	1	0
				4	1	1
LED_1 (PAP)	62		[0]	**MODE**	ANEG_SEL0	
				1	0	
				2	0	
				3	1	
				4	1	
LED_0(4)	63	47	[0]	**MODE**	Mirror Enable	
				1	0	
				2	N/A	
				3	1	
				4	N/A	
GPIO_0 (3)		39	[00]	**MODE**	RGMII Clock Skew RX[0]	
				1	0	
				2	Not Applicable	
				3	1	
				4	Not Applicable	
GPIO_1		40	[00]	**MODE**	RGMII Clock Skew RX[2]	RGMII Clock Skew RX[1]
				1	0	0
				2	0	1
				3	1	0
				4	1	1

Level Strap Pins

MODE	ANEG_SEL	REMARKS
10/100/1000	0	advertise ability of 10/100/1000
100/1000	1	advertise ability of 100/1000 only

MODE	RGMII CLOCK SKEW TX[2]	RGMII CLOCK SKEW TX[1]	RGMII CLOCK SKEW TX[0]	RGMII TX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

MODE	RGMII CLOCK SKEW RX[2]	RGMII CLOCK SKEW RX[1]	RGMII CLOCK SKEW RX[0]	RGMII RX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

RGMII Clock Skew Details

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Title	STRAP CONFIGURATION OF ETHERNET PHYS		
Size	PROC100A 002		Rev
D			A
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HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

BARE PCB

PCB1

PROC100

JUMPERS

ACC1

SPC02SYAN

LOGOs

PCB LOGO
Do Not Stuff
Texas Intruments

PCB LOGO
Do Not Stuff
For Evaluation only; not FCC approved for resale

PCB LOGO
Do Not Stuff
WEEE Mark

PCB LOGO
Do Not Stuff
CE Mark

FIDUCIALS

FID1 Do Not Stuff
FID2 Do Not Stuff
FID3 Do Not Stuff
FID4 Do Not Stuff
FID5 Do Not Stuff
FID6 Do Not Stuff

LABELS

Board Serial No.

LBL1
PCB LABEL
THT-103-423-10

Assembly Revision

LBL3
PCB LABEL
THT-103-423-10

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Title	HARDWARE SCHEMATICS	
Size: C	PROC100A 002	Rev: A
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