AM64x STARTER KIT EVM BOARD
SK-AM64B

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Revision Number

REV	A
VER	1.4
BOM Variant	002

Note :- Raspberry Pi is the trademark / wordmark of Raspberry Pi Foundation

D-Note :-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note:-

*Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of board design before board assembly
*A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor
*Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)

KEY LINKS TO COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprad67a/sprad67a.pdf
Schematic Design and Review Checklist : https://www.ti.com/lit/an/spracu5c/spracu5c.pdf
PMIC Power Solutions application note : https://www.ti.com/lit/an/slvafe9/slvafe9.pdf
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/an/spracu1a/spracu1a.pdf
SKs (Starter Kits) for reference : TMDS64EVM, SK-AM64B

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REVISION HISTORY

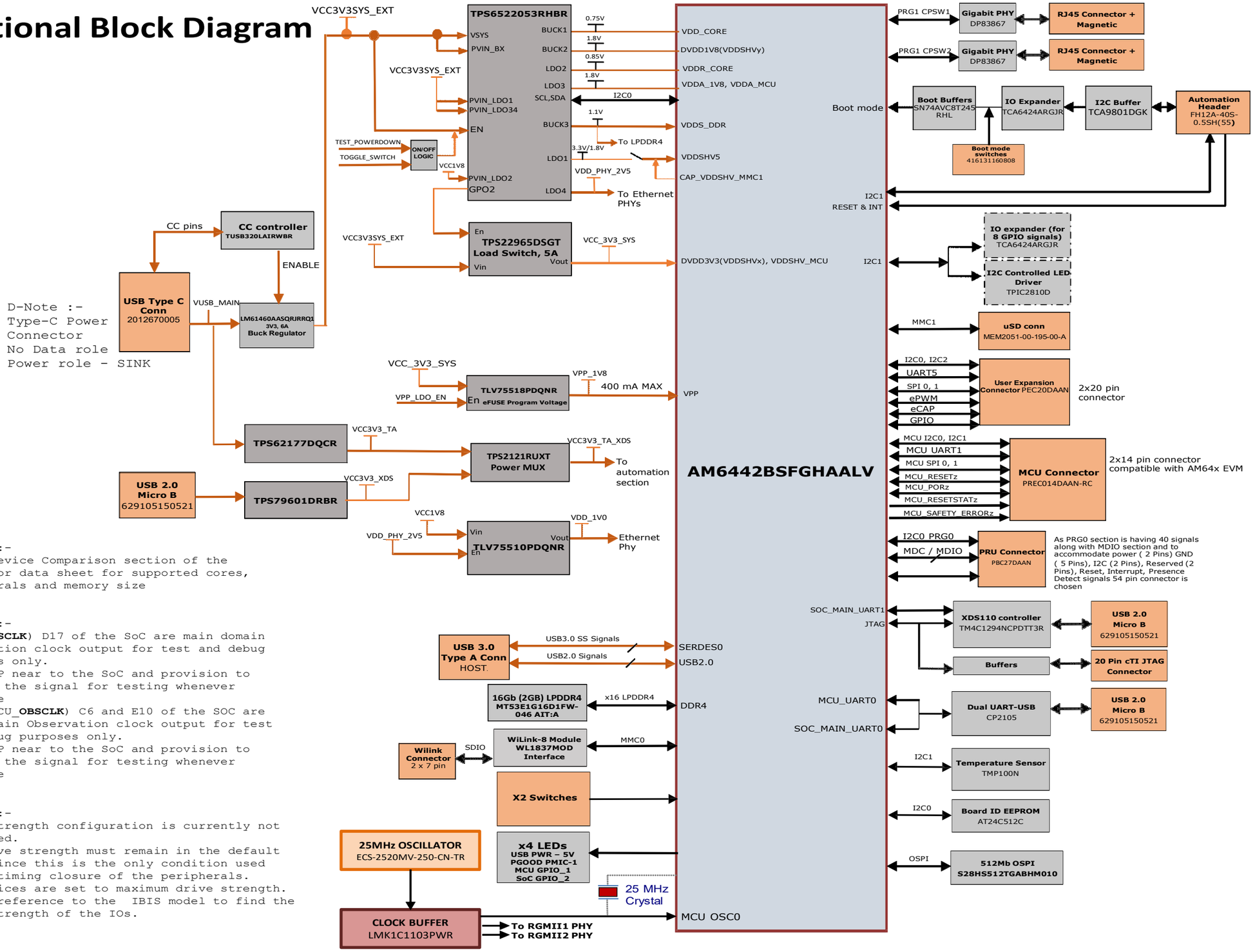
VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
1.0	20th APR 2022	Drafted from "PROC100E4_SCH" Document and updated PG2.0 changes.	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.1	21st APR 2022	Power Mux added, R375 added, R138 is replaced to 0E from 1M ohm, R469 & R470 are removed, C343 is made as DNI.	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.2	21st APR 2022	Antenna Tuning Network C2, L2 and L4 values updated	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.3	12th SEPT 2022	PMIC Buck Capacitors replaced with 47uF (C373, C374, C376), RSVD ball names updated in SoC and Replaced obsolete components with alternate components.	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.4	18 JUNE 2024	Updated SoC Part Number, Enabled Voltage ratings for all the capacitors and added Design Review notes Moved to DNI : C20, C21, Y1 Moved to Mount : R226, R227, R228, R229, R230, R236, R238, R240, R466, R84, R85, R68, R69, R70, R113, R266. C47 - 4.7uF changed to 1uF; C35 - 22uF changed to 4.7uF; C81 - 1uF changed to 0.1uF; C83 - 2.2uF changed to 1uF. Bootmode Buffers & DIP Switch Pullup resistors -1.1K_1% changed to 1K_1%;R251,R45 - 22E changed to 0E; R241 - 100K_1% changed to Std 10K; R400 - 10E changed to 0E; R286 - 16.5K_0.1% changed to 16.5K_1%; R294 - 3.48K_0.1% changed to 3.48K_1%; R31,R86 - 11K_1% changed to 10K_1%; R87,R334,R503,Bootmode DIP Switch's Pulldown resistors - 100K_1% changed to Std 100K; R284,R249 - Std 10K changed to 10K_1%; R84,R85,R68,R69,R70,R226,R227,R228,R229,R230,R236,R238,R240,R465,R35,R247,R233,R239,R245,R88, R253,R258,R105,R122,R113,R266,R7,R8,R9,R11,R13,R15,R16,R374,R373,R372,R371,R370,R369,R375,R513, R511,R518,R515,R323,R441,R223,R224,R231,R225,R76,R336,R235,R232,R321,R174,R461,R462,R463,R464, R368,R392,R124,R123, R120,R121,R109,R365,R366,R367,R391,R343,R188,R62,R405,R497 - 10K_1% changed to Std 10K; R206,R209,R387,R388,R512,R519,R107,R197,R275, I2C pull ups - 4.7K_1% changed to Std 4.7K.	Mistral Design Team		

LINKS TO KEY FAQs

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1185502/faq-am6442-am6441-am6422-am6421-am6412-am6411-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-am62px-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1347060/faq-am6442-am6441-am6422-am6421-am6412-am6411-custom-board-hardware-design---design-and-review-notes-for-reuse-of-sk-am64b-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1274160/faq-am6442-am6441-am6422-am6421-am6412-am6411-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-evm-starter-kit

BLOCK DIAGRAM_AM64x_SKEVM

Functional Block Diagram



D-Note :-
Refer Device Comparison section of the processor data sheet for supported cores, peripherals and memory size

D-Note :-
Pin (**OBSCLK**) D17 of the SoC are main domain Observation clock output for test and debug purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever possible
Pins (MCU_**OBSCLK**) C6 and E10 of the SOC are MCU Domain Observation clock output for test and debug purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever possible

D-Note :-
Drive strength configuration is currently not supported.
The drive strength must remain in the default state since this is the only condition used during timing closure of the peripherals.
The devices are set to maximum drive strength.
Please reference to the IBIS model to find the drive strength of the IOs.

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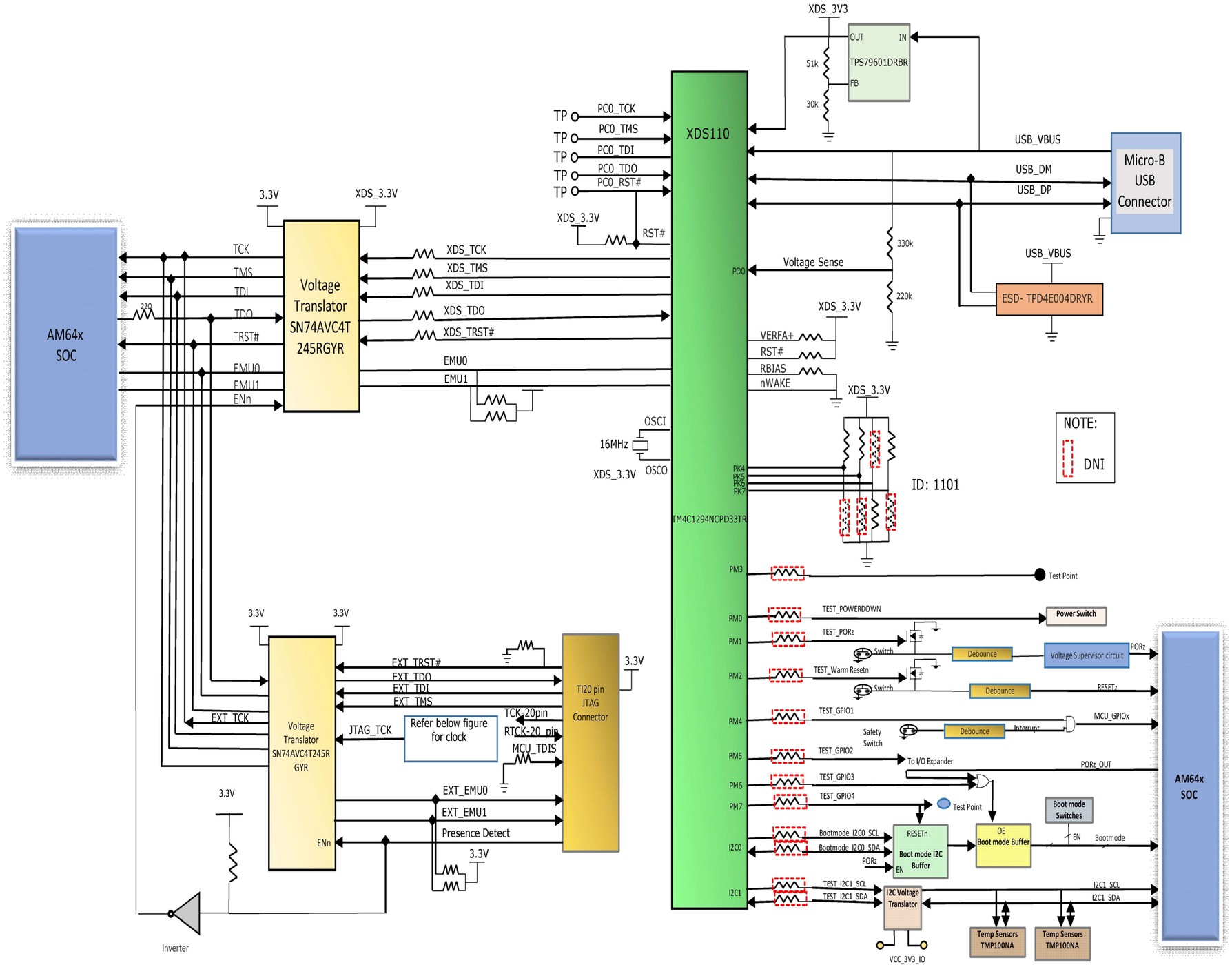
BLOCK DIAGRAM_XDS110



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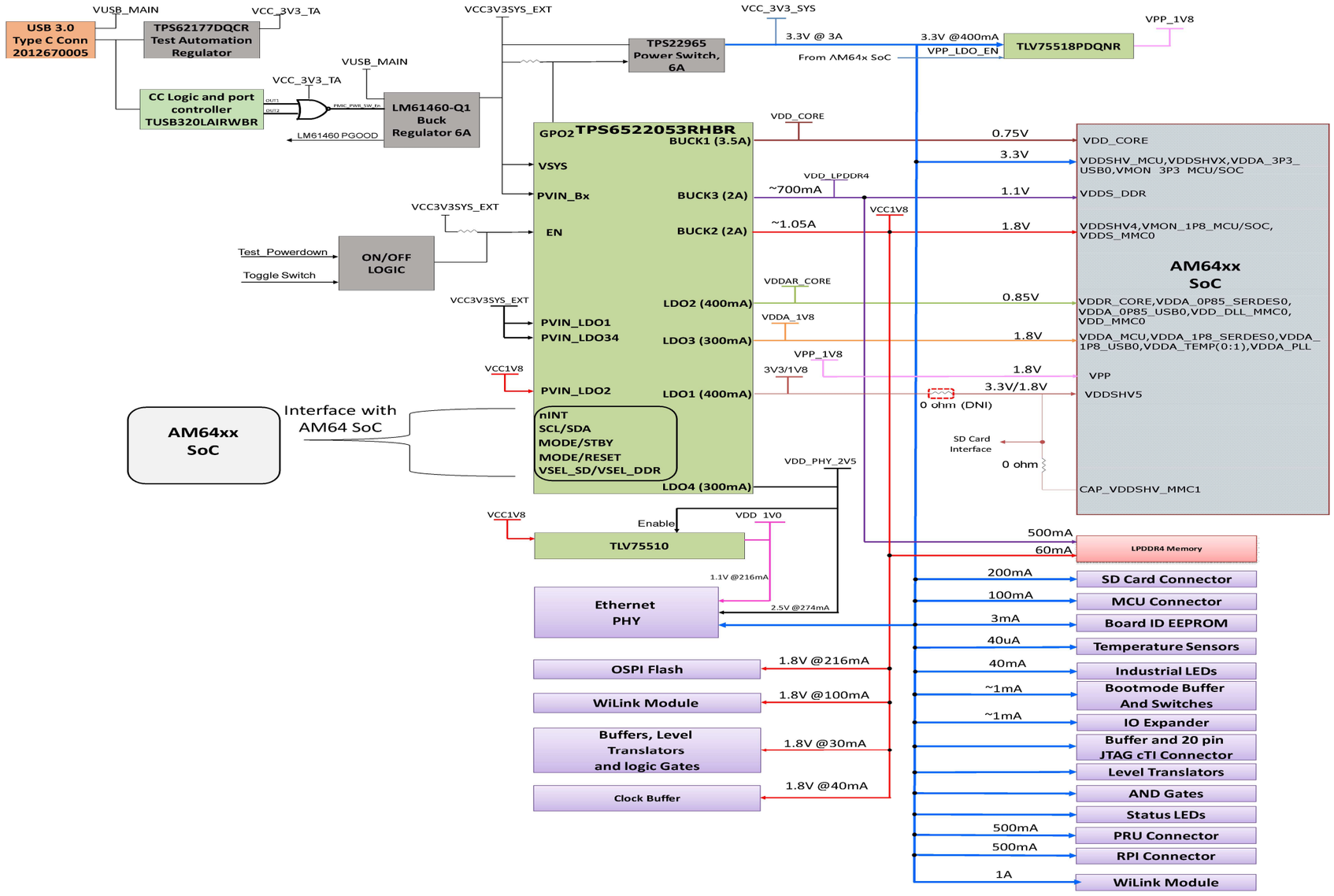
POWER BLOCK DIAGRAM



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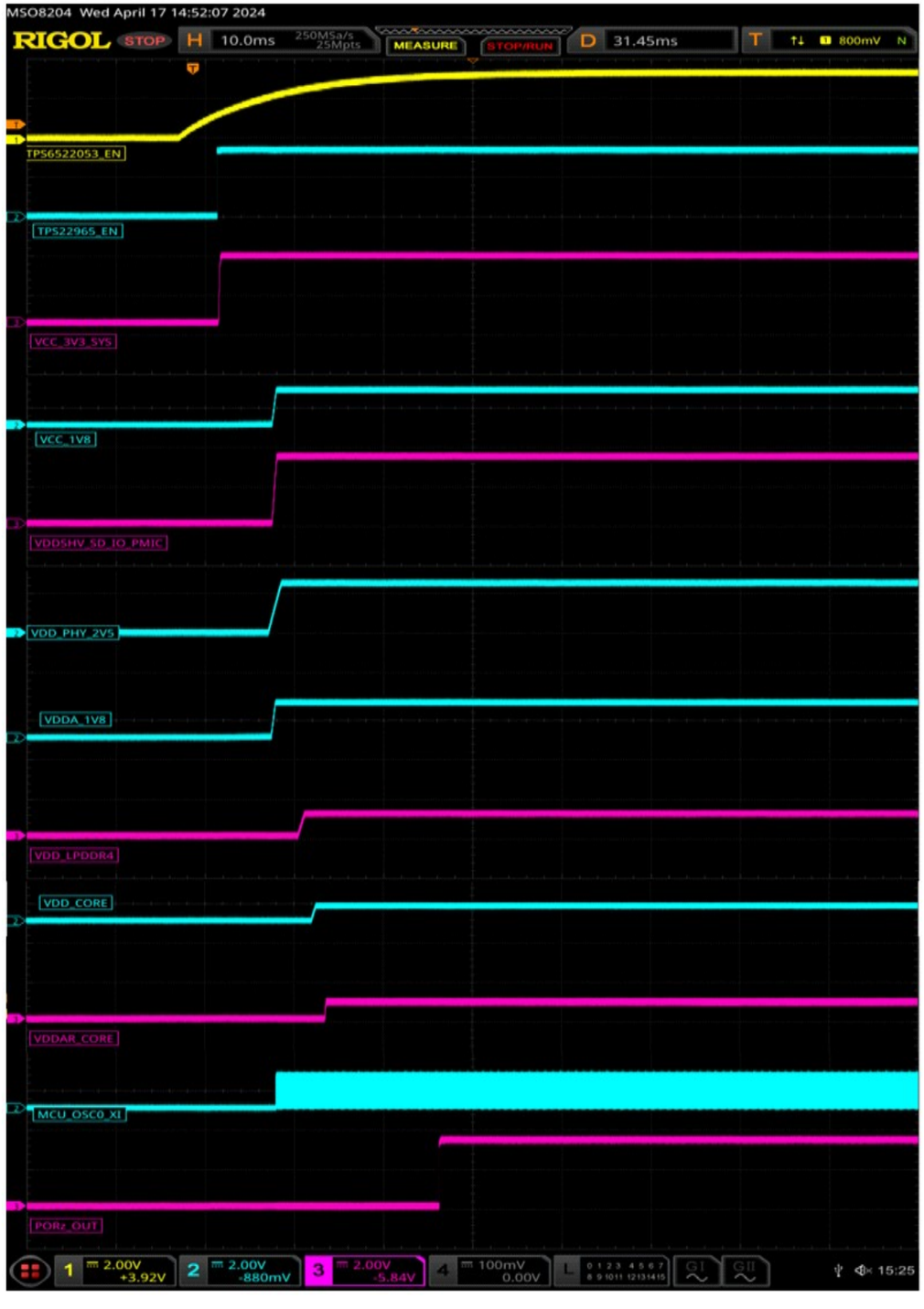
POWER SEQUENCE



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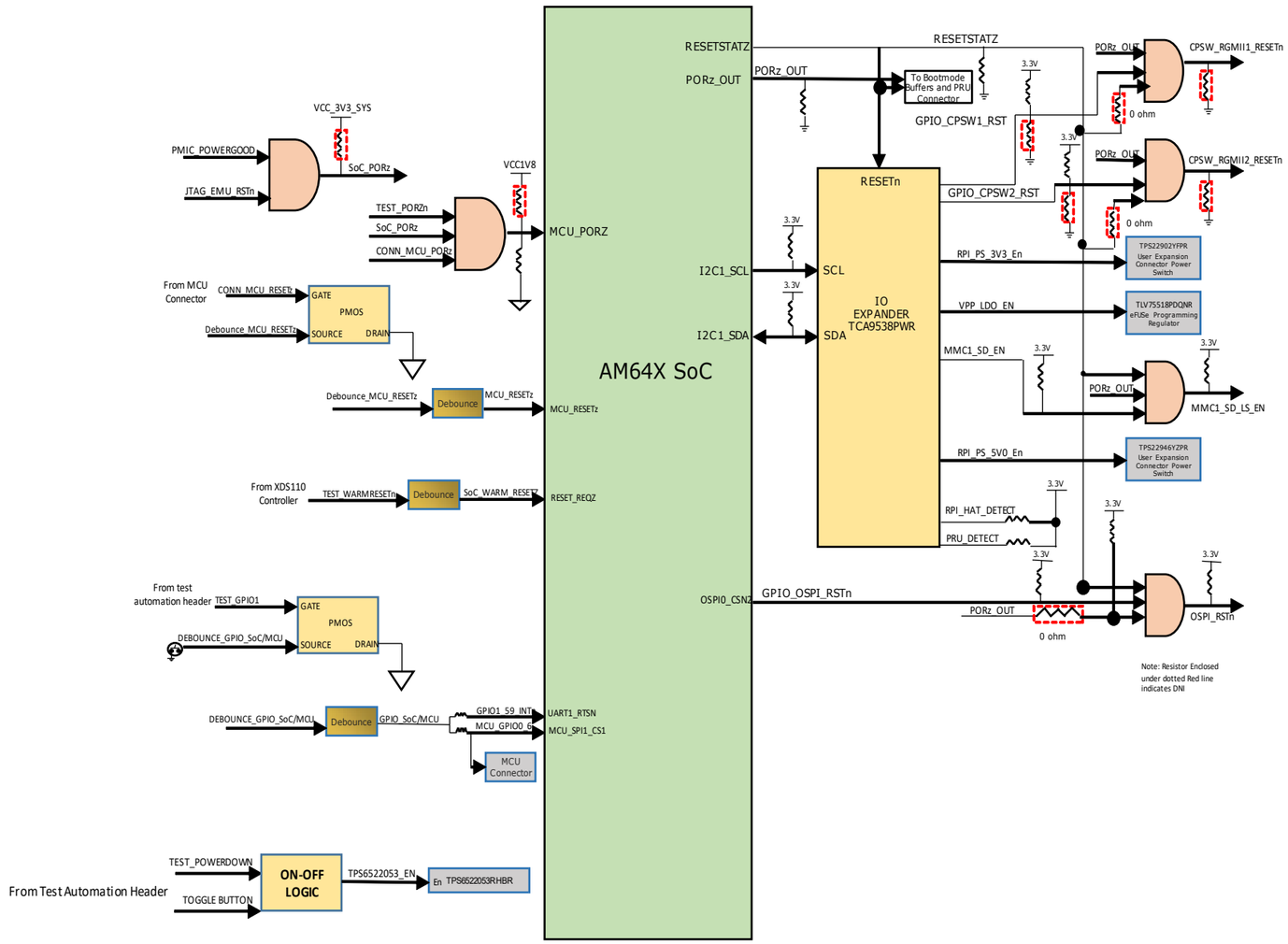
RESET ARCHITECTURE



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Title	RESET ARCHITECTURE		
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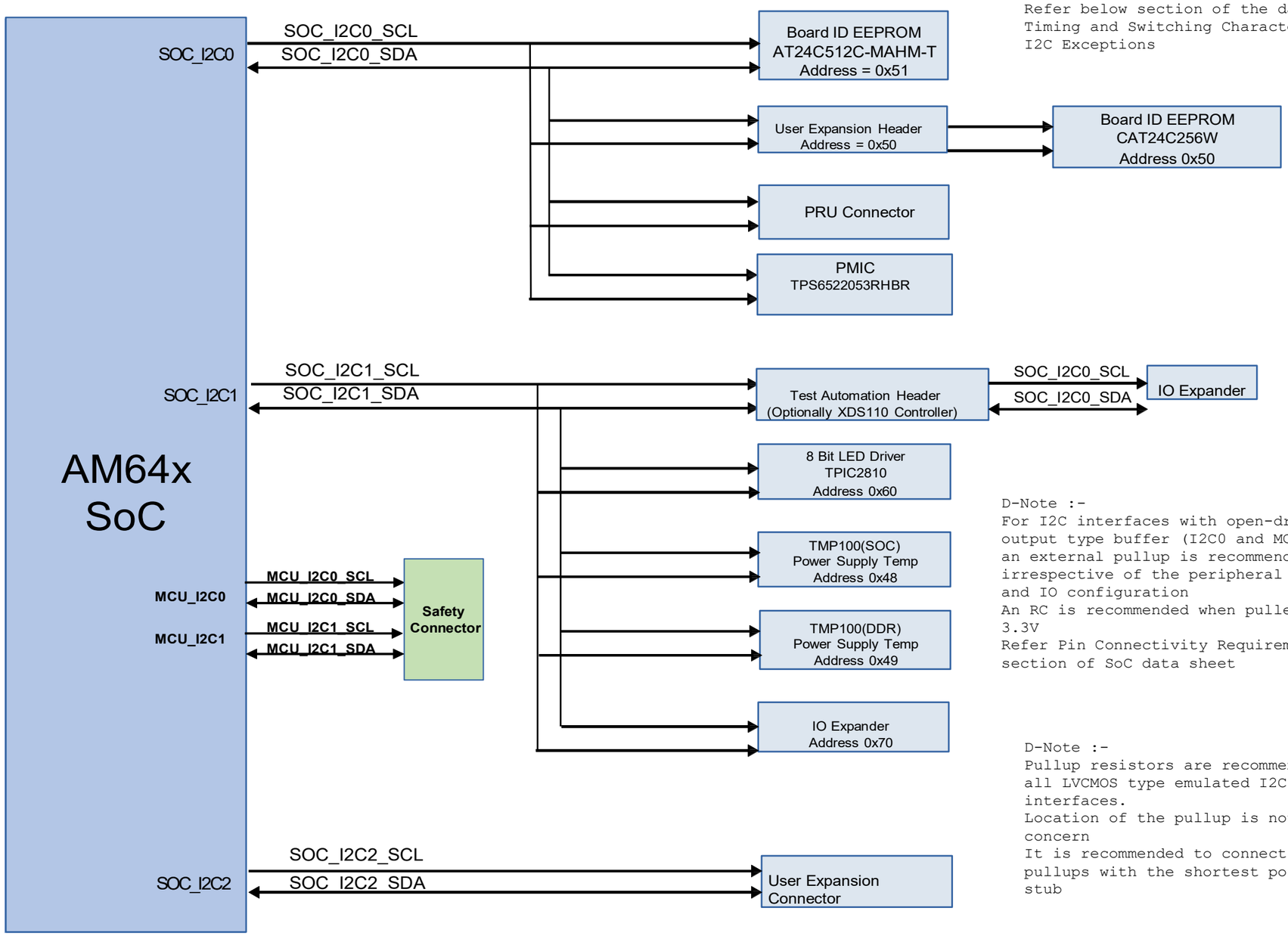
GPIO MAPPING TABLE

AM64x GPIO MAPPING TABLE										
Sl.NO	GPIO Description	GPIO Netname	Functionality	GPIO Used	SoC Muxed Signal Name	Direction with respect to SoC	Default State	Active State	Voltage Domain On Processor Side	Voltage Connected on SKEVM
1	IO Expander Interrupt	IO_EXP_INTn_SDIO	Interrupt	GPIO1_78	MMC1_SDWP	Input	High	Low	VDDSHV0	SoC_DVDD3V3
2	Enable for COM8 Level Translator	COM8_LS_EN	Enable	GPIO0_62	PRG1_PRU0_GPO17	Output	High	Low	VDDSHV2	SoC_DVDD3V3
3	Enable for WLAN Interface in COM8 Connector	WLAN_EN_SoC_LS	Enable	GPIO0_48	PRG1_PRU0_GPO3	Output	Low	High	VDDSHV2	SoC_DVDD3V3
4	Enable for BT Interface in COM8 Connector	BT_EN_SOC_LS	Enable	GPIO0_49	PRG1_PRU0_GPO4	Output	Low	High	VDDSHV2	SoC_DVDD3V3
5	WLAN SDIO out-of band interrupt line	WLAN_IRQ_LS	Interrupt	GPIO0_46	PRG1_PRU0_GPO1	Input	High	Low	VDDSHV2	SoC_DVDD3V3
6	OSPI Interrupt	OSPI_INTn	Interrupt	GPIO0_14	OSPI0_CSN3	Input	High	Low	VDDSHV4	SOC_DVDD1V8
7	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	Reset	GPIO0_13	OSPI0_CSN2	Output	High	Low	VDDSHV4	SOC_DVDD1V8
8	User LED	TEST_LED1	Test	GPIO0_60	PRG1_PRU0_GPO15	Output	Low	High	VDDSHV2	SoC_DVDD3V3
9	User LED	TEST_LED2	Test	MCU_GPIO0_5	MCU_SPI1_CS0	Output	Low	High	VDDSHV_MCU	SoC_DVDD3V3
10	SD card load switch enable control	MMC1_SD_EN	Enable	IO Expander-P3		Output	High	High	VDDSHV0	SoC_DVDD3V3
11	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn								
12	PRU Connector Interrupt	PRU_INTn	Interrupt	GPIO1_70	EXTINTn	Input	High	Low	VDDSHV0	SoC_DVDD3V3
13	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	Reset	IO Expander-P1		Output	High	Low	VDDSHV0	SoC_DVDD3V3
14	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	Reset	IO Expander-P0		Output	High	Low	VDDSHV0	SoC_DVDD3V3
15	TEST GPIO1 from Test Automation	TEST_GPIO1	GPIO for communication with AM64x	GPIO1_59 MCU_GPIO0_6	UART1_RTSN MCU_SPI1_CS1	Input Input	High High	Low Low	VDDSHV0 VDDSHV_MCU	SoC_DVDD3V3 SoC_DVDD3V3
16	BTUART_RTS or Bootmode10 switch select	BTUART_RTS_SEL	Switch Selection	GPIO0_63	PRG1_PRU0_GPO18	Output	Low	High	VDDSHV2	SoC_DVDD3V3
17	VPP 1.8V regulator Enable	VPP_LDO_EN	Enable	IO Expander-P4		Output	Low	High	VDDSHV0	SoC_DVDD3V3
18	MODE/STBY	PMIC_STBY	Standby Mode	GPIO0_51	PRG1_PRU0_GPO6	Output	High	Low	VDDSHV2	SoC_DVDD3V3
19	VSEL_SD/VSEL_DDR	VSEL_SD_SWITCH	SD Selection	GPIO0_45	PRG1_PRU0_GPO2	Output	High	High	VDDSHV2	SoC_DVDD3V3
20	Power Switch Enable for USB device	USB0_DRVBUS	Enable	GPIO1_79	USB0_DRVVBUS	Output	Low	High	VDDSHV0	SoC_DVDD3V3
21	RPI-HAT Detection	RPI_HAT_DETECT	Detection	IO Expander-P7		Input	High	Low	VDDSHV0	SoC_DVDD3V3
22	PRU Detection	PRU_DETECT	Detection	IO Expander-P2		Input	High	Low	VDDSHV0	SoC_DVDD3V3
23	PRU Power Switch Enable	PRU_3V3_En	Enable	GPIO0_64	PRG1_PRU0_GPO19	Output	Low	High	VDDSHV2	SoC_DVDD3V3
24	Rpi Power Switch Enable	RPI_PS_5V0_En	Enable	IO Expander-P6		Output	Low	High	VDDSHV0	SoC_DVDD3V3
25	Rpi Power Switch Enable	RPI_PS_3V3_En	Enable	IO Expander-P5		Output	Low	High	VDDSHV0	SoC_DVDD3V3

I2C TREE



R-Note :-
Refer below section of the data sheet
Timing and Switching Characteristics
I2C Exceptions

R-Note :-
Add - Indicates
Address

D-Note :-
For I2C interfaces with open-drain
output type buffer (I2C0 and MCU_I2C0),
an external pullup is recommended
irrespective of the peripheral usage
and IO configuration
An RC is recommended when pulled to
3.3V
Refer Pin Connectivity Requirements
section of SoC data sheet

D-Note :-
Pullup resistors are recommended for
all LVCMOS type emulated I2C
interfaces.
Location of the pullup is not a
concern
It is recommended to connect the
pullups with the shortest possible
stub

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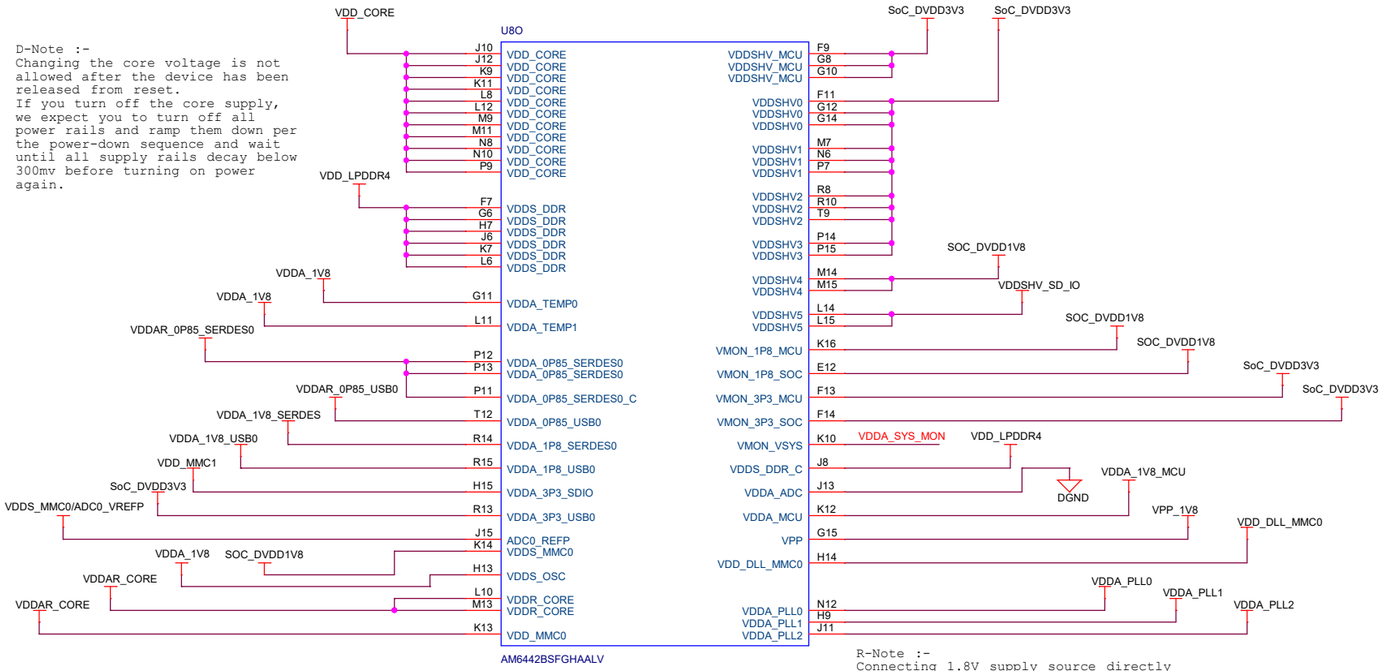
SOC POWER

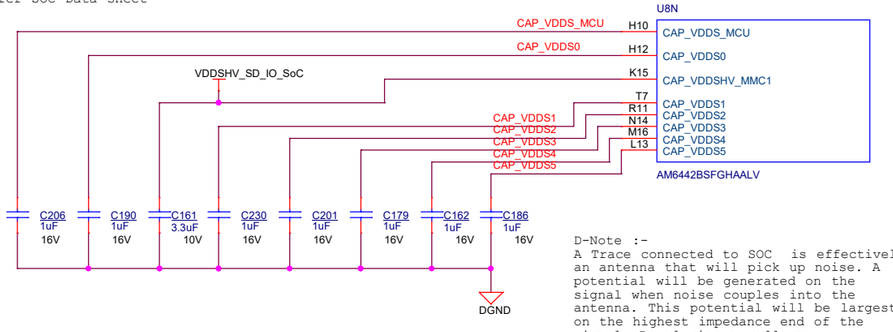
D-Note :-
Changing the core voltage is not allowed after the device has been released from reset.
If you turn off the core supply, we expect you to turn off all power rails and ramp them down per the power-down sequence and wait until all supply rails decay below 300mv before turning on power again.



D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

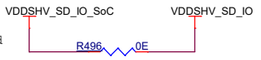
R-Note :-
Connecting 1.8V supply source directly to VPP continuously is not allowed

D-Note :-
Select a capacitor with ESR < 1 O.
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package
Refer SoC Data sheet



D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise. A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the highest impedance end of the signal. By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

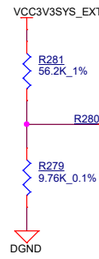
D-Note :-
VDDSHV_SD_IO
Refer pin connect table when SD card is not used



RESISTOR DIVIDER TBV

Vth : (0.45V+(+/-3% Tolerance))
Vth max: 0.4635
Vth min: 0.4365

AM64x Recommended Operating Conditions:
Vmin: 3.135V
Vnom: 3.3V
Vmax: 3.465V



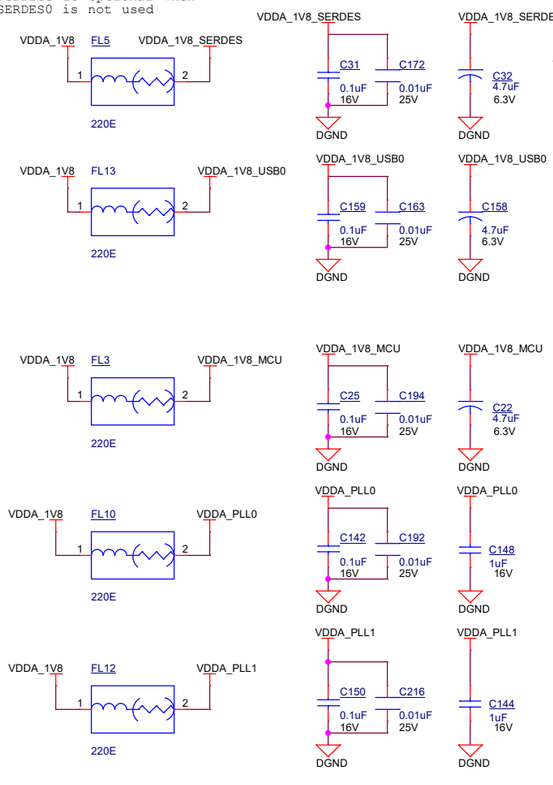
D-Note :-
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure

D-Note :-
Add a filter cap across R
Refer System Power Supply Monitor Design Guidelines section of SoC data sheet

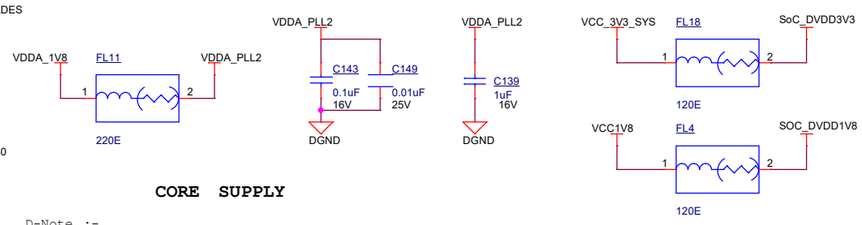
1.8V Analog SUPPLY

D-Note :-
Ferrite is optional when SERDES0 is not used

D-Note :-
Bulk caps are optional when SERDES0 is not used

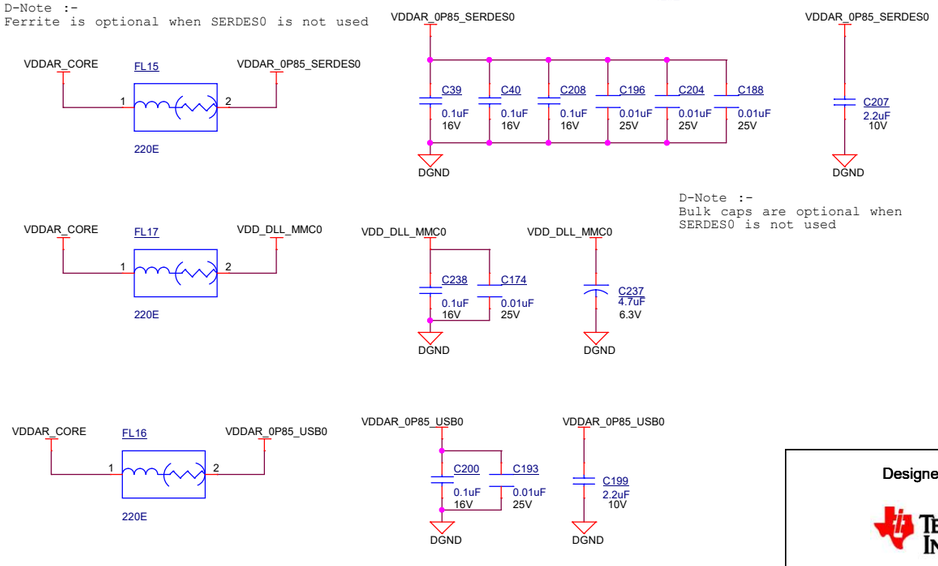


1.8V Analog SUPPLY



CORE SUPPLY

D-Note :-
Ferrite is optional when SERDES0 is not used



D-Note :-
Bulk caps are optional when SERDES0 is not used

PG2.0 Changes

If SR1.0 is installed, mount R522 and make R521 as DNI
If SR2.0 is installed, mount R521 and make R522 as DNI

R-Note :-
Currently shipped device are SR2.0

D-Note :-
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure
It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts. The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid false trigger
Refer System Power Supply Monitor Design Guidelines section of the data sheet

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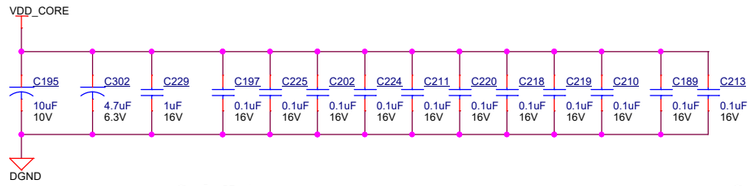
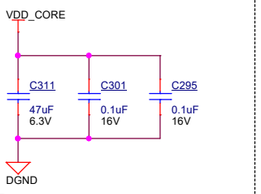
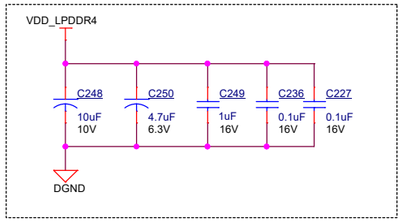
SOC POWER SUPPLIES - DECAPS

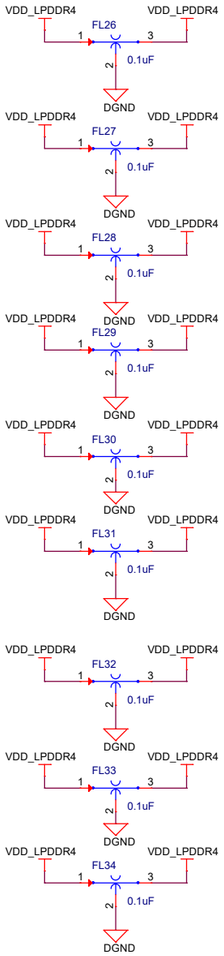


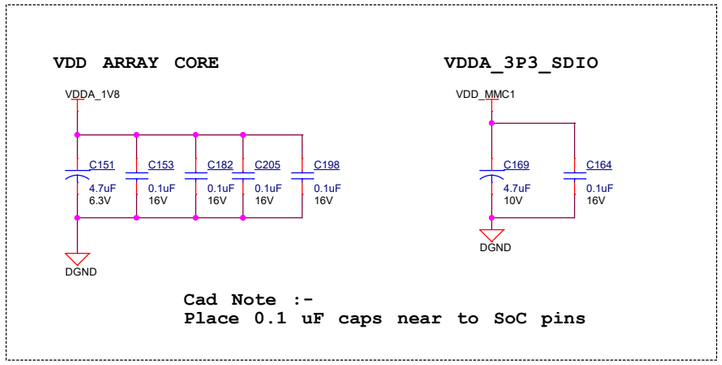
Cad Note :-
Place 0.1 uF caps near to SoC pins



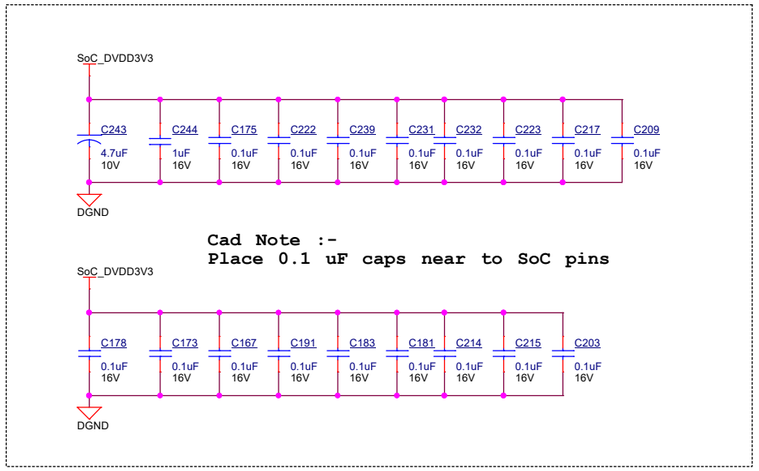
Cad Note :-
To place after current sense resistor on VDD_CORE plane







Cad Note :-
Place 0.1 uF caps near to SoC pins



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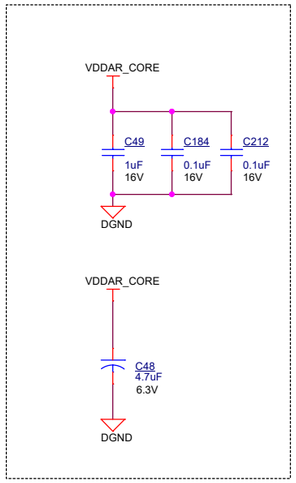

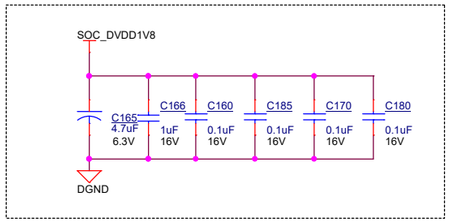

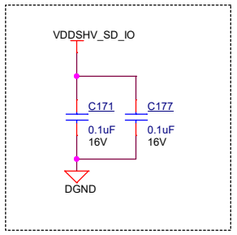

D-Note :-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IOs
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

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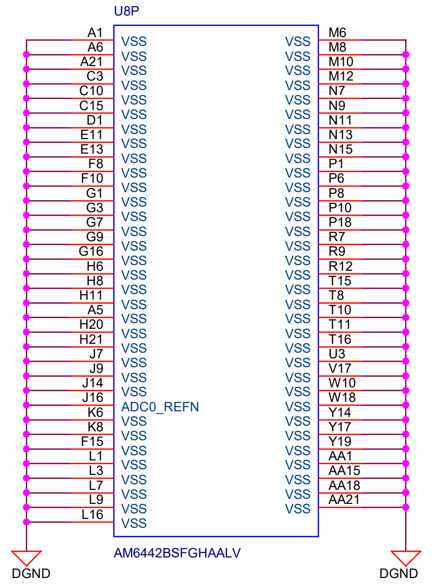
SOC POWER - VSS

D-Note :-
ADC0_REFN
Connect the decap to J16 directly
Connect J16 to ground through a 0R



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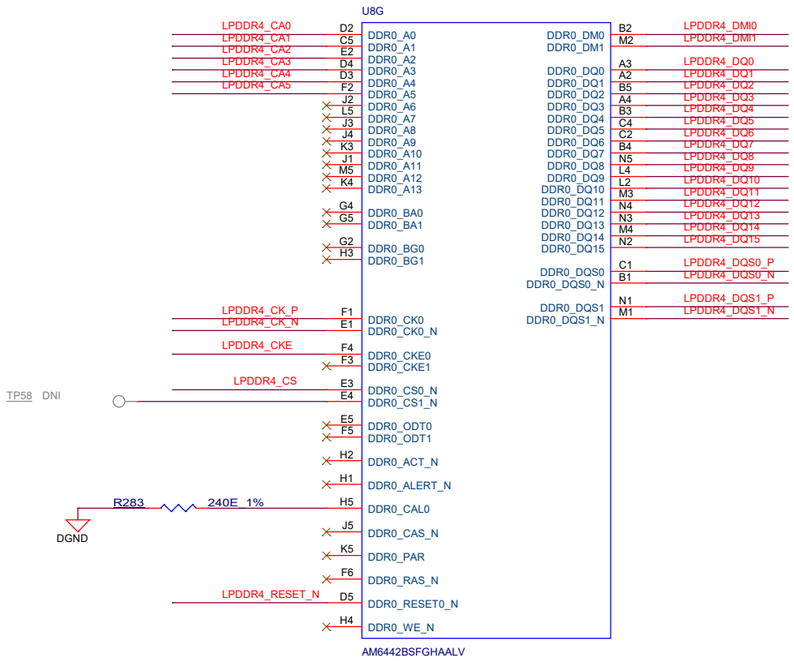
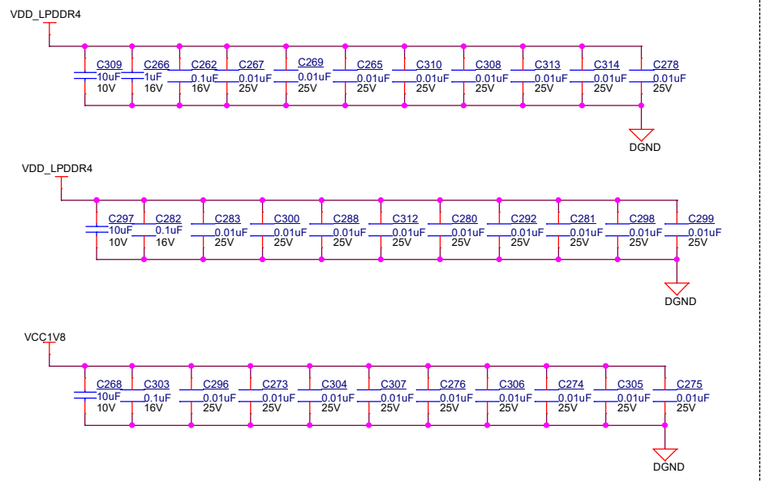
Title	SOC VSS			
Size	PROC100A 002		Rev	
C			A	
Date:	Tuesday, June 18, 2024	Sheet	12	of 43

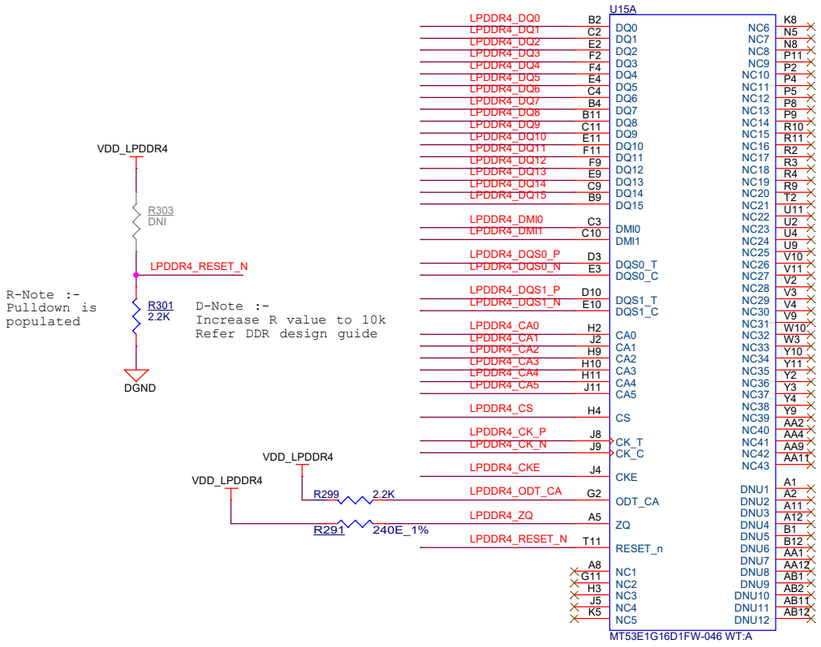
SOC LPDDR4 INTERFACE

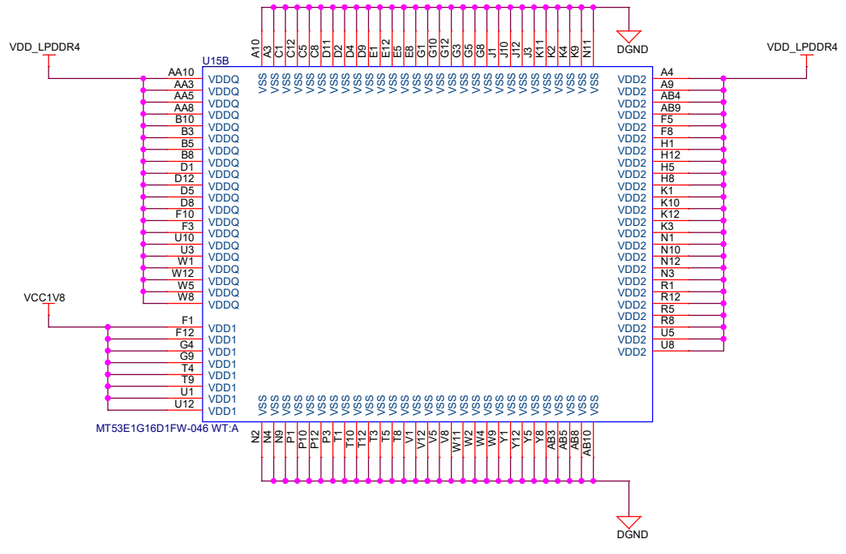


LPDDR4 POWER DECAPS



LPDDR4 DEVICE





Designed for TI by Mistral Solutions Pvt Ltd

Title	LPDDR4 INTERFACE		
Size C	PROC100A 002		Rev A
Date: Tuesday, June 18, 2024		Sheet 13 of 43	

WL1837 MODULE

D-Note :-
This family of processor implements a hard and dedicated PHY for eMMC interface.
The pull required for D0..D7, Clock and other eMMC interface control signals are enabled internal to the SOC during reset
Refer pin connectivity table for guidelines when eMMC is not used

D-Note :-
0E provision on MMC0_CLK
helps improve signal integrity

D-Note :-
MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)

Cad - Note :-
Place MMC1_CLK pulldown near to the SD card

R-Note :-
What is the reason we selected pulldown instead of pullup for SD card or other peripherals?
Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

U8I
AM6442BSFGHAALV

D-Note :-
Add a bulk cap near to the supply pin

MOD1A
WL1837MODGIMOCT

MOD1B
WL1837MODGIMOCT

BOOTMODE10/ BTUART RTS SELECT SWITCH

U2
TS5A3159MDBVREP

WILINK CONNECTOR

J17

PCB NOTE: PLACE SERIES RESISTOR NEAR WILINK CONNECTOR AND WLINK MODULE LIKE A TRIPAD RESISTOR, TO AVOID STUB

COM8 LEVEL TRANSLATOR-1

U3
SN74AVC4T245RSVR

COM8 LEVEL TRANSLATOR-2

U4
SN74AVC4T245RSVR

OFF PAGE CONNECTIONS

[25] WLAN_IRQ_LS	WLAN_IRQ_LS
[25] WLAN_EN_SoC_LS	WLAN_EN_SoC_LS
[25] BT_EN_SOC_LS	BT_EN_SOC_LS
[31] BT_HCI_TX_LS	BT_HCI_TX_LS
[31] BT_HCI_RX_LS	BT_HCI_RX_LS
[26] BT_HCI_CTS_LS	BT_HCI_CTS_LS
[25] COM8_LS_EN	COM8_LS_EN
[36] IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
[16] MMC1_D0	MMC1_D0
[16] MMC1_D1	MMC1_D1
[16] MMC1_D2	MMC1_D2
[14,16] MMC1_D3	MMC1_D3
[16] MMC1_CMD	MMC1_CMD
[16] MMC1_SDCD	MMC1_SDCD
[16] MMC1_CLK	MMC1_CLK
[26] BMODE10_GPMC_AD10	BMODE10_GPMC_AD10
[20] BOOTMODE10	BOOTMODE10
[25] BTUART_RTS_SEL	BTUART_RTS_SEL

Designed for TI by Mistral Solutions Pvt Ltd

Title	WL1837 MODULE	
Size C	PROC100A 002	Rev A
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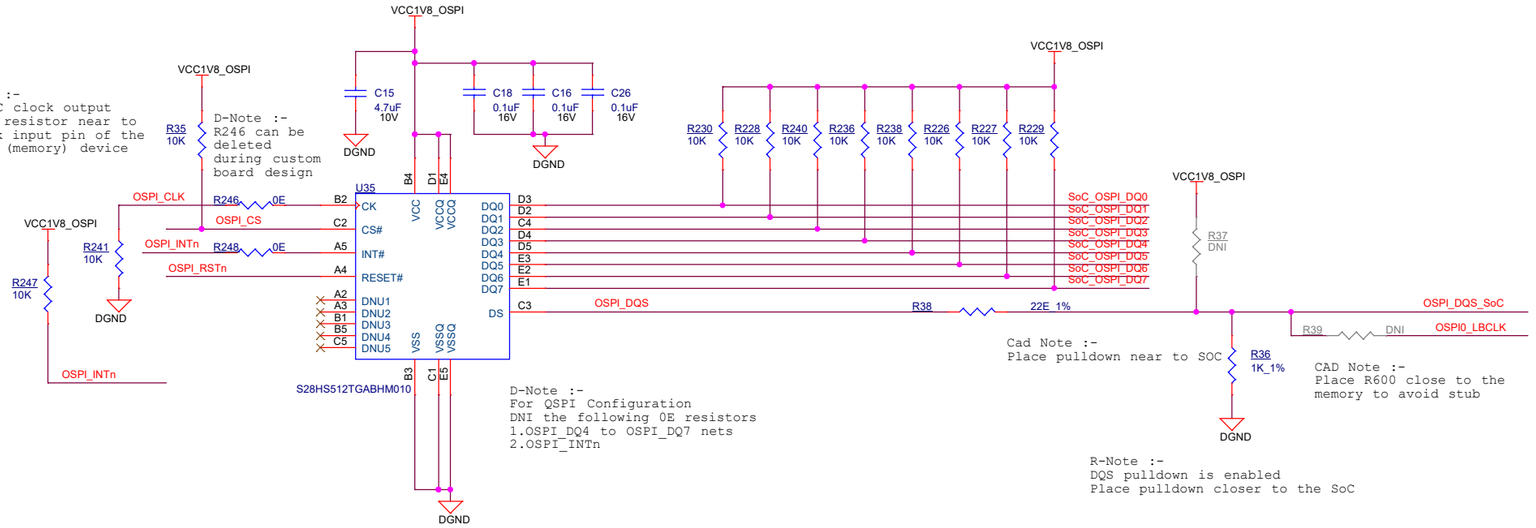
OSPI FLASH

R-Note :-
SOC IO buffers are off during power-up. A pullup is recommended near to the attached device, to hold the attached device IOs in a known state. Use of Pullups are attached device dependent

CAD Note :-
Place SOC clock output pulldown resistor near to the clock input pin of the attached (memory) device

D-Note :-
R246 can be deleted during custom board design



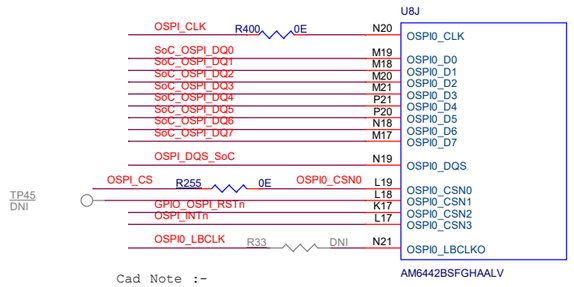
D-Note :-
For QSPI Configuration
DNI the following 0E resistors
1.OSPI_DQ4 to OSPI_DQ7 nets
2.OSPI_INTn

Cad Note :-
Place pulldown near to SOC

CAD Note :-
Place R600 close to the memory to avoid stub

R-Note :-
DQS pulldown is enabled
Place pulldown closer to the SoC

SOC OSPI INTERFACE

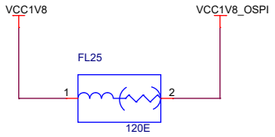


TP45 DNI

Cad Note :-
Place R33 close to the ball with as little trace as possible

R-Note :-
External loopback clock series resistors are DNI when DQS is connected

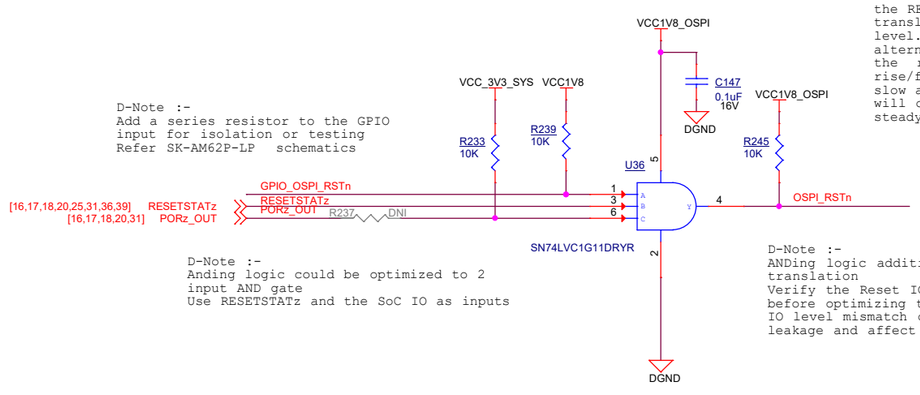
OSPI FLASH RESET



D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDI0 or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note :-
You could eliminate the GPIO option and only use the reset output (Warm or cold), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics



D-Note :-
Anding logic could be optimized to 2 input AND gate
Use RESETSTATz and the SoC IO as inputs

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

D-Note :-
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If too low it will cause the AM62x to source too much steady-state current during normal operation.

Designed for TI by Mistral Solutions Pvt Ltd

Title	OSPI INTERFACE		
Size	C	PROC100A 002	Rev A
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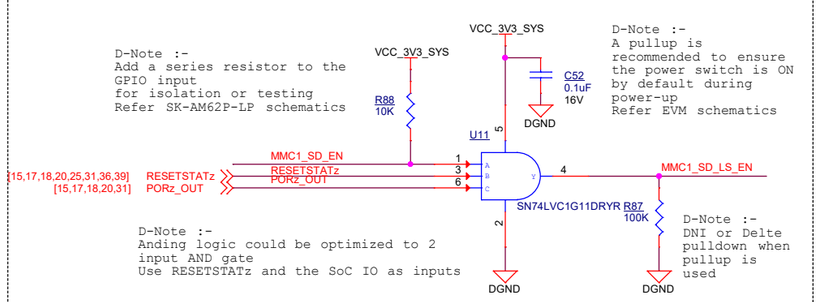
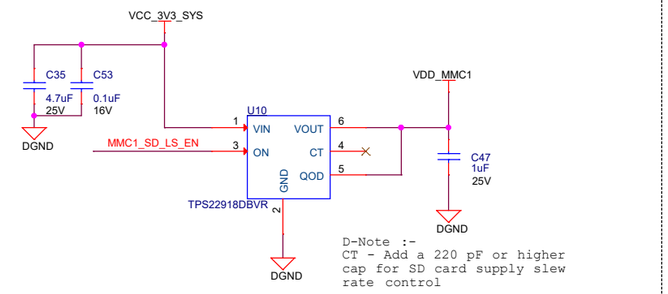
SD CARD INTERFACE

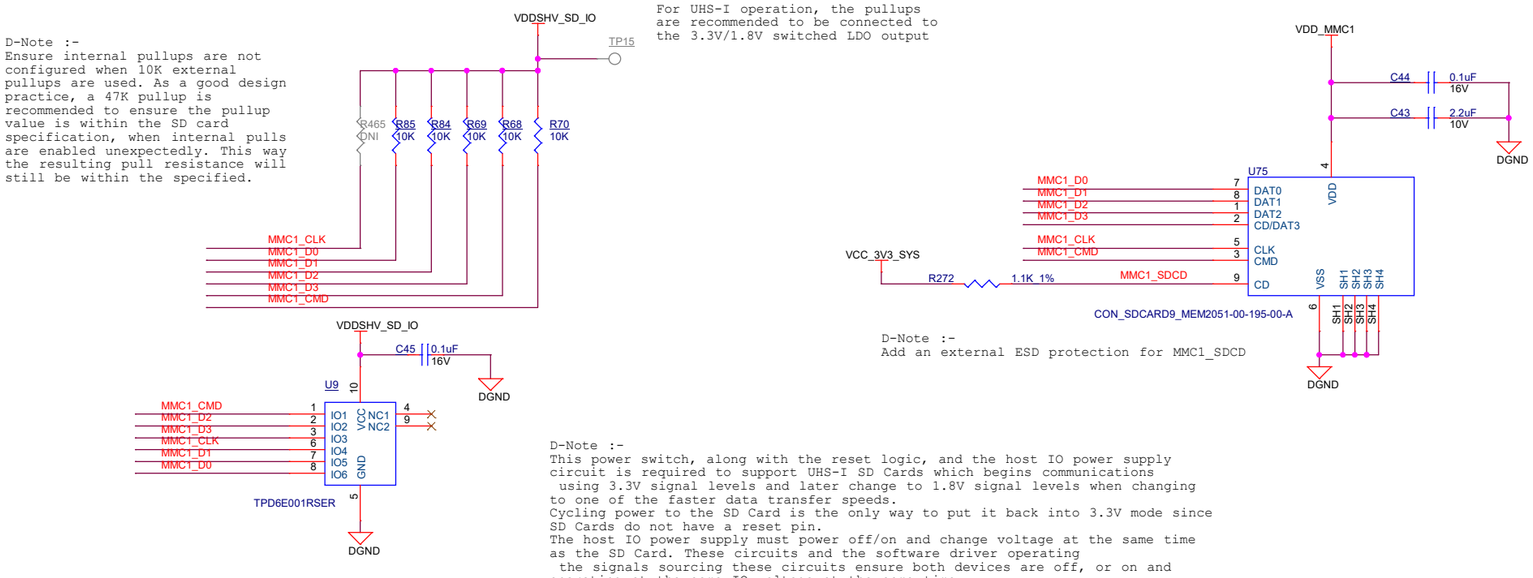
SD CARD RESET



LOAD SWITCH



SD CARD CONNECTOR



OFF PAGE CONNECTIONS

[14]	MMC1_CLK	MMC1_CLK
[36]	MMC1_SD_EN	MMC1_SD_EN
[14]	MMC1_D0	MMC1_D0
[14]	MMC1_D1	MMC1_D1
[14]	MMC1_D2	MMC1_D2
[14,16]	MMC1_D3	MMC1_D3
[14]	MMC1_CMD	MMC1_CMD
[14]	MMC1_SDCD	MMC1_SDCD

Designed for TI by Mistral Solutions Pvt Ltd

Title	SDCARD INTERFACE		
Size	C	PROC100A 002	Rev A
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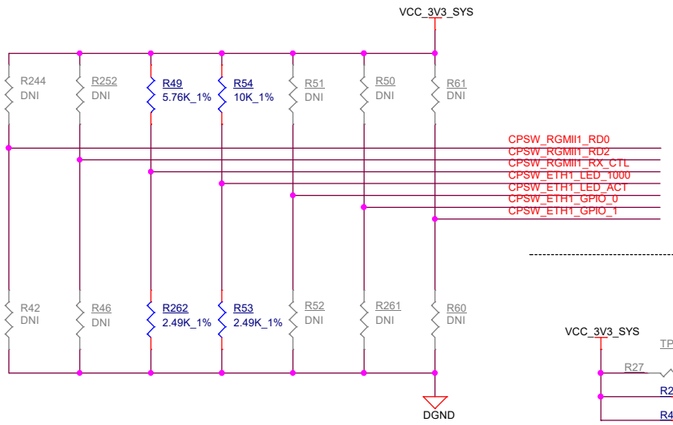
CPSW3G RGMII 1 - ETHERNET PHY

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

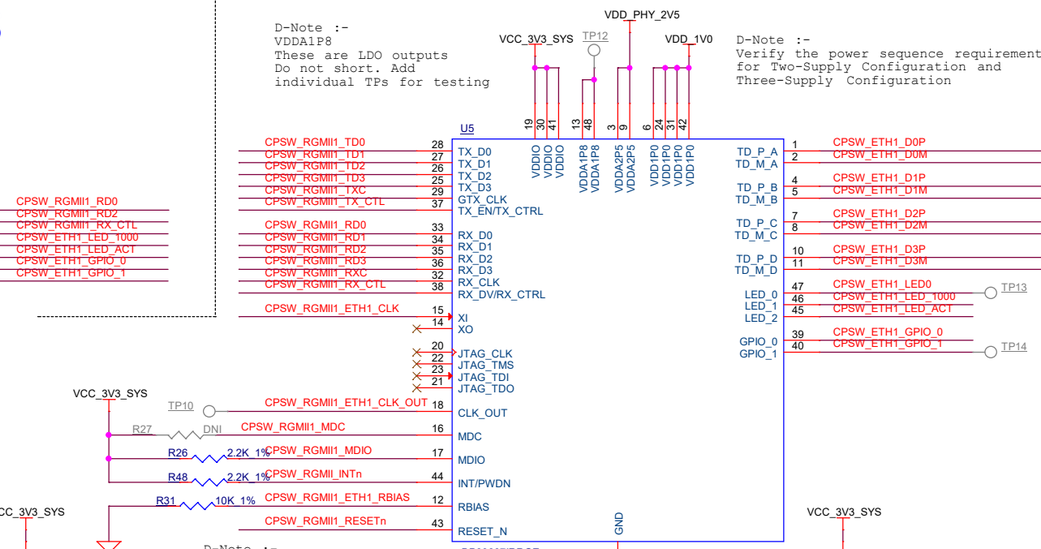
STRAPPING RESISTORS



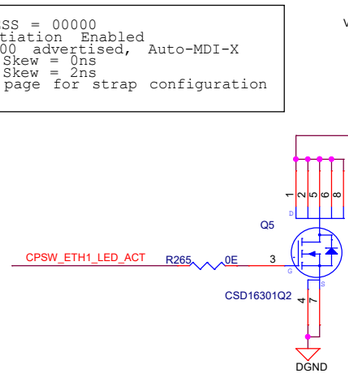
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
Refer 44 page for strap configuration

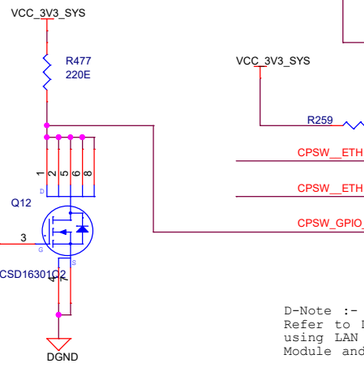
D-Note :-
VDDA1P8
These are LDO outputs
Do not short. Add
individual TPs for testing

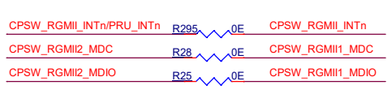
D-Note :-
Verify the power sequence requirements
for Two-Supply Configuration and
Three-Supply Configuration

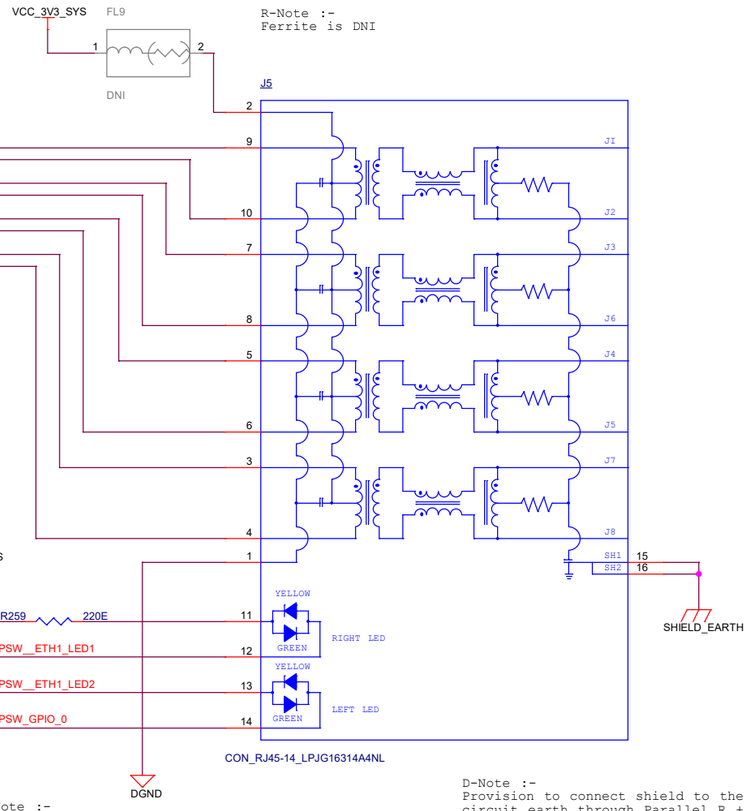


D-Note :-
Add a parallel 22 pF cap
These changes are for Ethernet
compliance test performance
improvement







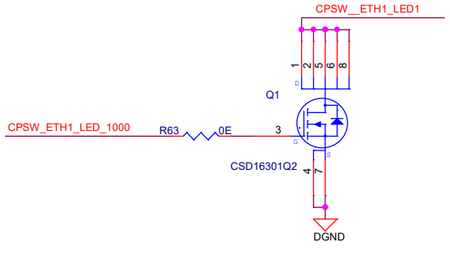


R-Note :-
Ferrite is DNI

D-Note :-
Refer to DP83867ERGZ-R-EVM when
using LAN Discrete Transformer
Module and RJ45 connector

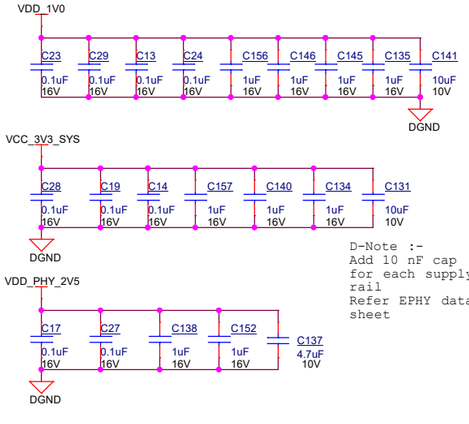
D-Note :-
Provision to connect shield to the
circuit earth through Parallel R +
C . Refer AM64x EVM schematics

LED STATUS



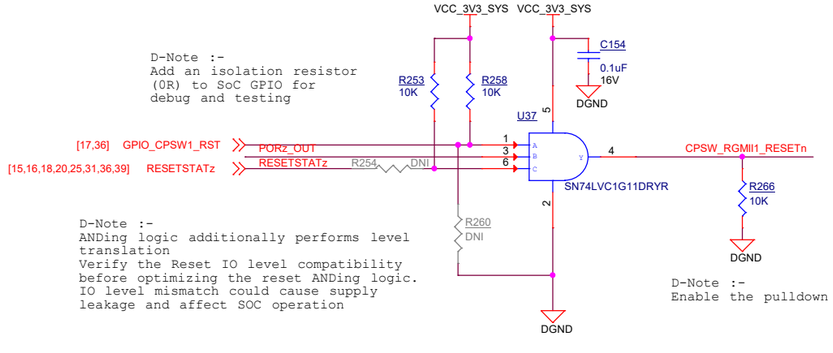
D-Note :-
The caps and values used are as per the
EPHY data sheet recommendations

DECAPS



D-Note :-
Add 10 nF cap
for each supply
rail
Refer EPHY data
sheet

CPSW3G EPHY - 1 RESET

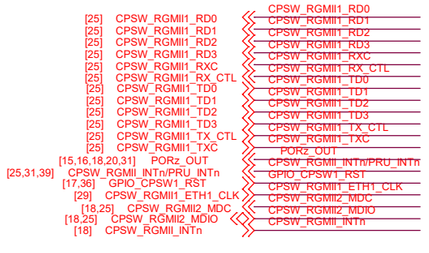


D-Note :-
Add an isolation resistor
(0R) to SoC GPIO for
debug and testing

D-Note :-
ANDing logic additionally performs level
translation
Verify the Reset IO level compatibility
before optimizing the reset ANDing logic.
IO level mismatch could cause supply
leakage and affect SOC operation

D-Note :-
Enable the pulldown

OFF PAGE CONNECTIONS



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Title	CPSW RGMII_1 ETHERNET PHY	
Size C	PROC100A 002	Rev A
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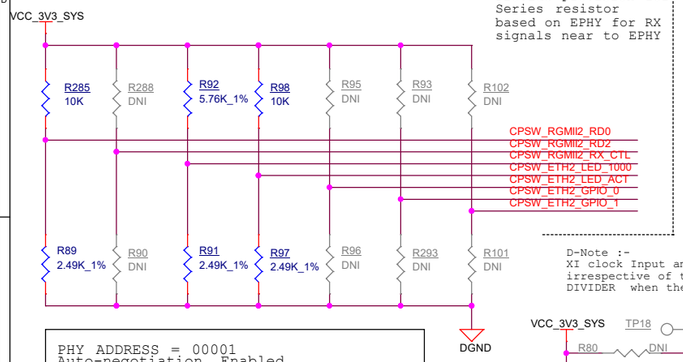
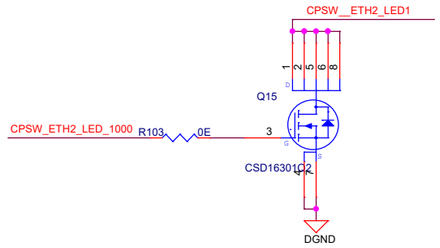
CPSW3G RGMII 2 - ETHERNET PHY

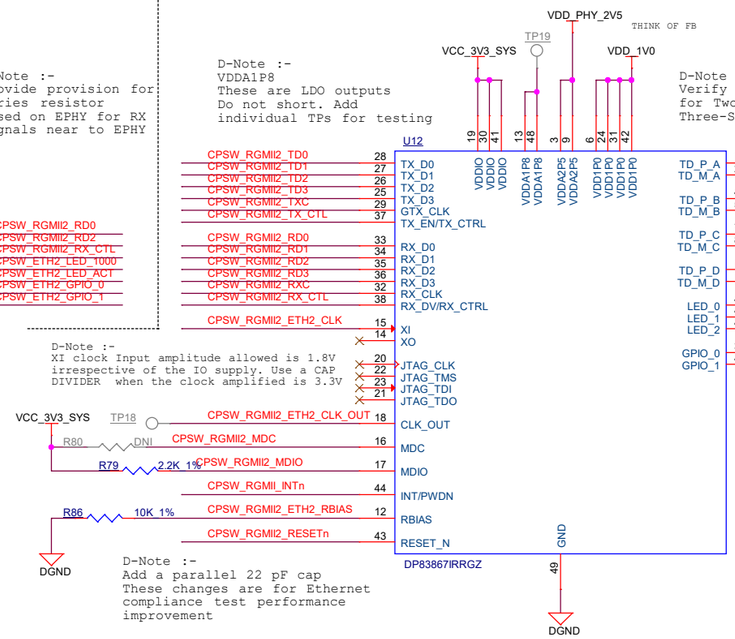
STRAPPING RESISTORS



D-Note :-
Provide provision for Series resistor based on EPHY for RX signals near to EPHY

PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
Refer 44 page for strap configuration



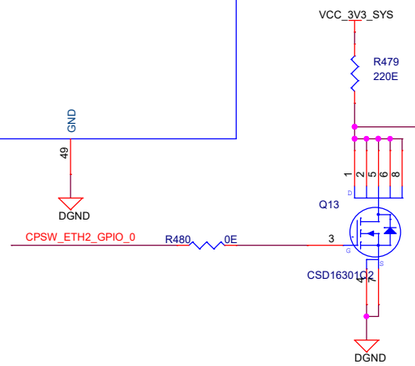


D-Note :-
VDDA1P8
These are LDO outputs
Do not short. Add individual TPs for testing

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

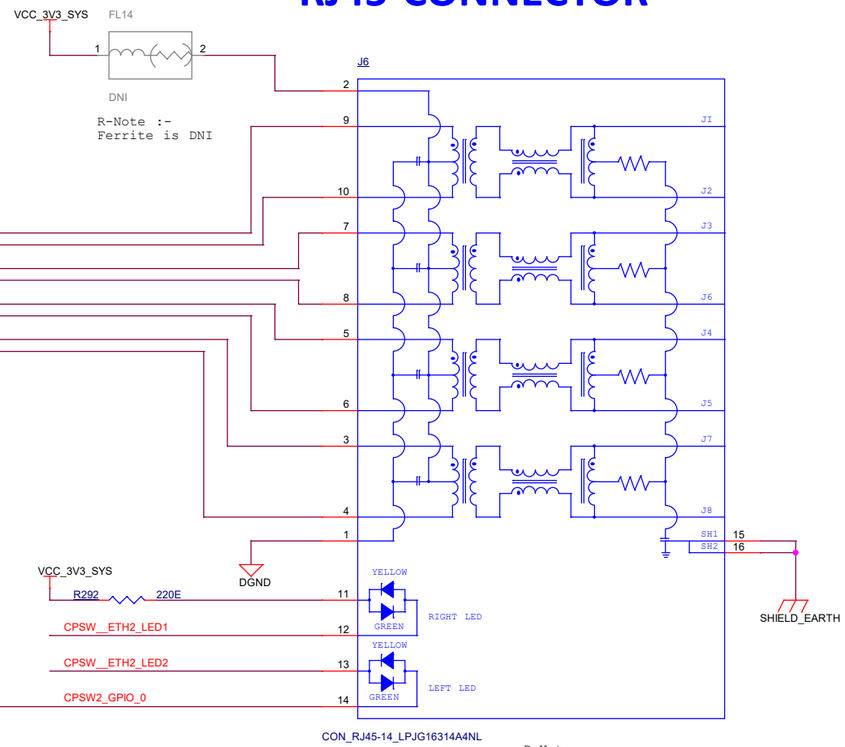
D-Note :-
XI clock Input amplitude allowed is 1.8V irrespective of the IO supply. Use a CAP DIVIDER when the clock amplified is 3.3V

D-Note :-
Add a parallel 22 pF cap These changes are for Ethernet compliance test performance improvement



D-Note :-
Refer to DP83867ERGZ-R-EVM when using LAN Discrete Transformer Module and RJ45 connector

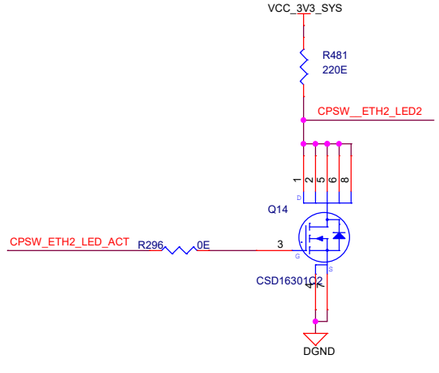
RJ45 CONNECTOR



R-Note :-
Ferrite is DNI

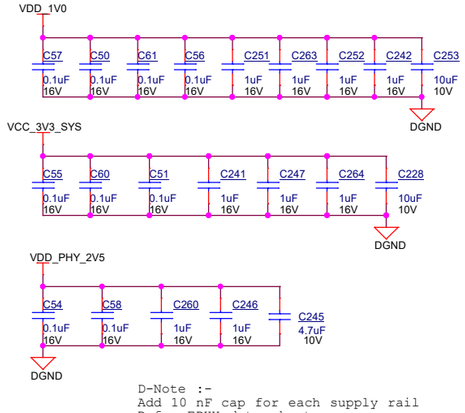
D-Note :-
Provision to connect shield to the circuit earth through Parallel R + C . Refer AM64x EVM schematics

CPSW PHY-2 SPEED AND ACTIVITY LED's DRIVERS



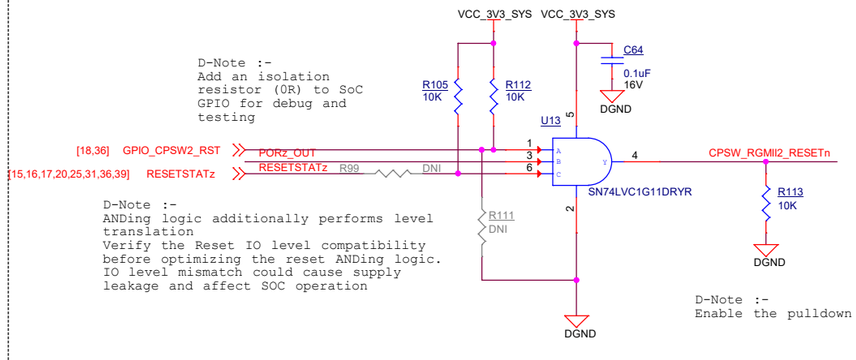
DECAPS

D-Note :-
The caps and values used are as per the EPHY data sheet recommendations



D-Note :-
Add 10 nF cap for each supply rail
Refer EPHY data sheet

CPSW3G EPHY - 2 RESET



D-Note :-
Add an isolation resistor (0R) to SoC GPIO for debug and testing

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

D-Note :-
Enable the pulldown

OFF PAGE CONNECTIONS

[25]	CPSW_RGMII2_RD0	CPSW_RGMII2_RD0
[25]	CPSW_RGMII2_RD1	CPSW_RGMII2_RD1
[25]	CPSW_RGMII2_RD2	CPSW_RGMII2_RD2
[25]	CPSW_RGMII2_RD3	CPSW_RGMII2_RD3
[25]	CPSW_RGMII2_RXC	CPSW_RGMII2_RXC
[25]	CPSW_RGMII2_RX_CTL	CPSW_RGMII2_RX_CTL
[25]	CPSW_RGMII2_TD0	CPSW_RGMII2_TD0
[25]	CPSW_RGMII2_TD1	CPSW_RGMII2_TD1
[25]	CPSW_RGMII2_TD2	CPSW_RGMII2_TD2
[25]	CPSW_RGMII2_TD3	CPSW_RGMII2_TD3
[25]	CPSW_RGMII2_TXC	CPSW_RGMII2_TXC
[25]	CPSW_RGMII2_TX_CTL	CPSW_RGMII2_TX_CTL
[15,16,17,20,31]	PORz_OUT	PORz_OUT
[18,36]	GPIO_CPSW2_RST	GPIO_CPSW2_RST
[29]	CPSW_RGMII2_ETH2_CLK	CPSW_RGMII2_ETH2_CLK
[17,25]	CPSW_RGMII2_MDC	CPSW_RGMII2_MDC
[17,25]	CPSW_RGMII2_MDIO	CPSW_RGMII2_MDIO
[17]	CPSW_RGMII_INTn	CPSW_RGMII_INTn

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Title	CPSW RGMII_2 ETHERNET PHY		
Size	PROC100A 002		Rev
C			A
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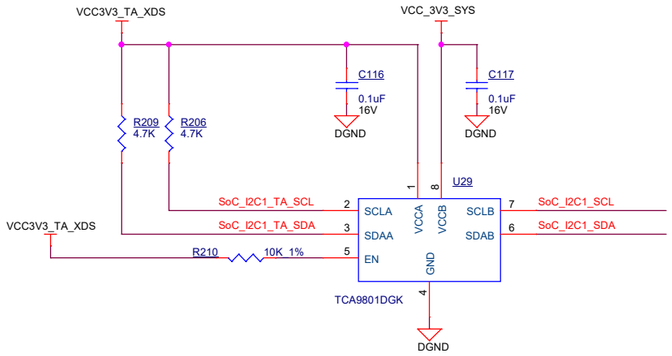
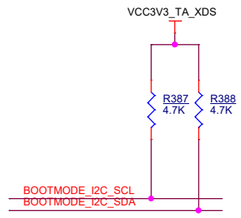
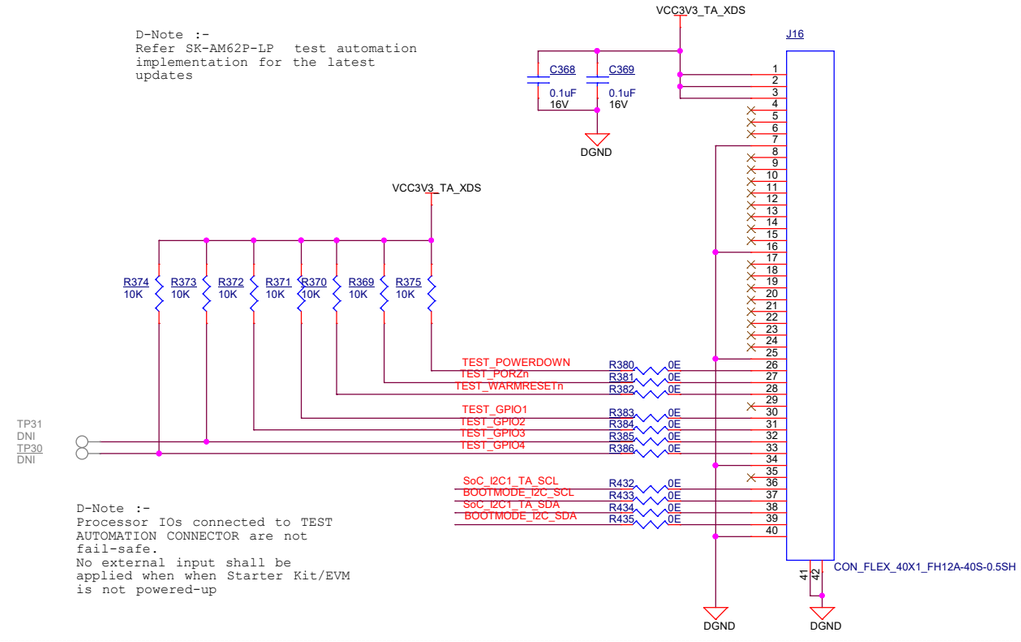
I2C BUS BUFFER

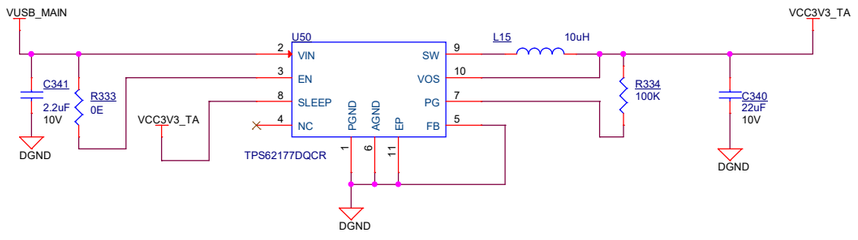




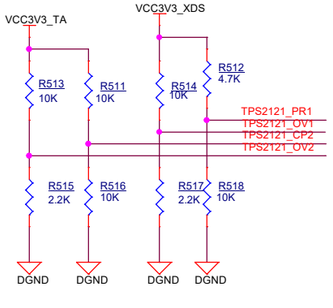
40-PIN AUTOMATION HEADER

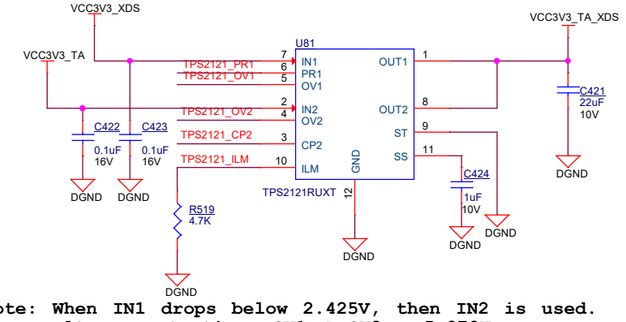


TEST AUTOMATION BOARD POWER



POWER MUX





Note: When IN1 drops below 2.425V, then IN2 is used.
Over voltage protection: OV1 & OV2 : 5.878V

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO1_59_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to SoC GPIO to Communicate	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Design	Specifications
VPR1	2.2V
VCP2	1.65V
VOV1	0.3V
VOV2	0.3V

OFF PAGE CONNECTIONS

[30,31,34,36] SoC_I2C1_SCL	SoC_I2C1_SCL
[30,31,34,36] SoC_I2C1_SDA	SoC_I2C1_SDA
[20,21] BOOTMODE_I2C_SCL	BOOTMODE_I2C_SCL
[20,21] BOOTMODE_I2C_SDA	BOOTMODE_I2C_SDA
[21,32] TEST_PORZn	TEST_PORZn
[21,39] TEST_POWERDOWN	TEST_POWERDOWN
[21,32] TEST_WARMRESETn	TEST_WARMRESETn
[21] TEST_GPIO2	TEST_GPIO2
[20,21] TEST_GPIO3	TEST_GPIO3
[20,21] TEST_GPIO4	TEST_GPIO4
[21,32] TEST_GPIO1	TEST_GPIO1
[21] SoC_I2C1_TA_SDA	SoC_I2C1_TA_SDA
[21] SoC_I2C1_TA_SCL	SoC_I2C1_TA_SCL

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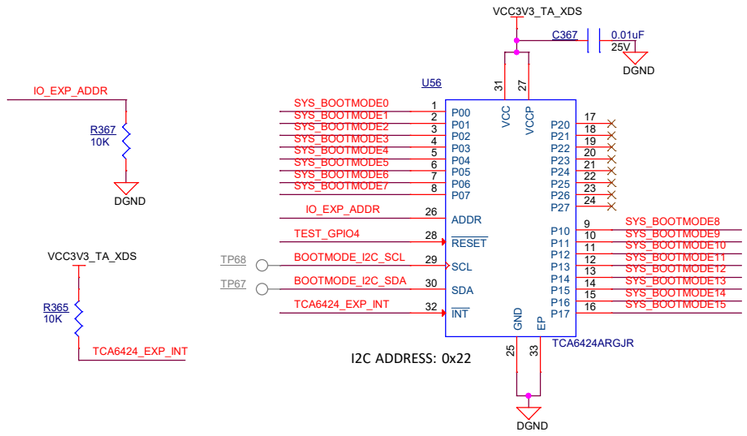
TEXAS INSTRUMENTS MISTRAL

Title	TEST AUTOMATION	
Size C	PROC100A 002	Rev A
Date: Tuesday, June 18, 2024	Sheet 19 of 43	

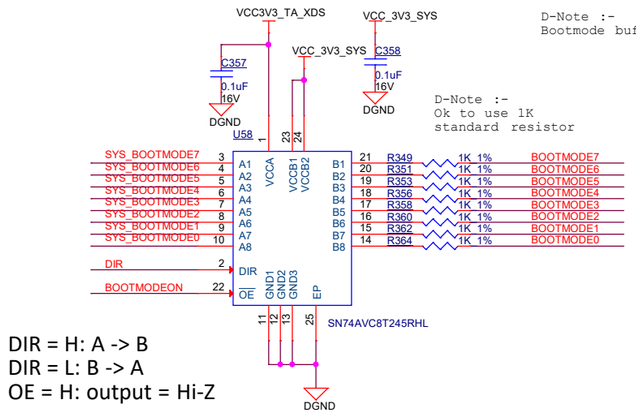
IO EXPANDER

D-Note :-
Add additional decap
Verify and terminate
unused IOs



I2C ADDRESS: 0x22

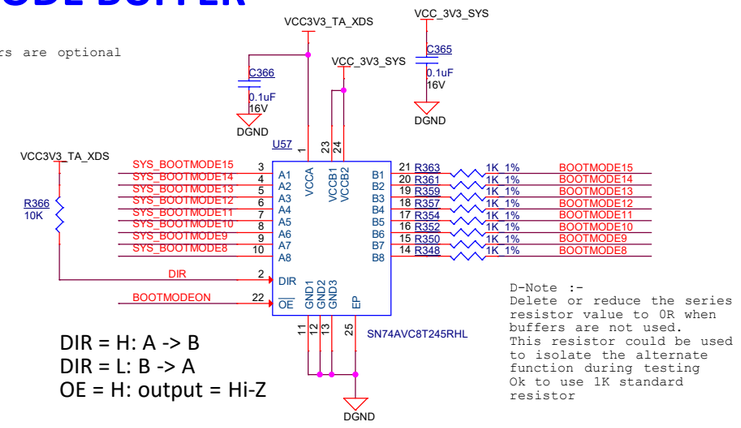
BOOT MODE BUFFER



D-Note :-
Ok to use 1K
standard resistor

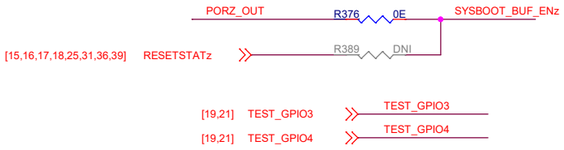
DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z

D-Note :-
Bootmode buffers are optional

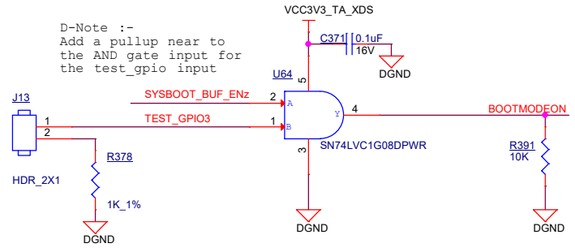


DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z

D-Note :-
Delete or reduce the series
resistor value to 0R when
buffers are not used.
This resistor could be used
to isolate the alternate
function during testing
Ok to use 1K standard
resistor



D-Note :-
Add a pullup near to
the AND gate input for
the test_gpio input



BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES

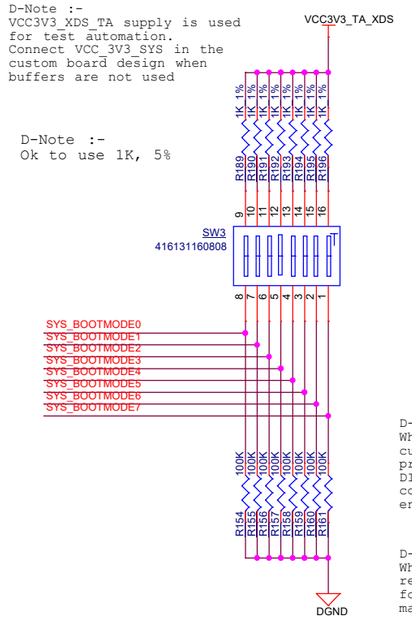
BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. CPSW Ethernet
4. USB Device
5. Ethernet

MCU Boot Mode Pins to be Finalized

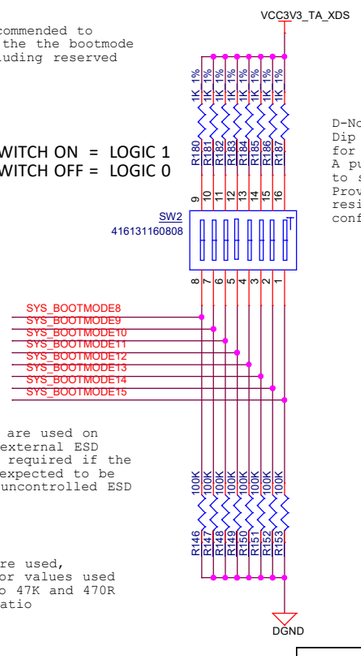
D-Note :-
VCC3V3_XDS_TA supply is used
for test automation.
Connect VCC_3V3_SYS in the
custom board design when
buffers are not used

D-Note :-
Ok to use 1K, 5%



D-Note :-
it is not recommended to
leave any of the the bootmode
pin open including reserved
pins

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

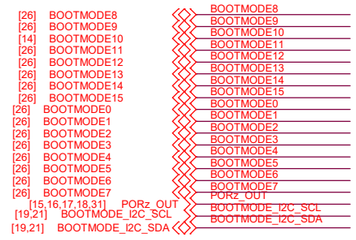


D-Note :-
Dip switch is optional and used on the SK
for ease of configuration
A pullup or pulldown resistor can be used
to set the BOOTMODE configuration
Provide provision for Pullup and Pulldown
resistors for the bootmode pins that have
configuration capability

D-Note :-
When dip switches are used on
custom board, an external ESD
protection may be required if the
DIP switches are expected to be
configured in an uncontrolled ESD
environment

D-Note :-
When DIP switch are used,
reduce the resistor values used
for the divider to 47K and 470R
maintaining the ratio

OFF PAGE CONNECTIONS



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Title	BOOT MODE BUFFER & SWITCHES		
Size C	PROC100A 002		Rev A
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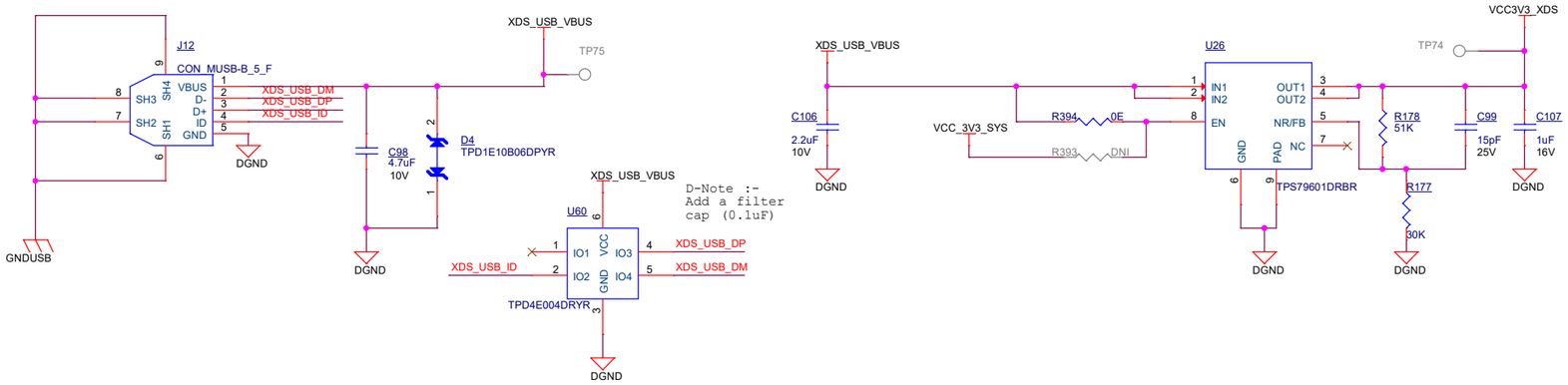
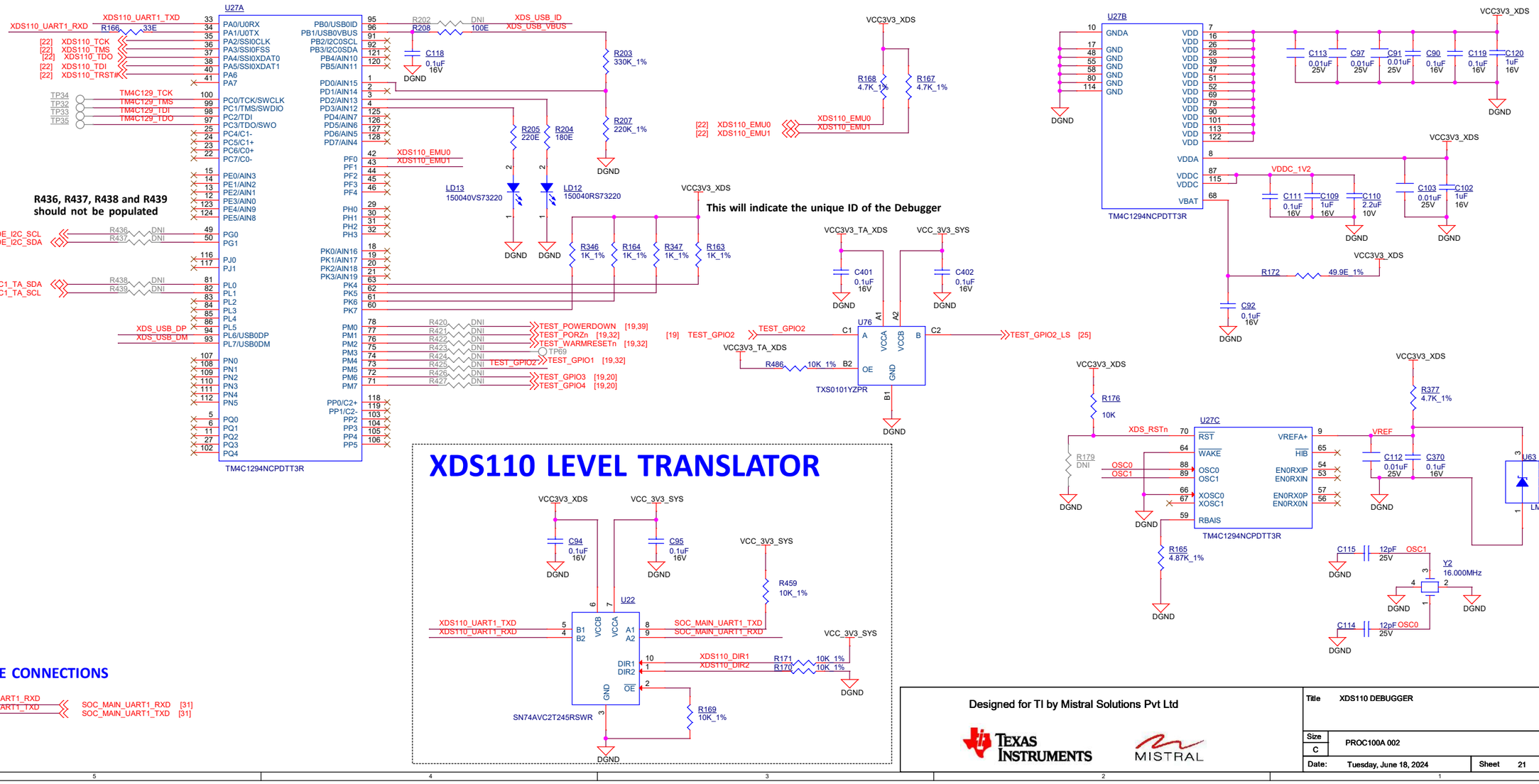
XDS110 POWER

USB Connector

D-Note :-
Please follow SK-AM62P-LP
implementations for latest
updates on XDS110



XDS110 DEBUGGER



XDS110 LEVEL TRANSLATOR

OFF PAGE CONNECTIONS

SOC_MAIN_UART1_RXD
SOC_MAIN_UART1_TXD
SOC_MAIN_UART1_RXD [31]
SOC_MAIN_UART1_TXD [31]

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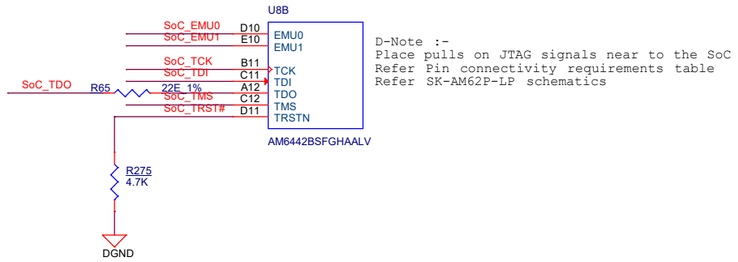
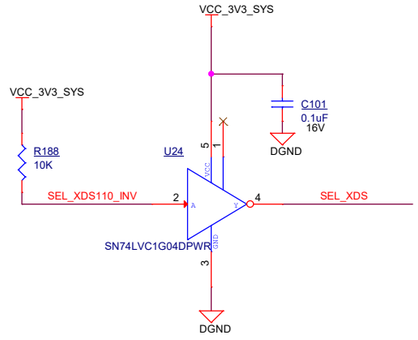
Title	XDS110 DEBUGGER	
Size	PROC100A 002	Rev
C		A
Date: Tuesday, June 18, 2024	Sheet 21 of 43	

JTAG SoC SECTION

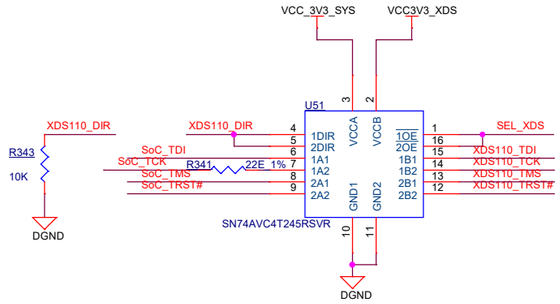


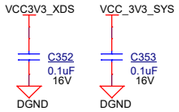
D-Note :-
Place pulls on JTAG signals near to the SoC
Refer Pin connectivity requirements table
Refer SK-AM62P-LP schematics

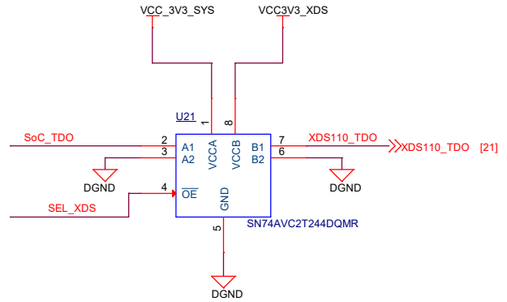
INVERTER

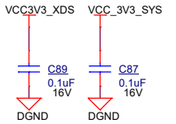


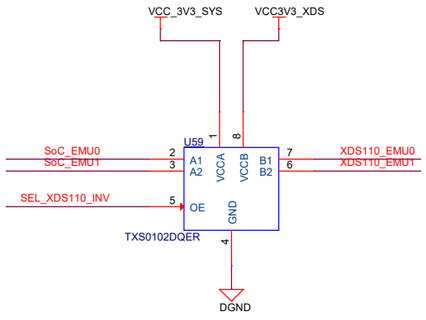
BUFFER XDS110

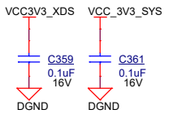












OFF PAGE CONNECTIONS

[23] SEL_XDS110_INV	SEL_XDS110_INV
[21] XDS110_TDI	XDS110_TDI
[21] XDS110_TCK	XDS110_TCK
[21] XDS110_TMS	XDS110_TMS
[21] XDS110_TRST#	XDS110_TRST#
[23] SoC_TDO	SoC_TDO
[23] SoC_TDI	SoC_TDI
[23] SoC_TCK	SoC_TCK
[23] SoC_TMS	SoC_TMS
[21] XDS110_EMU0	XDS110_EMU0
[21] XDS110_EMU1	XDS110_EMU1
[23] SEL_XDS	SEL_XDS
[23] SoC_EMU0	SoC_EMU0
[23] SoC_EMU1	SoC_EMU1
[23] SoC_TRST#	SoC_TRST#

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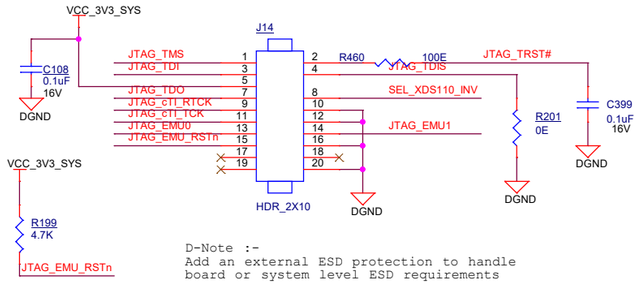
Title	JTAG BUFFER	
Size: C	PROC100A 002	Rev: A
Date: Tuesday, June 18, 2024	Sheet 22 of 43	

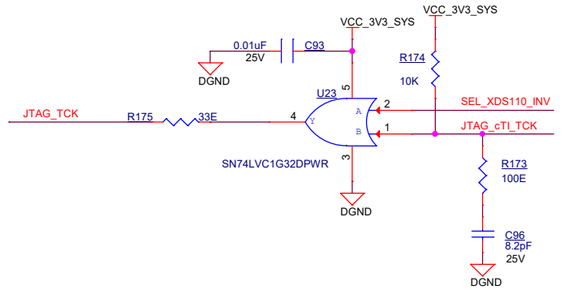
JTAG 20 PIN cTI CONNECTOR

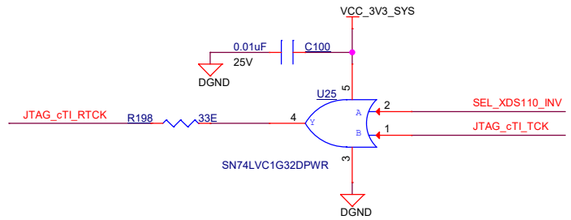


D-Note :-
Add an external ESD protection to handle
board or system level ESD requirements

D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled low, and thus the JTAG remains in reset as it is not being used.
When a JTAG pod is connected, the pod will eventually drive this signal high to release the JTAG logic from reset and enable a JTAG connection.

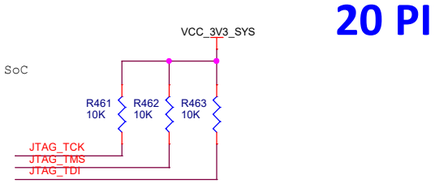
JTAG CLOCK BUFFER

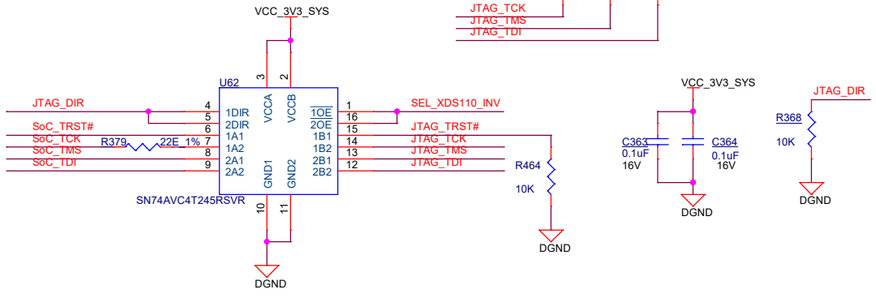


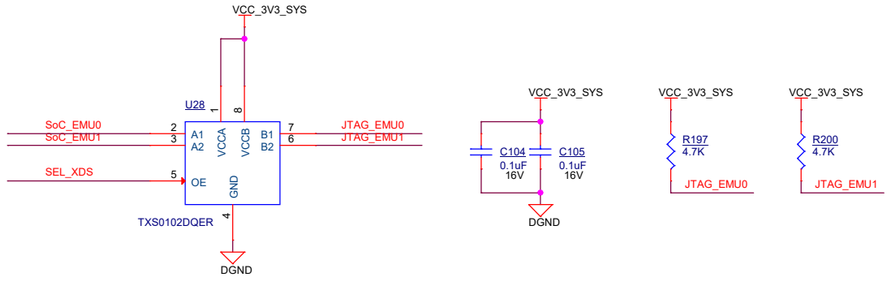


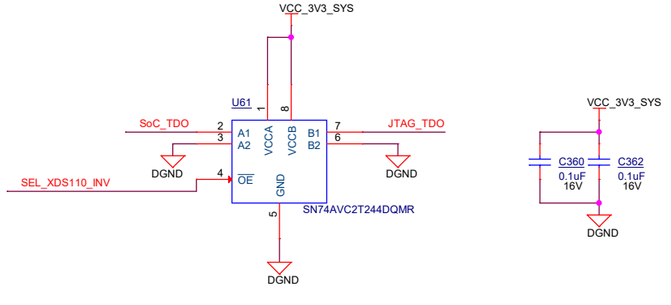
20 PIN JTAG BUFFERS

D-Note :-
Place pulls on JTAG signals near to the SoC
Refer SK-AM62P-LP schematics

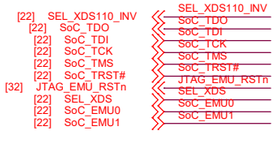








OFF PAGE CONNECTIONS



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Title	JTAG 20 PIN cTI CONNECTOR	
Size C	PROC100A 002	Rev A
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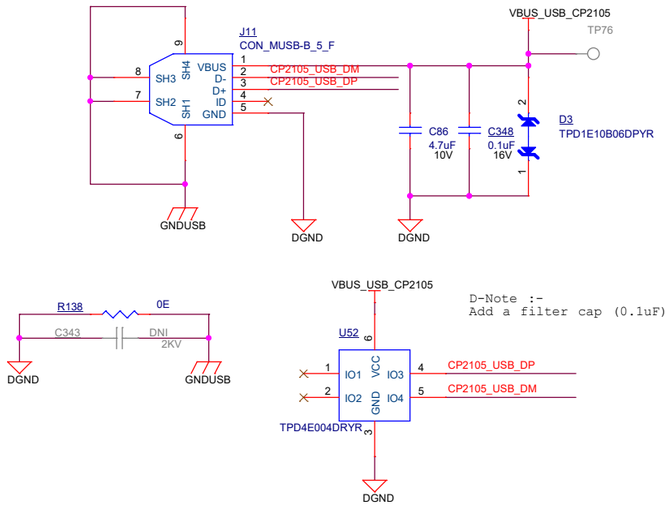
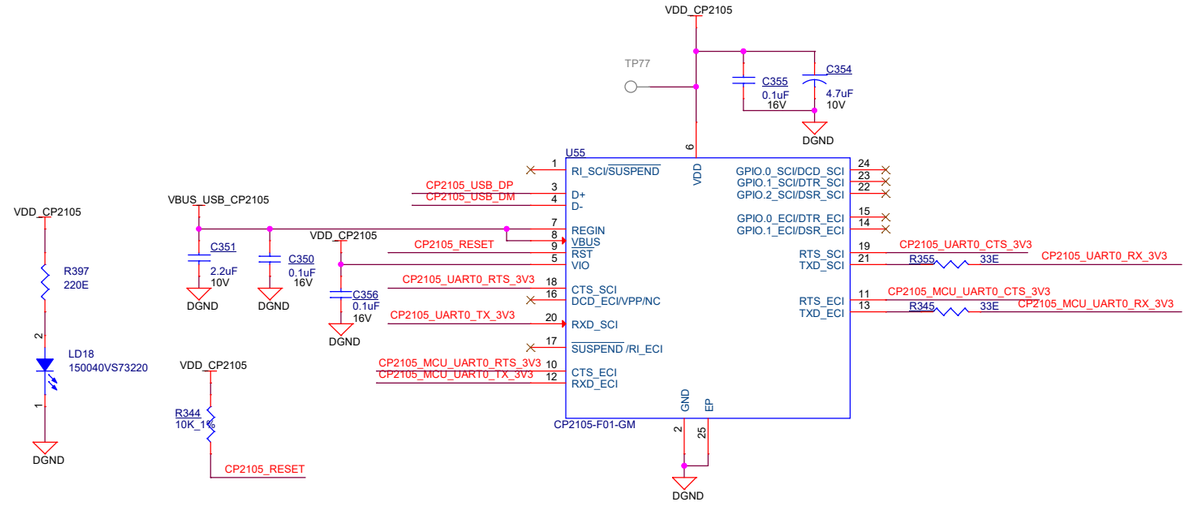
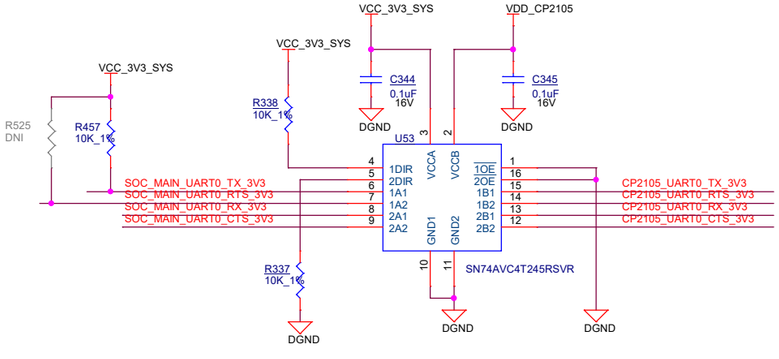
USB Micro B CONNECTOR

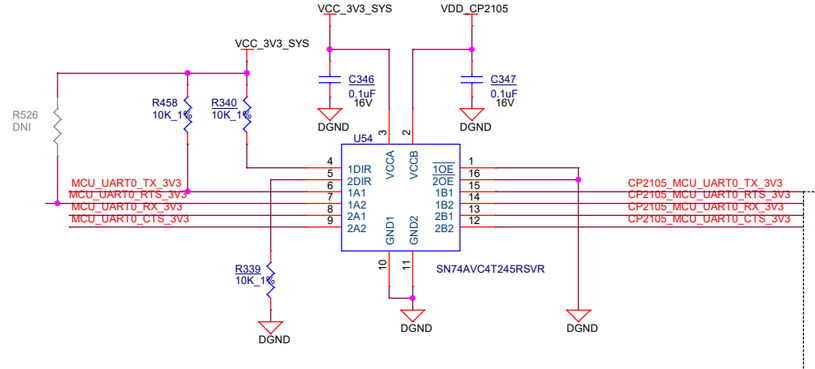


USB TO DUAL UART BRIDGE



CP2105 LEVEL TRANSLATOR





OFF PAGE CONNECTIONS

SOC_MAIN_UART0_RX_3V3 >> SOC_MAIN_UART0_RX_3V3 [31]
SOC_MAIN_UART0_TX_3V3 >> SOC_MAIN_UART0_TX_3V3 [31]
SOC_MAIN_UART0_RTS_3V3 >> SOC_MAIN_UART0_RTS_3V3 [31]
SOC_MAIN_UART0_CTS_3V3 >> SOC_MAIN_UART0_CTS_3V3 [31]

MCU_UART0_RX_3V3 >> MCU_UART0_RX_3V3 [31]
MCU_UART0_TX_3V3 >> MCU_UART0_TX_3V3 [31]
MCU_UART0_RTS_3V3 >> MCU_UART0_RTS_3V3 [31]
MCU_UART0_CTS_3V3 >> MCU_UART0_CTS_3V3 [31]

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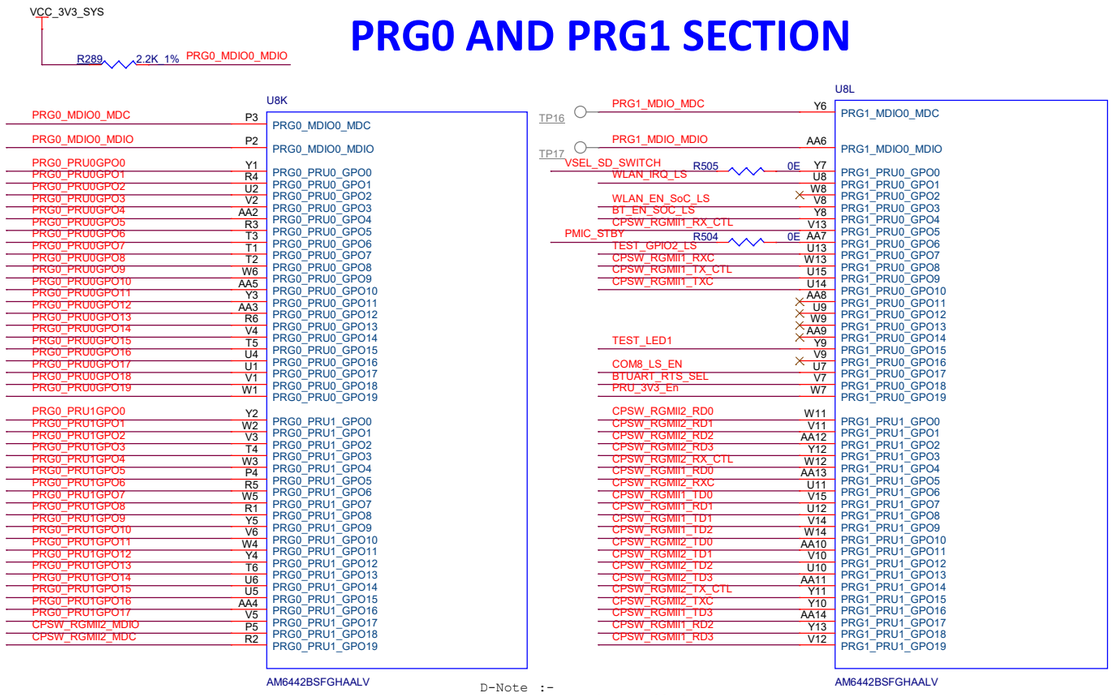
Title	CP2105 UART TO USB BRIDGE	
Size: C	PROC100A 002	Rev: A
Date: Tuesday, June 18, 2024	Sheet 24 of 43	

PRG0 AND PRG1 SECTION



D-Note :-
Add series resistors 22 R on the Ethernet interface TX (TDx) signals near to the SoC

PRU HEADER

NOTE:

AM64x Starter Kit shall not be powered through the 3V3 pins on the PRU Connector.

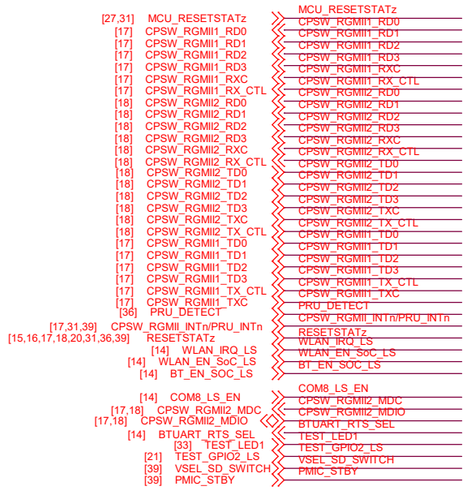
PRU Connector I/O are not fail-safe and shall not be driven when AM64x Starter Kit is not powered.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

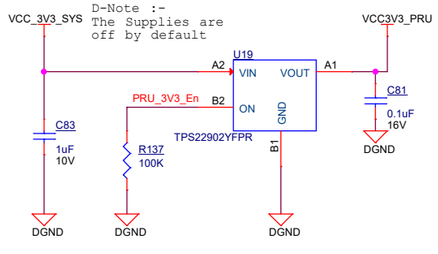
D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull

D-Note:-
Processor IOs connected to PRU Header are not fail-safe.
No external input shall be driven when Starter Kit is not powered-up.

OFF PAGE CONNECTIONS



LOAD SWITCH FOR 3.3V TO PRU CONNECTOR



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Title	PRU CONNECTOR		
Size C	PROC100A 002		Rev A
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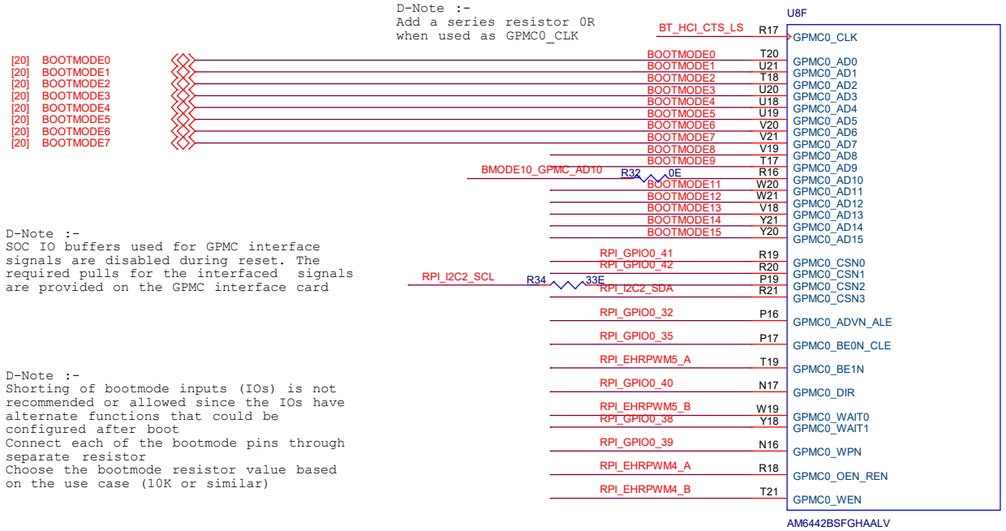
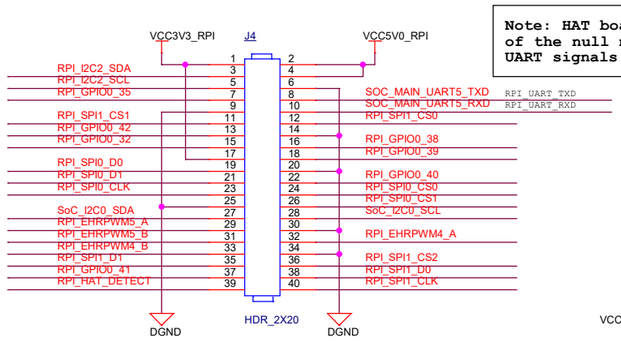
GPMC



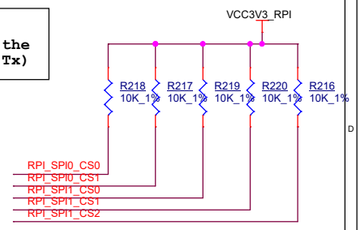
D-Note :-
SOC IO buffers used for GPMC interface signals are disabled during reset. The required pulls for the interfaced signals are provided on the GPMC interface card

D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot
Connect each of the bootmode pins through separate resistor
Choose the bootmode resistor value based on the use case (10K or similar)

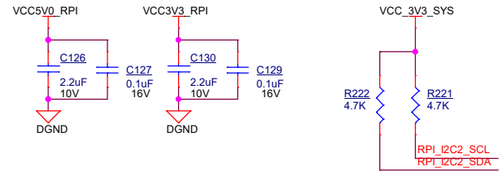
USER EXPANSION CONNECTOR



Note: HAT boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



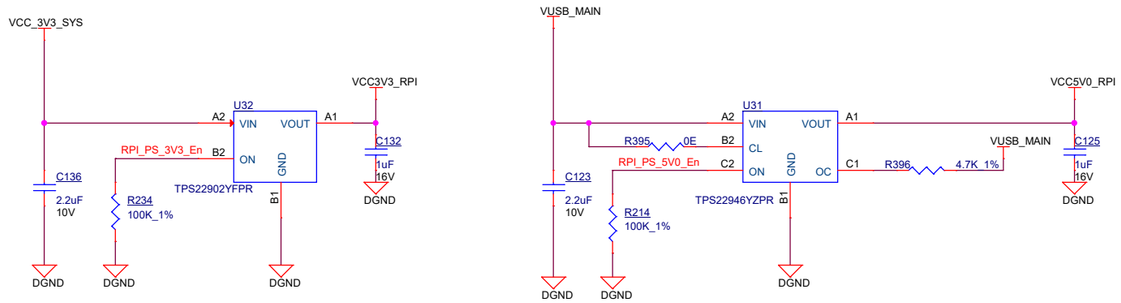
D-Note :-
Processor IOs connected to User expansion connector are not fail-safe. No external input shall be driven when Starter Kit is not powered-up.



Note: This connector is compatible to GPIO Expansion Header (J8) found on the Raspberry Pi Boards

Note: Raspberry Pi is the trademark / wordmark of Raspberry Pi Foundation

LOAD SWITCH FOR USER EXPANSION CONNECTOR



D-Note :-

AM64x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM64x Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

OFF PAGE CONNECTIONS

RPI_HAT_DETECT	RPI_HAT_DETECT [36]
RPI_SPI1_CLK	RPI_SPI1_CLK [31]
RPI_SPI1_D0	RPI_SPI1_D0 [31]
RPI_SPI1_D1	RPI_SPI1_D1 [31]
RPI_SPI1_CS0	RPI_SPI1_CS0 [31]
RPI_SPI1_CS1	RPI_SPI1_CS1 [31]
RPI_SPI1_CS2	RPI_SPI1_CS2 [31]
RPI_SPI0_CLK	RPI_SPI0_CLK [31]
RPI_SPI0_D0	RPI_SPI0_D0 [31]
RPI_SPI0_D1	RPI_SPI0_D1 [31]
RPI_SPI0_CS0	RPI_SPI0_CS0 [31]
RPI_SPI0_CS1	RPI_SPI0_CS1 [31]
SoC_I2C0_SCL	SoC_I2C0_SCL [25,31,35,39]
SoC_I2C0_SDA	SoC_I2C0_SDA [25,31,35,39]
BT_HCI_CTS_LS	BT_HCI_CTS_LS [14]
BOOTMODE8	BOOTMODE8 [20]
BOOTMODE9	BOOTMODE9 [20]
BOOTMODE11	BOOTMODE11 [20]
BOOTMODE12	BOOTMODE12 [20]
BOOTMODE13	BOOTMODE13 [20]
BOOTMODE14	BOOTMODE14 [20]
BOOTMODE15	BOOTMODE15 [20]
SOC_MAIN_UART5_RXD	SOC_MAIN_UART5_RXD [31]
SOC_MAIN_UART5_TXD	SOC_MAIN_UART5_TXD [31]
RPI_PS_3V3_En	RPI_PS_3V3_En [36]
RPI_PS_5V0_En	RPI_PS_5V0_En [36]
BMODE10_GPMC_AD10	BMODE10_GPMC_AD10 [14]

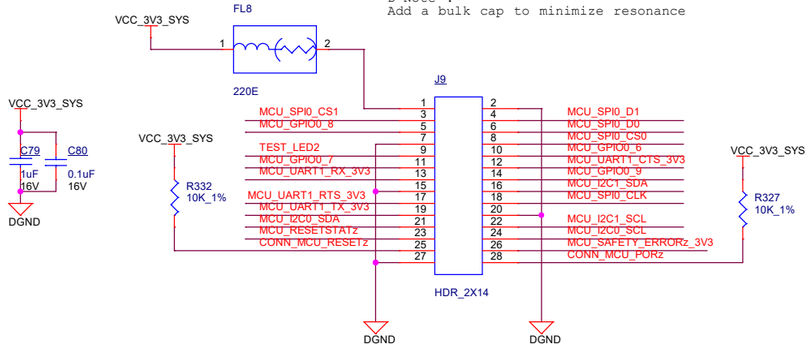
Designed for TI by Mistral Solutions Pvt Ltd

Title	USER EXPANSION CONNECTOR	
Size	PROC100A 002	Rev
C		A
Date:	Tuesday, June 18, 2024	Sheet 26 of 43

SOC MCU CONNECTOR

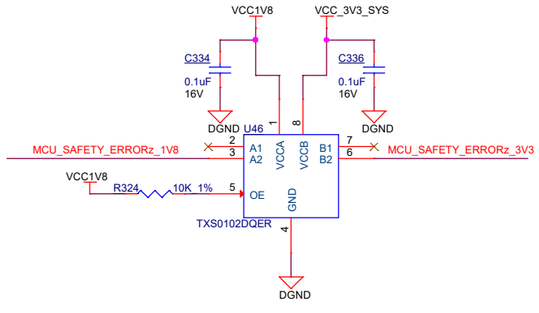
Only 100mA supported on this pin

D-Note :-
Add a bulk cap to minimize resonance



D-Note :-
Processor IOs connected to SOC MCU
connector are not fail-safe.
No external input shall be driven
when Starter Kit is not powered-up.

LEVEL TRANSLATOR



OFF PAGE CONNECTIONS

[32]	CONN_MCU_RESETz	CONN_MCU_RESETz
[32]	CONN_MCU_PORz	CONN_MCU_PORz
[31]	MCU_SPI0_CS1	MCU_SPI0_CS1
[31]	MCU_GPIO0_8	MCU_GPIO0_8
[31,33]	TEST_LED2	TEST_LED2
[31]	MCU_GPIO0_7	MCU_GPIO0_7
[31]	MCU_UART1_RX_3V3	MCU_UART1_RX_3V3
[31]	MCU_UART1_RTS_3V3	MCU_UART1_RTS_3V3
[31]	MCU_UART1_TX_3V3	MCU_UART1_TX_3V3
[31]	MCU_I2C0_SDA	MCU_I2C0_SDA
[25,31]	MCU_RESETSTATz	MCU_RESETSTATz
[31]	MCU_SPI0_D1	MCU_SPI0_D1
[31]	MCU_SPI0_D0	MCU_SPI0_D0
[31]	MCU_SPI0_CS0	MCU_SPI0_CS0
[31,32]	MCU_GPIO0_6	MCU_GPIO0_6
[31]	MCU_UART1_CTS_3V3	MCU_UART1_CTS_3V3
[31]	MCU_GPIO0_9	MCU_GPIO0_9
[31]	MCU_I2C1_SDA	MCU_I2C1_SDA
[31]	MCU_SPI0_CLK	MCU_SPI0_CLK
[31]	MCU_I2C1_SCL	MCU_I2C1_SCL
[31]	MCU_I2C0_SCL	MCU_I2C0_SCL
[31]	MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8

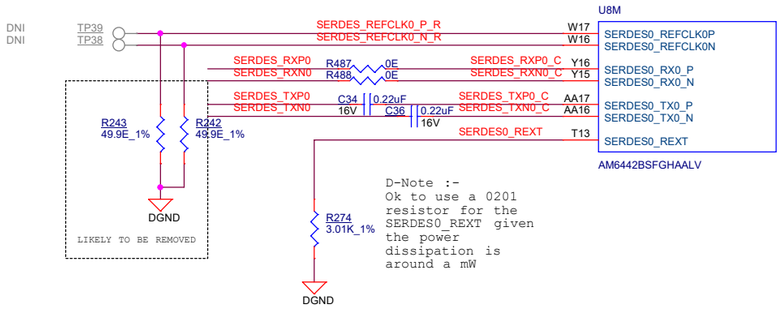
Designed for TI by Mistral Solutions Pvt Ltd

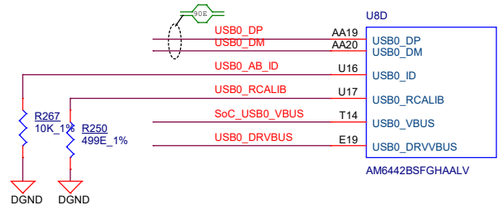
Title	MCU CONNECTOR		
Size C	PROC100A 002		Rev A
Date:	Tuesday, June 18, 2024	Sheet 27 of 43	

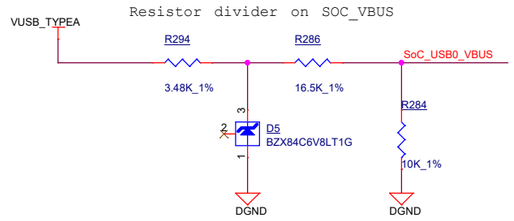
USB 3.0 INTERFACE

D-Note :-
SERDES0 inputs are not fail-safe.
If clock or data inputs are available before the SOC supply ramps, VDDR_CORE rail could be affected causing booting issues based on the power architecture implementation.

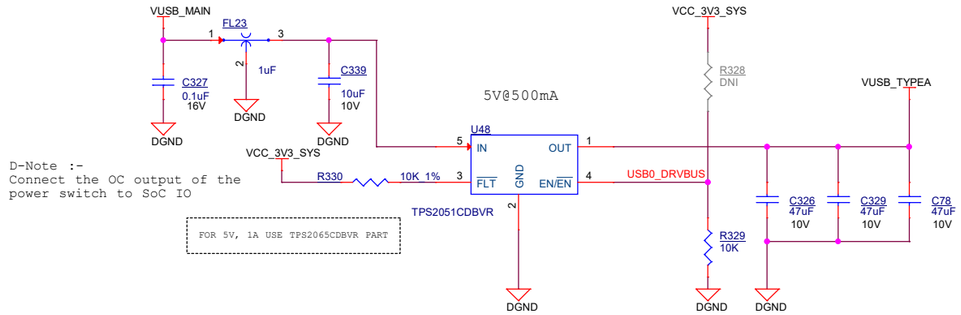
D-Note :-
Errata i2326 PCIe refclk Applicable?
i2326 does not apply when PCIe refclk is from an external source. It only applies if AM64x is generating the refclk.



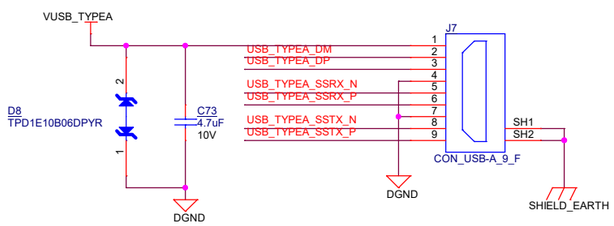


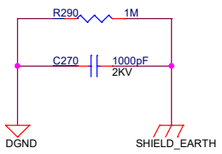


5V Power switch for USB 3.0 Device

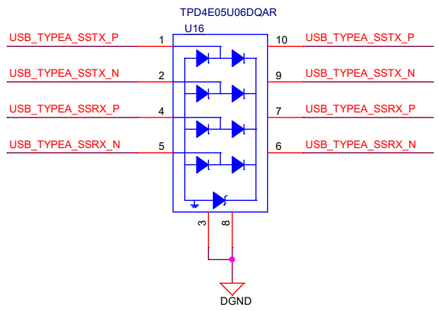


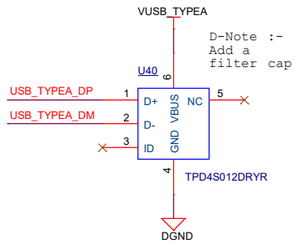
Type-A Connector



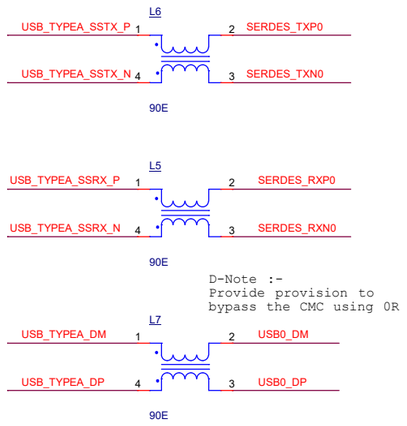


ESD DIODES





CHOKE



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Title	USB 3.0 INTERFACE		
Size C	PROC100A 002		Rev A
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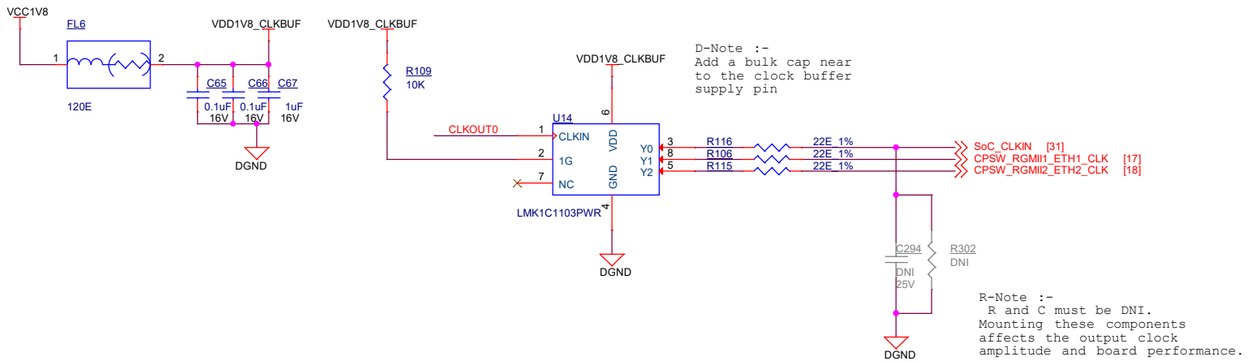
SOC AND ETHERNET PHY CLOCK BUFFER



OFF PAGE CONNECTIONS

[31,37] CLKOUT0 <<— CLKOUT0

Designed for TI by Mistral Solutions Pvt Ltd

Title	ETHERNET PHY CLOCK BUFFER	
Size C	PROC100A 002	Rev A
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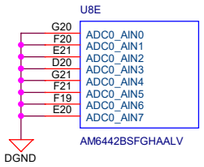
INDUSTRIAL COMMUNICATION LED's

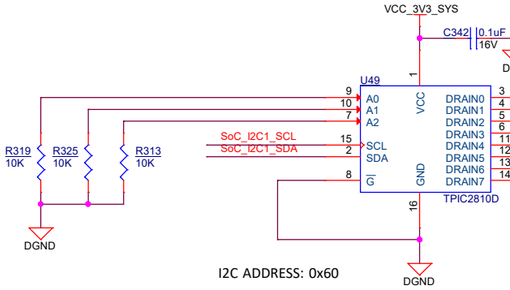
D-Note :-
ADC inputs are not fail-safe. No input voltage should be apply before the SOC supply ramps.
Use a FET switch to control the input voltage in case they are available before the SOC supply ramps

D-Note :-
For connecting the ADC0 signals, Refer Pin connectivity table when entire ADC0 is not used or any ADC input is not used

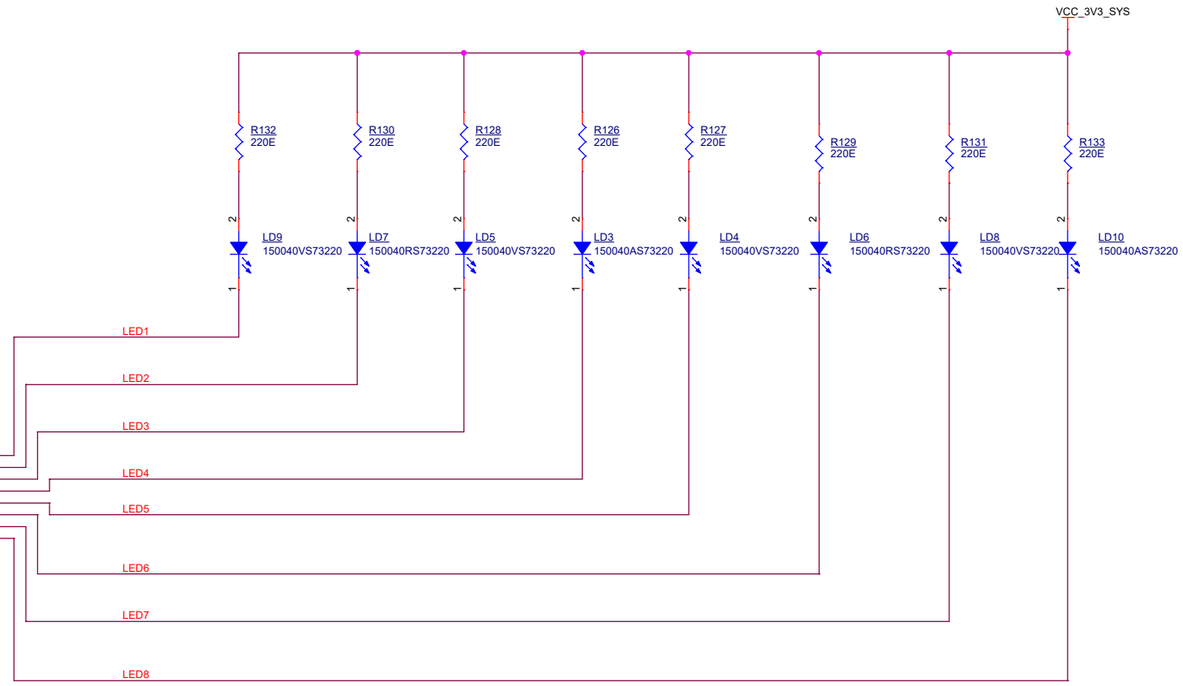


D-Note :-
Short through 0R.
Add a TP near to the ADC for future expansion

D-Note :-
ADC0_AIN when not used for ADC function can be used ad General Purpose Input
The assignment of each ADC0 pin to the GPIO1 module is defined in the ADC0 Signal Description table found in the data sheet.



I2C ADDRESS: 0x60



OFF PAGE CONNECTIONS

SoC_I2C1_SCL
SoC_I2C1_SDA
SoC_I2C1_SCL [19,31,34,36]
SoC_I2C1_SDA [19,31,34,36]

Designed for TI by Mistral Solutions Pvt Ltd

Title	INDUSTRIAL COMMUNICATION LED's	
Size C	PROC100A 002	Rev A
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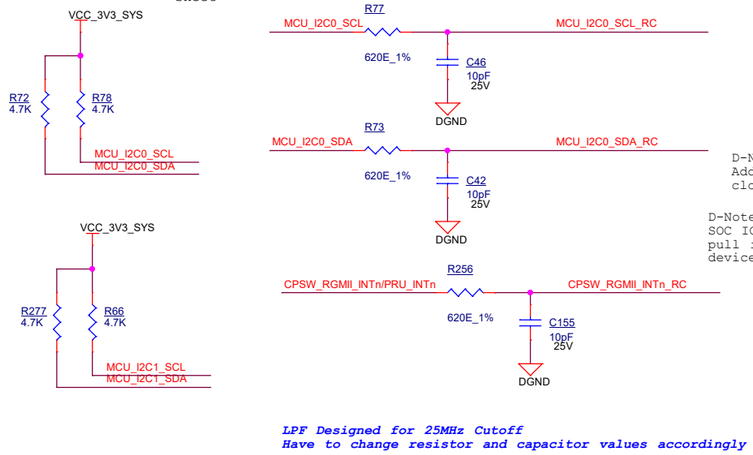
MCU_GENERAL

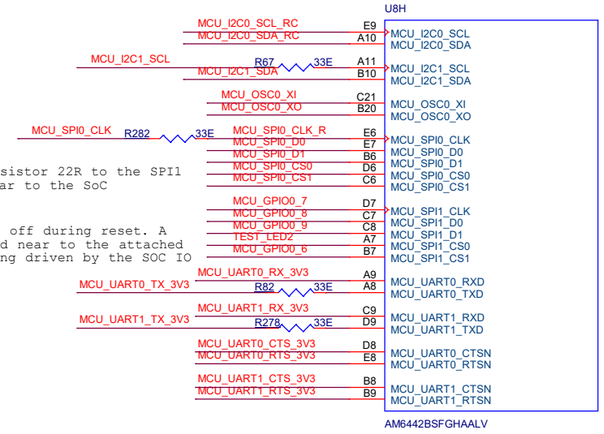
D-Note :-
RC for Open drain output type I2C interface for slew rate control when pulled to 3.3V. Refer SOC Data sheet

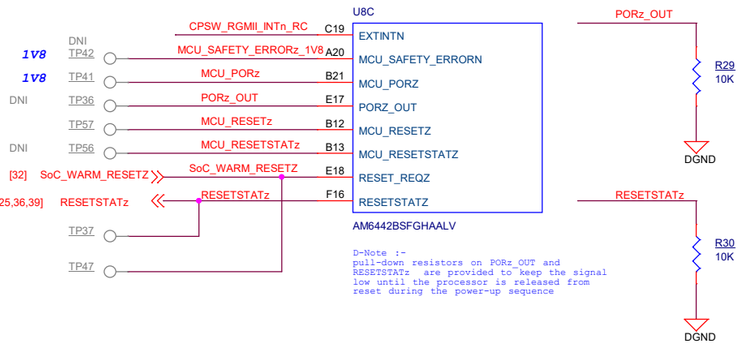


LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly

D-Note :-
Add a series resistor 22R to the SPI1 clock output near to the SoC

D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO



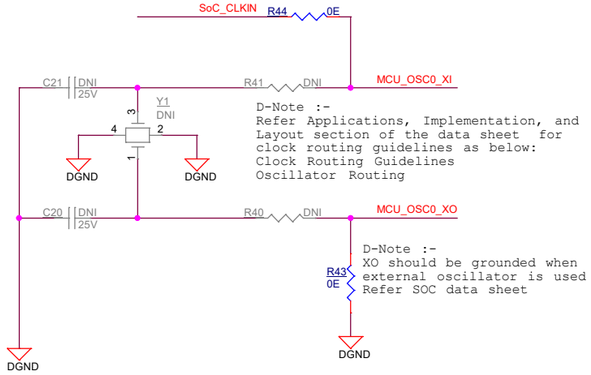


D-Note :-
pull-down resistors on PORz_OUT and RESETSTATz are provided to keep the signal low until the processor is released from reset during the power-up sequence

CRYSTAL FOR SOC MCU_OSC0

Only Footprint option to mount the Oscillator is provided.
By default the part is not mounted on the board.

D-Note :-
No HFOSC0 registers are required to be changed. These registers should remain in their default state.
Select the appropriate crystal circuit components that are compliant to the values defined in the MCU_OSC0 Crystal Circuit Requirements table.
Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.



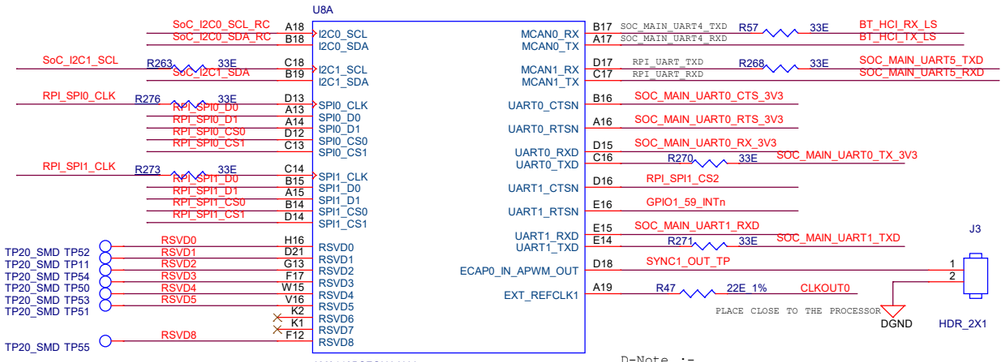
D-Note :-
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines
Oscillator Routing

D-Note :-
XO should be grounded when external oscillator is used
Refer SOC data sheet

D-Note :-
Connect the 25 MHz crystal directly to the SOC Xi and Xo pins (No Series or parallel resistors are recommended).
The internal oscillator implements AGC (Automatic Gain Control) for amplitude control . Match the SOC and the EPHY crystal specs

D-Note :-
MCU_OSC0 has been validated only with a 25 MHz clock source, so that is the only frequency supported. The datasheet shows MCU_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD_CORE is valid. In most cases it will start as early as VDDS_OSC0, but this may not always be the case. This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.

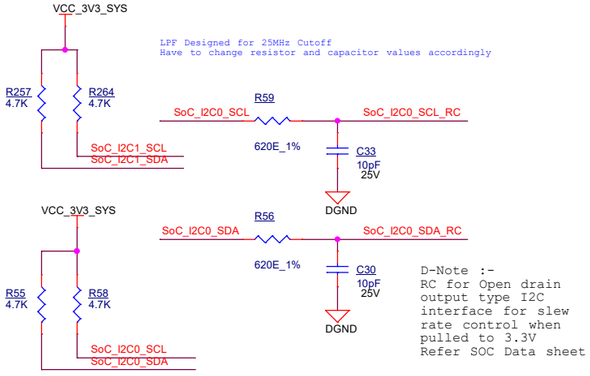
SoC MAIN DOMAIN



D-Note :-
Reserved Pins. Leave unconnected

D-Note :-
Ext_Refclk1 used as Clkout0
A clock signal should always be connected point to point without any branches. When connecting Clkout0 to more than one (multiple) clock inputs, use a buffer with one input and multiple outputs.

D-Note :-
Reserved pins
leave them unconnected



D-Note :-
RC for Open drain output type I2C interface for slew rate control when pulled to 3.3V
Refer SOC Data sheet

OFF PAGE CONNECTIONS

[32] MCU_RESETz
[32] MCU_PORz
[25,27,31] MCU_RESETSTATz
[15,16,17,18,20] PORz_OUT
[17,25,39] CPSW_RGMII_INTn/PRU_INTn
[27,31,33] TEST_LED2
[27,31,32] MCU_GPIO0_6
[29] SoC_CLKIN
[24] MCU_UART0_RX_3V3
[24] MCU_UART0_TX_3V3
[24] MCU_UART0_RTS_3V3
[24] MCU_UART0_CTS_3V3

MCU_RESETz
MCU_PORz
MCU_RESETSTATz
PORz_OUT
CPSW_RGMII_INTn/PRU_INTn
TEST_LED2
MCU_GPIO0_6
SoC_CLKIN
MCU_UART0_RX_3V3
MCU_UART0_TX_3V3
MCU_UART0_RTS_3V3
MCU_UART0_CTS_3V3

[27] MCU_SPI0_CS1
[27] MCU_GPIO0_8
[27,31,33] TEST_LED2
[27] MCU_GPIO0_7
[27] MCU_UART1_RX_3V3
[27] MCU_UART1_RTS_3V3
[27] MCU_UART1_TX_3V3
[27] MCU_I2C0_SDA
[25,27,31] MCU_RESETSTATz
[27] MCU_SPI0_D1
[27] MCU_SPI0_D0
[27] MCU_SPI0_CS0
[27,31,32] MCU_GPIO0_6
[27] MCU_UART1_CTS_3V3
[27] MCU_GPIO0_9
[27] MCU_I2C1_SDA
[27] MCU_SPI0_CLK
[27] MCU_I2C1_SCL
[27] MCU_I2C0_SCL
[27] MCU_SAFETY_ERRORz_1V8

MCU_SPI0_CS1
MCU_GPIO0_8
TEST_LED2
MCU_GPIO0_7
MCU_UART1_RX_3V3
MCU_UART1_RTS_3V3
MCU_UART1_TX_3V3
MCU_I2C0_SDA
MCU_RESETSTATz
MCU_SPI0_D1
MCU_SPI0_D0
MCU_SPI0_CS0
MCU_GPIO0_6
MCU_UART1_CTS_3V3
MCU_GPIO0_9
MCU_I2C1_SDA
MCU_SPI0_CLK
MCU_I2C1_SCL
MCU_I2C0_SCL
MCU_SAFETY_ERRORz_1V8

BT_HCI_TX_LS
BT_HCI_RX_LS
SOC_MAIN_UART5_RXD
SOC_MAIN_UART5_TXD
RPI_SPI1_CLK
RPI_SPI1_D0
RPI_SPI1_D1
RPI_SPI1_CS0
RPI_SPI1_CS1
RPI_SPI1_CS2
SOC_MAIN_UART0_RX_3V3
SOC_MAIN_UART0_TX_3V3
SOC_MAIN_UART0_RTS_3V3
SOC_MAIN_UART0_CTS_3V3
SoC_I2C0_SCL
SoC_I2C0_SDA
SoC_I2C1_SCL
SoC_I2C1_SDA
CLKOUT0
RPI_SPI0_CLK
RPI_SPI0_D0
RPI_SPI0_D1
RPI_SPI0_CS0
RPI_SPI0_CS1
GPIO1_59_INTn
SOC_MAIN_UART1_RXD
SOC_MAIN_UART1_TXD

BT_HCI_TX_LS [14]
BT_HCI_RX_LS [14]
SOC_MAIN_UART5_RXD [26]
SOC_MAIN_UART5_TXD [26]
RPI_SPI1_CLK [26]
RPI_SPI1_D0 [26]
RPI_SPI1_D1 [26]
RPI_SPI1_CS0 [26]
RPI_SPI1_CS1 [26]
RPI_SPI1_CS2 [26]
SOC_MAIN_UART0_RX_3V3 [24]
SOC_MAIN_UART0_TX_3V3 [24]
SOC_MAIN_UART0_RTS_3V3 [24]
SOC_MAIN_UART0_CTS_3V3 [24]
SoC_I2C0_SCL [25,26,35,39]
SoC_I2C0_SDA [25,26,35,39]
SoC_I2C1_SCL [19,30,34,36]
SoC_I2C1_SDA [19,30,34,36]
CLKOUT0 [29,37]
RPI_SPI0_CLK [26]
RPI_SPI0_D0 [26]
RPI_SPI0_D1 [26]
RPI_SPI0_CS0 [26]
RPI_SPI0_CS1 [26]
GPIO1_59_INTn [32]
SOC_MAIN_UART1_RXD [21]
SOC_MAIN_UART1_TXD [21]

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Title	SoC MAIN AND MCU DOMAIN	
Size C	PROC100A 002	Rev A
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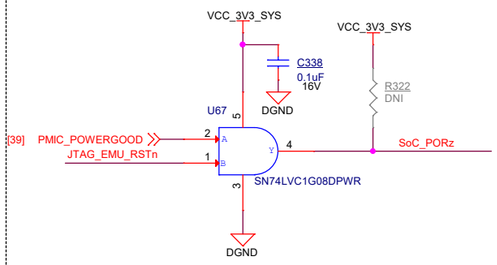
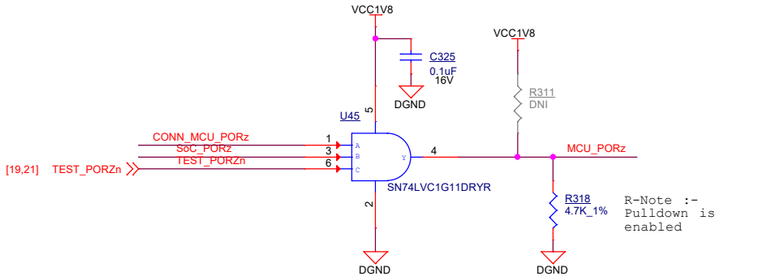
POR

D-Note :-
Not connecting a valid MCU_PORz could cause unpredictable and probably random behavior, since the device is not getting a valid reset, internal circuits would be in random states. Slow rising reset signal could cause glitches internal to the SOC reset circuit. Use a discrete buffer and have the fast rising output of the buffer drive the MCU_PORz is recommended



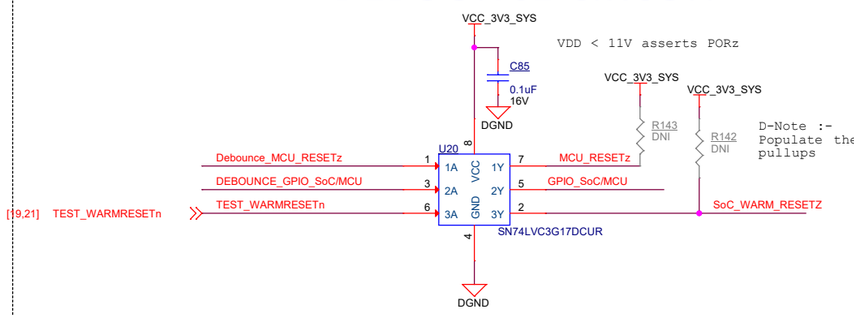
D-Note :-
MCU_PORz input have a maximum rise/fall time requirements when PMIC_POWERGOOD is connected to the MCU_PORz
Adjust the pullup to minimize the rise time (100..200 ns) when using open drain output MCU_PORz is fail-safe and 3.3v tolerant. Therefore, you can pull the MCU_PORz signal to 1.8V or 3.3V.

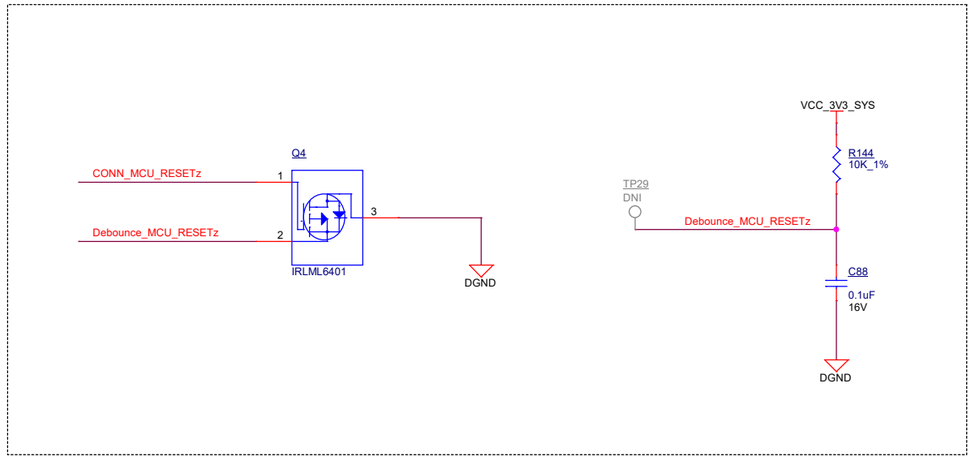


R-Note :-
Pulldown is enabled

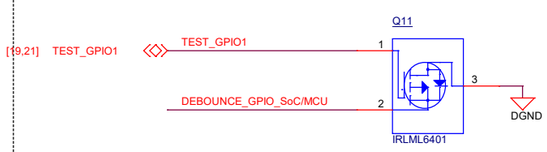
D-Note :-
It is recommended to connect the output from logic gate or discrete buffer (with fast rise time) as MCU_PORz input
rather than slow rising open drain output (could glitch internally).

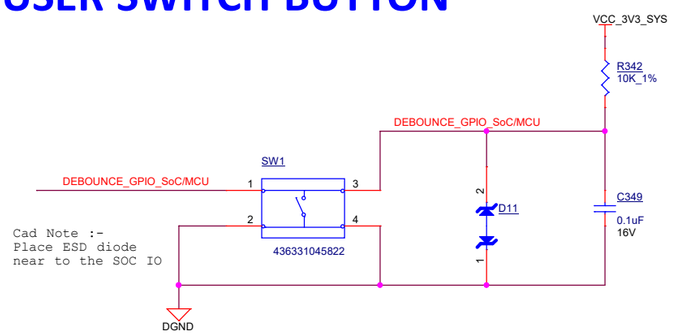
DEBOUNCE CIRCUIT





USER SWITCH BUTTON





OFF PAGE CONNECTIONS

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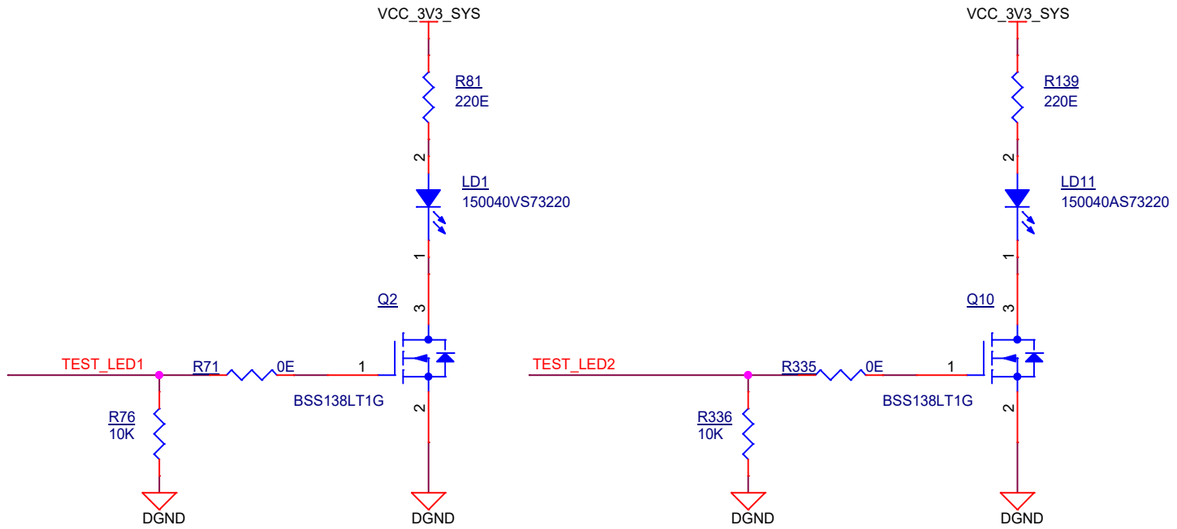
Title	RESET CIRCUIT	
Size: C	PROC100A 002	Rev: A
Date: Tuesday, June 18, 2024	Sheet 32 of 43	

USER TEST LEDs



OFF PAGE CONNECTIONS

TEST_LED1 — TEST_LED1 [25]
TEST_LED2 — TEST_LED2 [27,31]

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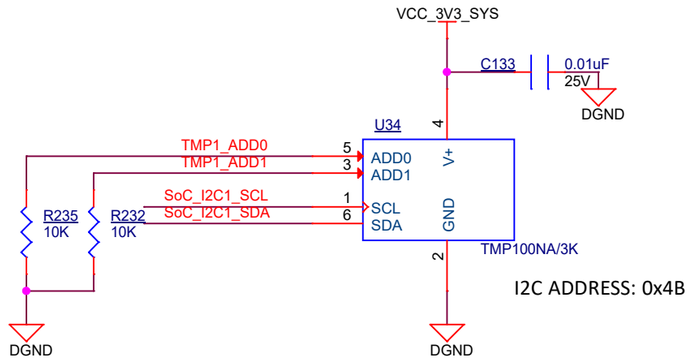
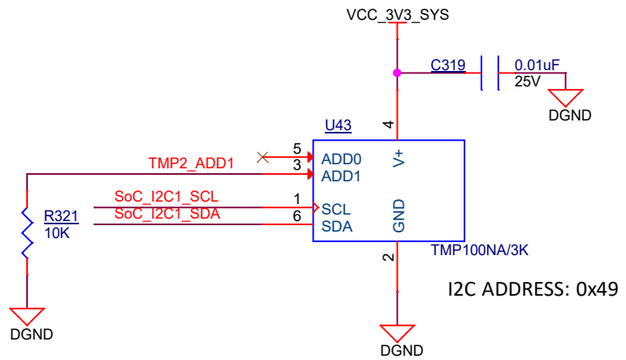
Title	USER TEST LED's	
Size: B	PROC100A 002	Rev: A
Date: Tuesday, June 18, 2024	Sheet 33 of 43	

DIGITAL TEMPERATURE SENSOR



Cad Note :- PLACE TEMP SENSOR CLOSE TO SoC



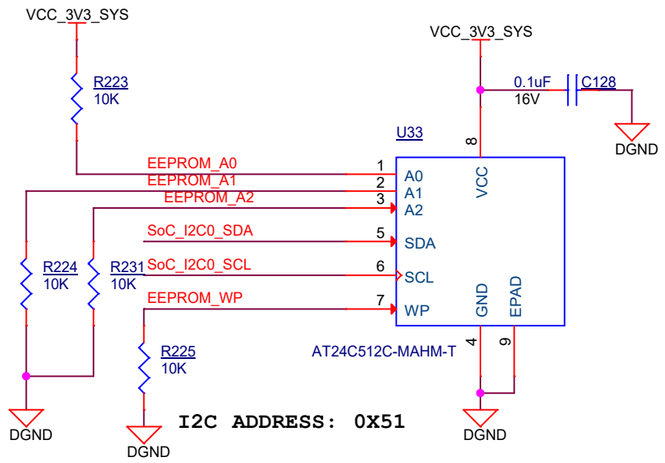
Cad Note :- PLACE TEMP SENSOR CLOSE TO LPDDR4

OFF PAGE CONNECTIONS

Designed for TI by Mistral Solutions Pvt Ltd

Title	TEMPERATURE SENSORS	
Size B	PROC100A 002	Rev A
Date: Tuesday, June 18, 2024	Sheet 34 of 43	

BOARD ID EEPROM



OFF PAGE CONNECTIONS

SoC_I2C0_SDA
SoC_I2C0_SCL

SoC_I2C0_SDA [25,26,31,39]
SoC_I2C0_SCL [25,26,31,39]

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOARD ID EEPROM	
Size: B	PROC100A 002	Rev: A
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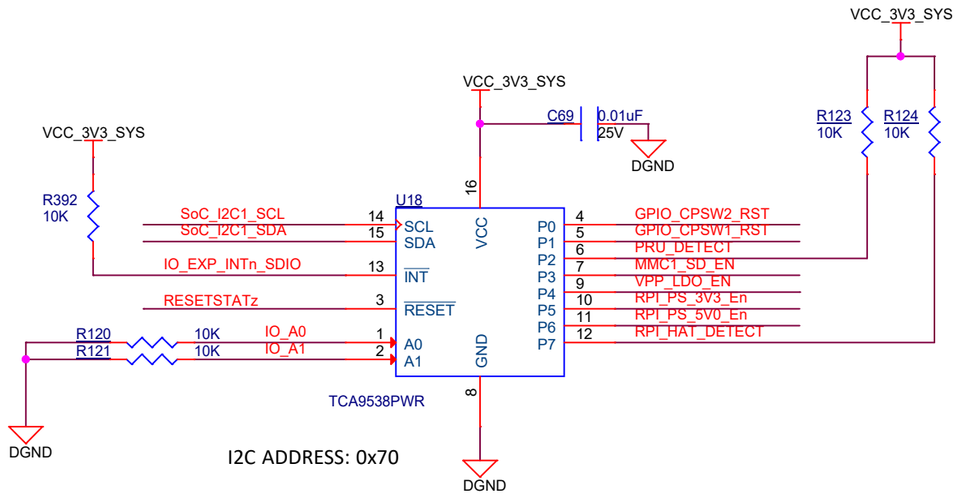
IO EXPANDER



OFF PAGE CONNECTIONS

RPI_PS_3V3_En	RPI_PS_3V3_En [26]
RPI_PS_5V0_En	RPI_PS_5V0_En [26]
GPIO_CPSW2_RST	GPIO_CPSW2_RST [18]
GPIO_CPSW1_RST	GPIO_CPSW1_RST [17]
MMC1_SD_EN	MMC1_SD_EN [16]
VPP_LDO_EN	VPP_LDO_EN [40]
RESETSTATz	RESETSTATz [15,16,17,18,20,25,31,39]
IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO [14]
SoC_I2C1_SCL	SoC_I2C1_SCL [19,30,31,34]
SoC_I2C1_SDA	SoC_I2C1_SDA [19,30,31,34]
RPI_HAT_DETECT	RPI_HAT_DETECT [26]
PRU_DETECT	PRU_DETECT [25]

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TEXAS INSTRUMENTS

MISTRAL

Title	IO EXPANDER	
Size	PROC100A 002	Rev
B		A
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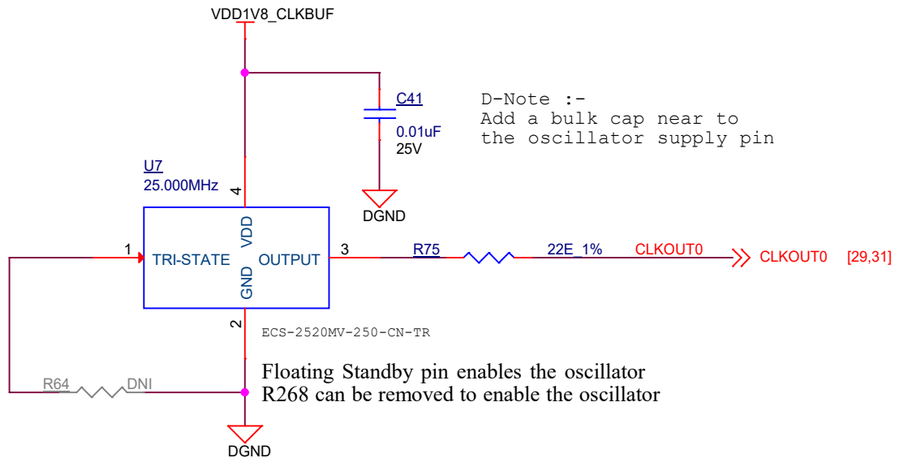
OSCILLATOR



Designed for TI by Mistral Solutions Pvt Ltd

Title	OSCILLATOR		
Size	PROC100A 002		Rev
B			A
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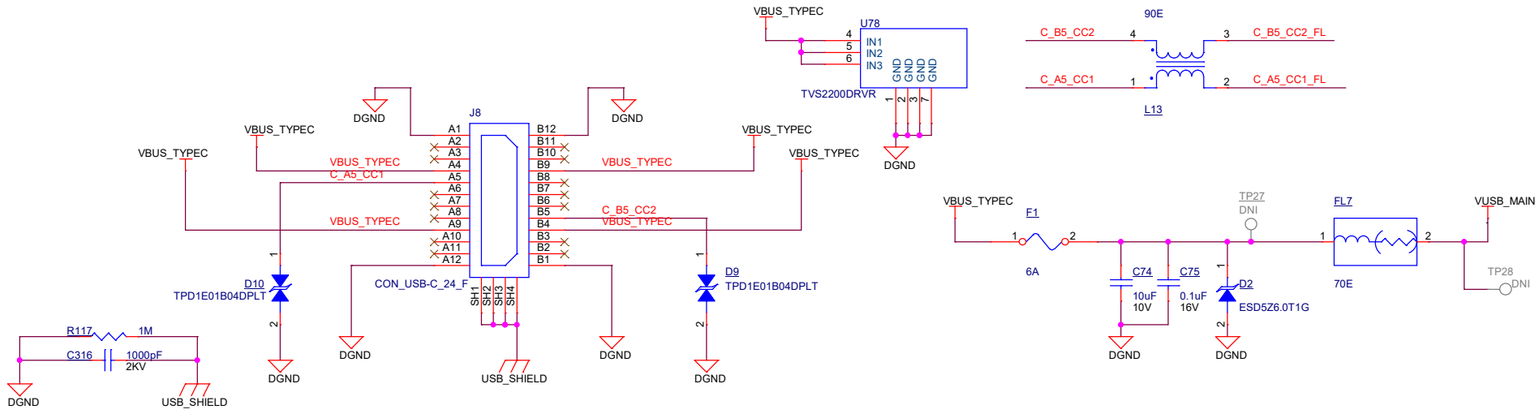
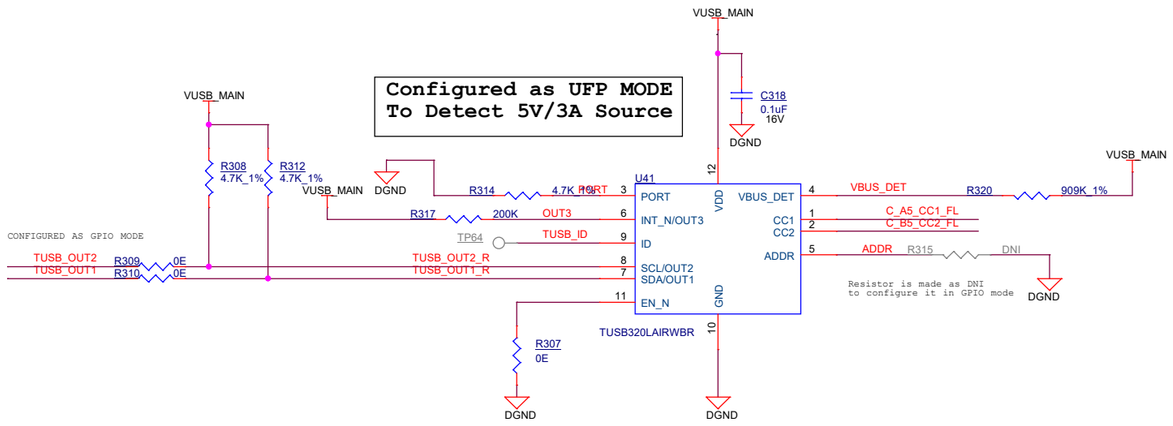
USB TYPE-C CONNECTOR

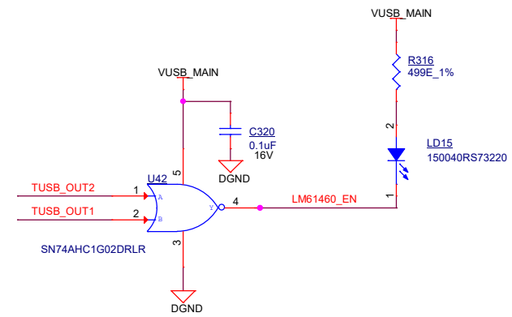


R-Note :-
Connect an LED to VBUS_TYPEC pin
for indicating the negotiation
indicator. ON indicates success.
Refer AM62x SK

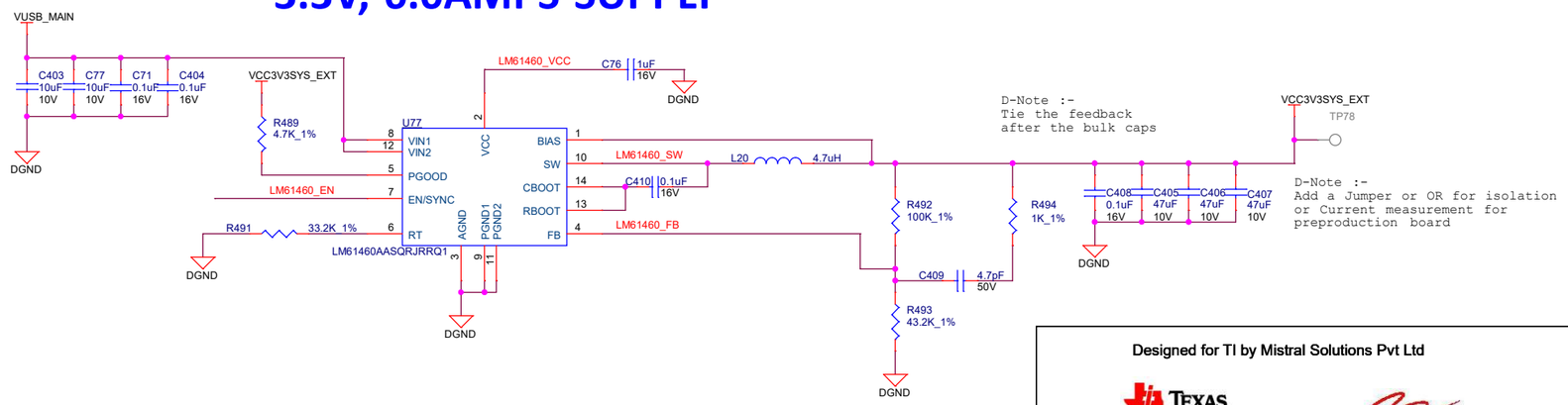
USB TYPE C CONFIGURATION CHANNEL LOGIC AND PORT CONTROLLER



Enable Logic for 3V3 Regulator



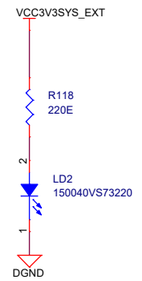
3.3V, 6.0AMPS SUPPLY



D-Note :-
Tie the feedback
after the bulk caps

D-Note :-
Add a Jumper or OR for isolation
or Current measurement for
preproduction board

POWER INDICATION LED



Designed for TI by Mistral Solutions Pvt Ltd

Title	USB MAIN 5V POWER SUPPLY		
Size	C	PROC100A 002	Rev A
Date:	Tuesday, June 18, 2024	Sheet 38 of 43	

TPS6522053 PMIC

D-Note :-
Refer AM64x EVM schematics for
implementing current monitoring

D-Note :-
Refer PMIC data sheet for
the bulk capacitor value

D-Note :-
Add a 0R series resistor at the
output of the DC/DC for isolation
or current measurement

D-Note :-
Show the bulk caps connection for each of the DC/DC
inputs separately. Add a 0.1 uF across the bulk caps
PVIN_B1_1, PVIN_B1_2 can share the same bulk cap

Input Caps for pin 4,5,26,30

Input Caps for pin 22,6

D-Note :-
Add a 2.2 uF cap to VSYS pin

Configured as EN (Active High)

D-Note :-
Tie the feedback
after the DC/DC
output bulk cap

U65 TPS6522053RHBR

4	PVIN_B1_1	LX_B1_1	2
5	PVIN_B1_2	LX_B1_2	3
30	PVIN_B2	LX_B2	29
26	PVIN_B3	LX_B3	27
6	PVIN_LDO1	VLDO1	7
20	PVIN_LDO2	VLDO2	19
22	PVIN_LDO34	VLDO3	21
		VLDO4	23
10	SCL	VSEL_SD/VSEL_DDR	12
9	SDA	MODE/RESET	28
11	nINT	MODE/STBY	31
18	nRSTOUT	FB_B1	1
13	VSYS	FB_B2	32
25	EN/PB/VSENSE	FB_B3	24
16	GPIO		
8	GPO1		
17	GPO2		
14	VDD1P8		
15	AGND		
33	PGND		

ON/OFF LOGIC

D-Note :-
Ensure the switch in placed in
the ON position before
connecting the USB cables to
power the starter kit

3V3 LOAD SWITCH

U79 TPS22965DSGT

D-Note:-
Add a cap (>220 pF) to
the CT pin for SoC IO
supply slew rate control.
SoC IO supplies have slew
rate requirements
specified

POWER INDICATION LED

Designed for TI by Mistral Solutions Pvt Ltd		Title	TPS6522053RHBR PMIC
		Size C	PROC100A 002
		Rev	A
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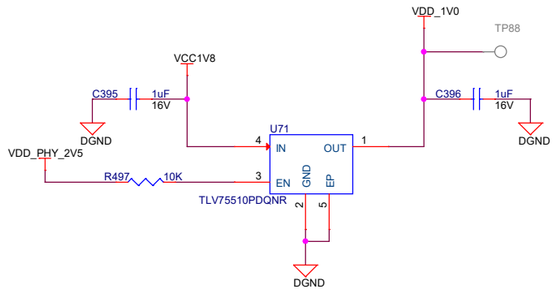
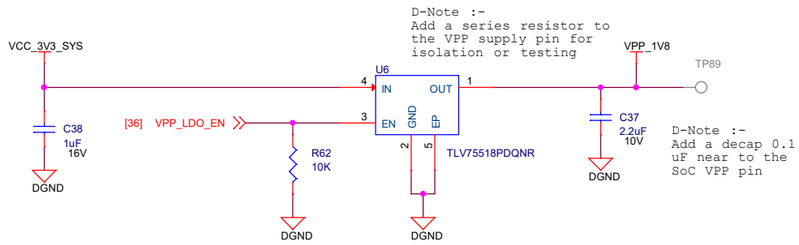
ETHERNET PHY CORE VOLTAGE

1.0V, 500 mA SUPPLY



eFUSE PROGRAMMING SUPPLY (500 mA) TO SoC

D-Note :-
It is very important to select an LDO with very fast transient response and connect its output to the VPP pin with a low loop inductance path to ensure it is able to source the high transient load, where the VPP pin never drops below the minimum operating voltage.



1.8V VPP, 0.5 A SUPPLY

Designed for TI by Mistral Solutions Pvt Ltd

Title	DISCRETE POWER REGULATORS		
Size C	PROC100A 002		Rev A
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STRAP CONFIGURATION OF ETHERNET PHYS

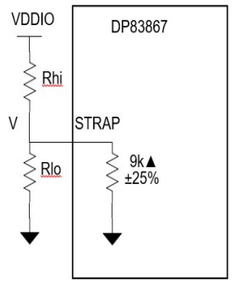

Figure 25. Strap Circuit

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
1	0	0	0.098 × VDDIO	OPEN	OPEN
2	0.140 × VDDIO	0.165 × VDDIO	0.191 × VDDIO	10	2.49
3	0.225 × VDDIO	0.255 × VDDIO	0.284 × VDDIO	5.76	2.49
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

Level Strap Resistor Ratios

PIN NAME	64 HTQFP PIN #	48 QFN PIN #	DEFAULT	STRAP FUNCTION		
RX_D0	44	33	[00]	**MODE**	PHY_ADD1	PHY_ADD0
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D2	46	35	[00]	**MODE**	PHY_ADD3	PHY_ADD2
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D4	48		[00]	**MODE**	ANEG_SEL1	PHY_ADD4
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D5	49		[00]	**MODE**	Force MDI/X	Half-Duplex Enable (FD/HD)
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D6	50		[00]	**MODE**	RGMII Disable	AMDIX Disable
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D7	51		[00]	**MODE**	Speed Optimization Enable	Clock Out Disable
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_DV/RX_CTRL (1) (Straps Required)	53	38	[0]	**MODE**		Autoneg Disable
				1		N/A
				2		N/A
				3		0
				4		1
CRS(2)	56		[0]	**MODE**		Fast Link Drop (FLD)
				1		0
				2		1
				3		N/A

Level Strap Pins

PIN NAME	64 HTQFP PIN #	48 QFN PIN #	DEFAULT	STRAP FUNCTION		
LED_2(3)		45	[00]	**MODE**	RGMII Clock Skew TX[1]	RGMII Clock Skew TX[0]
				1	0	0
				2	0	1
				3	1	0
				4	1	1
LED_1 (RGZ)		46	[00]	**MODE**	ANEG_SEL	RGMII Clock Skew TX[2]
				1	0	0
				2	0	1
				3	1	0
				4	1	1
LED_1 (PAP)	62		[0]	**MODE**	ANEG_SEL0	
				1	0	
				2	0	
				3	1	
				4	1	
LED_0(4)	63	47	[0]	**MODE**	Mirror Enable	
				1	0	
				2	N/A	
				3	1	
				4	N/A	
GPIO_0 (3)		39	[00]	**MODE**	RGMII Clock Skew RX[0]	
				1	0	
				2	Not Applicable	
				3	1	
				4	Not Applicable	
GPIO_1		40	[00]	**MODE**	RGMII Clock Skew RX[2]	RGMII Clock Skew RX[1]
				1	0	0
				2	0	1
				3	1	0
				4	1	1

Level Strap Pins

MODE	ANEG_SEL	REMARKS
10/100/1000	0	advertise ability of 10/100/1000
100/1000	1	advertise ability of 100/1000 only

RGMII Clock Skew Details

MODE	RGMII CLOCK SKEW TX[2]	RGMII CLOCK SKEW TX[1]	RGMII CLOCK SKEW TX[0]	RGMII TX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

MODE	RGMII CLOCK SKEW RX[2]	RGMII CLOCK SKEW RX[1]	RGMII CLOCK SKEW RX[0]	RGMII RX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

RGMII Clock Skew Details

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TEXAS INSTRUMENTS MISTRAL

Title	STRAP CONFIGURATION OF ETHERNET PHYS		
Size	PROC100A 002		Rev
D			A
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MOUNTING HARDWARE

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

BARE PCB

PCB1

PROC100

JUMPERS

ACC1

SPC02SYAN

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

LABELS

Board Serial No.

LBL1

PCB LABEL

THT-103-423-10

Assembly Revision

LBL3

PCB LABEL

THT-103-423-10

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TEXAS INSTRUMENTS

MISTRAL

Title	HARDWARE SCHEMATICS	
Size: C	PROC100A 002	Rev: A
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