

# AM64x/AM243x EVM BOARD

## PROC101C

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REV	C
VER	1.1

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Size	Variant Name = PROC101C(005)TMDS243EVM	Rev	E2
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## REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	11th MARCH 2022	Drafted from "PROC101B_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	11th MARCH 2022	Removed Voltage Monitor circuit & added RC Delay Circuit for power down sequence requirement Fixed Power down sequence issue seen on AM243x REV B	Mistral Design Team	AJIT MB	AJIT MB
0.3	11th MARCH 2022	Updated schematics to support PG2 Silicon	Mistral Design Team	AJIT MB	AJIT MB
1.0	30th MARCH 2022	Baselined and Released	Mistral Design Team	AJIT MB	AJIT MB
1.1	5th AUG 2022	Updated SoC Part Number and OPN Details Updated SoC Symbol for Reserved pins	Mistral Design Team	AJIT MB	AJIT MB

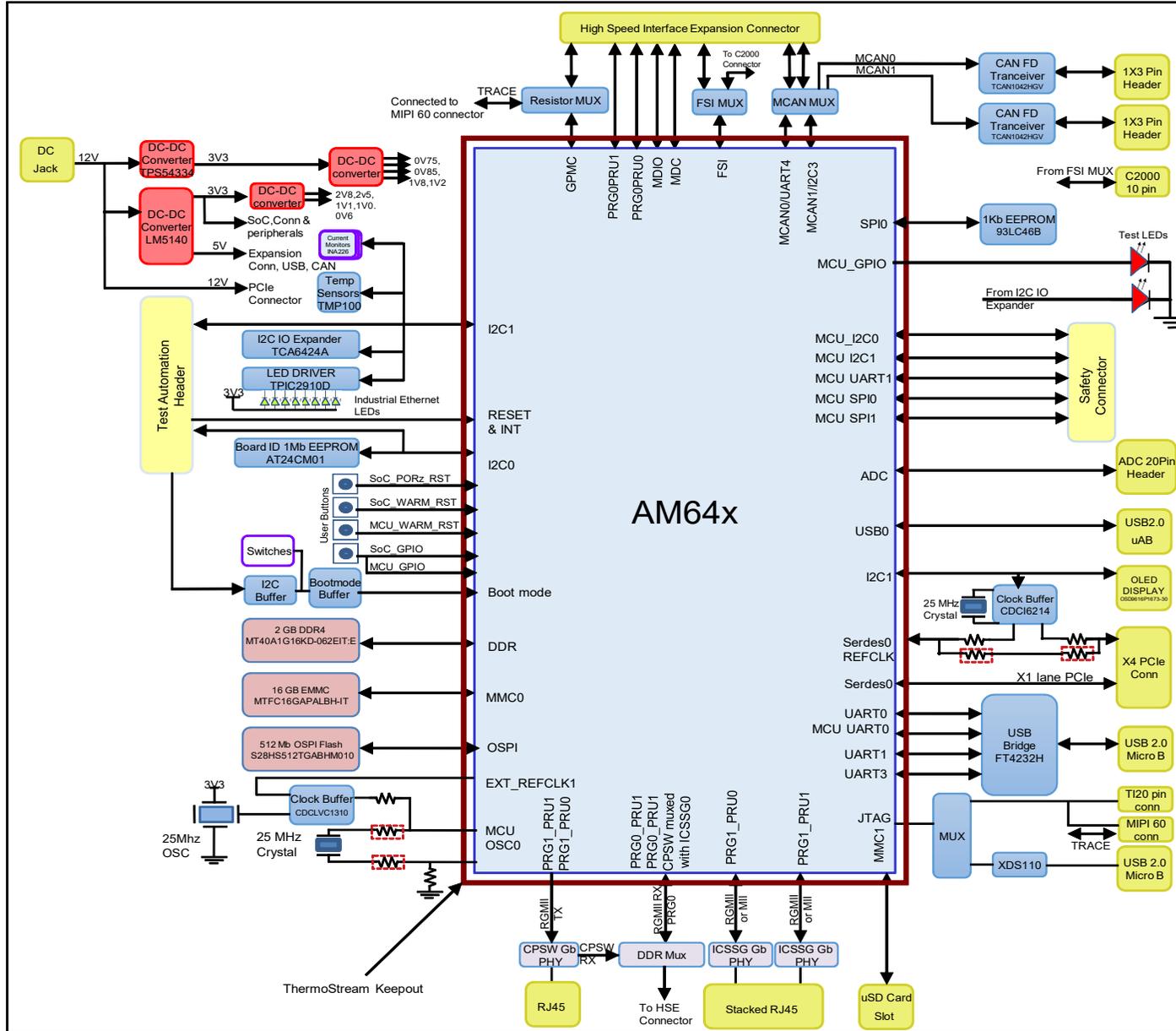
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Title REVISION HISTORY

Size	Variant Name = PROC101C(005) TMDS243EVM	Rev
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# BLOCK DIAGRAM\_AM64x\_EVM



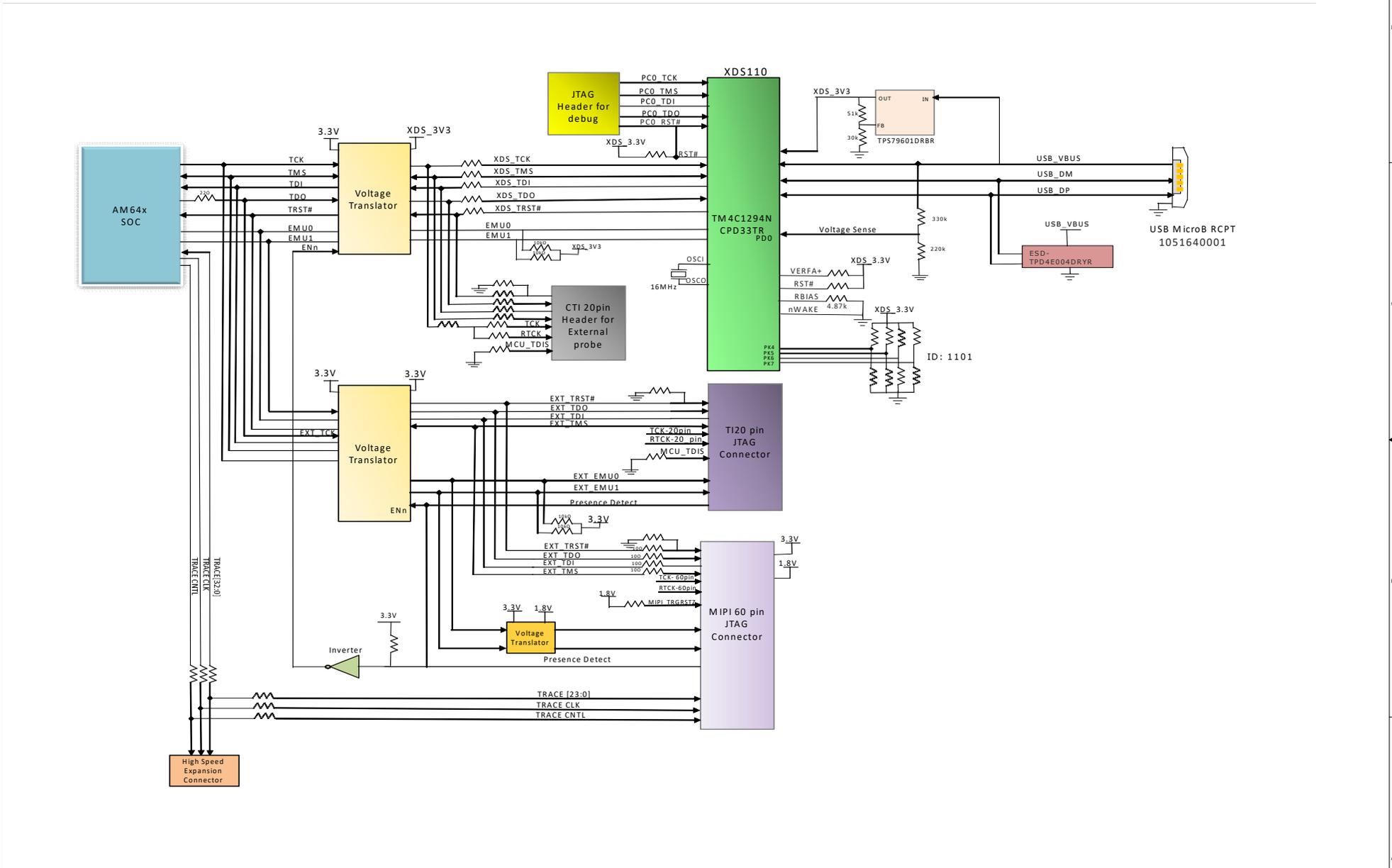
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Title BLOCK DIAGRAM\_CP BOARD

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev	E2
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# BLOCK DIAGRAM\_XDS110

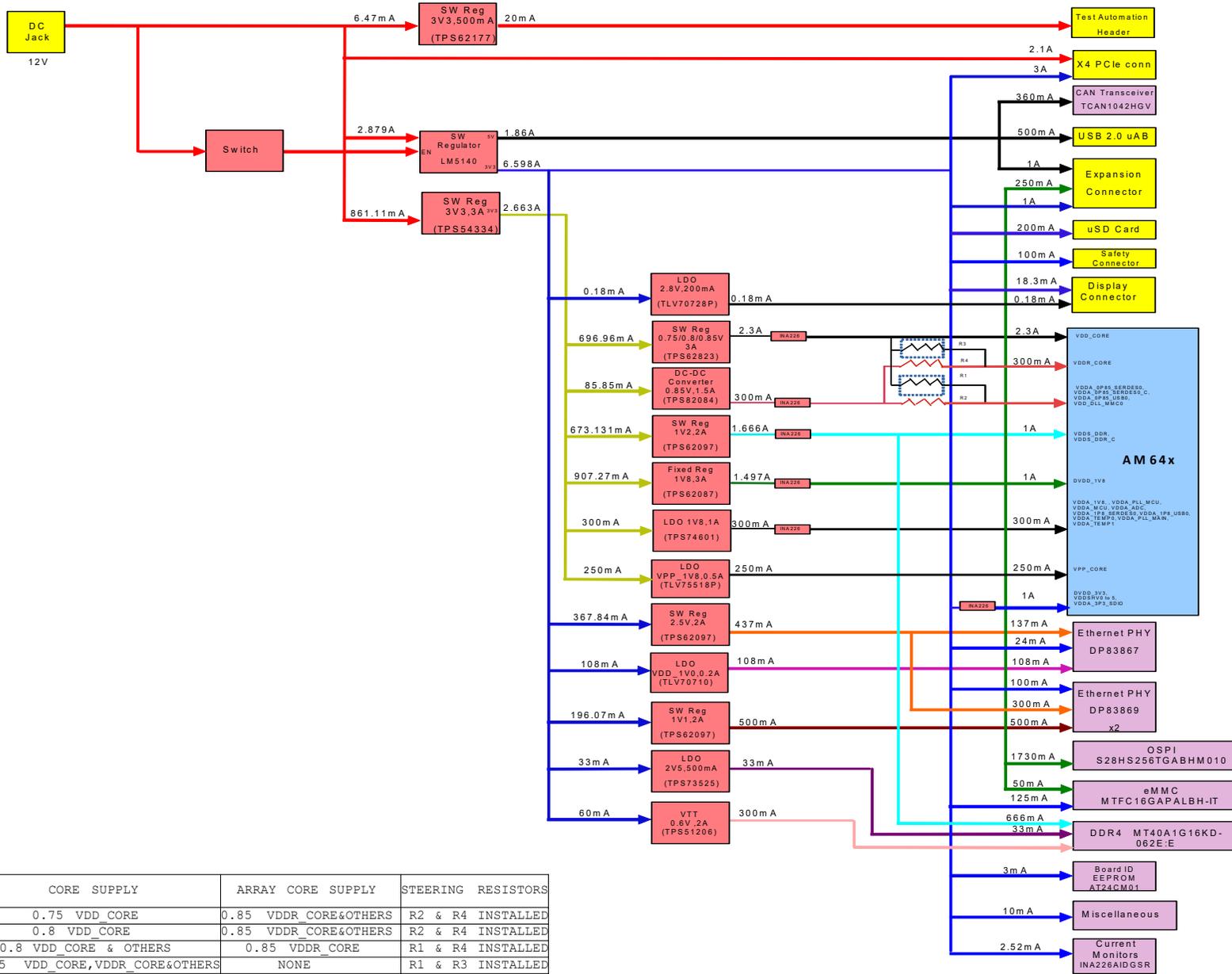


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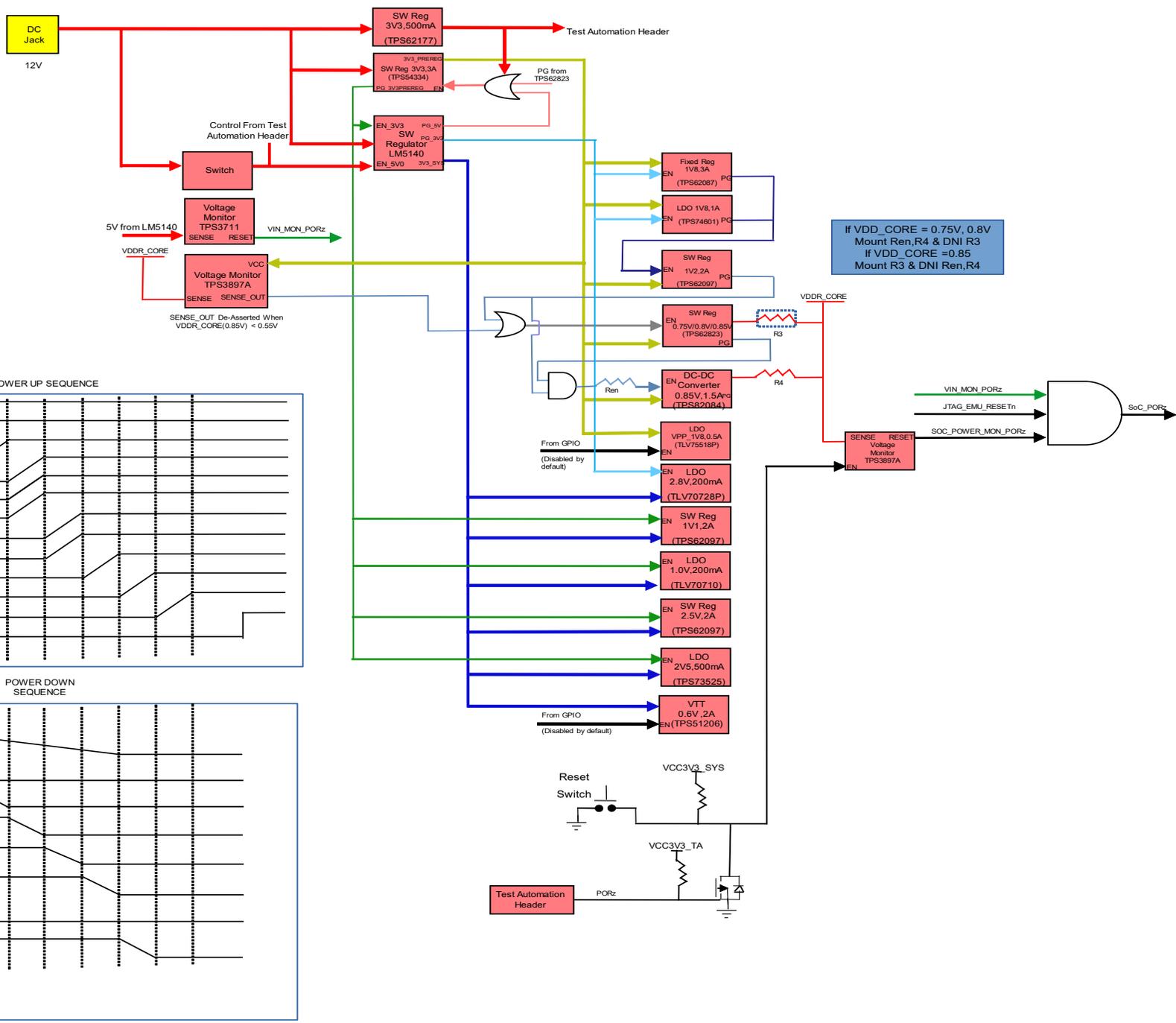
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Size	Variant Name = PROC101C(005) TMDS243EVM	Rev	E2
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# POWER FLOW DIAGRAM

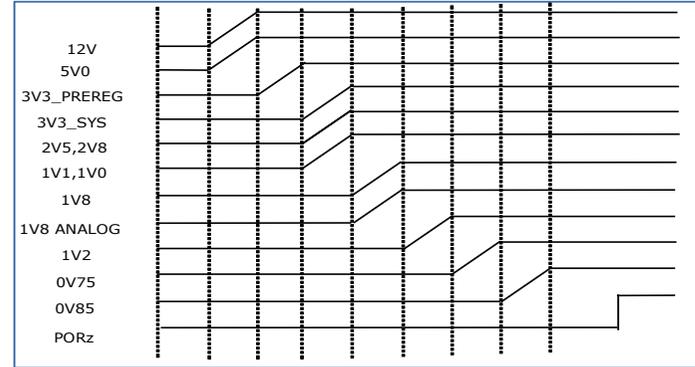


CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

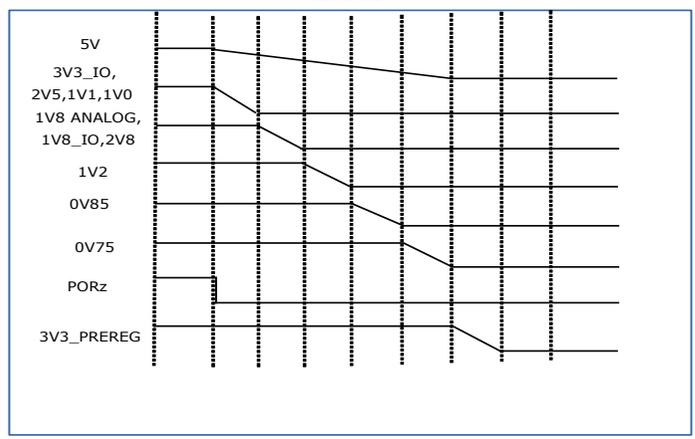
# POWER SEQUENCE



POWER UP SEQUENCE



POWER DOWN SEQUENCE



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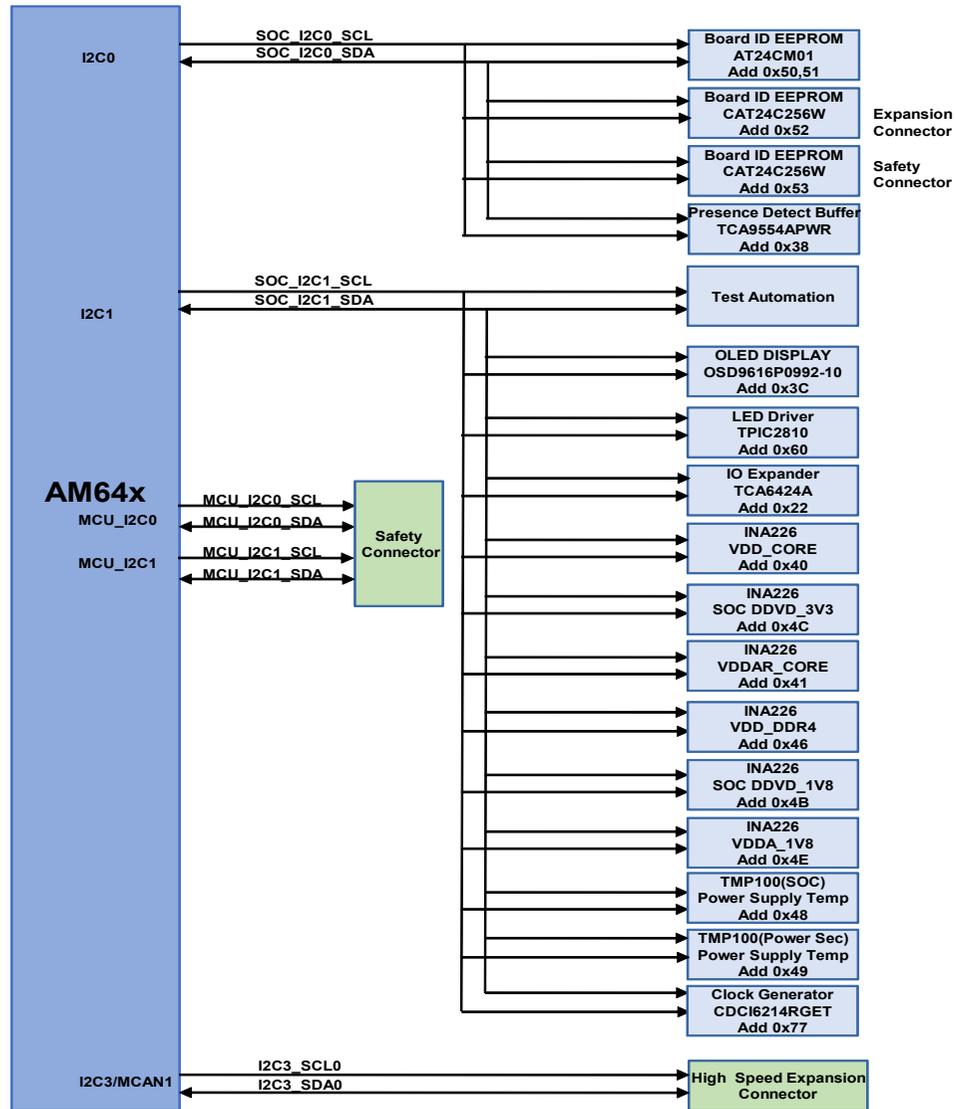


Title		POWER SEQUENCE	
Size	Variant Name = PROC101C(005) TMD2S243EVM	Rev	E2
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# GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPIO_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via OE res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1 Interrupt			Interrupt			INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2 Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCl_e_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN transceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN transceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPIO_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPIO_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESEtN	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Selection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

# I2C TREE



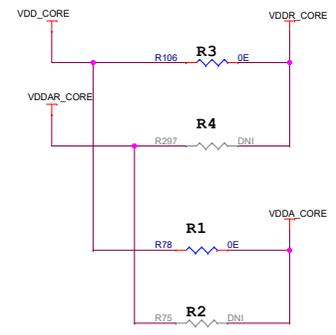
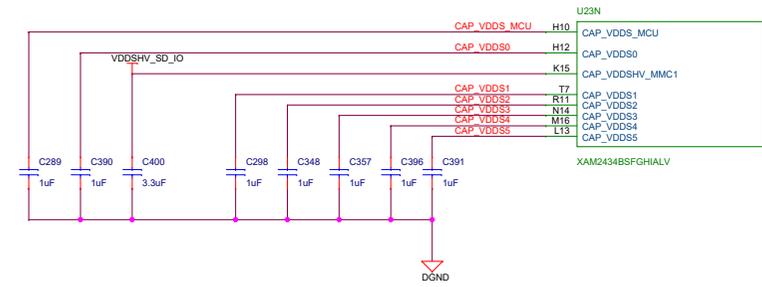
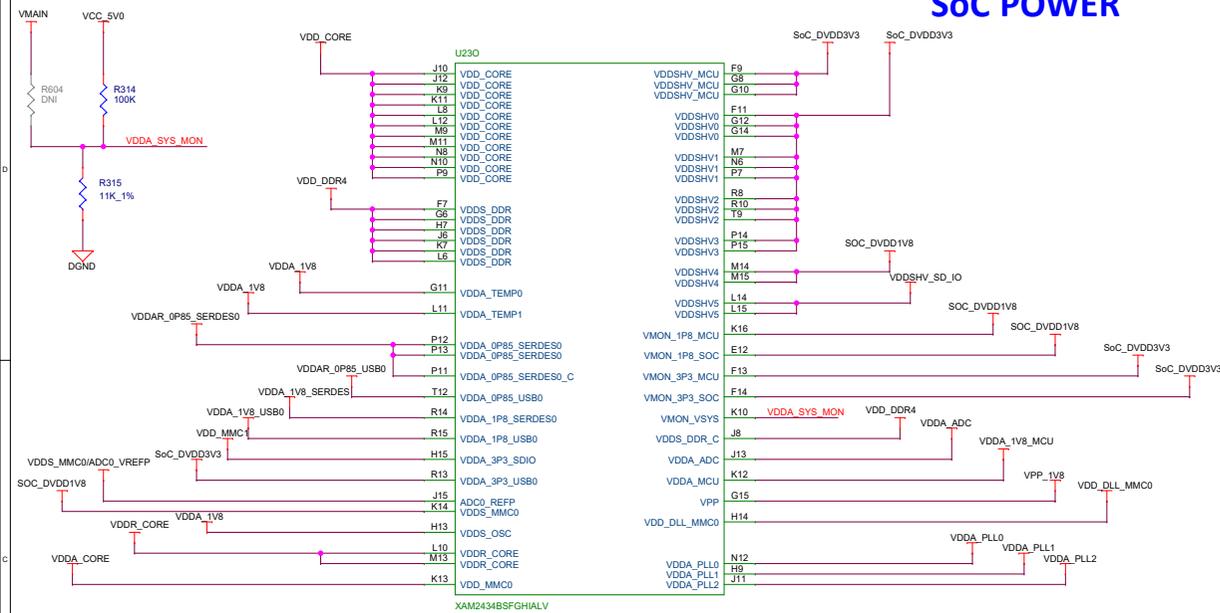
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Title I2C TREE

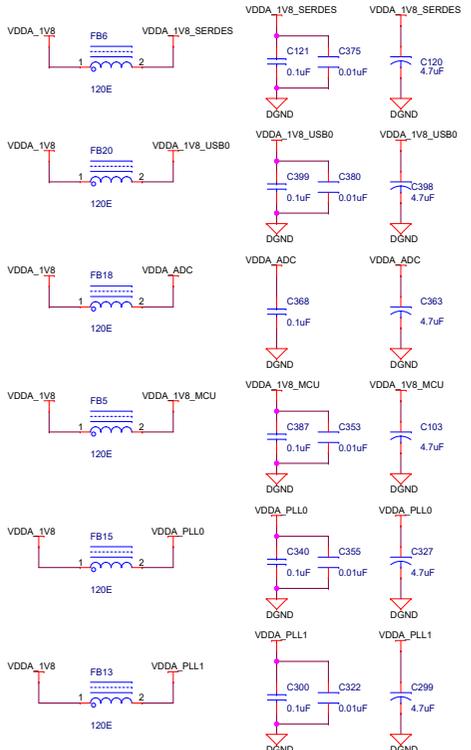
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
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# SoC POWER

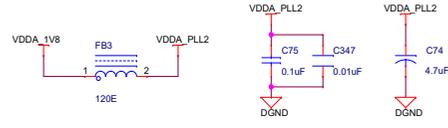


Note:  
Mount R699 and DNI R698 when SR2.0 Device is used  
Mount R698 and DNI R699 when SR1.0 Device is used

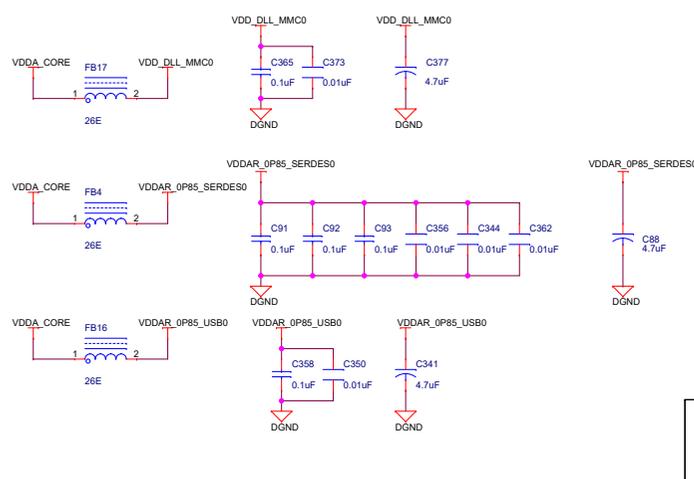
## 1.8V Analog SUPPLY



## 1.8V Analog SUPPLY



## CORE SUPPLY



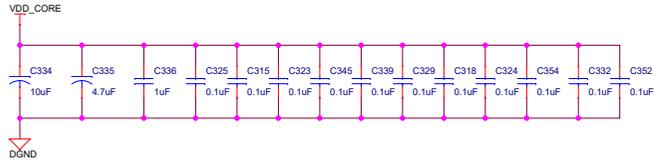
CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE, VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

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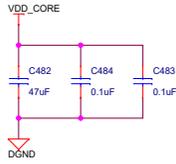


Title		SOC POWER	
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C		E2	
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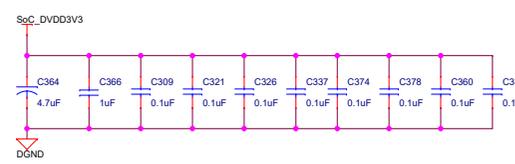
# SoC POWER Decaps



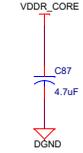
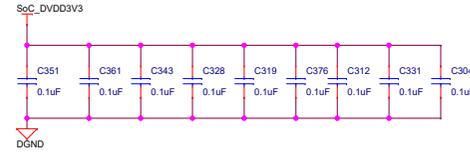
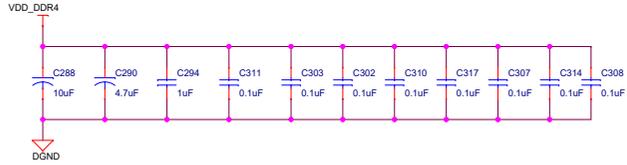
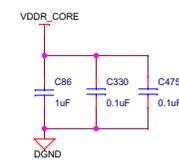
Place one 0.1uF cap near each Pin



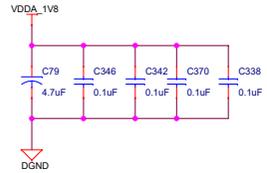
To place after current sense resistor on VDD\_CORE plane



Place one 0.1uF cap near each Pin

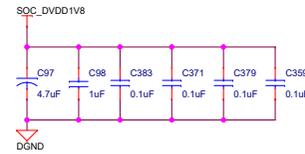
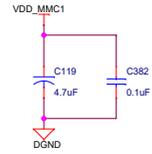


## VDD ARRAY CORE

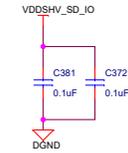


Place one 0.1uF cap near each Pin

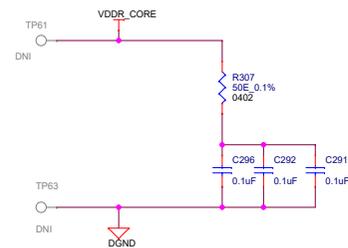
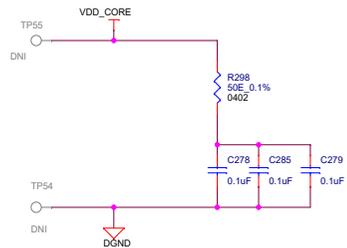
## VDDA\_3P3\_SDIO



Place one 0.1uF cap near each Pin



# Core & Array Core Supply Kelvin Sensing



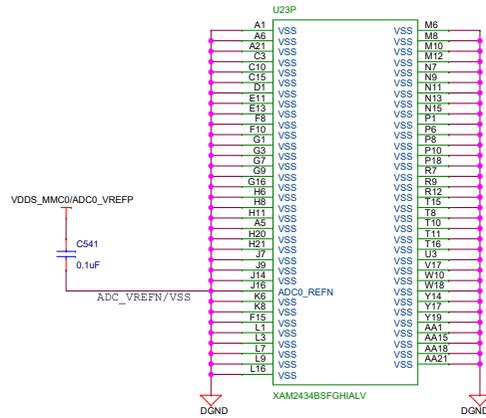
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Title: SOC POWER CAPS

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
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## SoC POWER - VSS



CAD Note:  
Place CAP C541  
between pins  
J15 and J16

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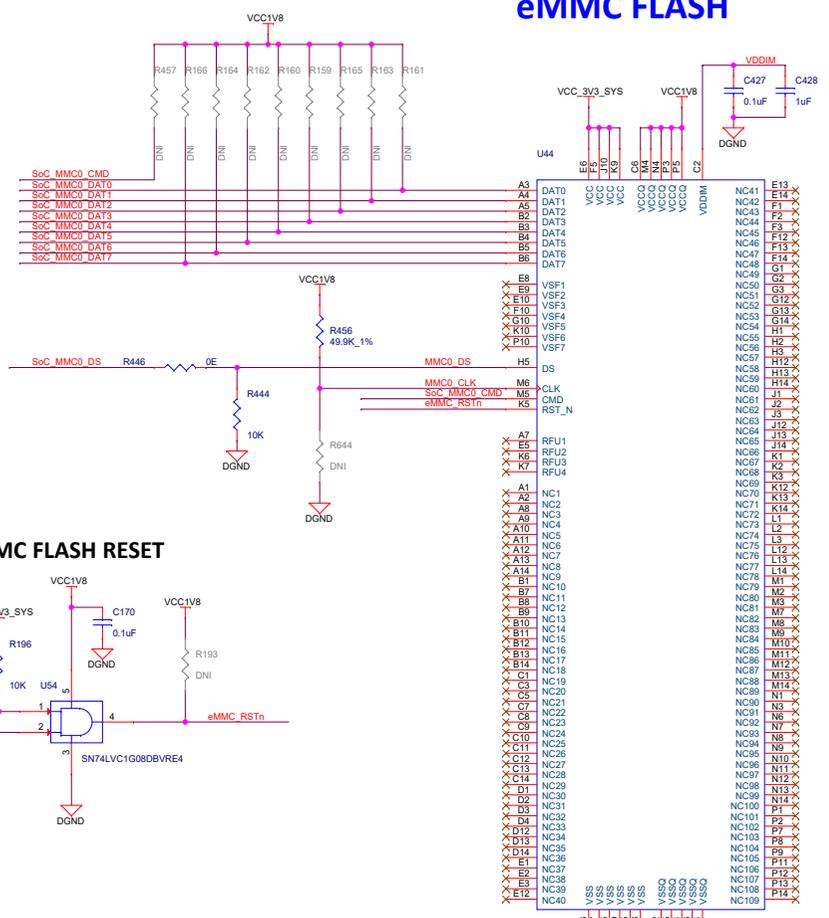
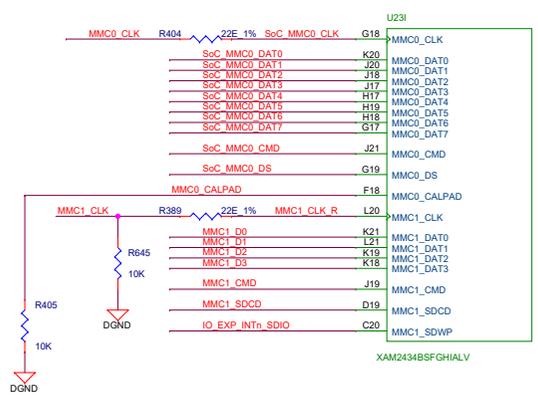


Title SOC VSS

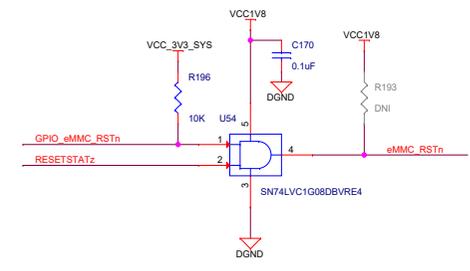
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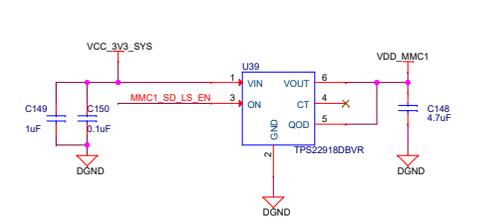
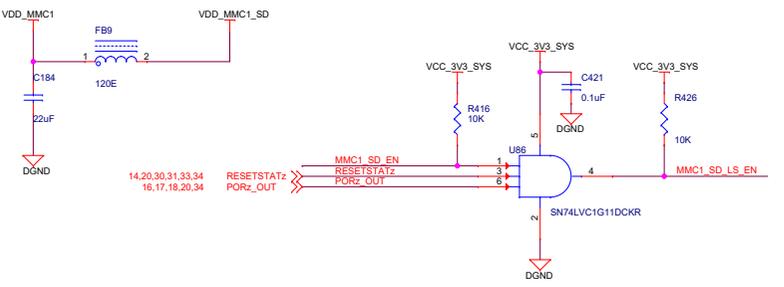
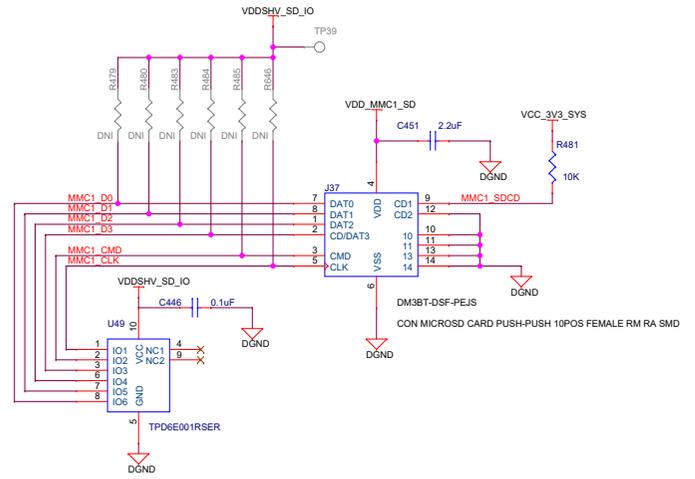
# eMMC FLASH



## eMMC FLASH RESET



## SD CARD INTERFACE

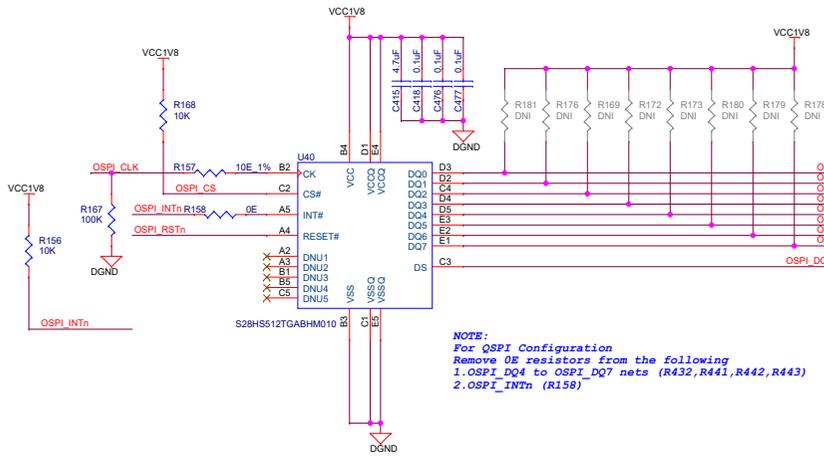


**Off Page Connections**

From & To IO Expander

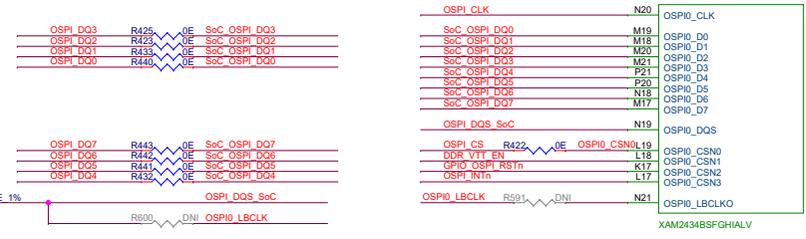
- 33 IO\_EXP\_INTn\_SDIO << IO\_EXP\_INTn\_SDIO
- 33 GPIO\_eMMC\_RSTn >> GPIO\_eMMC\_RSTn
- 33 MMC1\_SD\_EN >> MMC1\_SD\_EN

# OSPI FLASH



**NOTE:**  
**For OSPI Configuration**  
 Remove OE resistors from the following  
 1.OSPI\_DQ4 to OSPI\_DQ7 nets (R432,R441,R442,R443)  
 2.OSPI\_INTn (R158)

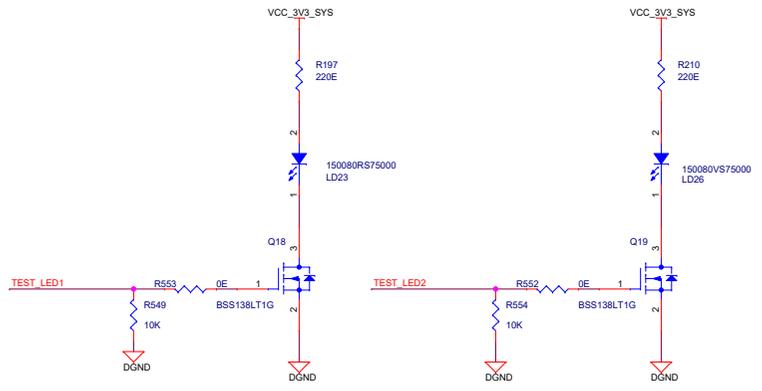
# SOC OSPI INTERFACE



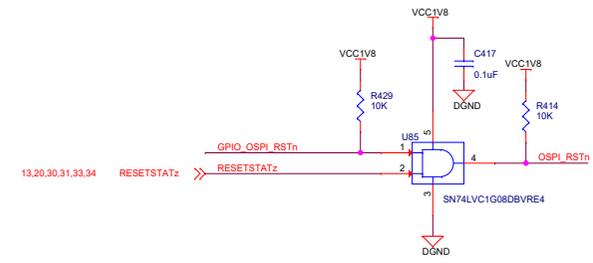
Place R600 close to the memory to avoid stub  
 Place R591 close to the ball with as little trace as possible

To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	Mount R601 & R592
DNI R601 & R592	DNI R591 & R600

# USER TEST LED

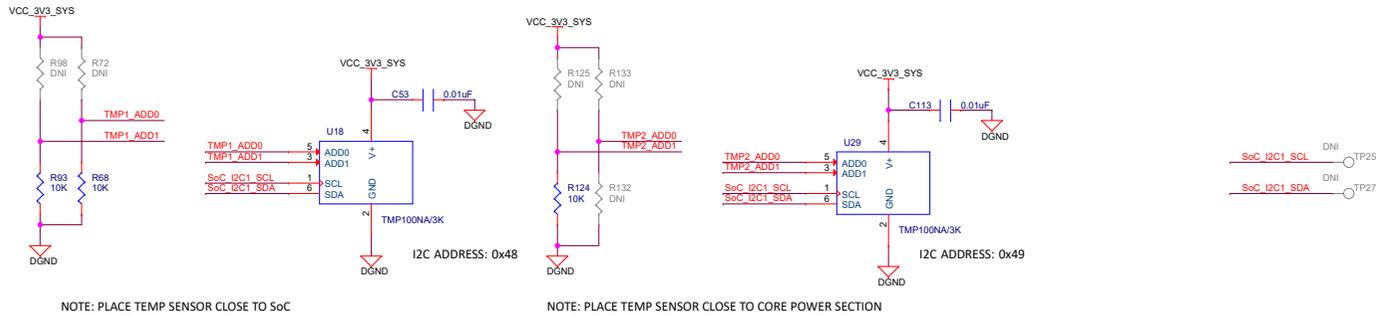


# OSPI FLASH RESET

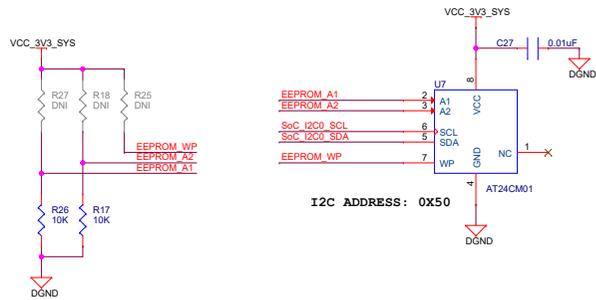


**Off Page Connections**  
 TEST\_LED1 << TEST\_LED1 33  
 TEST\_LED2 << TEST\_LED2 34  
**To Level Translator**  
 DDR\_VTT\_EN << DDR\_VTT\_EN 33

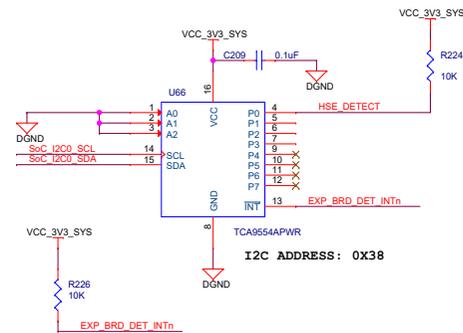
## TEMPERATURE SENSOR



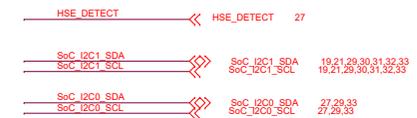
## BOARD ID EEPROM



## BOARD PRESENCE DETECT CIRCUIT



### Off Page Connections

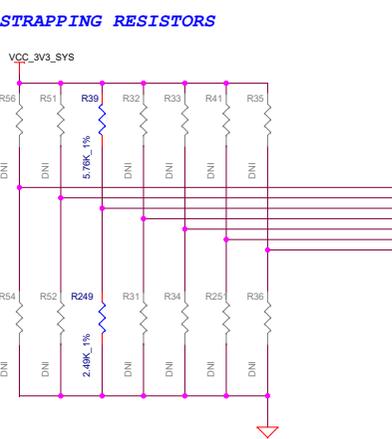
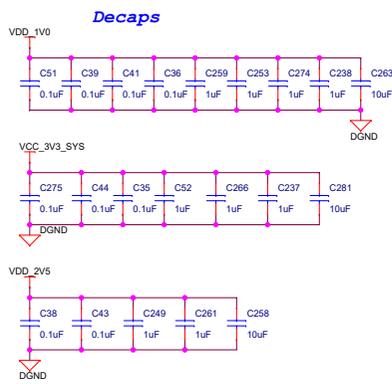


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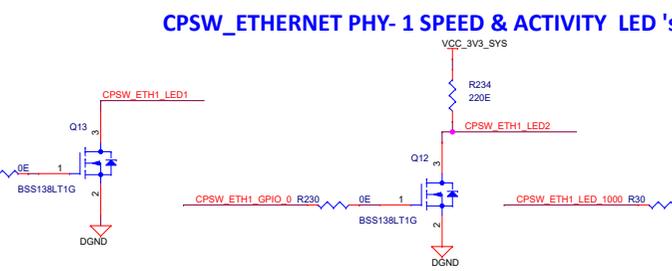
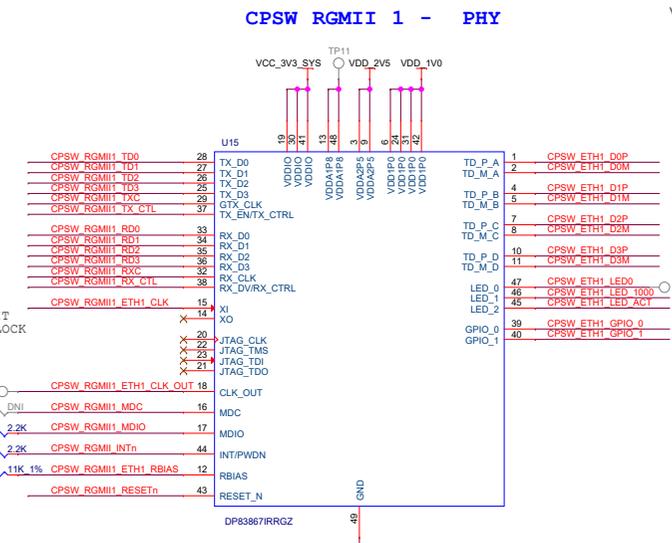
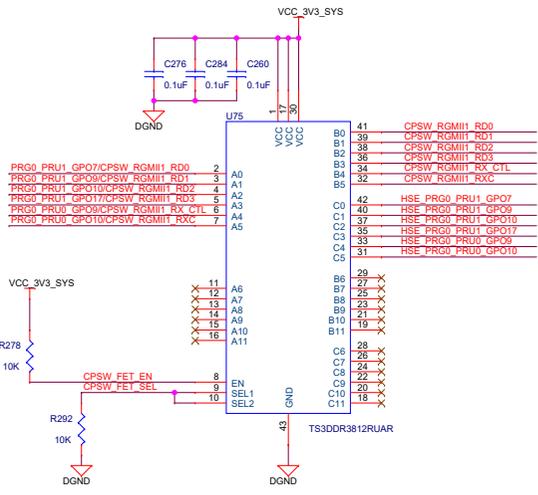


Title: EEPROM.PRESENCE DETECTION & TEMP SENSOR

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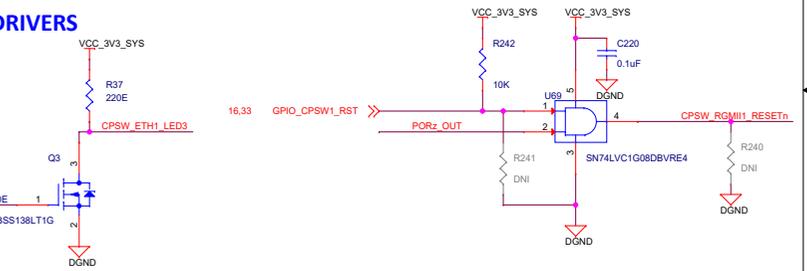
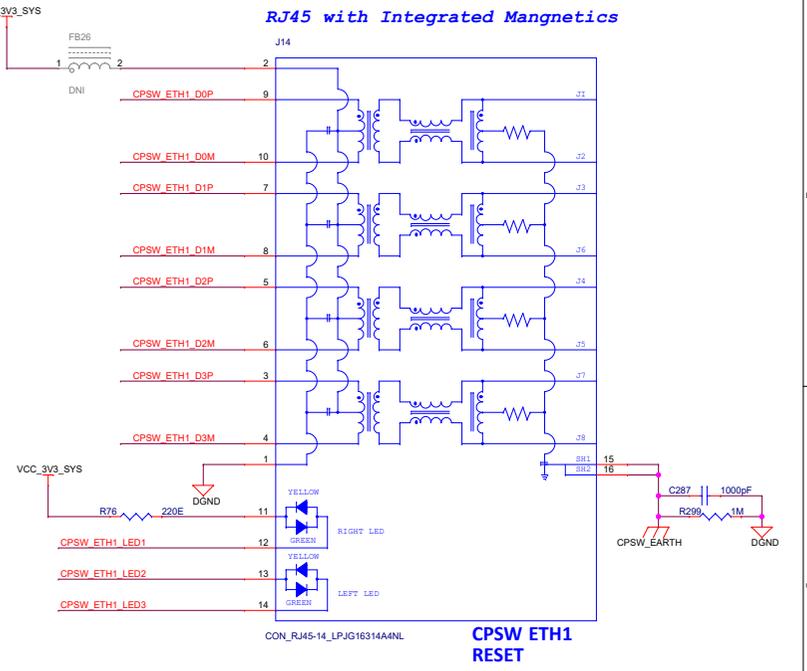


### CPSW RGMII 1 ETHERNET PHY SIGNALS & HSE CON SIGNALS



### TS3DDR3812RUAR Truth Table

EN	SEL1	SEL2	FUNCTION
L	X	X	A0 to A11, B0 to B11, and C0 to C11 are Hi-Z
H	L	L	A0 to A5 = B0 to B5 and A6 to A11 = B6 to B11
H	L	H	A0 to A5 = B0 to B5 and A6 to A11 = C6 to C11
H	H	L	A0 to A5 = C0 to C5 and A6 to A11 = B6 to B11
H	H	H	A0 to A5 = C0 to C5 and A6 to A11 = C6 to C11



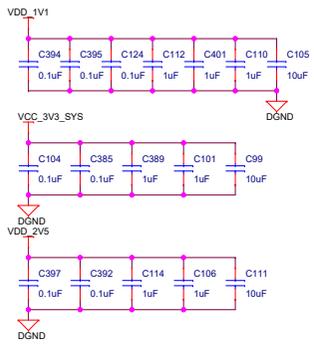
### Off Page Connections

From Processor	Signal	To
27	PRG0_PRU1_GPO7/CPSW_RGMII1_RD0	PRG0_PRU1_GPO7/CPSW_RGMII1_RD0
27	PRG0_PRU1_GPO8/CPSW_RGMII1_RD1	PRG0_PRU1_GPO8/CPSW_RGMII1_RD1
27	PRG0_PRU1_GPO10/CPSW_RGMII1_RD2	PRG0_PRU1_GPO10/CPSW_RGMII1_RD2
27	PRG0_PRU1_GPO17/CPSW_RGMII1_RD3	PRG0_PRU1_GPO17/CPSW_RGMII1_RD3
27	PRG0_PRU0_GPO0/CPSW_RGMII1_RX_CTL	PRG0_PRU0_GPO0/CPSW_RGMII1_RX_CTL
27	PRG0_PRU0_GPO10/CPSW_RGMII1_RXC	PRG0_PRU0_GPO10/CPSW_RGMII1_RXC
27	CPSW_RGMII1_TD0	CPSW_RGMII1_TD0
27	CPSW_RGMII1_TD1	CPSW_RGMII1_TD1
27	CPSW_RGMII1_TD2	CPSW_RGMII1_TD2
27	CPSW_RGMII1_TD3	CPSW_RGMII1_TD3
27	CPSW_RGMII1_TX_CTL	CPSW_RGMII1_TX_CTL
27	CPSW_RGMII1_TXC	CPSW_RGMII1_TXC
13,17,18,20,34	PORz_OUT	PORz_OUT
17,18,34	PRG1_RGMII1_INTn	PRG1_RGMII1_INTn
16,33	GPIO_CPSW1_RST	GPIO_CPSW1_RST
33	CPSW_FET_SEL	CPSW_FET_SEL
31	CPSW_RGMII1_ETH1_CLK	CPSW_RGMII1_ETH1_CLK
27	HSE_PRG0_PRU1_GPO7	HSE_PRG0_PRU1_GPO7
27	HSE_PRG0_PRU1_GPO9	HSE_PRG0_PRU1_GPO9
27	HSE_PRG0_PRU1_GPO10	HSE_PRG0_PRU1_GPO10
27	HSE_PRG0_PRU1_GPO17	HSE_PRG0_PRU1_GPO17
27	HSE_PRG0_PRU0_GPO9	HSE_PRG0_PRU0_GPO9
27	HSE_PRG0_PRU0_GPO10	HSE_PRG0_PRU0_GPO10
17,27	CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
17,27	CPSW_RGMII1_MDC	CPSW_RGMII1_MDC

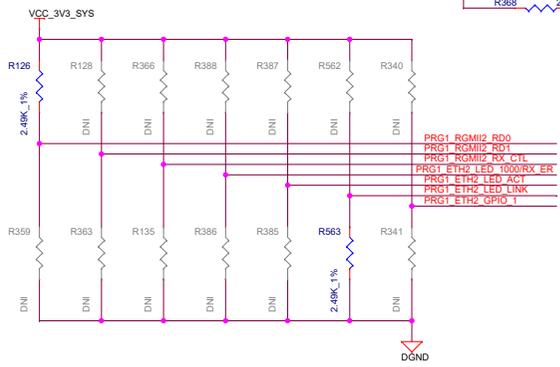
ICSSG1 - RGMII 2

Dual RJ45 CON With Integrated Magnetics

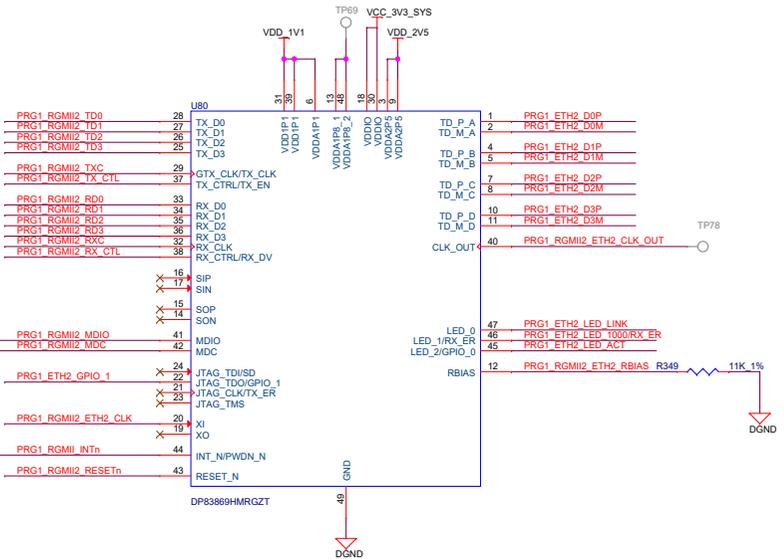
Decaps



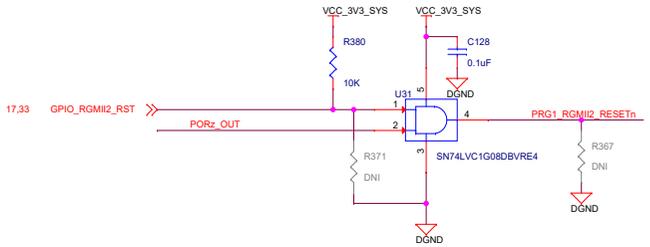
STRAPPING RESISTORS



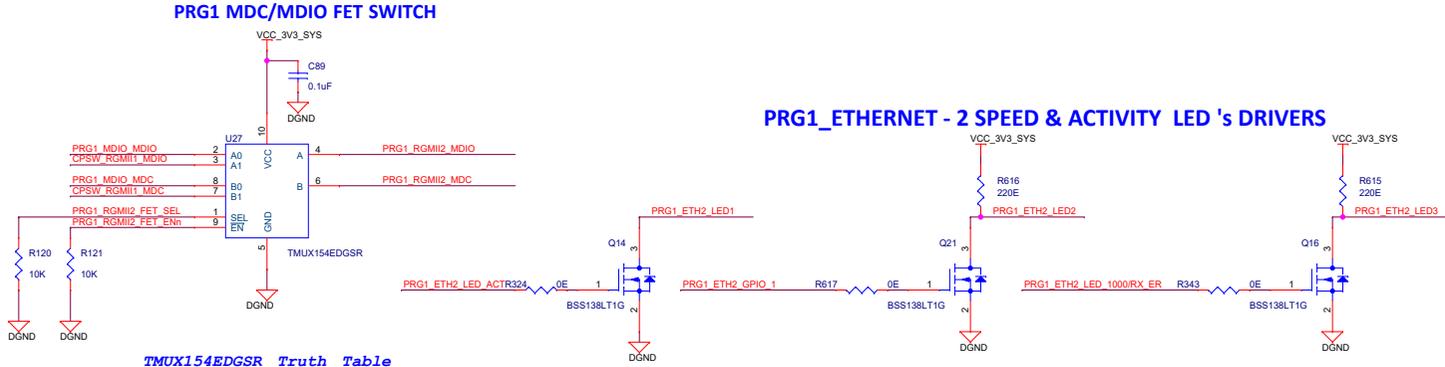
PHY ADDRESS = 00011  
 Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X  
 RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)



PRG1 ETH2 RESET

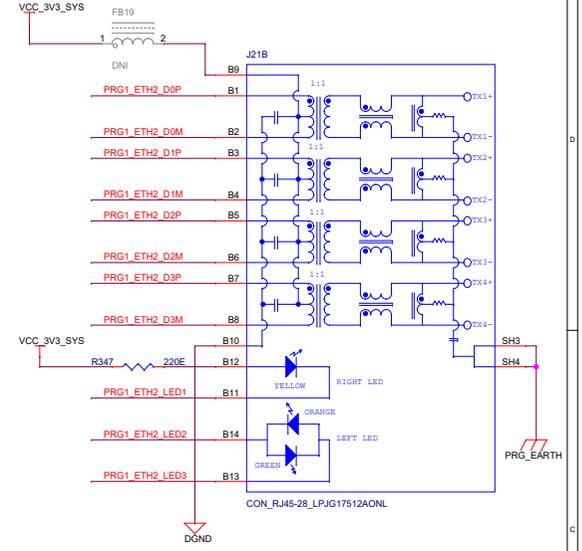


PRG1\_ETHERNET - 2 SPEED & ACTIVITY LED'S DRIVERS



TMUX154EDGSR Truth Table

SEL	EN	FUNCTION
X	H	Decoupled
L	L	A = A0 S = S0
H	L	A = A1 B = B1



Off Page Connections

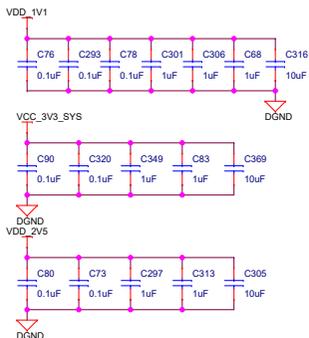
Source	Pin	Signal	Destination
To Processor	16,18,34	PRG1_RGMII_INTn	PRG1_RGMII_INTn
	27	PRG1_RGMII2_RD0	PRG1_RGMII2_RD0
	27	PRG1_RGMII2_RD1	PRG1_RGMII2_RD1
	27	PRG1_RGMII2_RD2	PRG1_RGMII2_RD2
	27	PRG1_RGMII2_RD3	PRG1_RGMII2_RD3
	27	PRG1_RGMII2_RXC	PRG1_RGMII2_RXC
	27	PRG1_RGMII2_TX_CTL	PRG1_RGMII2_TX_CTL
	27	PRG1_ETH2_LED_LINK	PRG1_ETH2_LED_LINK
	27	PRG1_ETH2_LED_1000RX_ER	PRG1_ETH2_LED_1000RX_ER
From Processor	27	PRG1_RGMII2_TD0	PRG1_RGMII2_TD0
	27	PRG1_RGMII2_TD1	PRG1_RGMII2_TD1
	27	PRG1_RGMII2_TD2	PRG1_RGMII2_TD2
	27	PRG1_RGMII2_TD3	PRG1_RGMII2_TD3
	27	PRG1_RGMII2_TXC	PRG1_RGMII2_TXC
	27	PRG1_RGMII2_TX_CTL	PRG1_RGMII2_TX_CTL
	13,16,18,20,34	PORz_OUT	PORz_OUT
	18,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	18,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From CPSW SW	16,27	CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
	16,27	CPSW_RGMII1_MDC	CPSW_RGMII1_MDC
From IO Expander	17,33	GPIO_RGMII2_RST	GPIO_RGMII2_RST
	33	PRG1_RGMII2_FET_SEL	PRG1_RGMII2_FET_SEL
From Clock Buffer	31	PRG1_RGMII2_ETH2_CLK	PRG1_RGMII2_ETH2_CLK

Designed for TI by Mistral Solutions Pvt Ltd

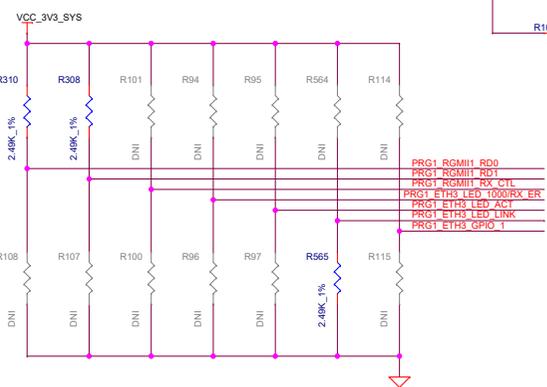


Title		ICSSG1 RGMII_2 ETHERNET PHY	
Size	Variant Name = PROC101C(005) TMS243EVM	Rev	
C		E2	
Date:	Thursday, August 18, 2022	Sheet	17 of 40

Decaps

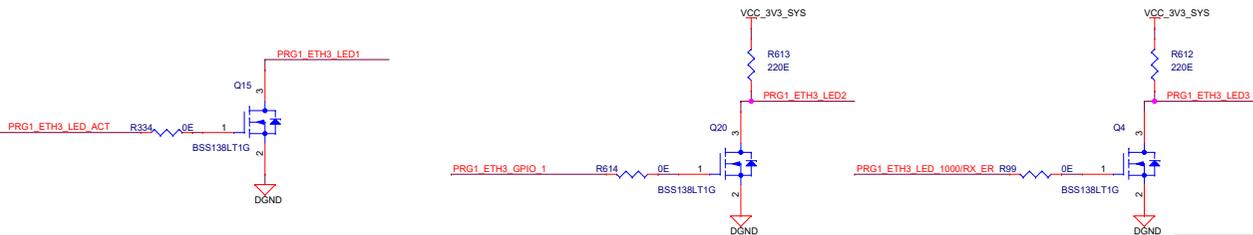


STRAPPING RESISTORS

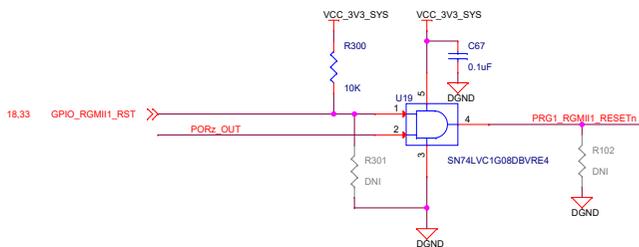


PHY ADDRESS = 01111  
 Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X  
 RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)

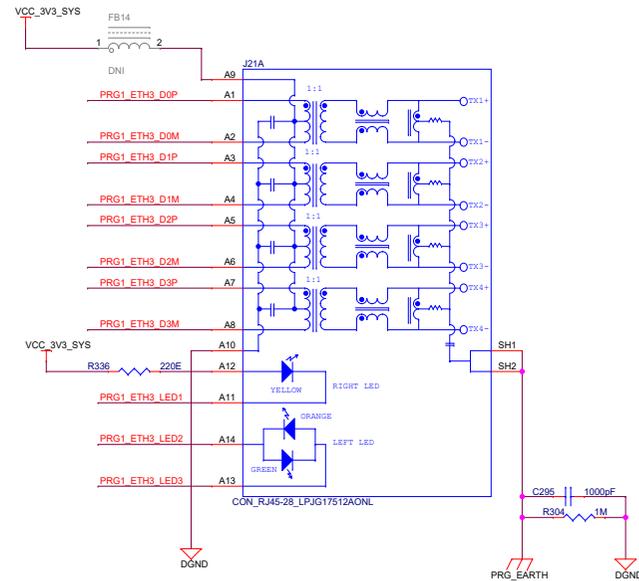
PRG1\_ETHERNET - 3 SPEED & ACTIVITY LED'S DRIVERS



PRG1 ETH2 RESET



Dual RJ45 CON With Integrated Magnetics



Off Page Connections

Signal	Processor Pin	Processor Label	IO Expander Pin	IO Expander Label
To Processor	16,17,34	PRG1_RGMII1_INTn	18,33	GPIO_RGMII1_RST
To Processor	27	PRG1_RGMII1_RD0		
To Processor	27	PRG1_RGMII1_RD1		
To Processor	27	PRG1_RGMII1_RD2		
To Processor	27	PRG1_RGMII1_RD3		
To Processor	27	PRG1_RGMII1_RXC		
To Processor	27	PRG1_RGMII1_RX_CTL		
From Processor	27	PRG1_RGMII1_TD0		
From Processor	27	PRG1_RGMII1_TD1		
From Processor	27	PRG1_RGMII1_TD2		
From Processor	27	PRG1_RGMII1_TD3		
From Processor	27	PRG1_RGMII1_TXC		
From Processor	27	PRG1_RGMII1_TX_CTL		
From Processor	17,27	PRG1_MDIO_MDIO		
From Processor	17,27	PRG1_MDIO_MDC		
From IO Expander	18,33	GPIO_RGMII1_RST		
From Clock Buffer	31	PRG1_RGMII1_ETH3_CLK		

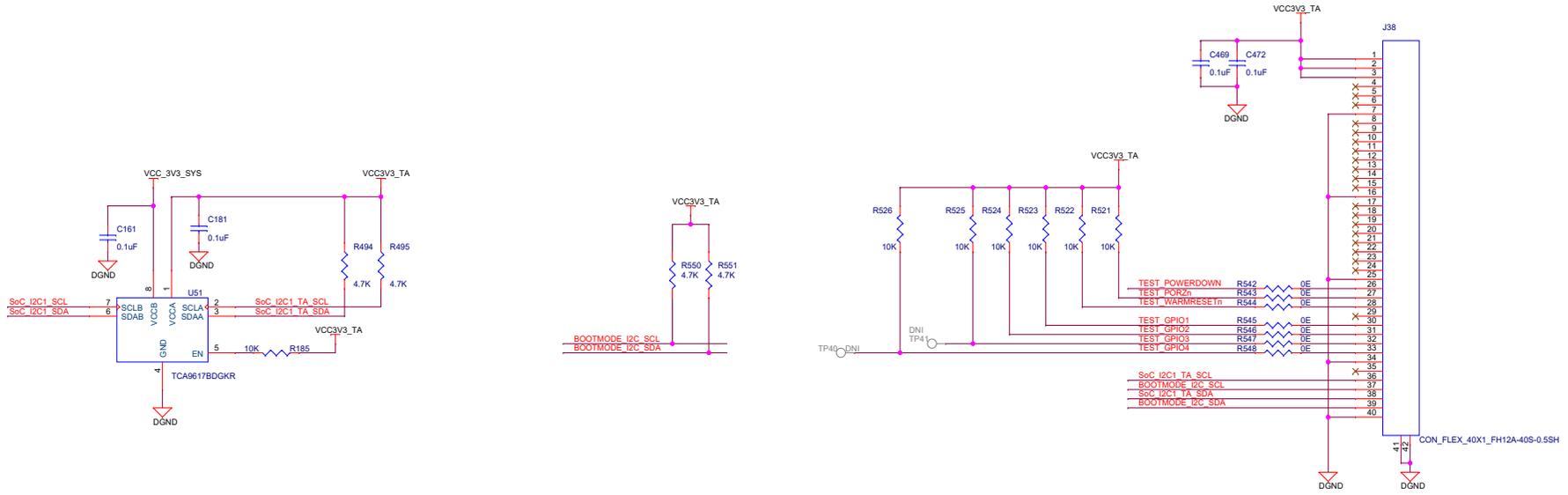
Designed for TI by Mistral Solutions Pvt Ltd



Title		ICSSG2 RGMII1_ETHERNET PHY	
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev E2	
Date:	Thursday, August 18, 2021	Sheet	18 of 40

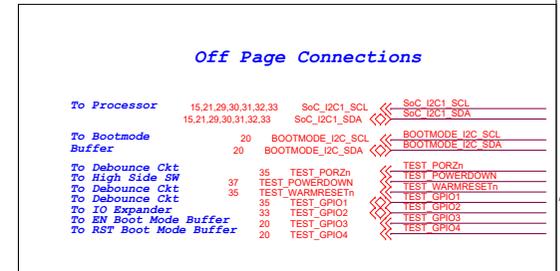
# TEST AUTOMATION

## 40-PIN AUTOMATION HEADER

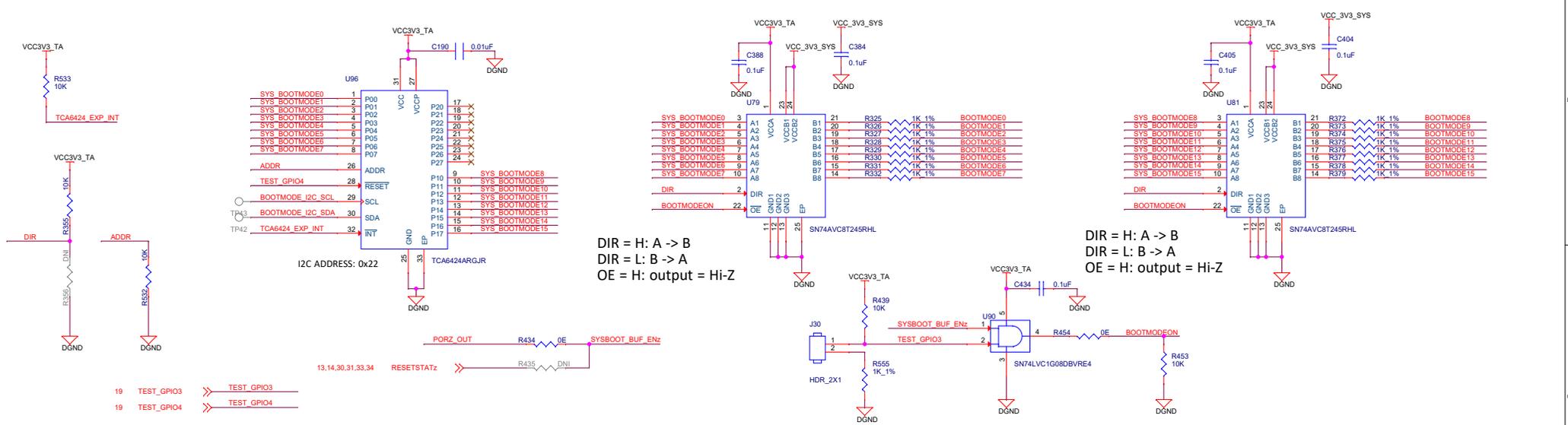


## TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETh	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_13_INTh Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to I/O Expander to Communicate with SoC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

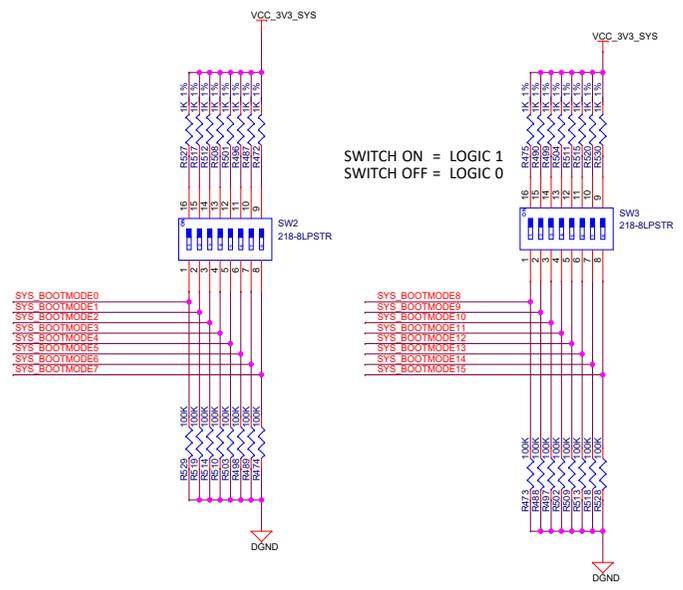


# BOOT MODE BUFFER & SWITCHES



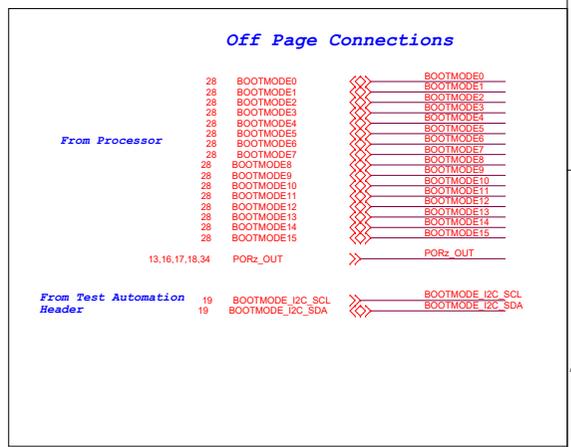
19 TEST\_GPIO3 >>> TEST\_GPIO3  
 19 TEST\_GPIO4 >>> TEST\_GPIO4

13,14,30,31,33,34 RESESTATZ >>> R435 DNI



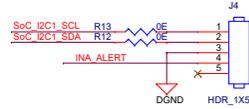
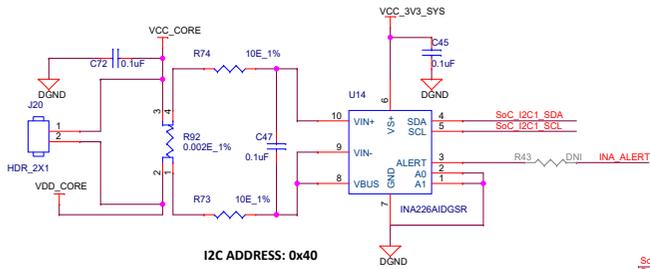
- BOOT MODES SUPPORTED**

  1. OSPI
  2. MMC1 - SD CARD
  3. MMC0 - eMMC
  4. CPSW Ethernet Slave
  5. USB Host
  6. USB Device
  7. UART
  8. Ethernet

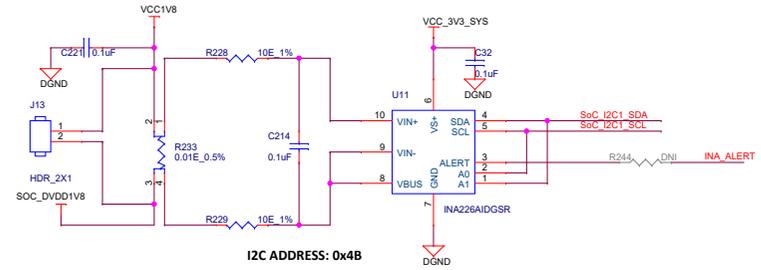


# CURRENT MONITORING DEVICES

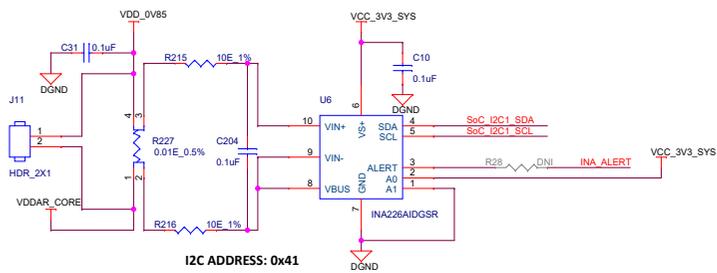
## VDD\_CORE



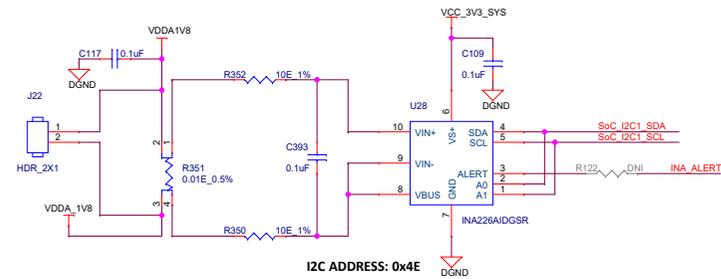
## SoC\_DVDD1V8



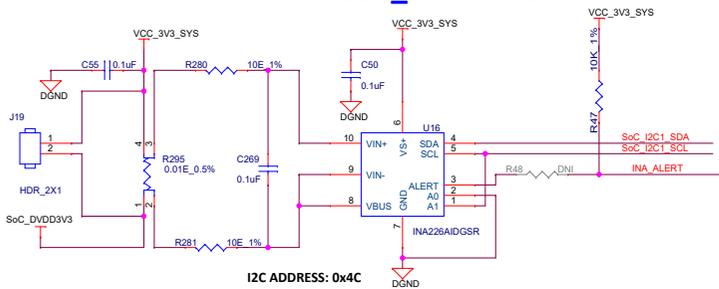
## VDDAR\_CORE



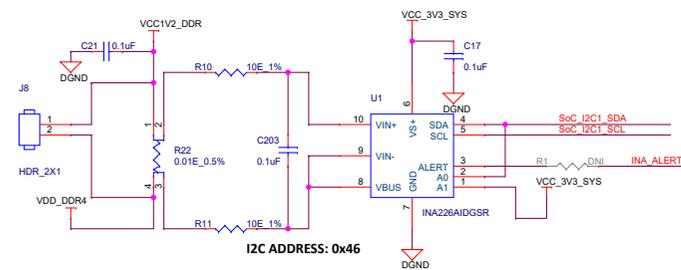
## VDDA\_1V8



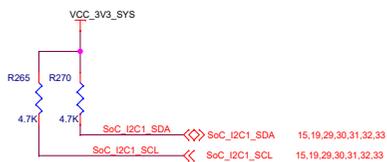
## SoC\_DVDD3V3



## VDD\_DDR4



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_0V85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA_1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46



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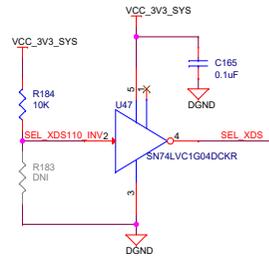
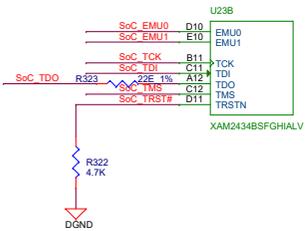
Title CURRENT MONITORING DEVICES

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev	E2
Date:	Thursday, August 18, 2022	Sheet	21 of 40

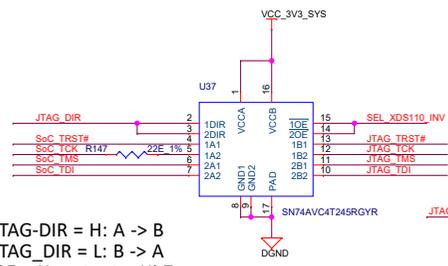


# JTAG BUFFER

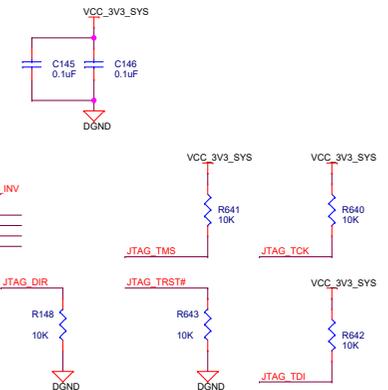
## JTAG SoC SECTION



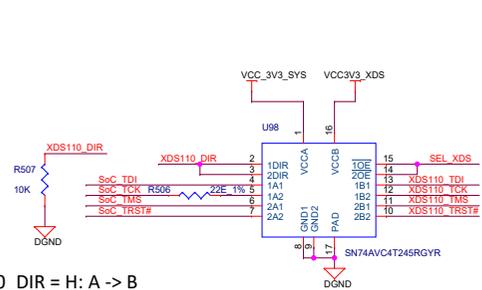
## BUFFER 20 PIN JTAG



JTAG-DIR = H: A -> B  
 JTAG\_DIR = L: B -> A  
 OE = H: output = Hi-Z

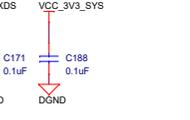
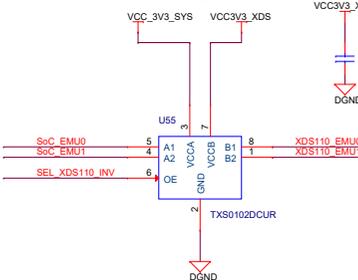
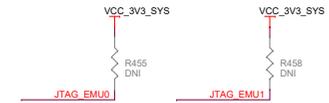
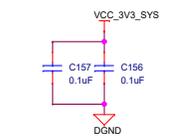
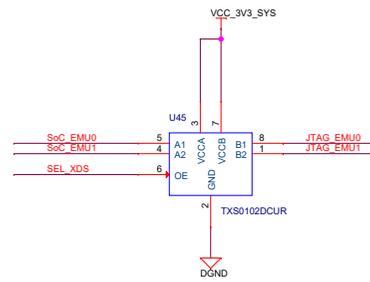
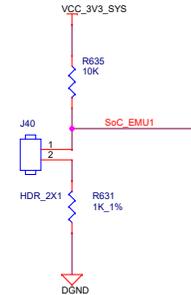
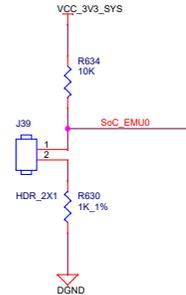
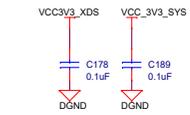
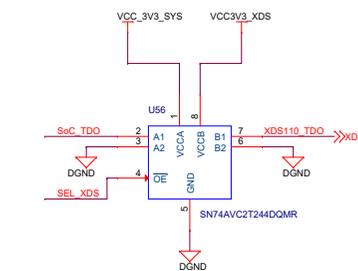
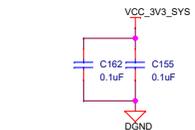
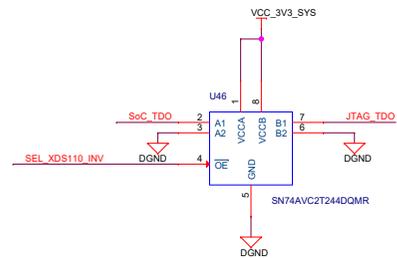
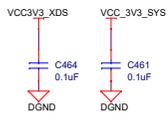


## BUFFER XDS110



XDS110\_DIR = H: A -> B  
 XDS110\_DIR = L: B -> A  
 OE = H: output = Hi-Z

Placement of Buffers U37, U46, U56 and U98 to be changed to reduce Stub length of the JTAG signals. These buffers need to be placed closer to the CTI-20pin connector -J25



### Off Page Connections

24	SEL_XDS110_INV	XDS110_INV
24	JTAG_EMU0	JTAG_EMU0
24	JTAG_EMU1	JTAG_EMU1
22	XDS110_TDI	XDS110_TCK
22	XDS110_TCK	XDS110_TMS
22	XDS110_TMS	XDS110_TRST#
22	XDS110_TRST#	JTAG_TDI
24	JTAG_TDI	JTAG_TCK
24	JTAG_TCK	JTAG_TMS
24	JTAG_TMS	JTAG_TRST#
24	JTAG_TRST#	JTAG_TDO
22	XDS110_EMU0	XDS110_EMU0
22	XDS110_EMU1	XDS110_EMU1

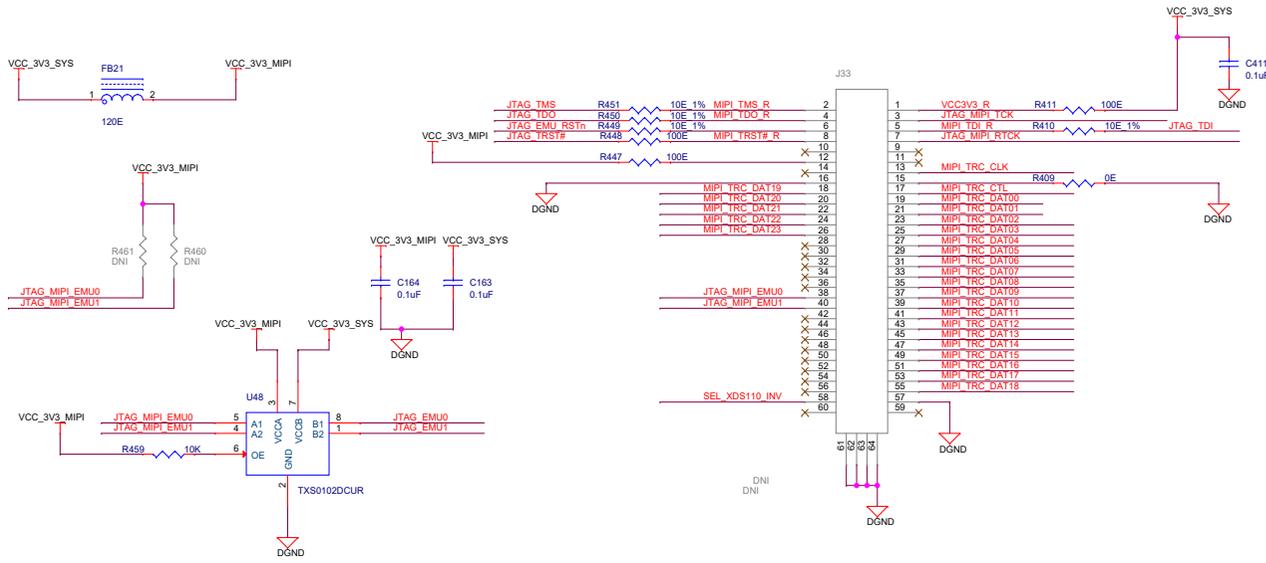
From XDS110 Debugger

Designed for TI by Mistral Solutions Pvt Ltd

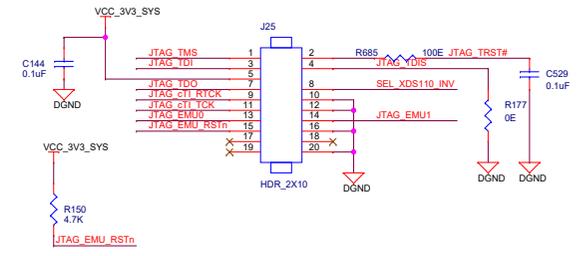


Title		JTAG BUFFER
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev E2
Date:	Thursday, August 18, 2022	Sheet 23 of 40

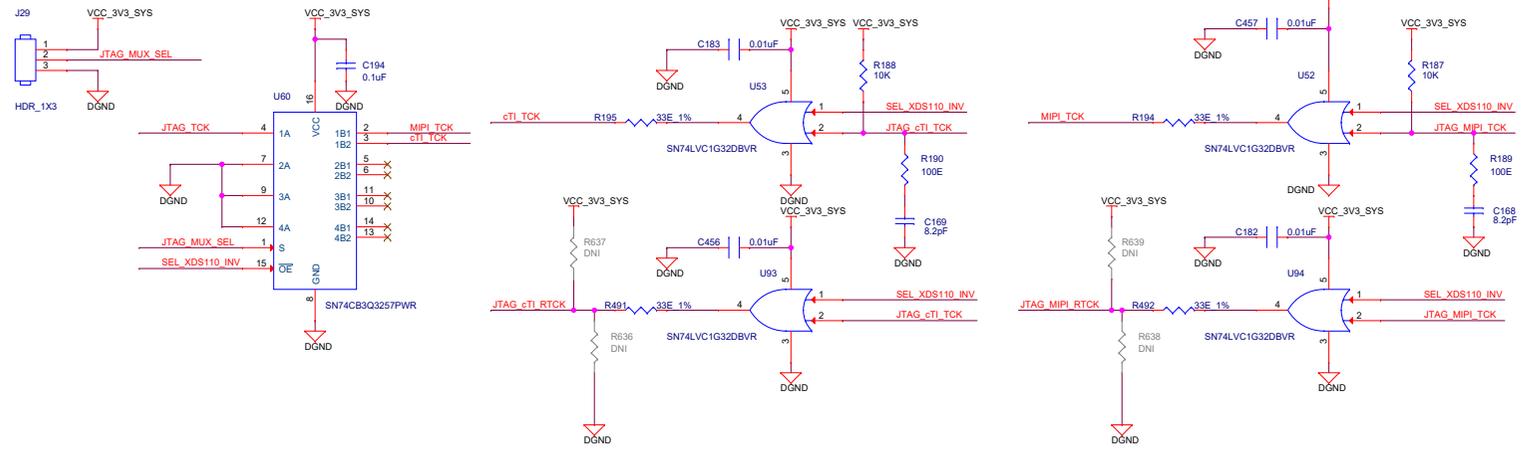
# MIPI 60 PIN CONNECTOR



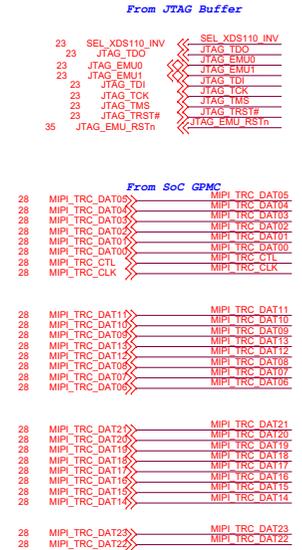
# JTAG 20 PIN cTI CONNECTOR



# JTAG CLOCK BUFFER



# Off Page Connections



Designed for TI by Mistral Solutions Pvt Ltd

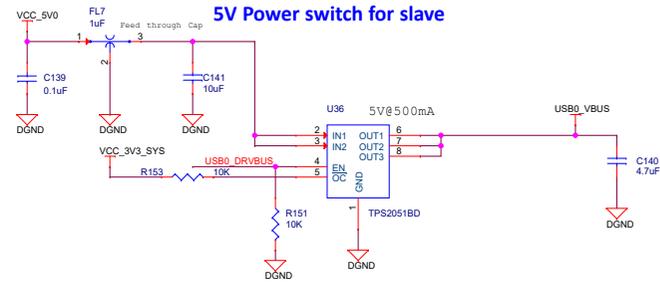
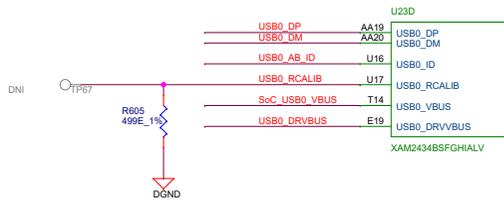


Title: MIPI 60 PIN CONNECTOR

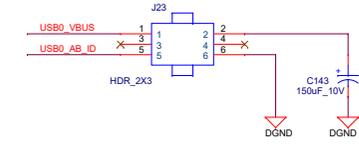
Size: Variant Name = PROC101C(005) TMD5243EVM  
 Date: Thursday, August 18, 2022

Rev: E2  
 Sheet: 24 of 40

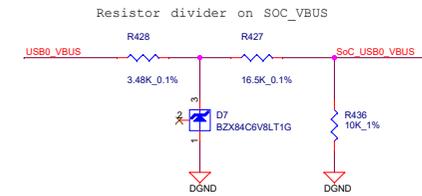
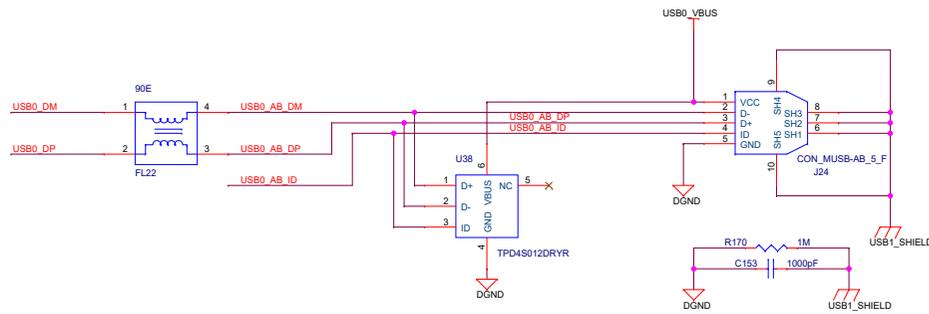
# USB 2.0 INTERFACE



X3 header to enable bulk capacitance on USB0\_VBUS in host mode and to ground USB0\_AB\_ID pin, if a non standard cable is used



## Micro USB 2.0 AB Connector



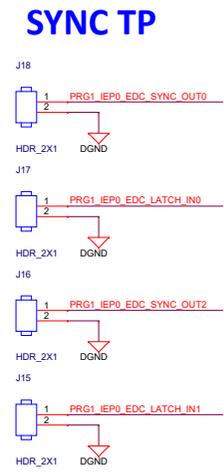
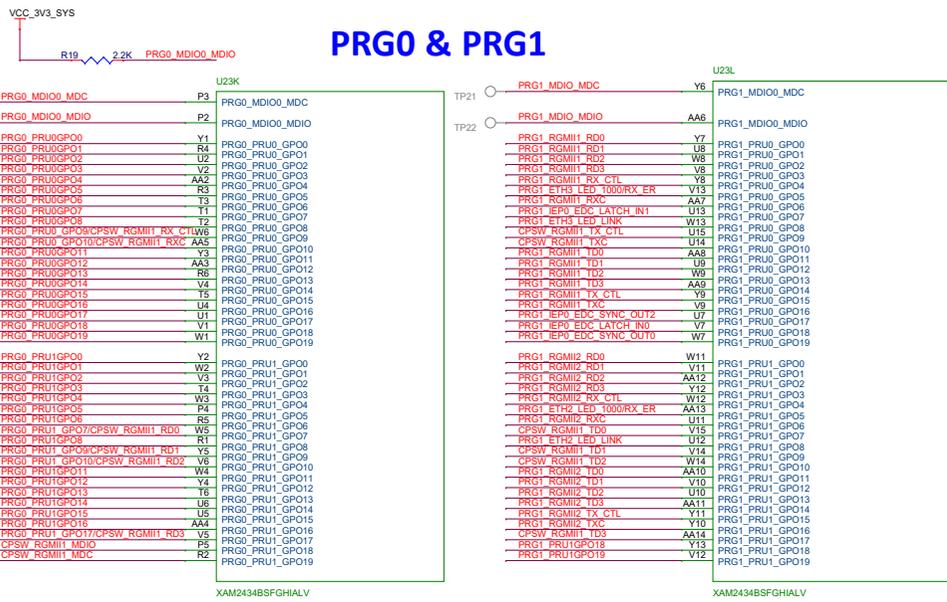
Designed for TI by Mistral Solutions Pvt Ltd



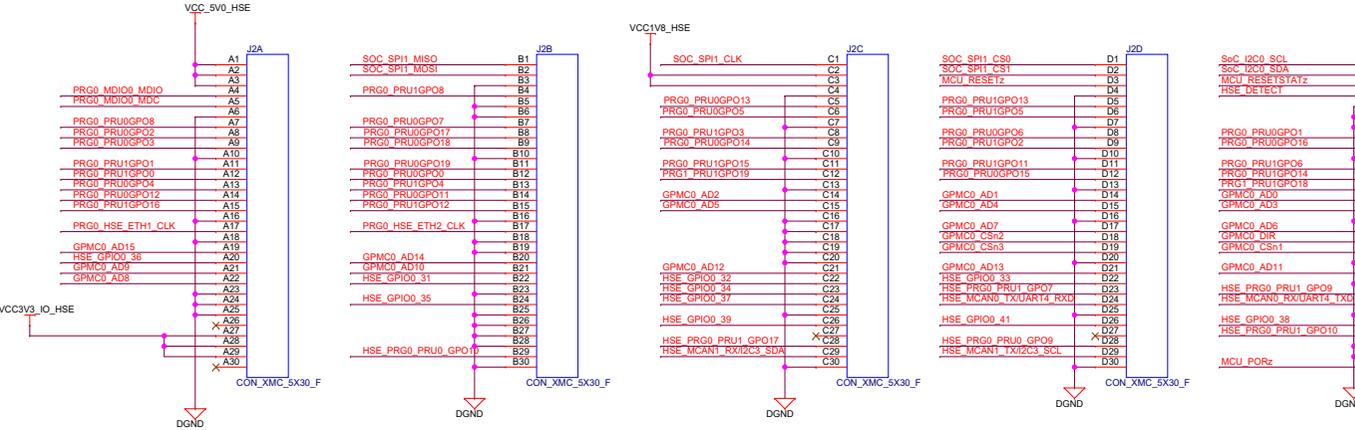
Title: USB 2.0 INTERFACE

Size	Variant Name = PROC101C(005) TMDS243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 25 of 40

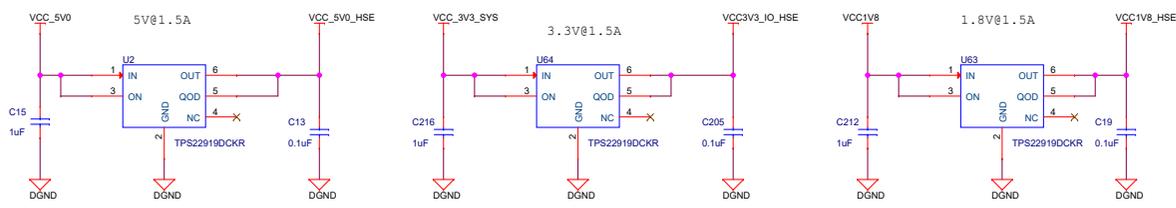




### HIGH SPEED EXPANSION CONNECTOR



### HSE CONNECTOR LOAD SWITCHES



### Off Page Connections

<b>To Presence Detect Buffer</b>	15	HSE_DETECT	HSE_DETECT
<b>From Processor GPMC</b>	28	GPMC0_CSn1	GPMC0_CSn1
	28	GPMC0_CSn2	GPMC0_CSn2
	28	GPMC0_CSn3	GPMC0_CSn3
	28	GPMC0_DIR	GPMC0_DIR
<b>From FSI mux</b>	28	GPMC0_A08	GPMC0_A08
	28	GPMC0_A09	GPMC0_A09
	28	GPMC0_A10	GPMC0_A10
	28	GPMC0_A14	GPMC0_A14
	28	GPMC0_A15	GPMC0_A15
	28	HSE_GPI00_38	HSE_GPI00_38
<b>From Processor GPMC resistor muxed with MIFI</b>	28	GPMC0_A01	GPMC0_A01
	28	GPMC0_A02	GPMC0_A02
	28	GPMC0_A03	GPMC0_A03
	28	GPMC0_A04	GPMC0_A04
	28	GPMC0_A05	GPMC0_A05
	28	GPMC0_A06	GPMC0_A06
	28	GPMC0_A07	GPMC0_A07
	28	GPMC0_A11	GPMC0_A11
	28	GPMC0_A12	GPMC0_A12
	28	GPMC0_A13	GPMC0_A13
	28	HSE_GPI00_31	HSE_GPI00_31
	28	HSE_GPI00_32	HSE_GPI00_32
	28	HSE_GPI00_33	HSE_GPI00_33
	28	HSE_GPI00_34	HSE_GPI00_34
	28	HSE_GPI00_35	HSE_GPI00_35
	28	HSE_GPI00_36	HSE_GPI00_36
	28	HSE_GPI00_37	HSE_GPI00_37
	28	HSE_GPI00_38	HSE_GPI00_38
	28	HSE_GPI00_39	HSE_GPI00_39
	28	HSE_GPI00_40	HSE_GPI00_40
	28	HSE_GPI00_41	HSE_GPI00_41
<b>From Processor</b>	34	MCU_PORz	MCU_PORz
	34	MCU_RESETz	MCU_RESETz
	34	MCU_RESETATz	MCU_RESETATz
	29	HSE_MCAN0_RXUART4_TXD	HSE_MCAN0_RXUART4_TXD
	29	HSE_MCAN0_TXUART4_RXD	HSE_MCAN0_TXUART4_RXD
	29	HSE_MCAN1_RXI2C3_SDA	HSE_MCAN1_RXI2C3_SDA
	29	HSE_MCAN1_TXI2C3_SCL	HSE_MCAN1_TXI2C3_SCL
	29	SOC_SPHI_CLK	SOC_SPHI_CLK
	29	SOC_SPHI_MOS	SOC_SPHI_MOS
	29	SOC_SPHI_MISO	SOC_SPHI_MISO
	29	SOC_SPHI_CS0	SOC_SPHI_CS0
	29	SOC_SPHI_CS1	SOC_SPHI_CS1
	29	SOC_SPHI_CS2	SOC_SPHI_CS2
	15,29,33	Soc_I2C0_SCL	Soc_I2C0_SCL
	15,29,33	Soc_I2C0_SDA	Soc_I2C0_SDA
<b>From clock Buffer</b>	31	PRG0_HSE_ETH1_CLK	PRG0_HSE_ETH1_CLK
	31	PRG0_HSE_ETH2_CLK	PRG0_HSE_ETH2_CLK
<b>To and from ICSSG1 RGMII 2 Ethernet PHY</b>	17	PRG1_RGMII2_RD0	PRG1_RGMII2_RD0
	17	PRG1_RGMII2_RD1	PRG1_RGMII2_RD1
	17	PRG1_RGMII2_RD2	PRG1_RGMII2_RD2
	17	PRG1_RGMII2_RD3	PRG1_RGMII2_RD3
	17	PRG1_RGMII2_RXC	PRG1_RGMII2_RXC
	17	PRG1_RGMII2_RX_CTL	PRG1_RGMII2_RX_CTL
	17	PRG1_ETH2_LED_1000RX_ER	PRG1_ETH2_LED_1000RX_ER
	17	PRG1_RGMII2_TD0	PRG1_RGMII2_TD0
	17	PRG1_RGMII2_TD1	PRG1_RGMII2_TD1
	17	PRG1_RGMII2_TD2	PRG1_RGMII2_TD2
	17	PRG1_RGMII2_TD3	PRG1_RGMII2_TD3
	17	PRG1_RGMII2_TXC	PRG1_RGMII2_TXC
	17	PRG1_RGMII2_TX_CTL	PRG1_RGMII2_TX_CTL
<b>To and from ICSSG2 RGMII 1 Ethernet PHY</b>	17,18	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	17,18	PRG1_MDIO_MDC	PRG1_MDIO_MDC
	18	PRG1_ETH3_LED_LINK	PRG1_ETH3_LED_LINK
	17	PRG1_ETH3_LED_LINK	PRG1_ETH3_LED_LINK
	18	PRG1_RGMII1_RD0	PRG1_RGMII1_RD0
	18	PRG1_RGMII1_RD1	PRG1_RGMII1_RD1
	18	PRG1_RGMII1_RD2	PRG1_RGMII1_RD2
	18	PRG1_RGMII1_RD3	PRG1_RGMII1_RD3
	18	PRG1_RGMII1_RXC	PRG1_RGMII1_RXC
	18	PRG1_RGMII1_RX_CTL	PRG1_RGMII1_RX_CTL
	18	PRG1_ETH3_LED_1000RX_ER	PRG1_ETH3_LED_1000RX_ER
	18	PRG1_RGMII1_TD0	PRG1_RGMII1_TD0
	18	PRG1_RGMII1_TD1	PRG1_RGMII1_TD1
	18	PRG1_RGMII1_TD2	PRG1_RGMII1_TD2
	18	PRG1_RGMII1_TD3	PRG1_RGMII1_TD3
	18	PRG1_RGMII1_TXC	PRG1_RGMII1_TXC
	18	PRG1_RGMII1_TX_CTL	PRG1_RGMII1_TX_CTL
<b>From MUX To HSE</b>	16	HSE_PRG0_PRUI_GPO7	HSE_PRG0_PRUI_GPO7
	16	HSE_PRG0_PRUI_GPO9	HSE_PRG0_PRUI_GPO9
	16	HSE_PRG0_PRUI_GPO10	HSE_PRG0_PRUI_GPO10
	16	HSE_PRG0_PRUI_GPO17	HSE_PRG0_PRUI_GPO17
	16	HSE_PRG0_PRUI_GPO9	HSE_PRG0_PRUI_GPO9
	16	HSE_PRG0_PRUI_GPO10	HSE_PRG0_PRUI_GPO10
<b>To MUX From SoC</b>	16,17	CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
	16,17	CPSW_RGMII1_MDC	CPSW_RGMII1_MDC
	16	PRG0_PRUI_GPO7/CPSW_RGMII1_RD0	PRG0_PRUI_GPO7/CPSW_RGMII1_RD0
	16	PRG0_PRUI_GPO9/CPSW_RGMII1_RD2	PRG0_PRUI_GPO9/CPSW_RGMII1_RD2
	16	PRG0_PRUI_GPO17/CPSW_RGMII1_RD3	PRG0_PRUI_GPO17/CPSW_RGMII1_RD3
	16	PRG0_PRUI_GPO7/CPSW_RGMII1_RX_CTL	PRG0_PRUI_GPO7/CPSW_RGMII1_RX_CTL
	16	PRG0_PRUI_GPO9/CPSW_RGMII1_RXC	PRG0_PRUI_GPO9/CPSW_RGMII1_RXC
	16	PRG0_PRUI_GPO10/CPSW_RGMII1_RXC	PRG0_PRUI_GPO10/CPSW_RGMII1_RXC
<b>From CPSW RGMII 1 PHY</b>	16	CPSW_RGMII1_TD0	CPSW_RGMII1_TD0
	16	CPSW_RGMII1_TD1	CPSW_RGMII1_TD1
	16	CPSW_RGMII1_TD2	CPSW_RGMII1_TD2
	16	CPSW_RGMII1_TD3	CPSW_RGMII1_TD3
	16	CPSW_RGMII1_TX_CTL	CPSW_RGMII1_TX_CTL
	16	CPSW_RGMII1_TXC	CPSW_RGMII1_TXC

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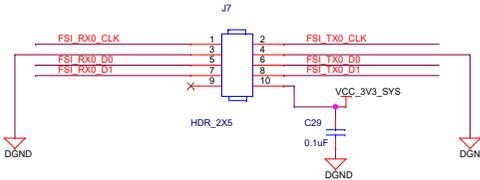
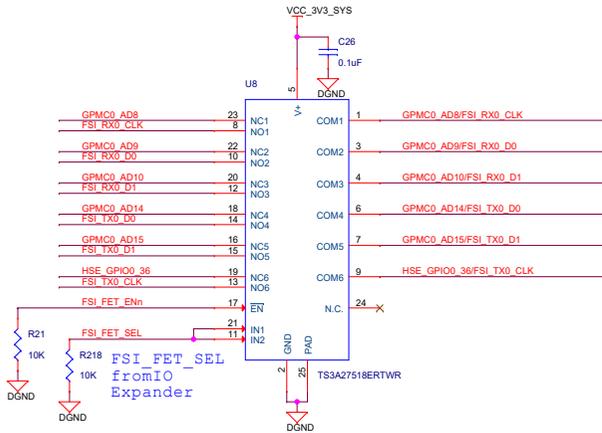
Title		HSE CONNECTOR	
Size	Variant Name =	PR0C101C(005) TMD5243EVM	Rev
C			E2
Date:	Thursday, August 18, 2022	Sheet	27 of 40

# GPMC



## GPMC TO FSI & HSE CONNECTOR

## FSI CONNECTOR



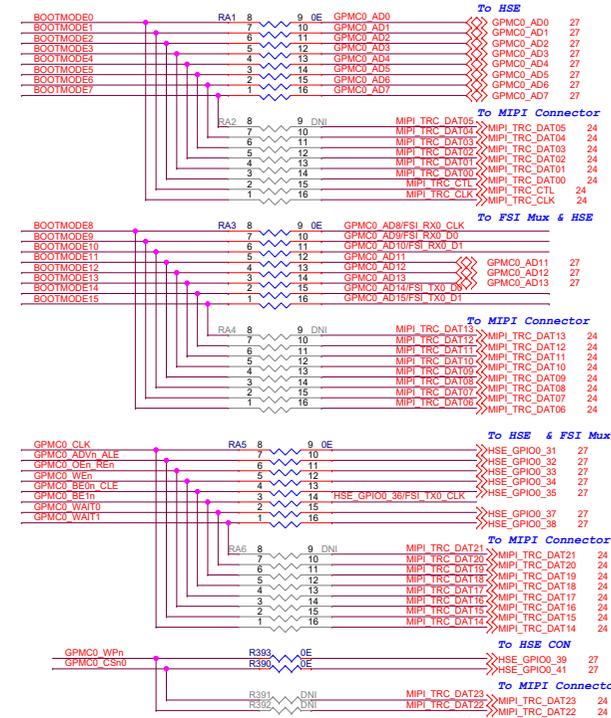
**TS3A27518ERTWR Truth Table**

EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & NC1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6 & NC4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & NO1/2/3 TO NO1/2/3	NC4/5/6 TO COM4/5/6 & NC4/5/6 TO NC4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

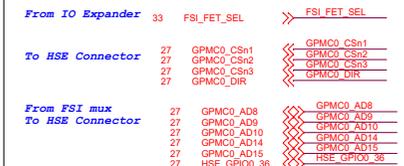
0- Ohm Res MUX between HSE Connector and TRACE Functionality

-For HSE Connector RA1, RA3, RA5, R393 & R390 Should be installed and RA2, RA4, RA6, R391 & R392 Should be DNI'd.

-For TRACE RA2, RA4, RA6, R391 & R392 Should be installed and RA1, RA3, RA5, R393 & R390 Should be DNI'd.



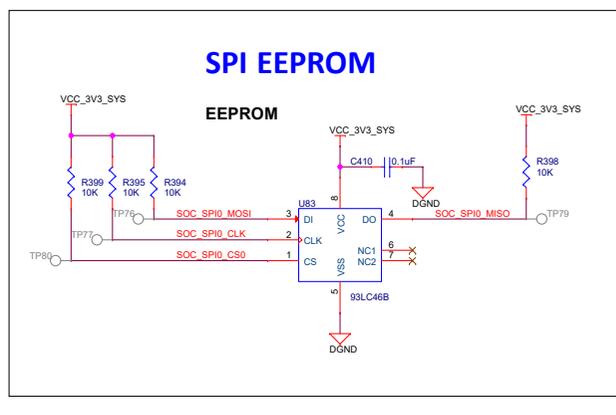
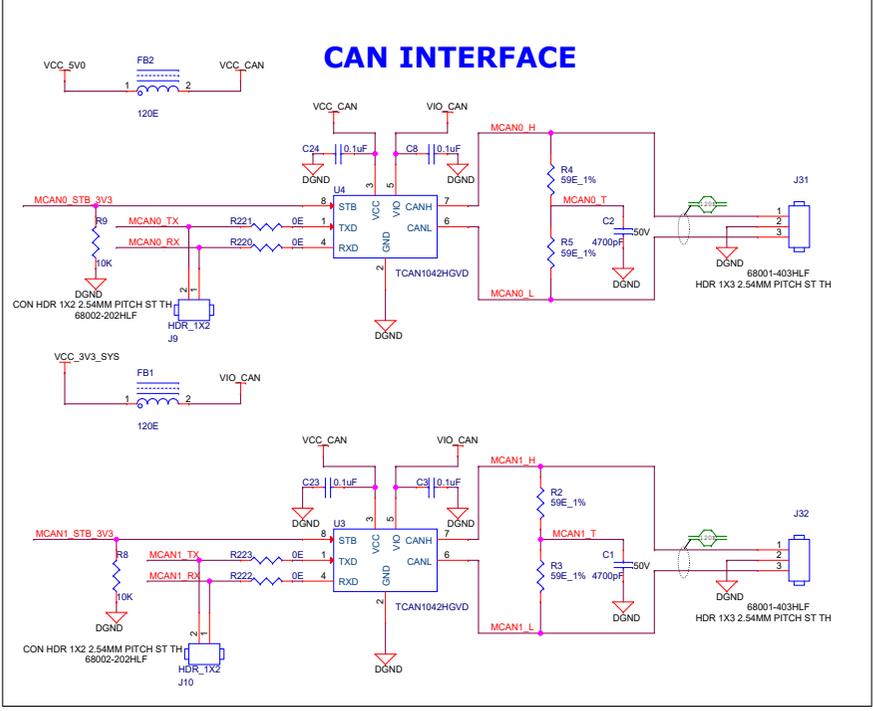
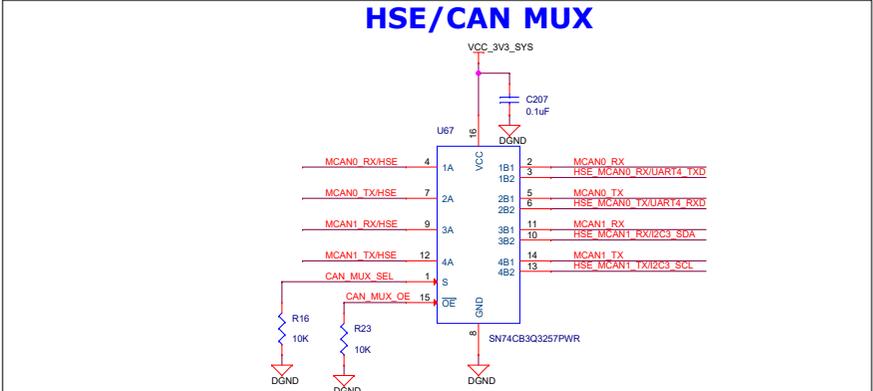
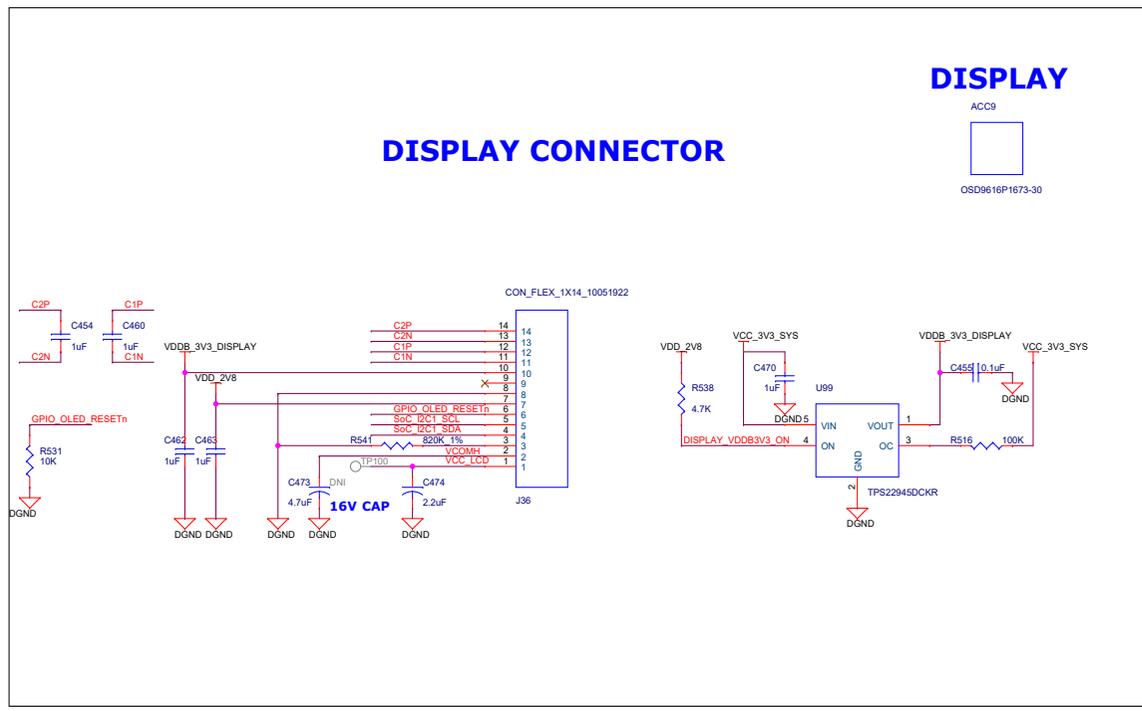
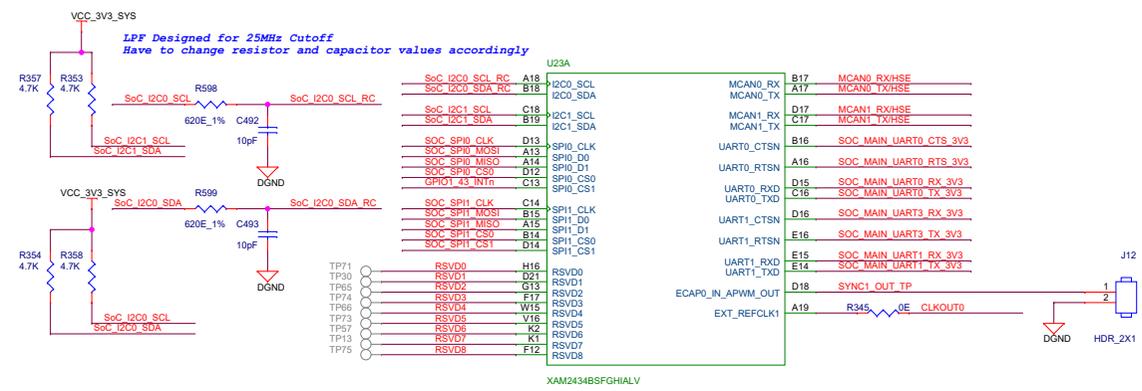
## Off Page Connections



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Title		GPMC	
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev	
C		E2	
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**Off Page Connections**

From Debounce Circuit	GPIO1_43_INn	GPIO1_43_INn	35
From IO Expander	GPIO_OLED_RESETn	GPIO_OLED_RESETn	33
From IO Expander	MCAN1_STB_3V3	MCAN1_STB_3V3	33
From IO Expander	MCAN0_STB_3V3	MCAN0_STB_3V3	33
To HSE Connector	CAN_MUX_SEL	CAN_MUX_SEL	33
To HSE Connector	HSE_MCAN0_RX/UART4_TXD	HSE_MCAN0_RX/UART4_TXD	27
To HSE Connector	HSE_MCAN0_TX/UART4_RXD	HSE_MCAN0_TX/UART4_RXD	27
To HSE Connector	HSE_MCAN1_RX/I2C3_SDA	HSE_MCAN1_RX/I2C3_SDA	27
To HSE Connector	HSE_MCAN1_TX/I2C3_SCL	HSE_MCAN1_TX/I2C3_SCL	27
To Clock Buffer	SOC_SPI1_CLK	SOC_SPI1_CLK	27
To Clock Buffer	SOC_SPI1_MOSI	SOC_SPI1_MOSI	27
To Clock Buffer	SOC_SPI1_CS0	SOC_SPI1_CS0	27
To Clock Buffer	SOC_SPI1_CS1	SOC_SPI1_CS1	27
To FT4232 Bridge	SOC_I2C0_SCL	SOC_I2C0_SCL	15,27,33
To FT4232 Bridge	SOC_I2C0_SDA	SOC_I2C0_SDA	15,27,33
To FT4232 Bridge	SOC_I2C1_SCL	SOC_I2C1_SCL	15,19,21,30,31,32,33
To FT4232 Bridge	SOC_I2C1_SDA	SOC_I2C1_SDA	15,19,21,30,31,32,33
To FT4232 Bridge	CLKOUT0	CLKOUT0	31
To FT4232 Bridge	SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3	26
To FT4232 Bridge	SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3	26
To FT4232 Bridge	SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3	26
To FT4232 Bridge	SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3	26
To FT4232 Bridge	SOC_MAIN_UART1_TX_3V3	SOC_MAIN_UART1_TX_3V3	26
To FT4232 Bridge	SOC_MAIN_UART1_RX_3V3	SOC_MAIN_UART1_RX_3V3	26
To FT4232 Bridge	SOC_MAIN_UART3_TX_3V3	SOC_MAIN_UART3_TX_3V3	26
To FT4232 Bridge	SOC_MAIN_UART3_RX_3V3	SOC_MAIN_UART3_RX_3V3	26

PROC101C(005) TMD8243EVM

Project : Designed for TI by Mistral Solutions Pvt Ltd

**<Project Name>**

**Texas Instruments**

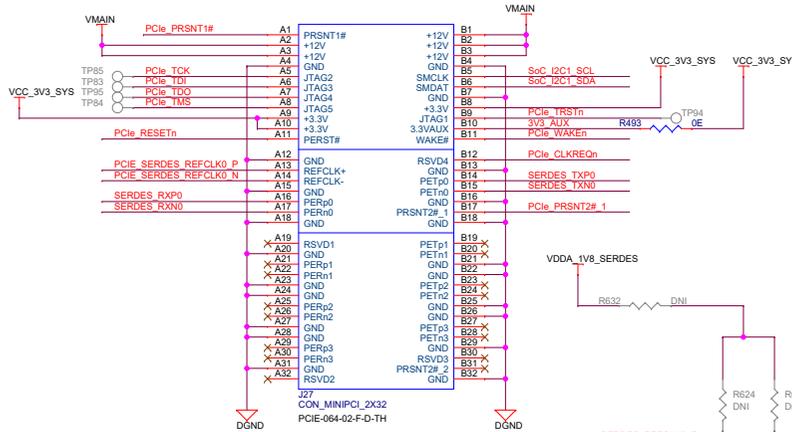
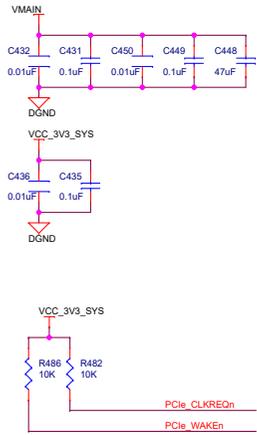
**MISTRAL**

**CAN & DISPLAY INTERFACE**

Size	Document Number	Rev
C	MS_TI_MAXIE_APPLICATION_CARD_SCH_REVA	E2

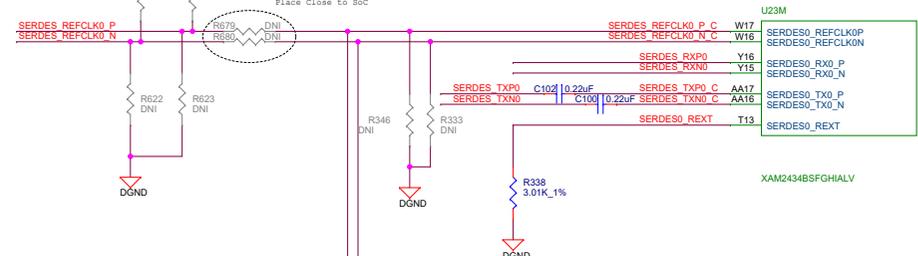
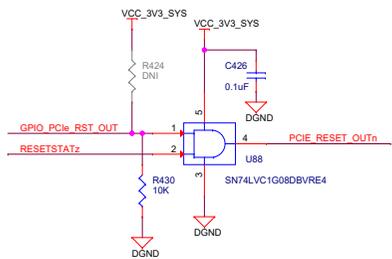
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# x4 Lane PCIe Connector

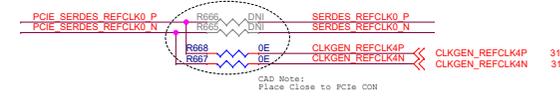


**Note:**  
 R679 , R680 Mounted with 0E Resistor when PCIe REFCLK is in no Re-biasing Mode.  
 R679 , R680 to be replaced with 100nf CAP 0402 package when PCIe REFCLK is in Re-biasing Mode.

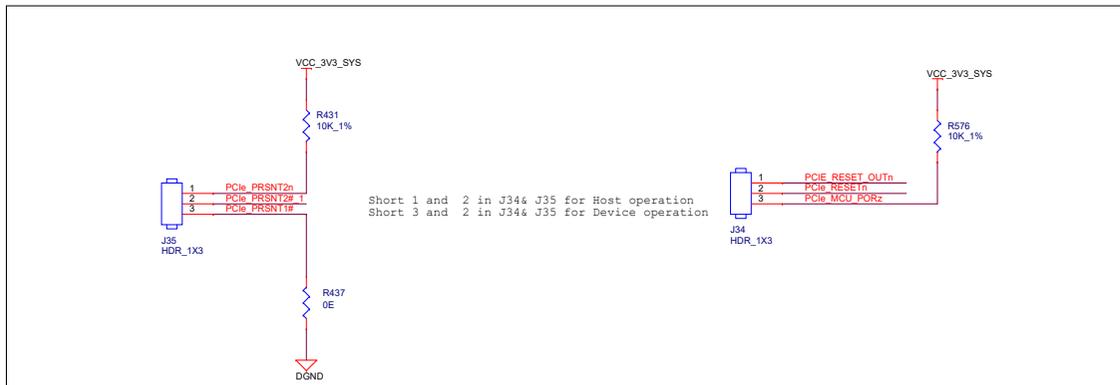
## PCIe Reset



## CLOCK SELECTION



## RC OR EP MODE SELECTION



## Off Page Connections

PCIe MCU_PORz	PCIe_MCU_PORz	34
GPIO_Pcie_RST_OUT	GPIO_Pcie_RST_OUT	33
RESETSTATz	RESETSTATz	13,14,20,31,33,34
SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,31,32,33
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,31,32,33

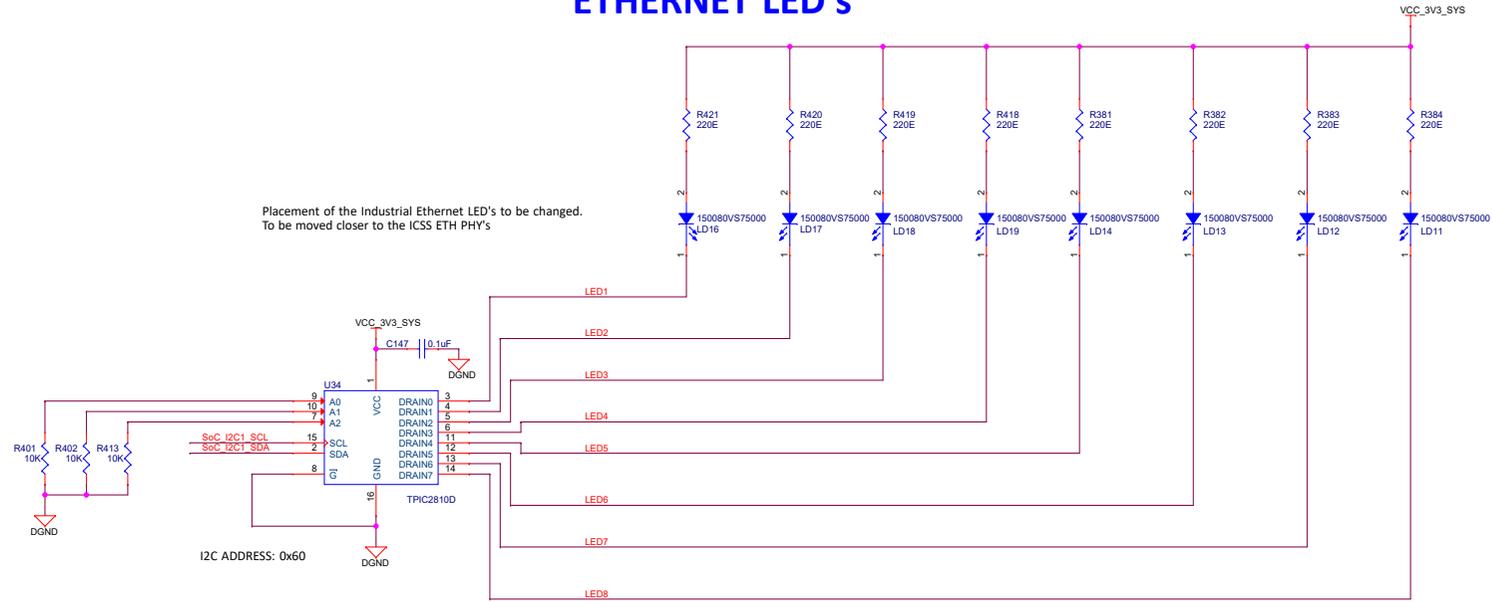
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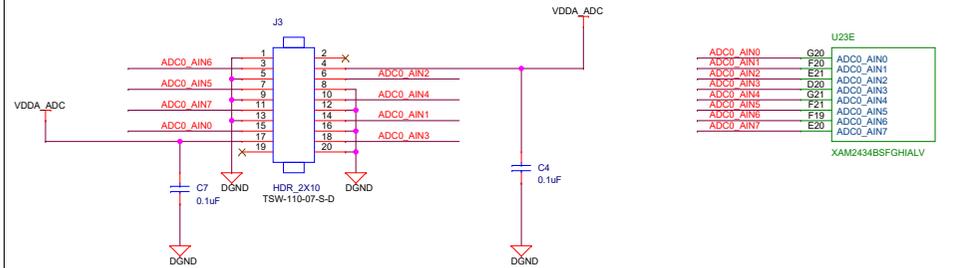
Title		PCIe INTERFACE	
Size	PROC101C(005)TMSD243EVM	Rev	
C		E2	
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# ETHERNET LED'S



# ADC CONNECTOR



## Off Page Connections

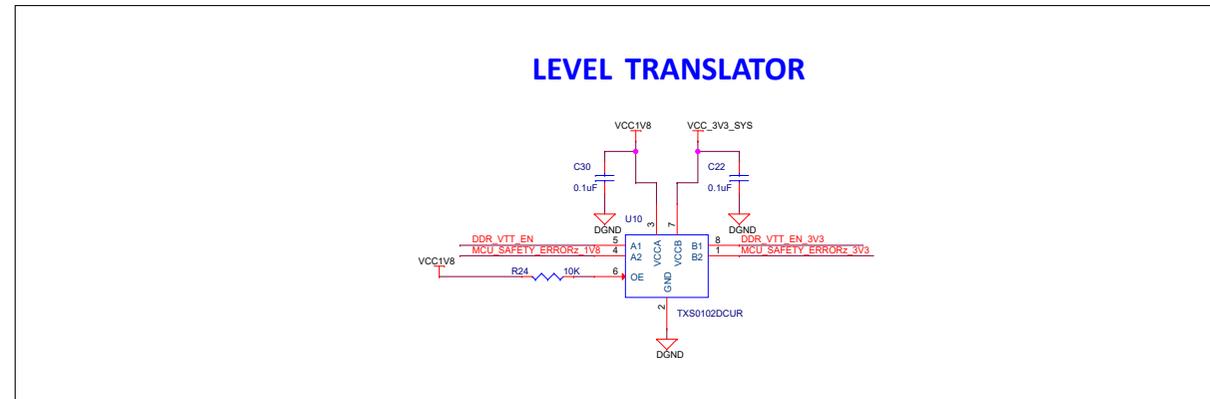
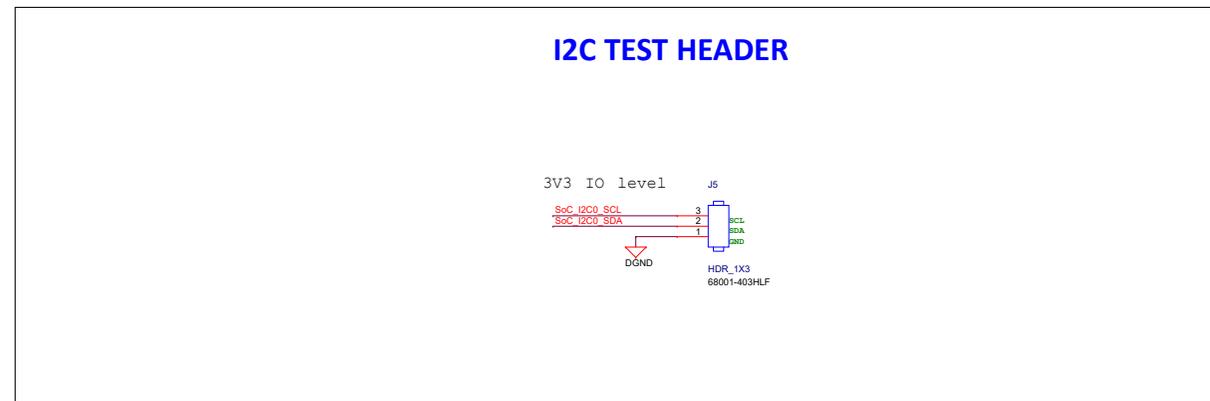
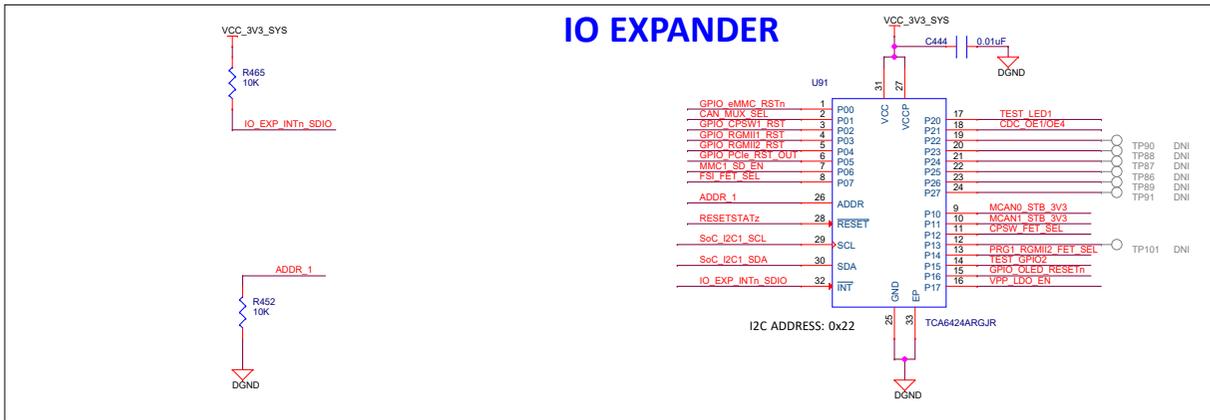


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Title ETHERNET LED's

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev	E2
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### Off Page Connections

GPIO_mMMC_RSTn	GPIO_mMMC_RSTn	13
GPIO_PClE_RST_OUT	GPIO_PClE_RST_OUT	30
GPIO_CPSW1_RST	GPIO_CPSW1_RST	16
GPIO_RGMII1_RST	GPIO_RGMII1_RST	18
GPIO_RGMII2_RST	GPIO_RGMII2_RST	17
MMC1_SD_EN	MMC1_SD_EN	13
FSI_FET_SEL	FSI_FET_SEL	28
MCAN1_STB_3V3	MCAN1_STB_3V3	29
MCAN0_STB_3V3	MCAN0_STB_3V3	29
CPSW_FET_SEL	CPSW_FET_SEL	16
PRG1_RGMII2_FET_SEL	PRG1_RGMII2_FET_SEL	17
TEST_GPIO2	TEST_GPIO2	19
GPIO_OLED_RESETrn	GPIO_OLED_RESETrn	29
VPP_LDO_EN	VPP_LDO_EN	38
CAN_MUX_SEL	CAN_MUX_SEL	29
TEST_LED1	TEST_LED1	14
CDC_OE1/OE4	CDC_OE1/OE4	31
RESESTATz_28	RESESTATz_28	13,14,20,30,31,34
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,30,31,32
SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,30,31,32
SoC_I2C0_SDA	SoC_I2C0_SDA	15,27,29
SoC_I2C0_SCL	SoC_I2C0_SCL	15,27,29

**From Safety Connector** MCU SAFETY\_ERRORz\_3V3 << MCU SAFETY\_ERRORz\_3V3 34

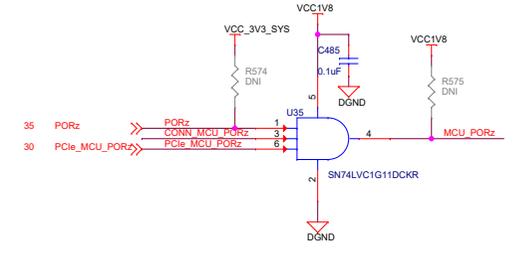
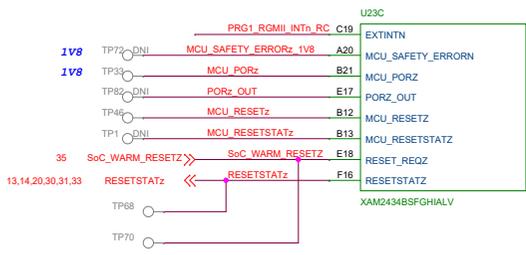
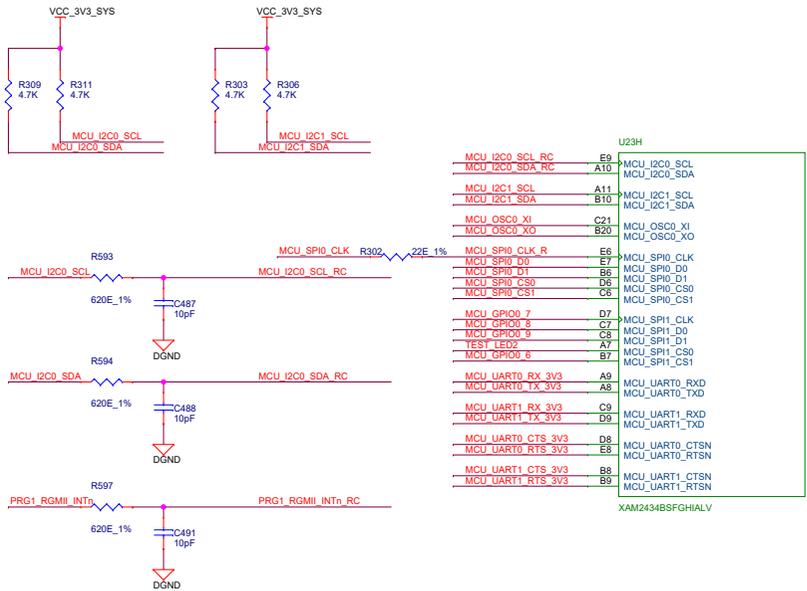
**From SoC OSPI Section** DDR\_VTT\_EN << DDR\_VTT\_EN 14

**To Processor** MCU SAFETY\_ERRORz\_1V8 >> MCU SAFETY\_ERRORz\_1V8 34

**To VTT Reg** DDR\_VTT\_EN\_3V3 >> DDR\_VTT\_EN\_3V3 30

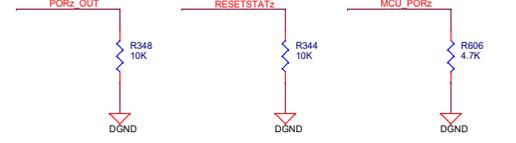
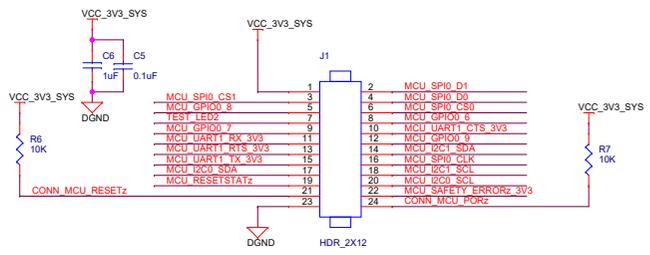
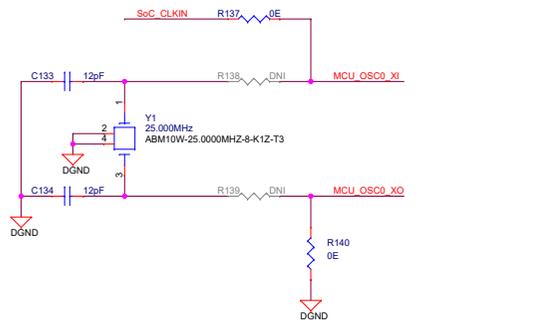
**To SoC MMC** IO\_EXP\_INTRn\_SDIO >> IO\_EXP\_INTRn\_SDIO 13

# MCU\_GENERAL



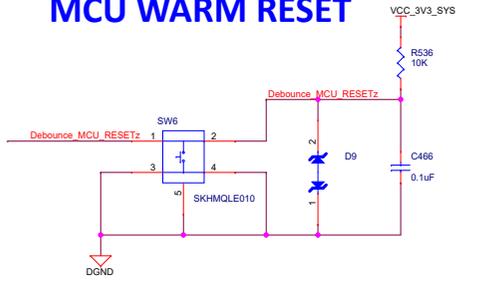
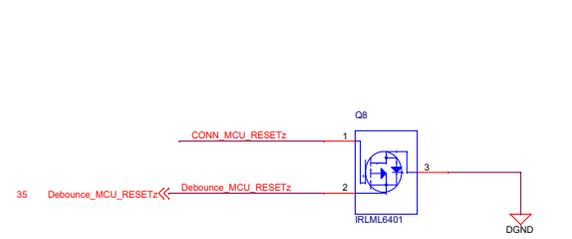
LFF Designed for 25MHz Cutoff  
Have to change resistor and capacitor values accordingly

# SAFETY CONNECTOR



pull-down resistor on PORz\_OUT is provided to keep the signal low until the processor is released from reset during the power-up sequence

# MCU WARM RESET



### Off Page Connections

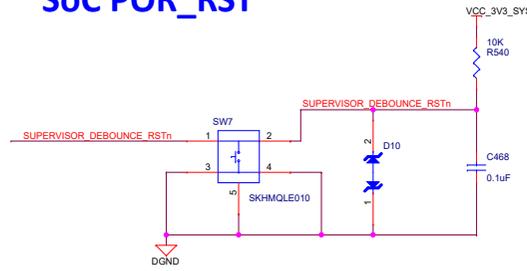
MCU_PORz	MCU_PORz	27
MCU_RESESTATz	MCU_RESESTATz	27,35
MCU_RESESTATz	MCU_RESESTATz	27
MCU_SAFETY_ERRORz_3V3	MCU_SAFETY_ERRORz_3V3	33
MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8	33
PORz_OUT	PORz_OUT	13,16,17,18,20
PRG1_RGMII_INTn	PRG1_RGMII_INTn	16,17,18
TEST_LED2	TEST_LED2	14
MCU_GPIO0_6	MCU_GPIO0_6	35
SoC_CLKIN	SoC_CLKIN	31
MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	26
MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	26
MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	26
MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	26

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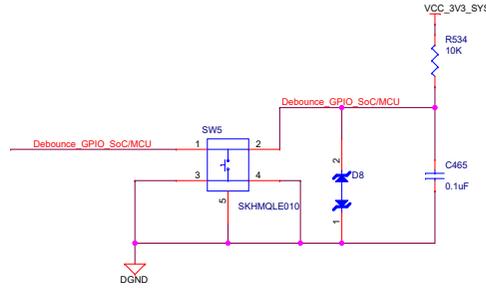
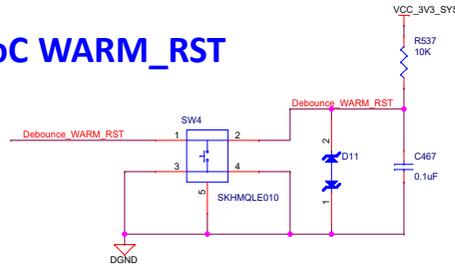


Title		MCU GENERAL & SAFETY CONNECTOR	
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev	
C		E2	
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## SoC POR\_RST

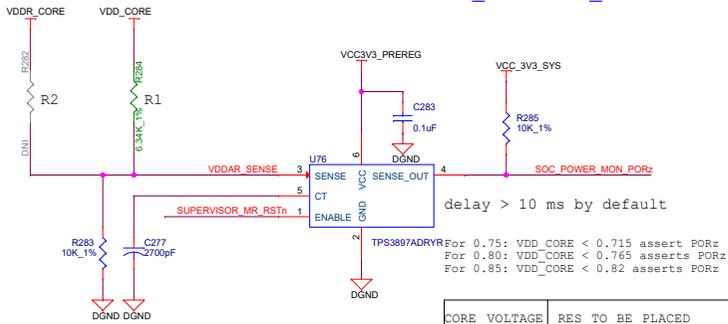


## SoC WARM\_RST



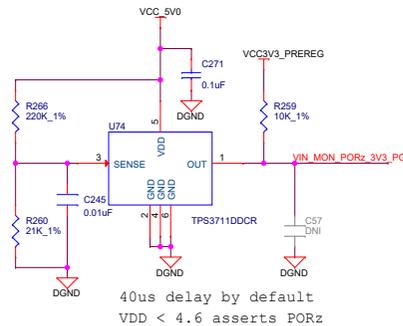
## VOLTAGE SUPERVISOR

### Core Voltage Monitor (VDDAR\_CORE/VDD\_CORE)

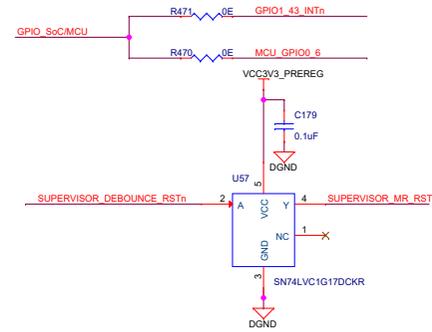
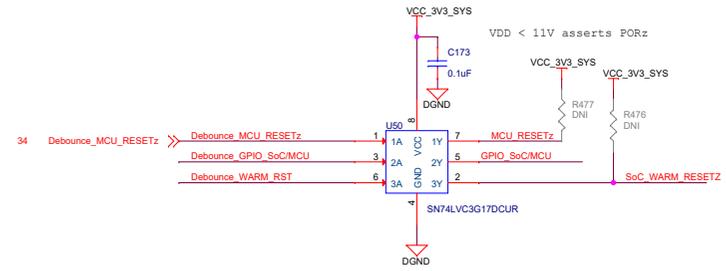


CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.80V	R2 = 5.23K
0.85V	R2 = 6.34K

### 5V OUTPUT MONITOR (VCC\_5V0)

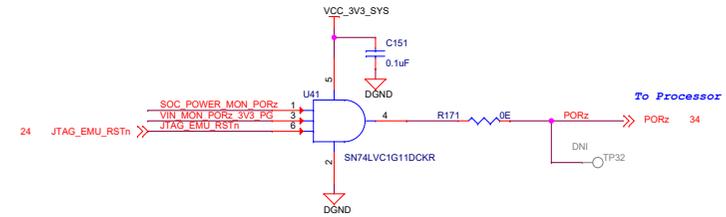


## DEBOUNCE CIRCUIT



Off Page Connections		
To Processor	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG 37,39
	SoC_WARM_RESETz	SoC_WARM_RESETz 34
	GPIO1_43_INTn	GPIO1_43_INTn 29
	MCU_RESETz	MCU_RESETz 27,34
	MCU_GPIO0_6	MCU_GPIO0_6 34

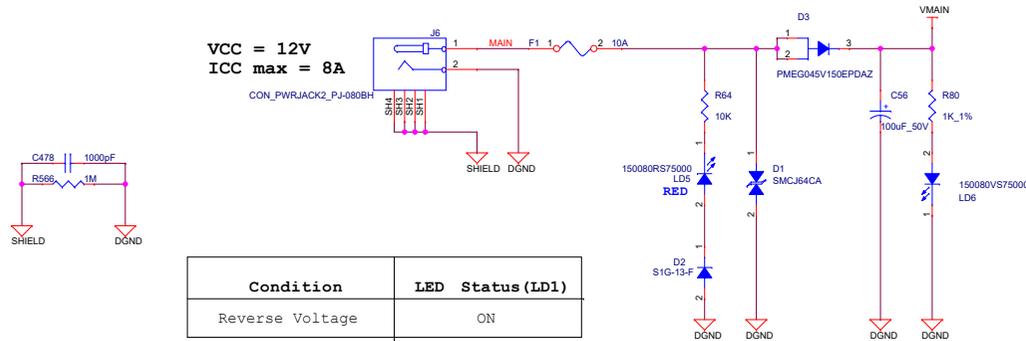
### JTAG EMU\_RSTn



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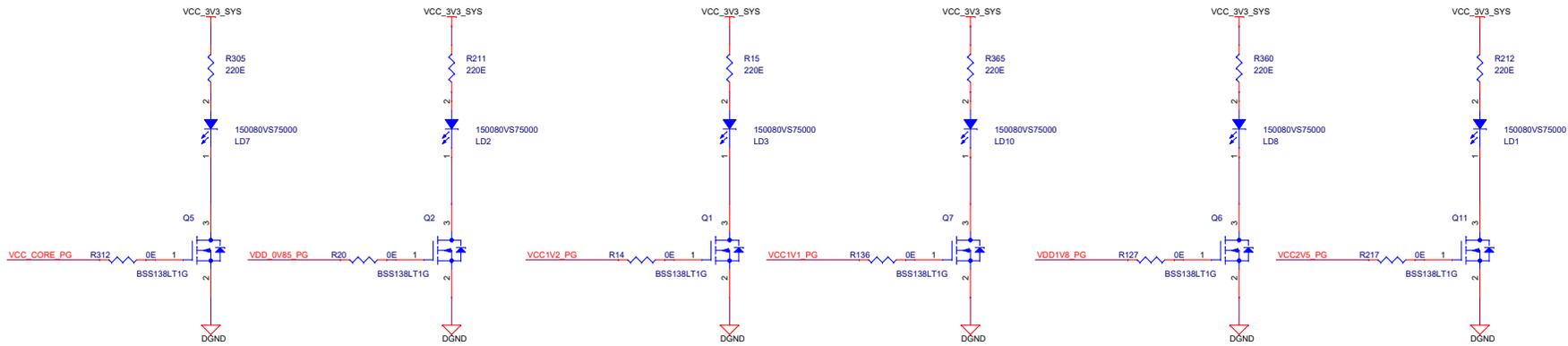
Title		DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR	
Size	Variant Name = PROC101C(005) TMS243EVM	Rev	
C		E2	
Date:	Thursday, August 18, 2022	Sheet	35 of 40

# MAIN INPUT 12V DC

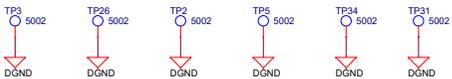


Condition	LED Status (LD1)
Reverse Voltage	ON

# POWER INDICATION LED'S



## Ground test points



## Off Page Connections

VCC_CORE_PG	VCC_CORE_PG	37,38
VDD_0V85_PG	VDD_0V85_PG	38
VCC1V2_PG	VCC1V2_PG	38
VCC1V1_PG	VCC1V1_PG	39
VDD1V8_PG	VDD1V8_PG	38
VCC2V5_PG	VCC2V5_PG	39

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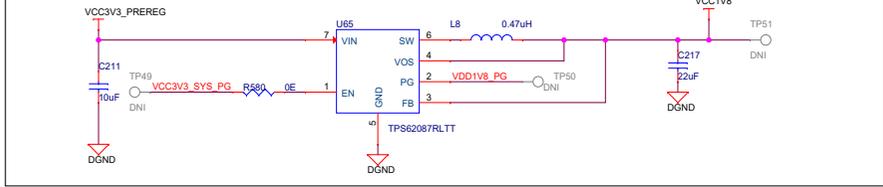
Title MAIN 12V POWERSUPPLY

Size	Variant Name = PROC101C(005) TMDS243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 36 of 40

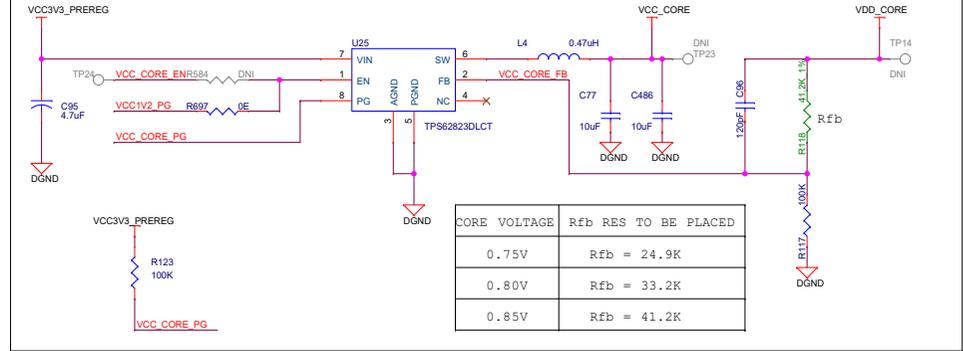


# SoC POWER SUPPLY

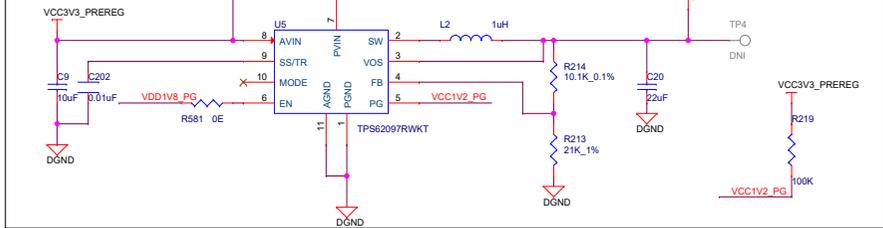
### 1.8V IO, 3.0AMPS SUPPLY



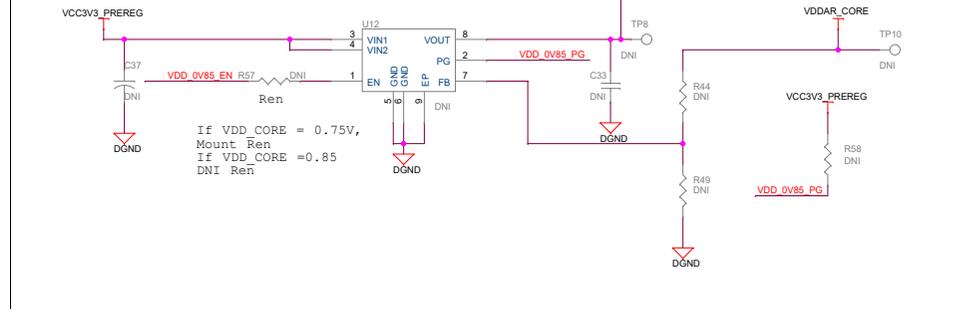
### 0.75 / 0.8 / 0.85V, 3.0AMPS SUPPLY



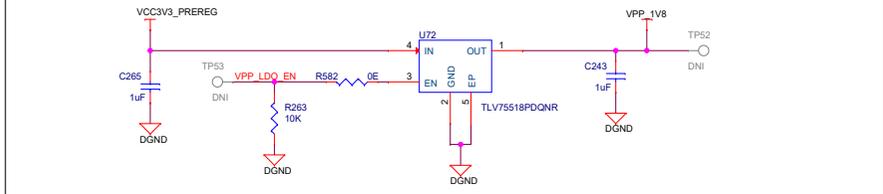
### 1.2V, 2.0AMPS SUPPLY



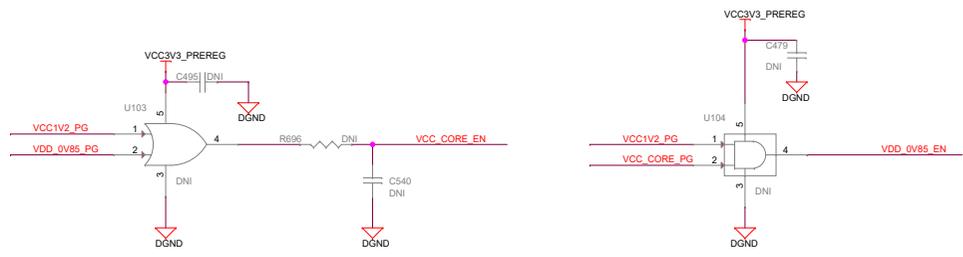
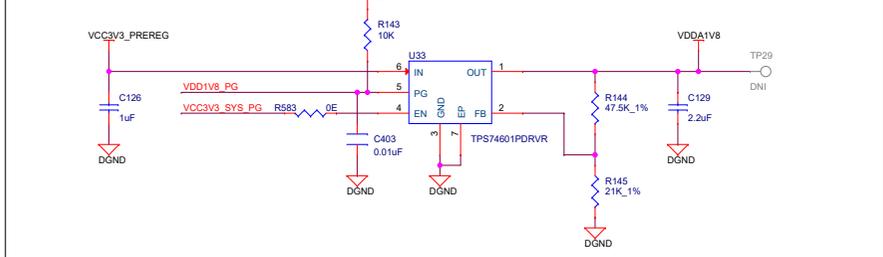
### 0.85 V, 1.5AMPS SUPPLY



### 1.8V VPP, 0.15AMPS SUPPLY



### 1.8V Analog , 1AMPS SUPPLY



#### Off Page Connections

- 36.37 VCC\_CORE\_PG
- 36 VDD\_0V85\_PG
- 36 VCC1V2\_PG
- 36 VDD1V8\_PG
- 33 VPP\_LDO\_EN
- 35,37,39 VIN\_MON\_PORz\_3V3\_PG
- 37,39 VCC3V3\_SYS\_PG
- VCC\_CORE\_PG
- VDD\_0V85\_PG
- VCC1V2\_PG
- VDD1V8\_PG
- VPP\_LDO\_EN
- VIN\_MON\_PORz\_3V3\_PG
- VCC3V3\_SYS\_PG

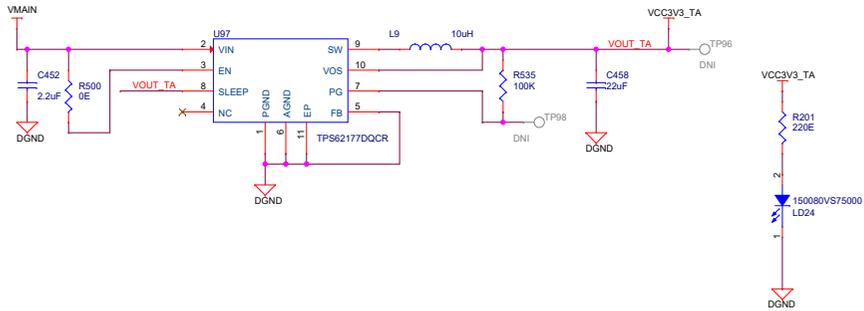
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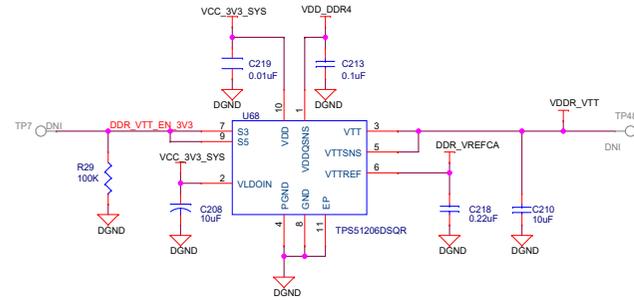
Title		SoC POWER SUPPLY	
Size	Variant Name = PROC101C(005) TMS243EVM	Rev	E2
Date:	Thursday, August 18, 2022	Sheet	38 of 40

# PERIPHERAL POWER SUPPLY

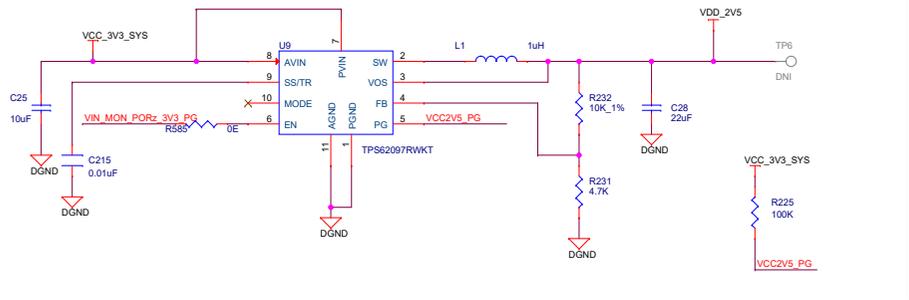
## TEST AUTOMATION BOARD POWER



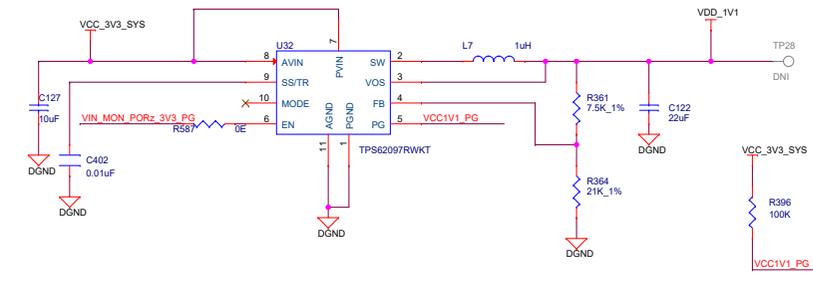
## VTT SUPPLY FOR DDR4



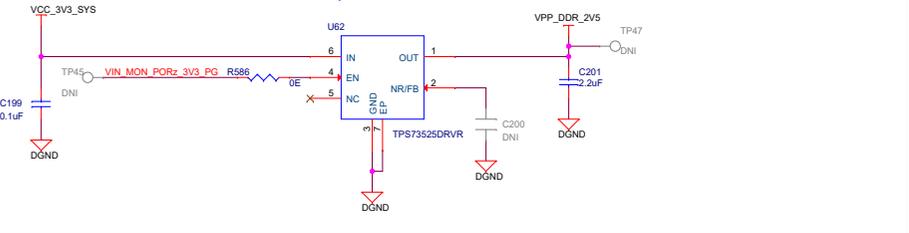
## 2.5V, 2.0AMPS SUPPLY



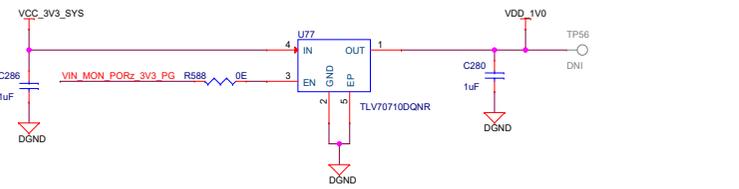
## 1.1V ETHERNET PHY POWER SUPPLY



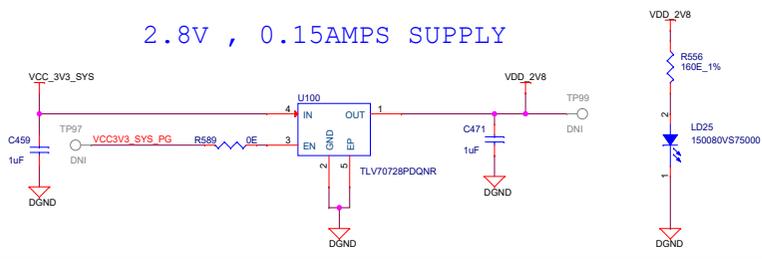
## 2.5V, .5 AMPS SUPPLY



## 1.0V ETHERNET PHY POWER SUPPLY



## 2.8V , 0.15AMPS SUPPLY



### Off Page Connections

33	DDR_VTT_EN_3V3	DDR_VTT_EN_3V3
36	VCC2V5_PG	VCC2V5_PG
38	VCC1V1_PG	VCC1V1_PG
37,38	VCC3V3_SYS_PG	VCC3V3_SYS_PG
35,37	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG

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Title PERIPHERAL POWER SUPPLY

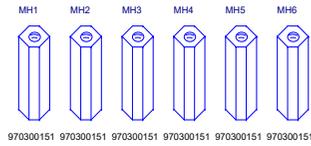
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev	E2
C		Date:	Thursday, August 18, 2022
		Sheet	39 of 40

# HARDWARE SCHEMATICS

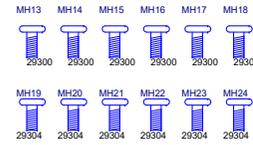
## ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

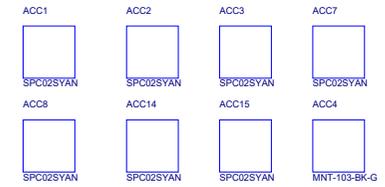
## STANDOFFS



## SCREWS



## JUMPERS



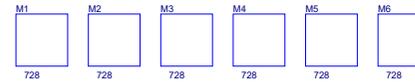
## WASHER'S



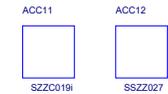
## FIDUCIALS



## RUBBER FEET



## TI EVM FLYERS



## Socket & Processor as Accessories



## BARE PCB



## LABELS

### Board Serial No.



### Assembly Revision



## ORDERABLE PART NO



### Orderable part number

Variant	Label Text
001	TMDS64GPEVM
002	TMDS243GPEVM
003	TMDS64HSEVM
004	TMDS64EVM
005	TMDS243EVM

## LOGOS



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Title: HARDWARE SCHEMATICS

Size	Variant Name = PROC101C(005) TMDS243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 40 of 40