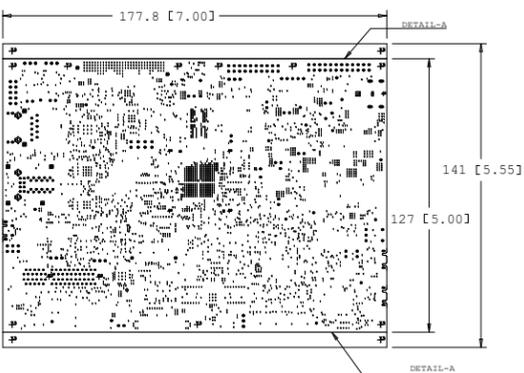


REVISIONS		
REV #	DESCRIPTION	DATE

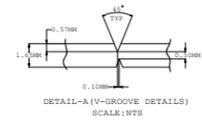
FABRICATION NOTES:

- FABRICATE PCB IN ACCORDANCE WITH IPC-6012B, CLASS 2; PER IPC-6011. PCB SHALL BE MANUFACTURED USING ITQI IF 180A OR EQUIVALENT (REF TO 17).
- MATERIALS:
 - LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/126.
- COVER FOIL TO BE IN ACCORDANCE WITH IPC-6010, UNLESS OTHERWISE SPECIFIED. ALL COVER WEIGHT FOR INNER SIGNAL LAYERS AND INNER PLANE LAYERS TO BE 35GM (1 OZ.). FOR OUTER LAYERS 35GM (1 OZ.), COPPER WEIGHT IS TO BE CONSIDERED "FINISHED". THE COPPER FOIL THICKNESS TOLERANCE SHALL BE AS PER IPC 6010 TABLE NO.3-7 AND 3-8.
- ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.15MM.
- ROW AND TRIST SHALL NOT EXCEED MORE THAN 0.75X OF THE DESIGN LENGTH.
- CONDUCTOR WIDTH SHALL NOT BE LESS THAN 25% FROM ITS ORIGINAL DATA. INCREASE FOR MATCHING IMPEDANCE MUST BE APPROVED BY THE CUSTOMER. TRACK WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
- BOARD FINISHED SHALL BE ACCORDING TO IPC-6012B CLASS 2.
- AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
- FINISH:
 - ALL EXPOSED CONDUCTIVE PATTERNS AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG. ELECTROLESS NICKEL/IMMERSION GOLD. ELECTROLESS NICKEL SHALL BE 1-4 MICRONS. TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
 - APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-6014, CLASS B, TO BOTH SIDES OF THE BOARD OVER BASE COVER. VIA HOLES SHALL BE RESIN FILLED AND COVERED WITH SOLDER MASK. ONLY SOLDER MASK IMAGES THAT ARE 0.08(10.0000) PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOR OF SOLDER MASK SHALL BE GREEN.
 - SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
 - SOLDER AND VIA HOLES FINISH SHALL NOT BE LESS THAN 200M (0.00079"), INCREASE OF LASER VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 120M (0.00047") AND BORED VIA'S SHALL NOT BE LESS THAN 150M (0.0006").
 - ALL HOLES SURROUNDED BY LAND $+0.010$ SHALL BE COMPLIANCE TO IPC6011, CLASS 2.
- MARKING:
 - BOARD SHALL MEET THE REQUIREMENTS OF UL-756 WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LAYER SHALL BE RENDERED IN SILKSCREEN.
- TEST REQUIREMENTS:
 - 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
 - TESTING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
 - TEAR DROPS SHALL BE ADDED ON VIA'S AND THROUGH HOLES PADS IN ALL INTERNAL AND OUTER LAYERS.
 - ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IF REQUIRED.
 - FINISHED PCB THICKNESS SHALL BE 0.565" (+/-0.010).
 - MIN TRACE WIDTH/SPACING ON BOARD IS 0.0032"/0.0037".
 - MINIMUM UL REGISTERED E-FILE NUMBER SHALL BE PRINTED ON THE PCB SILKSCREEN.
 - VIA ON PAD SHALL BE RESIN FILLED AND CAP-PLATED.
 - FOR STACKUP DETAIL FROCI010_STACKUP.PDF SHALL BE REFERRED.



DRILL CHART: TOP & BOTTOM
ALL UNITS ARE IN MILS

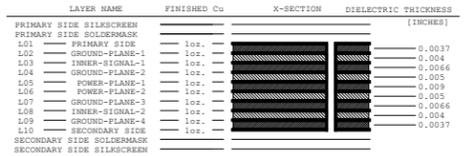
FIGURE	SIZE	TOLERANCE	PLATED	QTY
1	8.0	+0.0/-0.0	PLATED	1120
2	28.0	+0.0/-0.0	PLATED	84
3	36.0	+0.0/-0.0	PLATED	38
4	40.0	+0.0/-0.0	PLATED	33
5	40.0	+0.0/-0.0	PLATED	101
6	44.0	+0.0/-0.0	PLATED	18
7	56.0	+0.0/-0.0	PLATED	6
8	78.0	+0.0/-0.0	PLATED	1
9	34.0	+1.0/-1.0	NON-PLATED	2
10	40.0	+1.0/-1.0	NON-PLATED	2
11	55.0	+1.0/-1.0	NON-PLATED	2
12	64.0	+1.0/-1.0	NON-PLATED	1
13	65.0	+1.0/-1.0	NON-PLATED	4
14	92.0	+1.0/-1.0	NON-PLATED	2
15	108.0	+1.0/-1.0	NON-PLATED	13
16	124.0	+1.0/-1.0	NON-PLATED	4
17	52.0x24.0	+0.0/-0.0	PLATED	4
18	52.0x16.0	+0.0/-0.0	PLATED	2
19	44.0x32.0	+0.0/-0.0	PLATED	2
20	80.0x40.0	+0.0/-0.0	PLATED	4
21	82.0x34.0	+0.0/-0.0	PLATED	1



IMPEDANCE SPECIFICATIONS

ID#	TYPE	LAYER	TRACEDWIDTH (MILs)	SPACING (MILs)	IMPEDANCE (Ohms)	REF LAYER
01	EDGE COUPLED STRIPLINE	IN_18	3.2	7.5	100	2/21.4, 1/71.0
02	EDGE COUPLED MICROSTRIP	IN_18	3.2	7.5	100	2/21.4, 1/71.0
03	EDGE COUPLED STRIPLINE	IN_18	4.2	8	80	2/21.4, 1/71.0
04	EDGE COUPLED MICROSTRIP	IN_18	4.2	8	80	2/21.4, 1/71.0
05	EDGE COUPLED STRIPLINE	IN_18	5.2	8.5	80	2/21.4, 1/71.0
06	EDGE COUPLED MICROSTRIP	IN_18	5.2	8.5	80	2/21.4, 1/71.0
07	EDGE COUPLED STRIPLINE	IN_18	6.02	9.5	80	2/21.4, 1/71.0
08	EDGE COUPLED MICROSTRIP	IN_18	6.02	9.5	80	2/21.4, 1/71.0
09	STRIPLINE	IN_18	5.8	NA	40	2/21.4, 1/71.0
10	MICROSTRIP	IN_18	5.05	NA	80	2/21.4, 1/71.0
11	STRIPLINE	IN_18	3.6	NA	50	2/21.4, 1/71.0
12	MICROSTRIP	IN_18	3.2	NA	50	2/21.4, 1/71.0

LAYER STACKUP



SIGNATURES	DATE	 TEXAS INSTRUMENTS FROCI010C	AM64x EVM BOARD SCALE: NONE SHEET 1 OF 17
LAYOUT BY UD	120422		
REVIEWED BY SA	120422		
APPROVED BY AMB	120422		