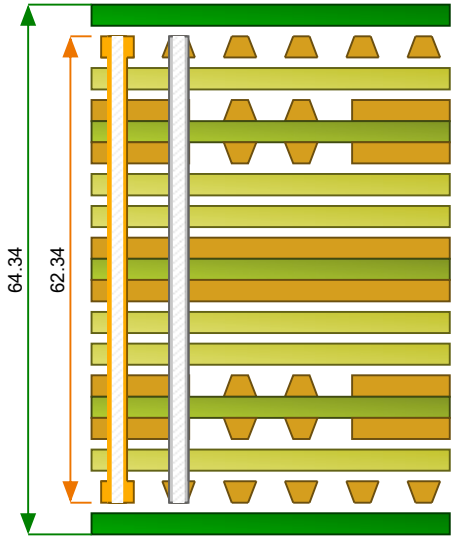
Layer	Stack up	Description	Type	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	SolderMask	1.000			3.500	
1		Copper Foil 12 microns	Copper	1.850		100.000		1, 2, 3, 4, 5
		Iteq IT180A Prepreg 2113 RC58-NEW	Dielectric	3.387	3.387		4.130	
2				1.260		60.000		
		Iteq IT180A 4 mil core 1/1	FR4	4.000	4.000		4.400	
3				1.260		30.000		6, 7, 8, 9, 10
		Iteq IT180A Prepreg 7628 RC43-NEW	Dielectric	6.577	13.154		4.450	
		Iteq IT180A Prepreg 7628 RC43-NEW	Dielectric	6.577	-		4.450	
4				1.260		60.000		
		Iteq IT180A 10 mil core 1/1	FR4	10.000	10.000		4.180	
5				1.260		60.000		
		Iteq IT180A Prepreg 7628 RC43-NEW	Dielectric	6.577	13.154		4.450	
		Iteq IT180A Prepreg 7628 RC43-NEW	Dielectric	6.577	-		4.450	
6				1.260		30.000		11, 12, 13, 14, 15
		Iteq IT180A 4 mil core 1/1	FR4	4.000	4.000		4.400	
7				1.260		60.000		
		Iteq IT180A Prepreg 2113 RC58-NEW	Dielectric	3.387	3.387		4.130	
8		Copper Foil 12 microns	Copper	1.850		100.000		16, 17, 18, 19, 20
		Taiyo PSR 4000 HFX DI-GREEN	SolderMask	1.000			3.500	

Copper Thickness = 11.260 | Dielectric Thickness = 51.082 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 62.341 | Stack Up Thickness with Soldermask = 64.341

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	1	Coated Microstrip 1B	2	0	8.000	0.000	0.000	40.160	40.000	10.000
2	1	Coated Microstrip 1B	2	0	5.200	0.000	0.000	50.070	50.000	10.000
3	1	Edge Coupled Coated Microstrip 1B	2	0	5.300	4.350	0.000	80.030	80.000	10.000
4	1	Edge Coupled Coated Microstrip 1B	2	0	4.350	5.150	0.000	89.890	90.000	10.000
5	1	Edge Coupled Coated Microstrip 1B	2	0	4.150	8.350	0.000	99.830	100.000	10.000
6	3	Offset Stripline 1B1A	2	4	6.800	0.000	0.000	39.980	40.000	10.000

StackName: Master						
Version:	Associated Documents:	Revision:	Modification:	Date of Revision:	Editor	Pag
Date: 14-02-2022						
Author: -						
Department: Engg-CAM						
Site: www.hiqelectronics.com						

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Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
7	3	Offset Stripline 1B1A	2	4	4.200	0.000	0.000	50.000	50.000	10.000
8	3	Edge Coupled Offset Stripline 1B1A	2	4	4.500	4.500	0.000	79.900	80.000	10.000
9	3	Edge Coupled Offset Stripline 1B1A	2	4	3.800	5.900	0.000	90.130	90.000	10.000
10	3	Edge Coupled Offset Stripline 1B1A	2	4	3.200	7.500	0.000	100.220	100.000	10.000
11	6	Offset Stripline 1B1A	5	7	6.800	0.000	0.000	39.980	40.000	10.000
12	6	Offset Stripline 1B1A	5	7	4.200	0.000	0.000	50.000	50.000	10.000
13	6	Edge Coupled Offset Stripline 1B1A	5	7	4.500	4.500	0.000	79.900	80.000	10.000
14	6	Edge Coupled Offset Stripline 1B1A	5	7	3.800	5.900	0.000	90.130	90.000	10.000
15	6	Edge Coupled Offset Stripline 1B1A	5	7	3.200	7.500	0.000	100.220	100.000	10.000
16	8	Coated Microstrip 1B	7	0	8.000	0.000	0.000	40.160	40.000	10.000
17	8	Coated Microstrip 1B	7	0	5.200	0.000	0.000	50.070	50.000	10.000
18	8	Edge Coupled Coated Microstrip 1B	7	0	5.300	4.350	0.000	80.030	80.000	10.000
19	8	Edge Coupled Coated Microstrip 1B	7	0	4.350	5.150	0.000	89.890	90.000	10.000
20	8	Edge Coupled Coated Microstrip 1B	7	0	4.150	8.350	0.000	99.830	100.000	10.000

Notes

StackName:							
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