

# AM62P STARTER KIT EVM

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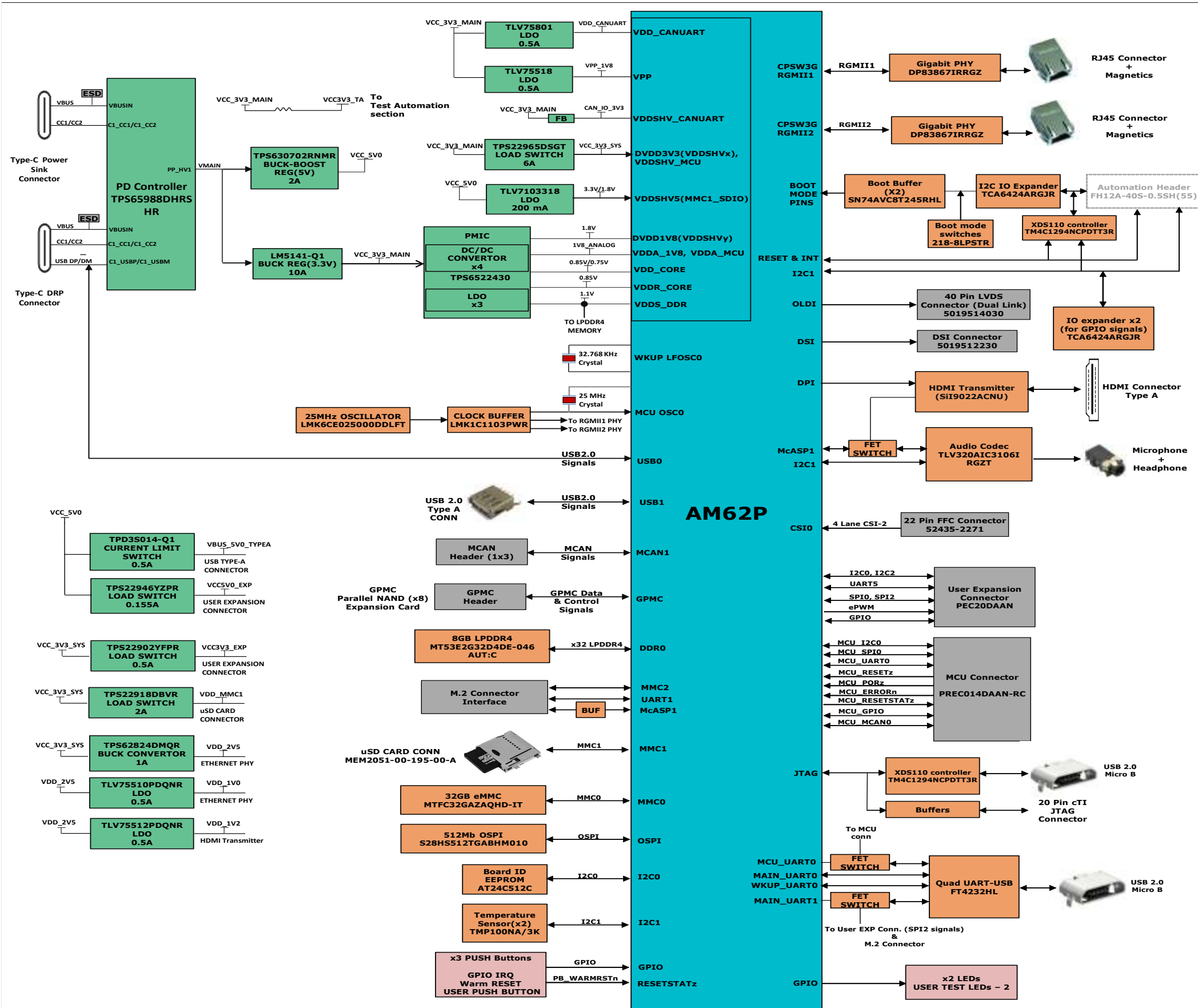
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REV	E1
VER	1.0

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	20 FEB 2023	Initial Draft derived from AM62A SK - PROC135E3 schematics	Mistral Design Team		
0.02	23 FEB 2023	Updated power section & PMIC part as per PDN	Mistral Design Team		
0.03	24 FEB 2023	1. Added pullups on XDS110 side for Test Automation signals 2. Added 5V0 sourcing caps to meet USB Specifications	Mistral Design Team	Nishant	
0.04	27 FEB 2023	Replaced parts : LPDDR4 (8 GB), eMMC (32 GB with HS400 support), OSPI (512 Mb NOR Flash)	Mistral Design Team		
0.05	28 FEB 2023	AM62P SoC part updated as per "AM62P_BGAmapping_20230213"	Mistral Design Team	Nishant	
0.06	01 MAR 2023	Added DSI, OLDI, GPMC (x8) connectors & updated respective net connections	Mistral Design Team	Nishant	
0.07	03 MAR 2023	Updated PMIC local caps, GPIO connections & assembly variants	Mistral Design Team		
0.08	08 MAR 2023	1. Updated INA section to include INA228 as default with footprint support for INA231 2. INA Kelvin sense resisitors moved to PMIC sheet as per modular design requirement	Mistral Design Team	Nishant	
0.09	10 MAR 2023	Updated internal review comments & shared to TI for review	Mistral Design Team	Nishant	Ajit
0.10	15 MAR 2023	1. Updated TI review comments 2. Updated PMIC connections as per PDN v1.5	Mistral Design Team	Nishant	
0.11	16 MAR 2023	Added separate dual LDO for VDDSHV_SDIO, 5V0 headers for OLDI & DSI daughter cards	Mistral Design Team		
0.12	20 MAR 2023	1. Updated PMIC Enable & GPIO connections 2. Modified RC shield connections for RGMII1, RGMII2 & USB Type A connectors	Mistral Design Team		
0.13	22 MAR 2023	1. Updated TI review comments on PD Controller 2. Replaced HDMI EXT_SWING resistor with 7.5K_5% ohms	Mistral Design Team	Nishant	
0.14	28 MAR 2023	Added extra local caps to PMIC Switching outputs as recommended in datasheet	Mistral Design Team		
0.15	04 APR 2023	Modified SoC decaps & added RC circuit for I2C	Mistral Design Team		
0.16	07 APR 2023	1. Added series resistors for RGMII TX signals 2. Swapped DDR DQ & DMI bits	Mistral Design Team		
0.17	13 APR 2023	Implemented review comments from TI	Mistral Design Team	Nishant	Ajit
0.18	18 APR 2023	1. Updated Internal and review comments from TI 2. Replaced Oscillator with new LMK6CE series (BAW), OLDI and DSI Connector.	Mistral Design Team	Nishant	Ajit
0.19	03 MAY 2023	Modified the 3T decaps as 4 pin IC's and updated a few review comments from TI	Mistral Design Team	Nishant	
0.20	10 MAY 2023	Modified the 2T current sense resistor parts to 4T sense similar to AM62A SK	Mistral Design Team	Nishant	
0.21	16 MAY 2023	1. Replaced USB Type A load switch (with OC) & ESD protection device 2. Added capacitor to CT pin of VCC_3V3_SYS & VDD_MMC1 load switches	Mistral Design Team	Nishant	Ajit
0.22	24 MAY 2023	1. VMON connection modified for PMIC to meet threshold of 3.3V 2. Part References Back annotated from PCB file	Mistral Design Team		
0.23	16 JUNE 2023	1. Updated OPN's for SoC and PMIC 2. Removed dip switch for VDD_CORE voltage configuration. 3. Replaced HDMI connector part	Mistral Design Team	Nishant	
0.24	20 JUNE 2023	Updated review comments from TI	Mistral Design Team	Nishant	
0.25	21 JUNE 2023	1. Removed shorting jumper for VCC_CORE rail 2. Added dip switch control for EMU0 & EMU1 signals	Mistral Design Team	Nishant	
0.26	23 JUNE 2023	Modified decaps for VDD_CORE	Mistral Design Team	Nishant	
0.27	26 JUNE 2023	Replaced 3T SoC decaps with correct symbol & footprints	Mistral Design Team	Nishant	
1.0	28 JUNE 2023	Baselined	Mistral Design Team	Nishant	Ajit

## BLOCK DIAGRAM AM62P-SKEVM



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Title	BLOCK DIAGRAM AM62A_ SKEVM
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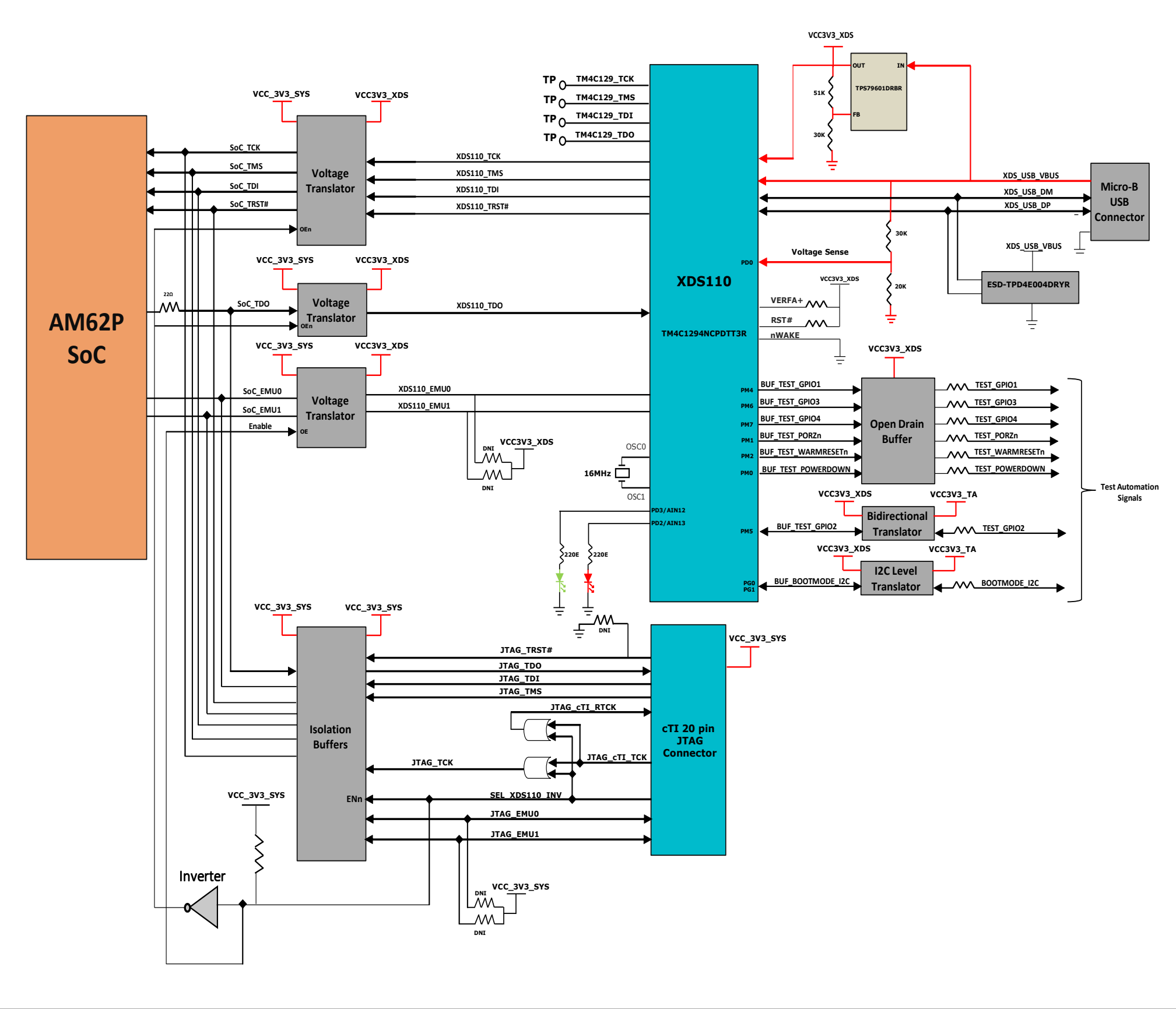
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Rev	
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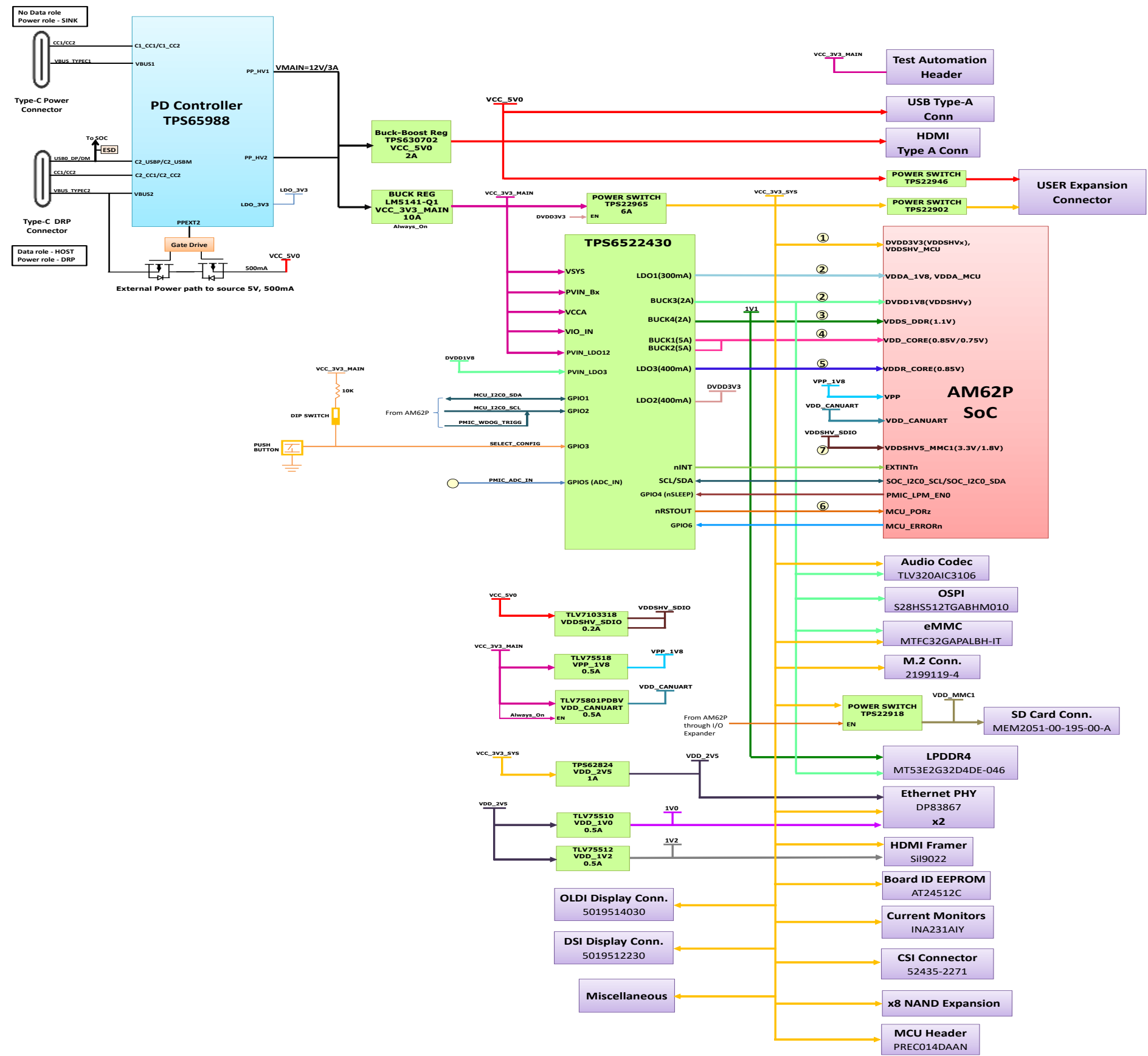
Date: Wednesday, June 28, 2023

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BLOCK DIAGRAM\_XDS110



POWER BLOCK DGM



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Title POWER BLOCK DGM

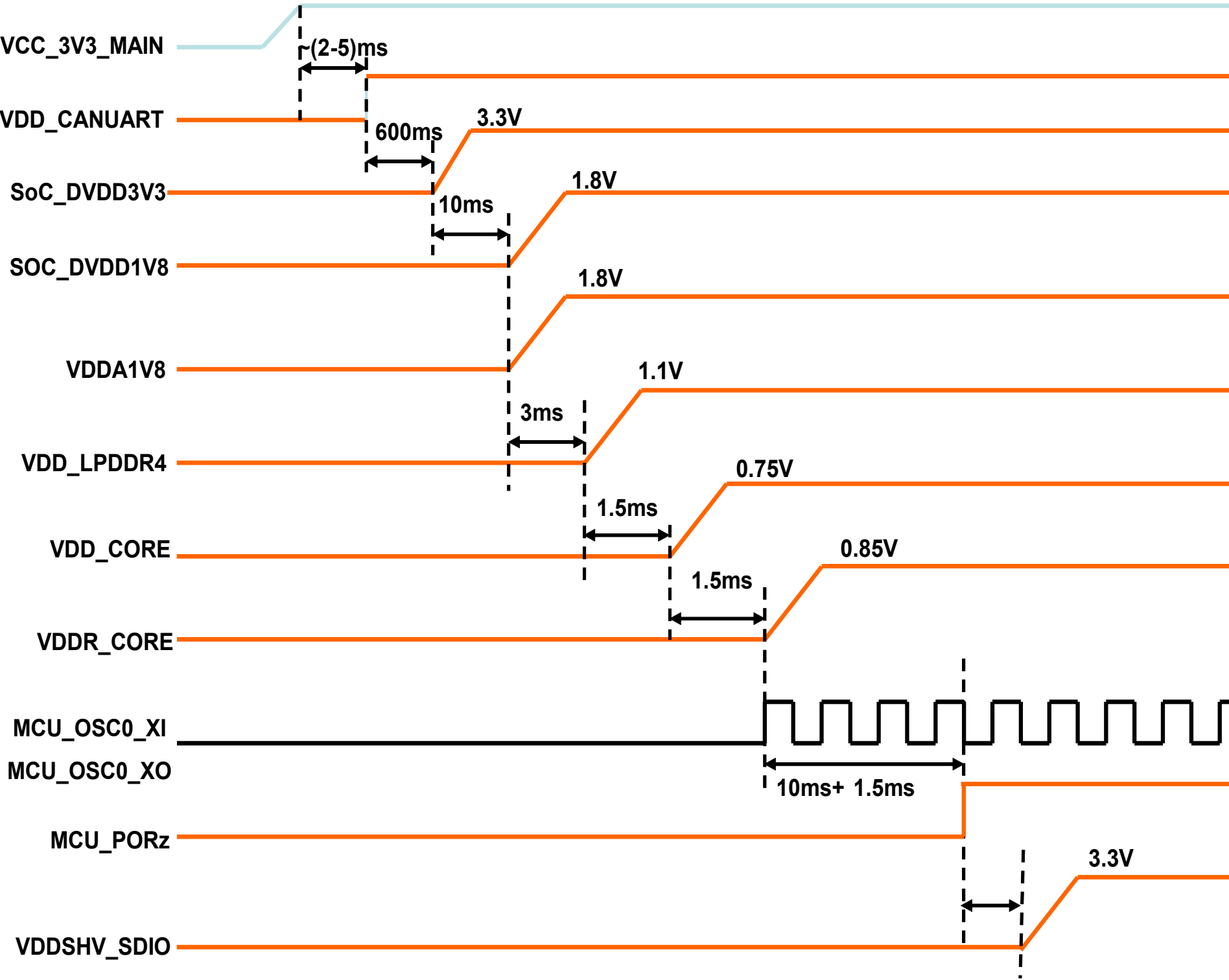
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Rev E1

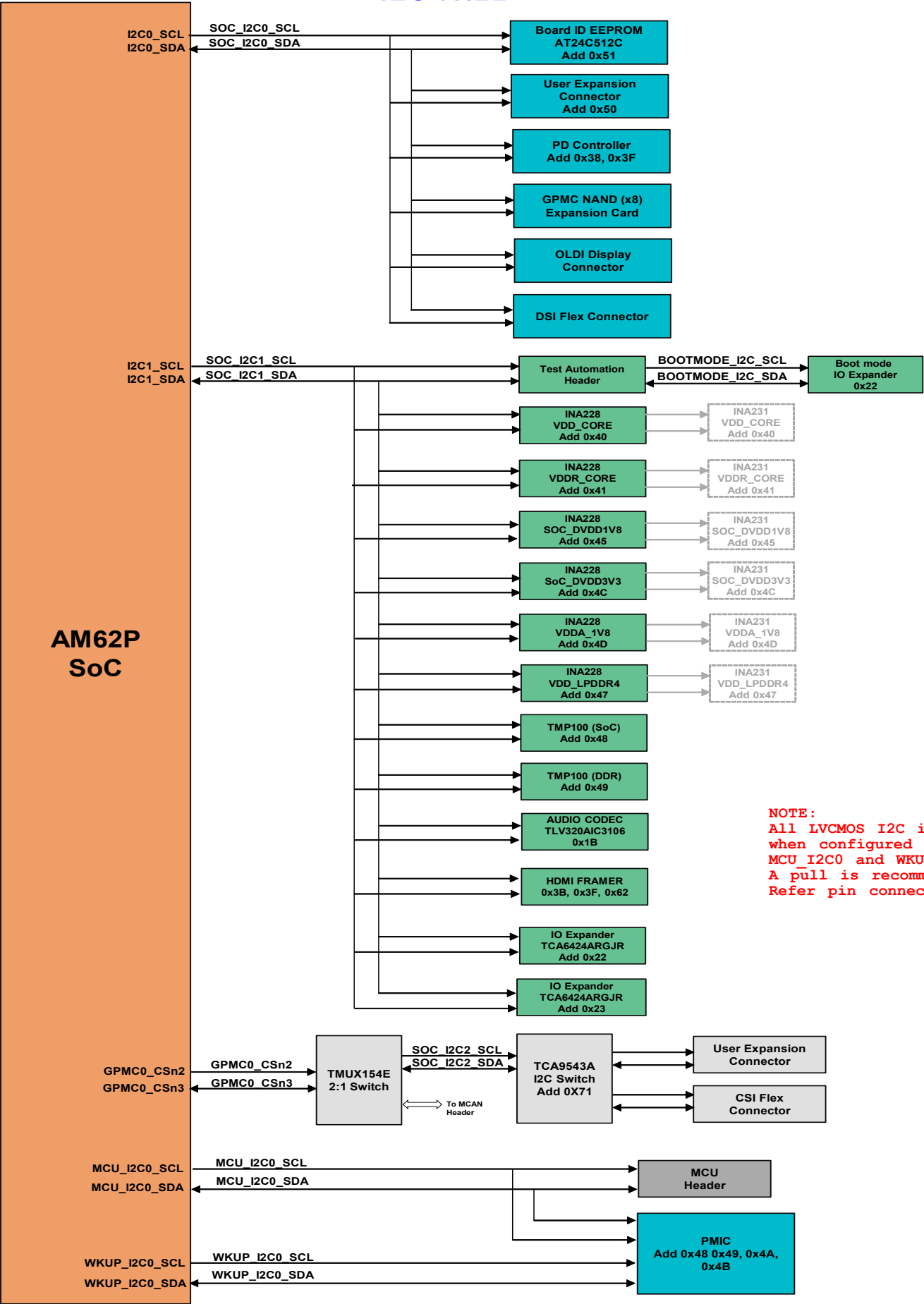
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POWER UP SEQUENCE



I2C TREE



NOTE:  
All LVCMOS I2C interfaces need a pullup  
when configured for I2C function.  
MCU\_I2C0 and WKUP\_I2C0 have open drain type buffer.  
A pull is recommended.  
Refer pin connectivity table from device datasheet

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Title I2C TREE		
Size	PROC164E1	Rev
C		E1
Date:	Monday, June 26, 2023	Sheet 7 of 47

GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	MCU Interrupt	MCU_INTn	INTERRUPT	MCU_GPIO0_0	MCU_SPI0_CS0	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
9	PMIC Interrupt	PMIC_INTn	INTERRUPT	GPIO0_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
11	CAN-FD fast wake signal from MCU header	CAN_FD_WKUP_HDR_INH								
12	User test LED control signal	SOC_GPIO1_49	ENABLE	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	User Interrupt									
15	Low power mode enable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
16	SD Card I/O Voltage Selection	VSEL_SD_SOC	SELECTION	GPIO0_31	GPMMC0_CLK	OUTPUT	NA	NA	VDDSHV2	SoC_DVDD3V3
IO EXPANDER – 01										
1	Interrupt from OLDI display	OLDI_INT#	INTERRUPT	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	x8 NAND Card Presence Detect	x8_NAND_DETECT	DETECTION	IO EXPANDER-P01		INPUT	HIGH	LOW		VCC_3V3_SYS
3	MCASP1 Enable and Direction Control	UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P02		OUTPUT	HIGH	-		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	SOC UART1 Mux Select	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	DSI Display GPIO0	DSI_GPIO0	GPIO	IO EXPANDER-P10		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
10	DSI Display GPIO1	DSI_GPIO1	GPIO	IO EXPANDER-P11		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
11	OLDI to HDMI Card Device ID interrupt	OLDI_EDID	INTERRUPT	IO EXPANDER-P12		INPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	USB Type A overcurrent indicator	USB_TYPEA_OC_INDICATION	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSIO GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSIO GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22	DSI to HDMI Card Device ID interrupt	DSI_EDID	INTERRUPT	IO EXPANDER-P25		INPUT	HIGH	LOW		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER – 02										
1	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
2	EXP CONN 5V Power Switch Enable	EXP_PS_SVO_EN	ENABLE	IO EXPANDER-P01		OUTPUT	LOW	HIGH		VCC_3V3_SYS
3	Wilink Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SoC I2C2 & MCAN MUX Selection	SoC_I2C2_MCAN_SEL	CONTROL	IO EXPANDER-P20		OUTPUT	HIGH	-		VCC_3V3_SYS
5	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P21		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P23		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	OLDI display Reset control GPIO	GPIO_OLDI_RSTn	RESET	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS

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Title GPIO MAPPING TABLE

Size

PROC164E1

Rev

E1

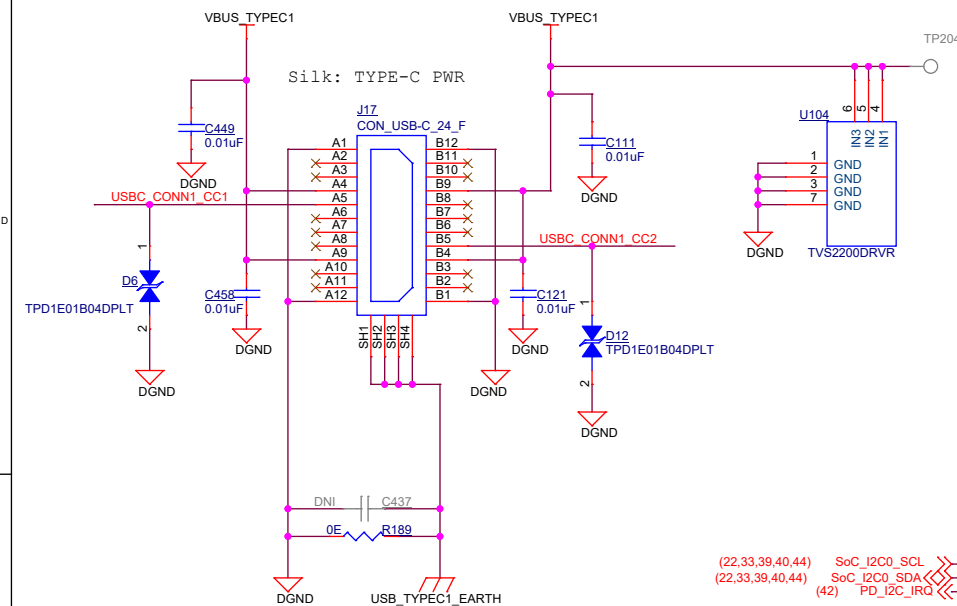
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Monday, July 03, 2023

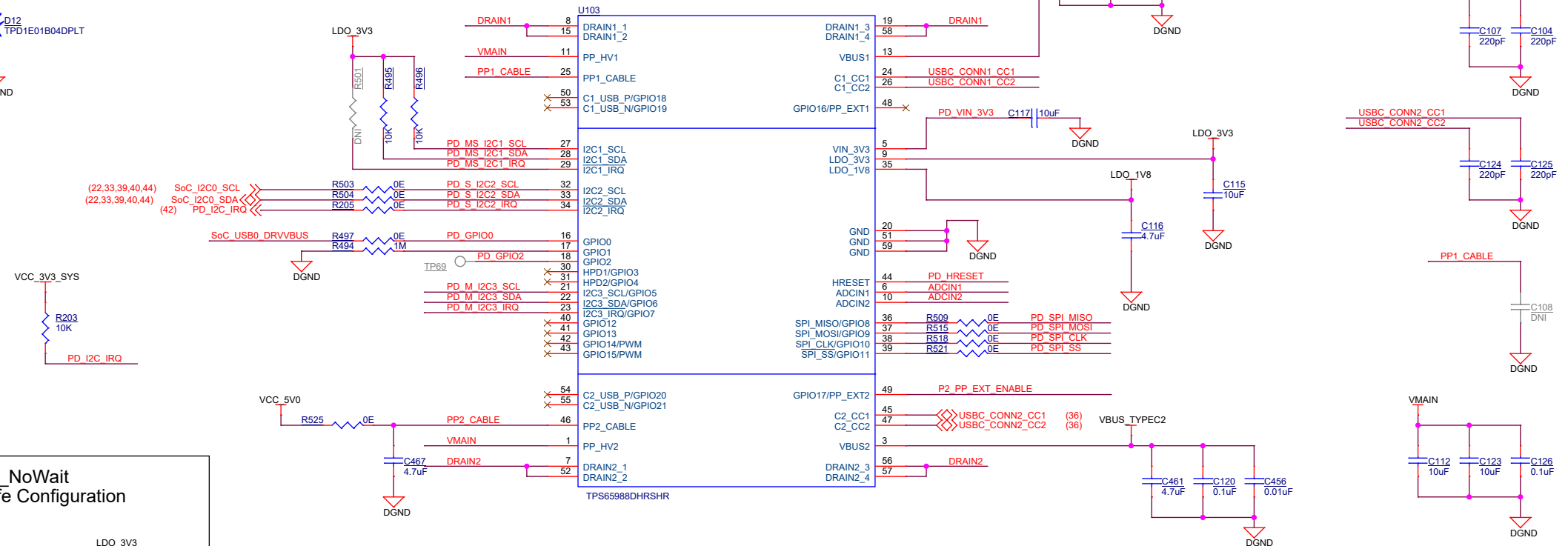
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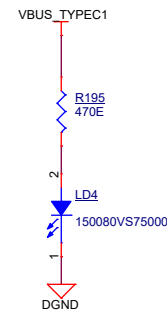
## USB TYPE-C POWER



## TYPE-C DUAL PD CONTROLLER

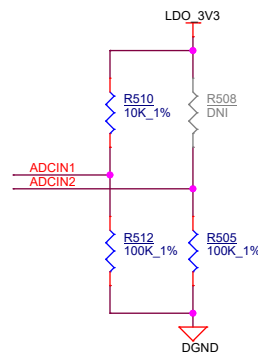


POWER INDICATION LED: VBUS\_TYPEC1

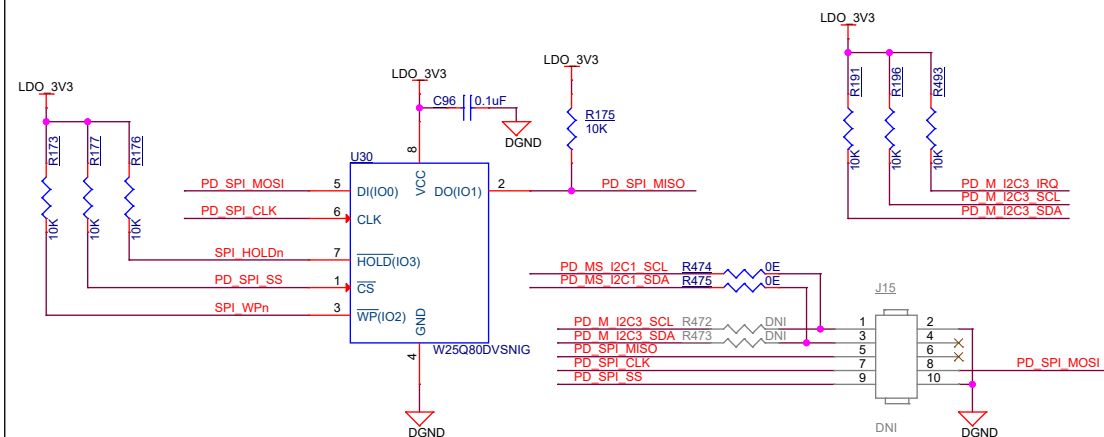


I2C Slave Address	Port1	Port2
I2C2 (Default)	0x38	0x3F
I2C1	0x20	0x24

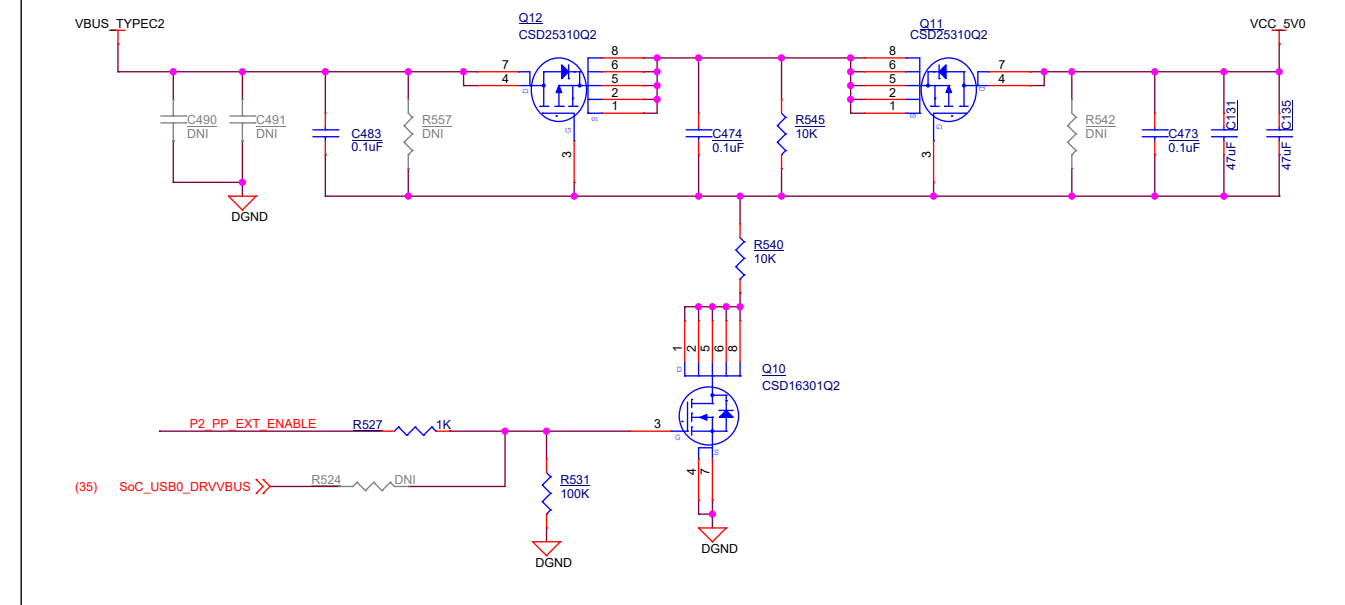
BP\_NoWait  
Safe Configuration



## SPI EEPROM & PROGRAMMING HEADER



### EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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Title	USB TYPE-C
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Size	PROC164E1
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Date: Monday, June 26, 2023

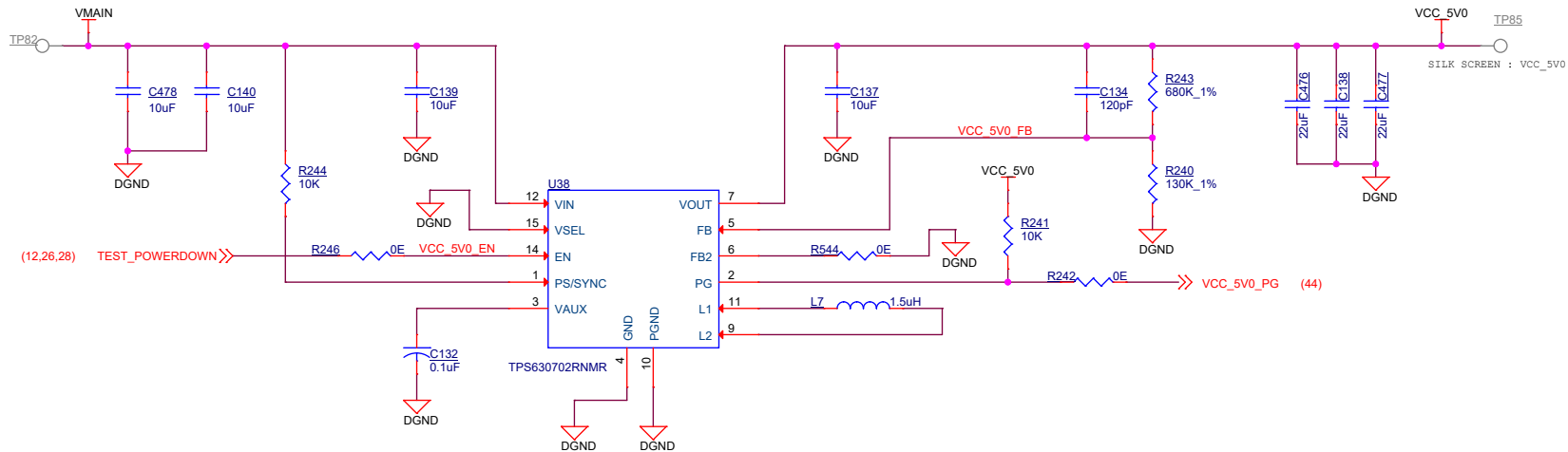
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Rev
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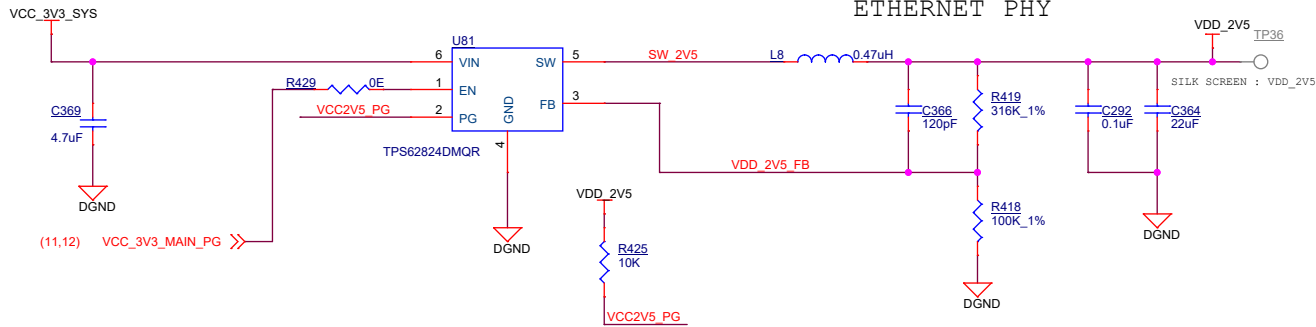
PERIPHERAL POWER SUPPLY-1

VinMin = 4.5V  
VinMax = 15V  
Vout = 5V @ 2A



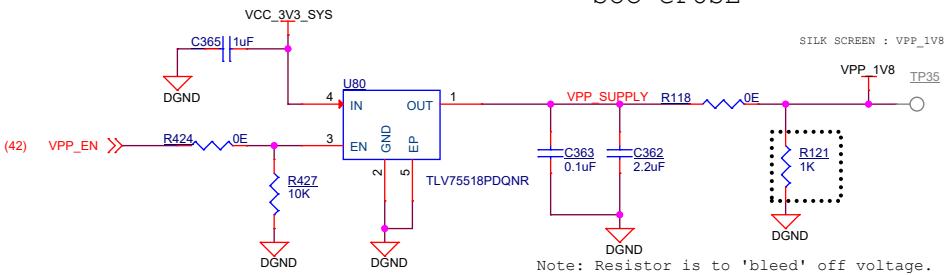
2.5V, 1.0AMPS SUPPLY

ETHERNET PHY



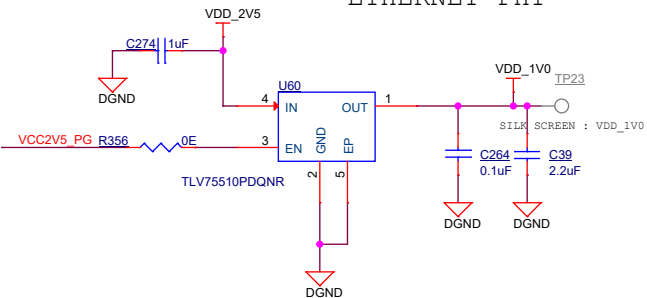
1.8V VPP, 0.5AMPS SUPPLY

SoC eFUSE

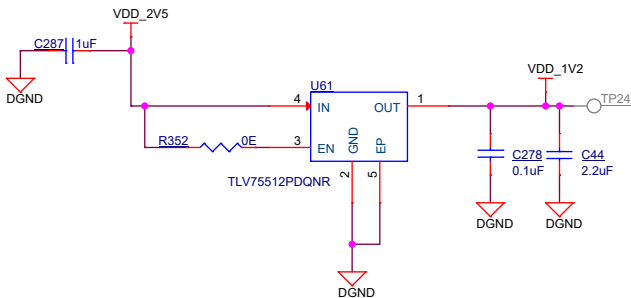


1.0V, 0.5AMPS SUPPLY

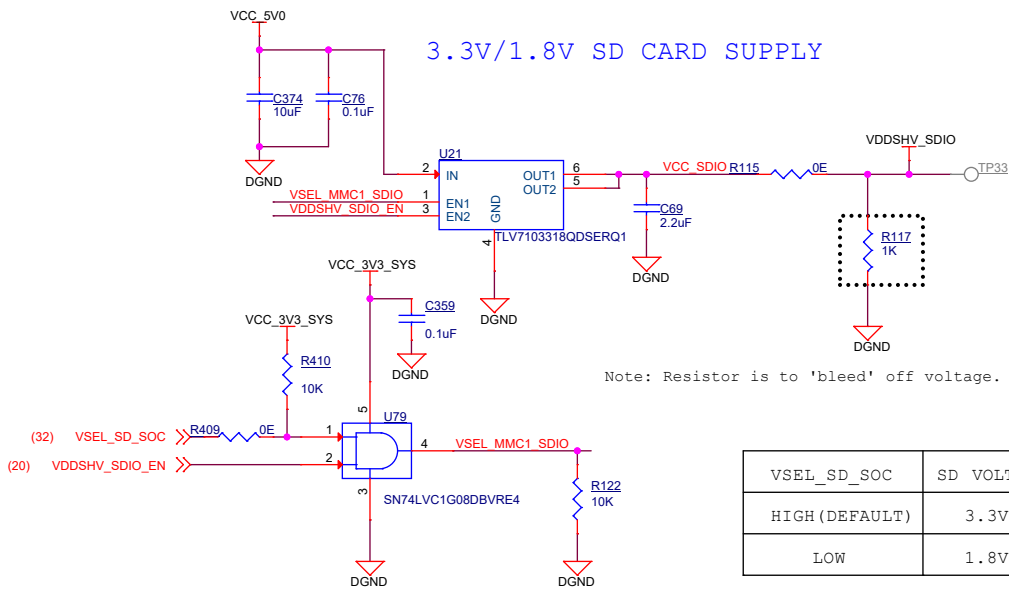
ETHERNET PHY



1.2V, 0.5AMPS SUPPLY



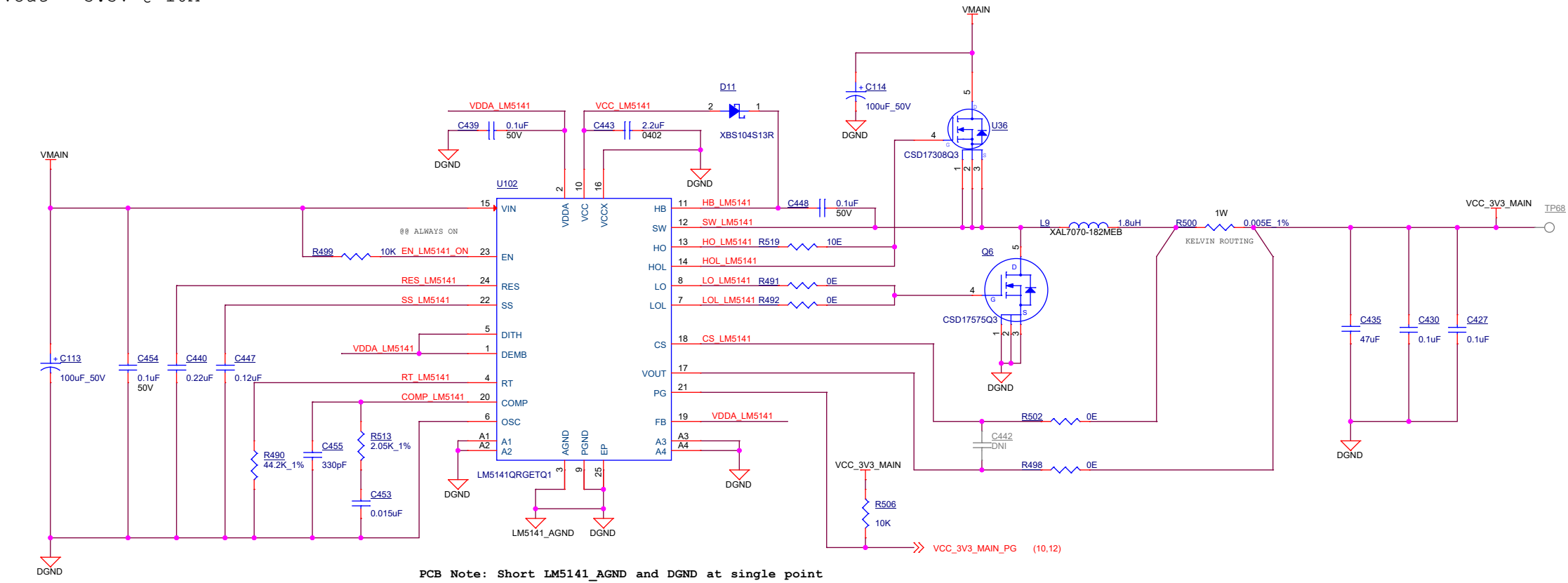
3.3V/1.8V SD CARD SUPPLY



PERIPHERAL POWER SUPPLY-2

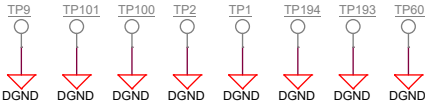
3.3V, 10.0 AMPS SUPPLY

VinMin = 4.5V  
VinMax = 15V  
Vout = 3.3V @ 10A



(34) ETH\_CAN\_INH\_PREREG >> DNI R75 EN\_LM5141\_ON

GND TEST POINTS

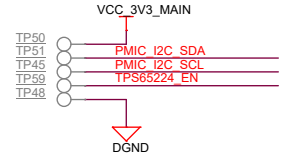


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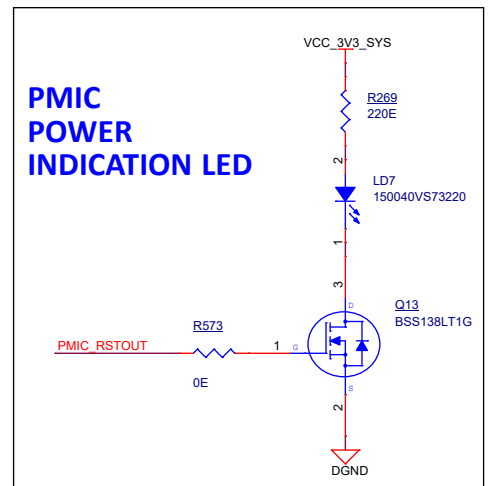
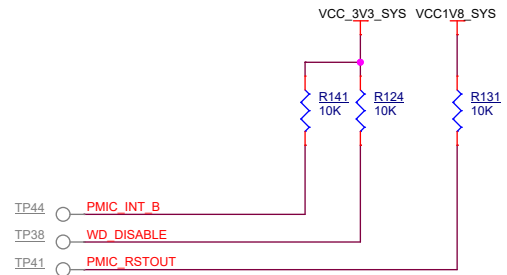
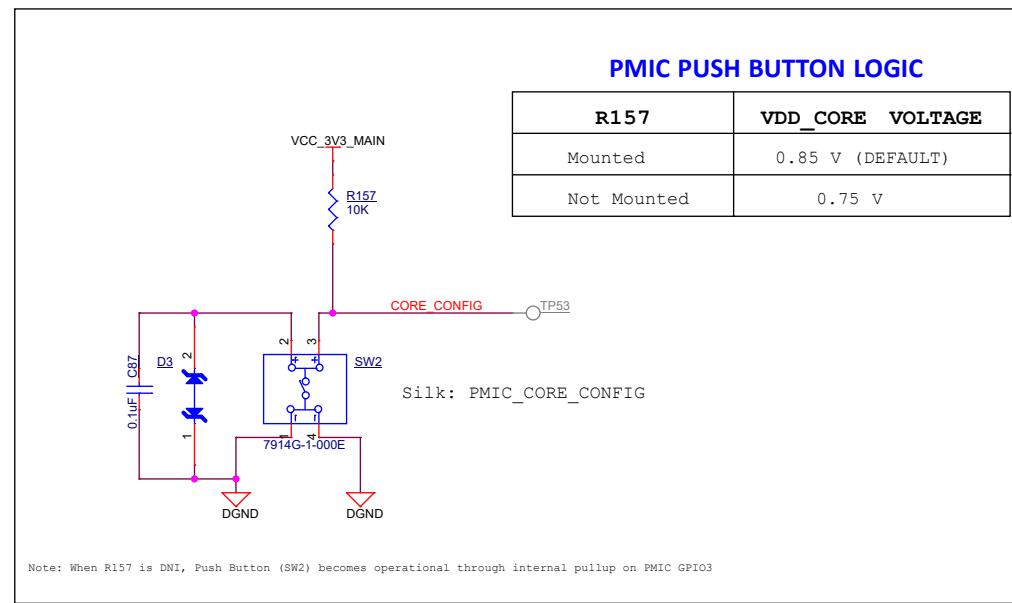
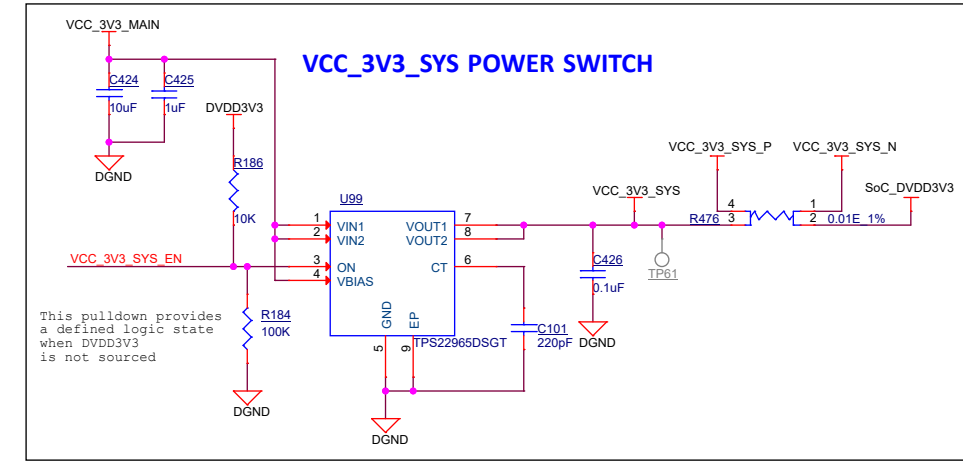
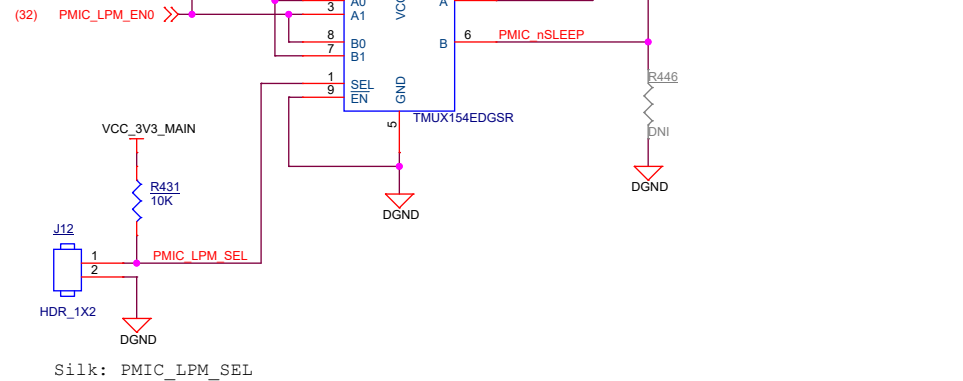
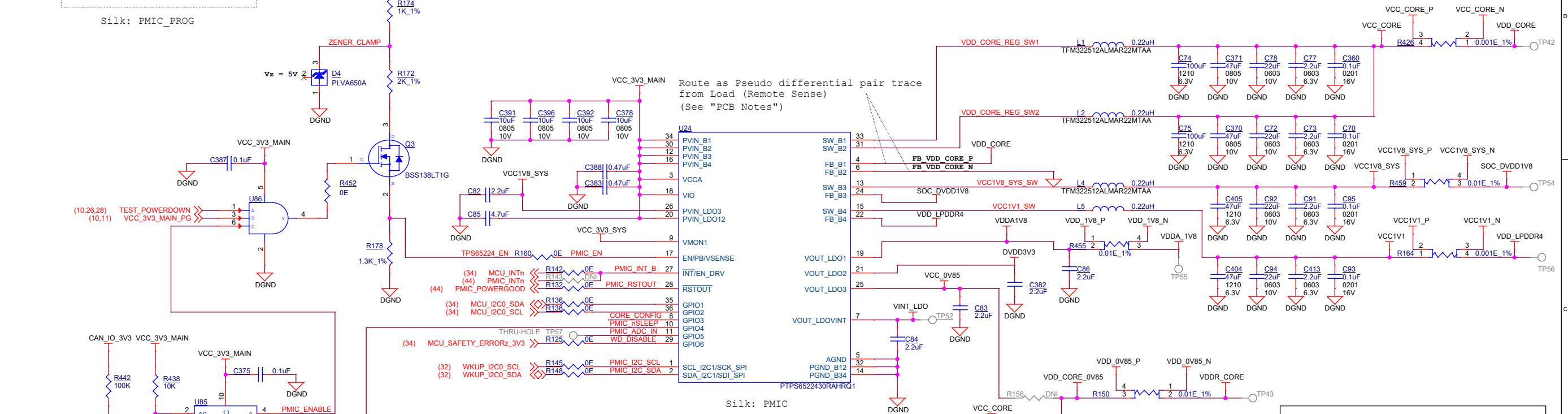
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Size	PROC164E1	Rev
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Date:	Monday, June 26, 2023	Sheet 11 of 47

## PMIC Config option



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# SOC POWER SUPPLY PMIC



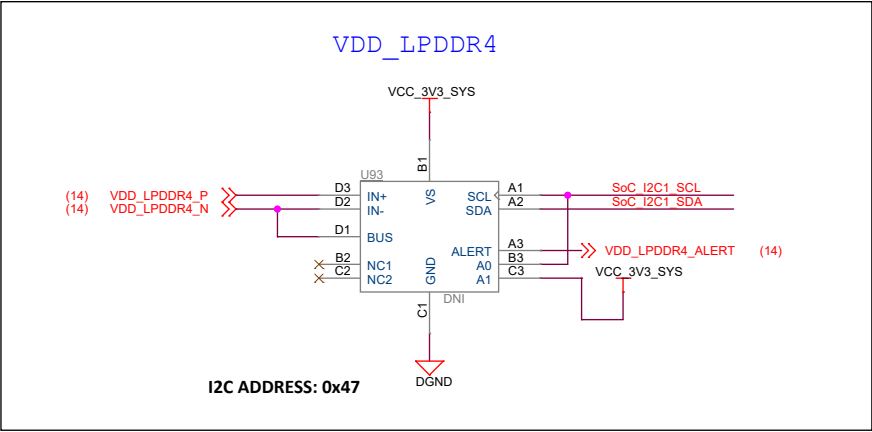
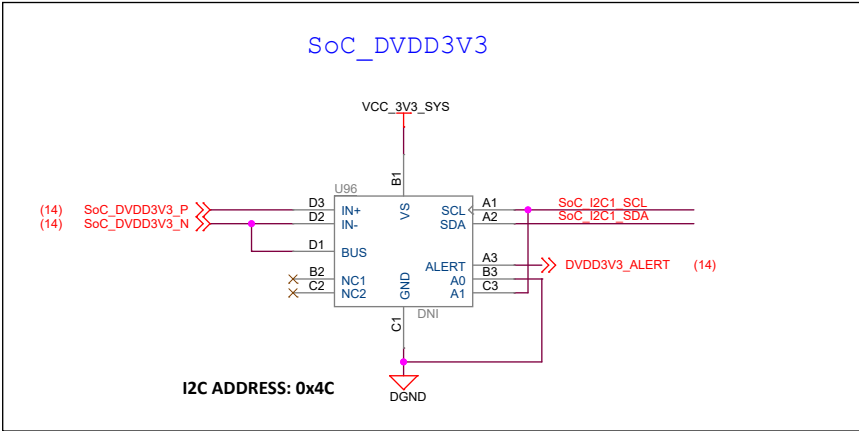
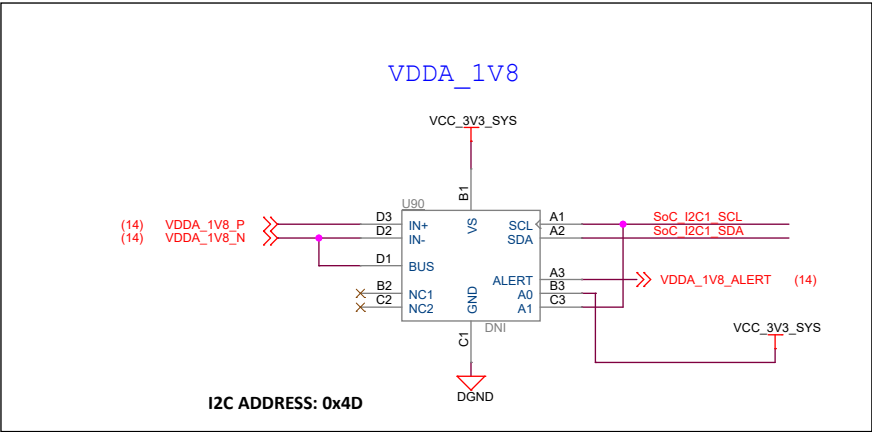
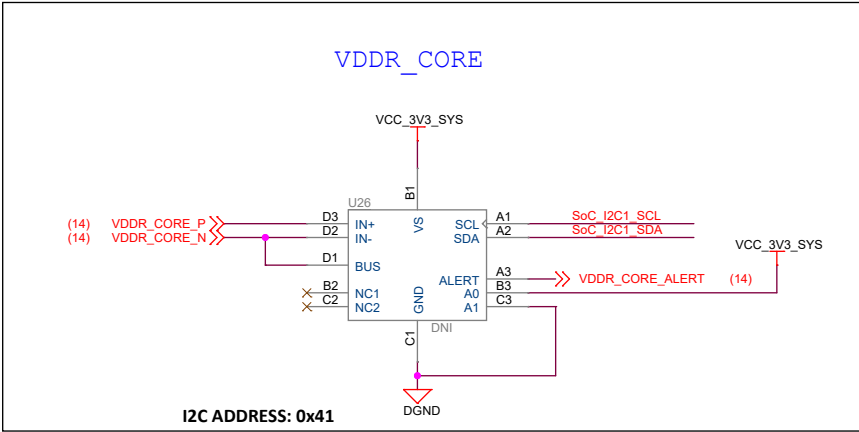
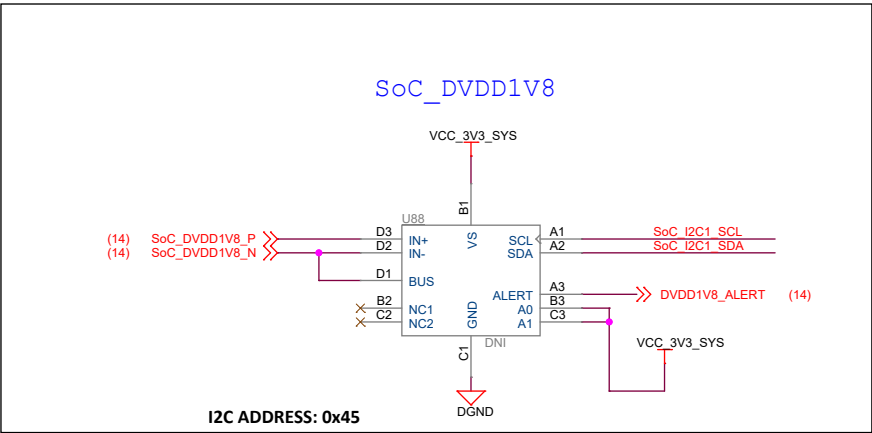
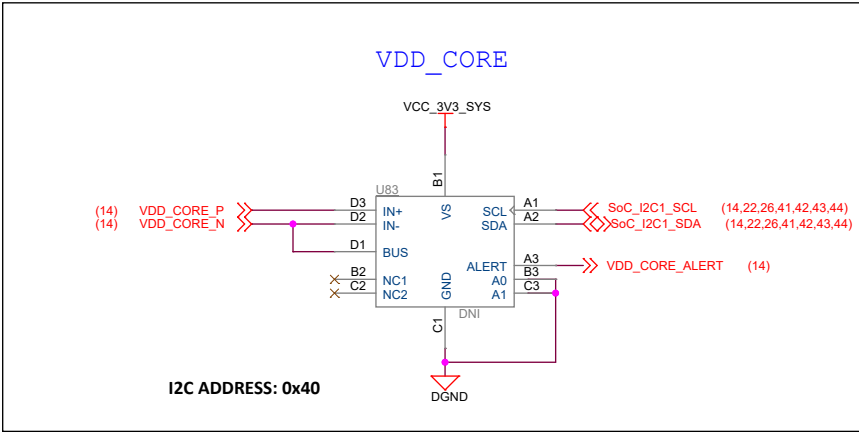
R157	VDD_CORE VOLTAGE
Mounted	0.85 V (DEFAULT)
Not Mounted	0.75 V

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Title SOC POWER SUPPLY PMIC		
Size	PROC164E1	Rev
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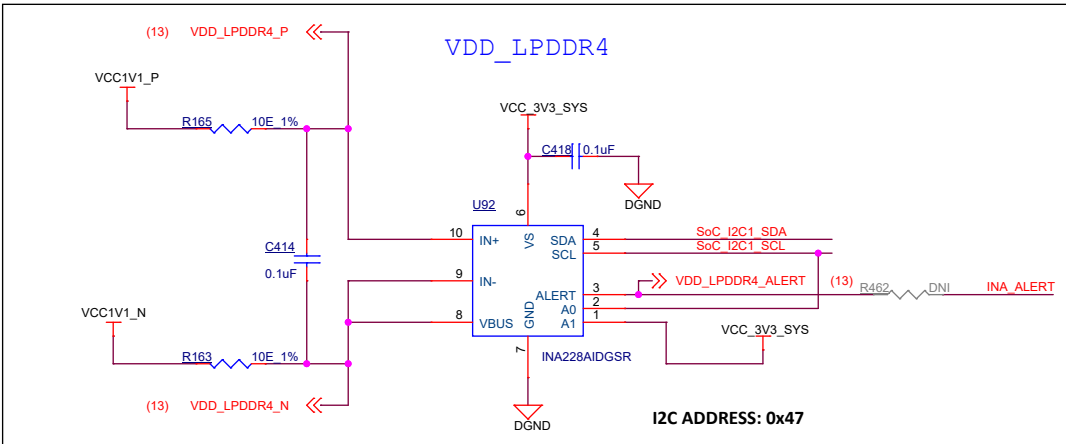
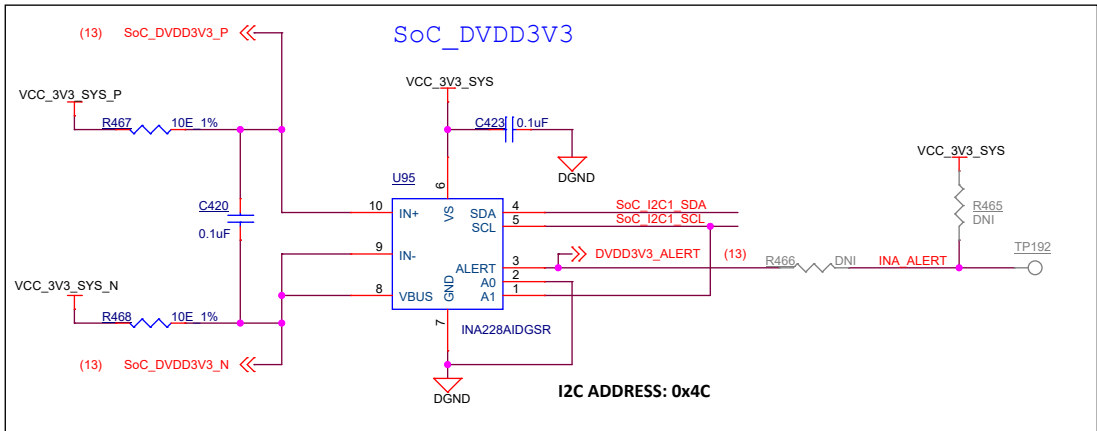
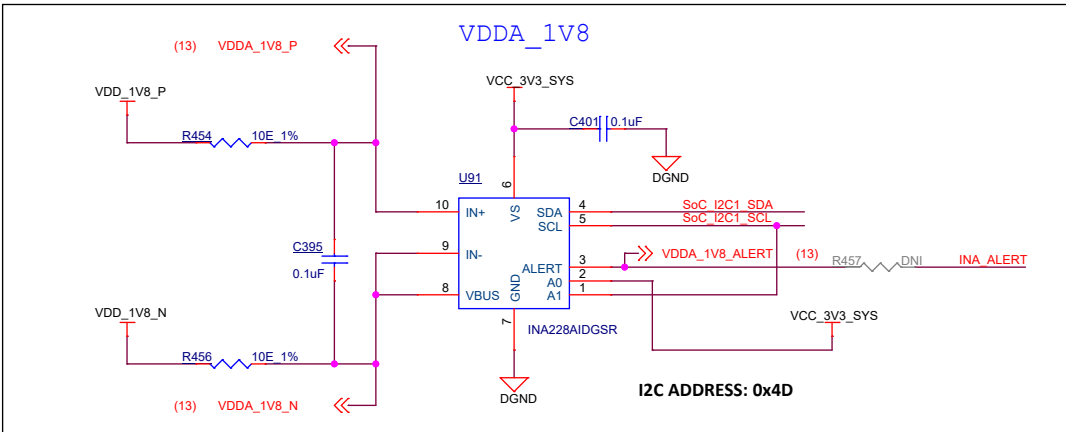
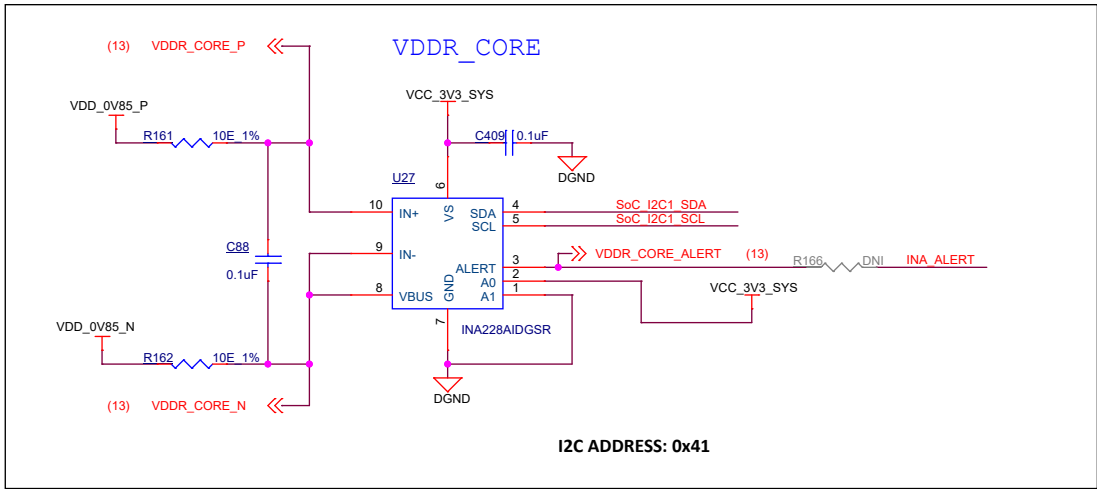
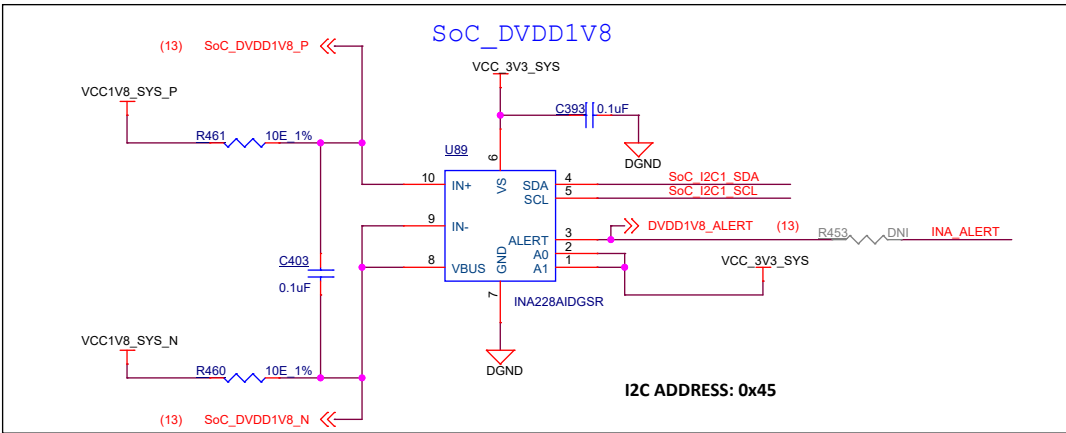
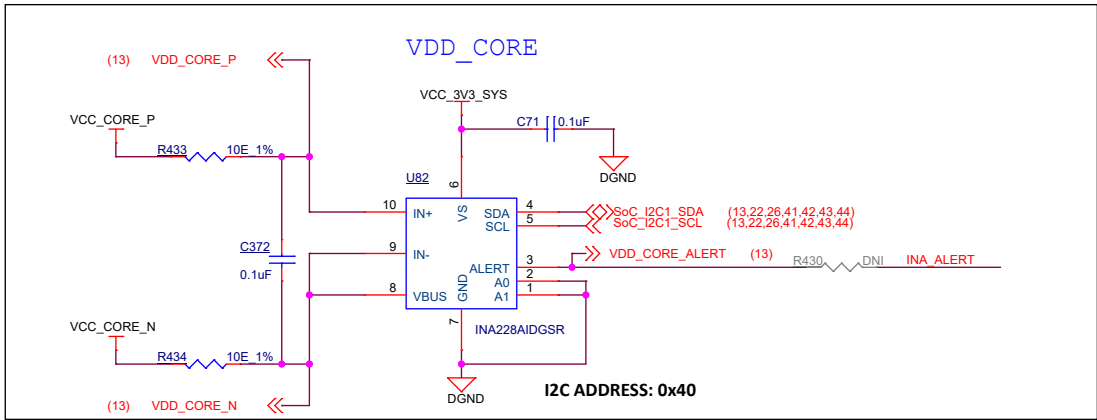
CURRENT MONITORING DEVICES - 1



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

# CURRENT MONITORING DEVICES - 2



Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

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Title CURRENT MONITORING DEVICES - 2

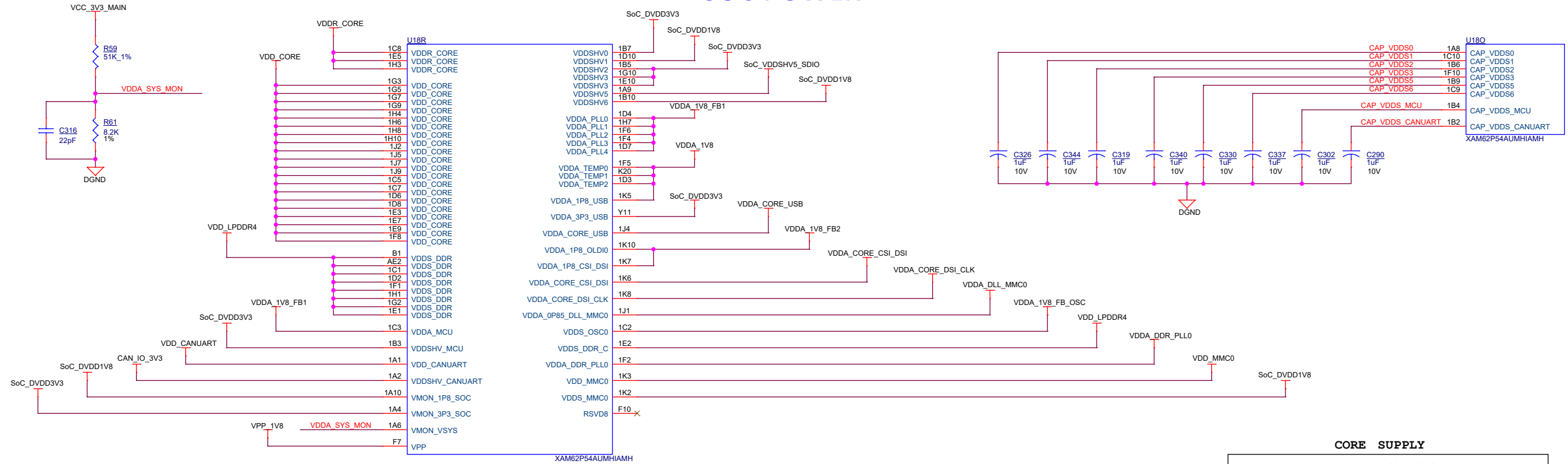
Size PROC164E1

Rev E1

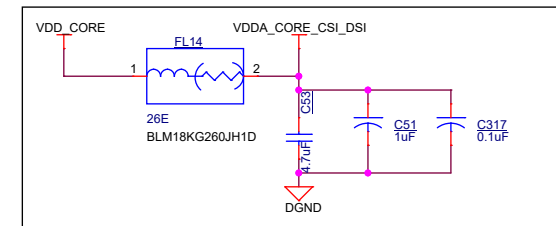
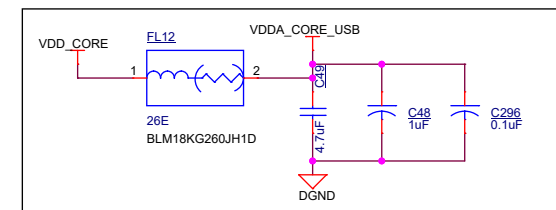
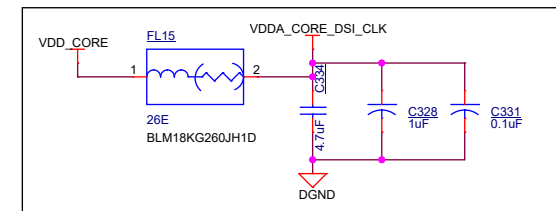
Date: Monday, June 26, 2023

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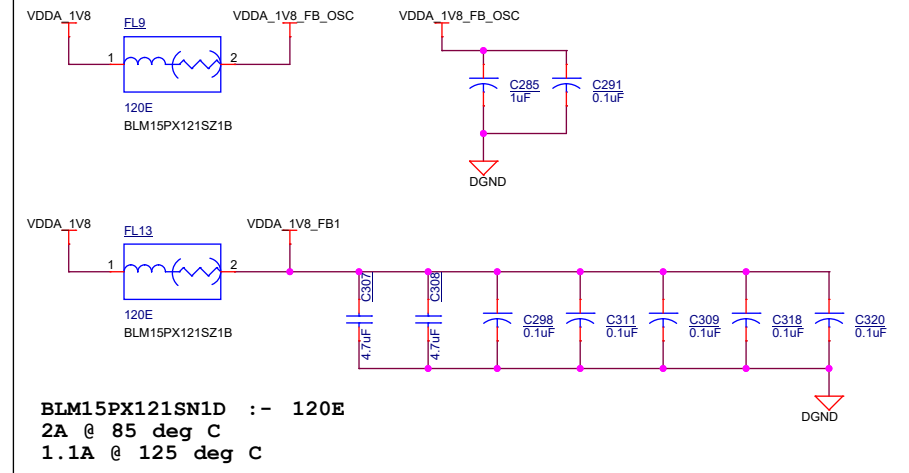
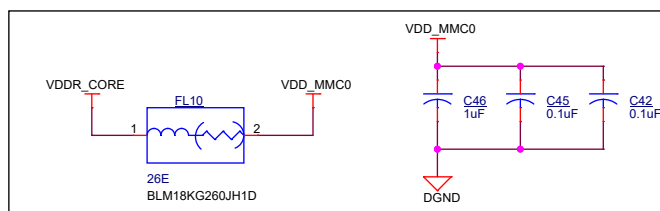
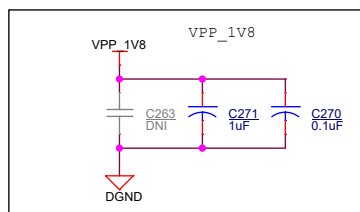
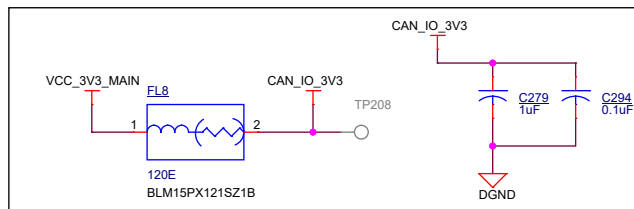
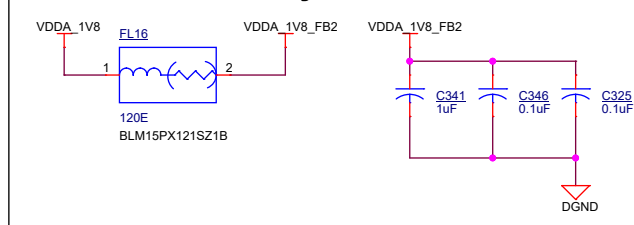
## SOC POWER



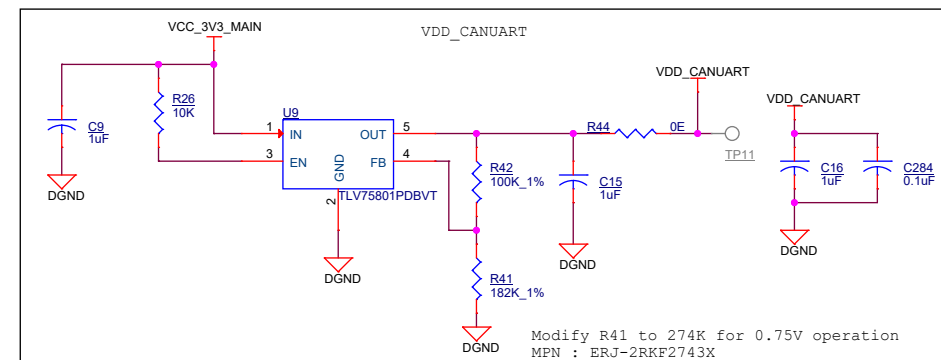
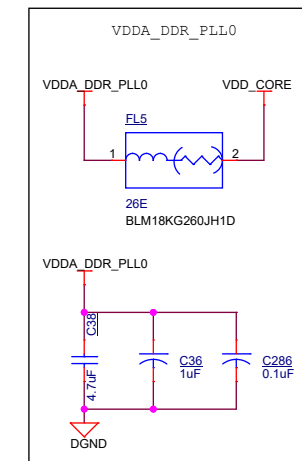
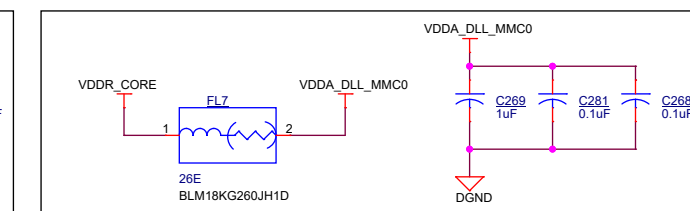
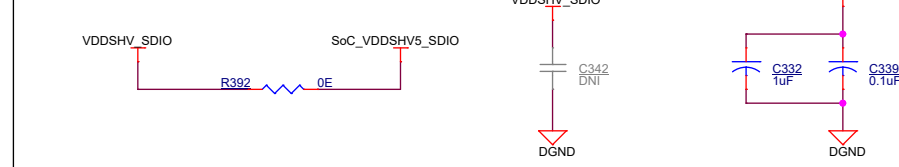
CORE SUPPLY



### 1.8V Analog SUPPLY



### 3.3V/1.8V MMC1 SUPPLY



Modify R41 to 274K for 0.75V operation  
MPN : ERJ-2RKF2743X

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Title	SOC POWER
-------	-----------

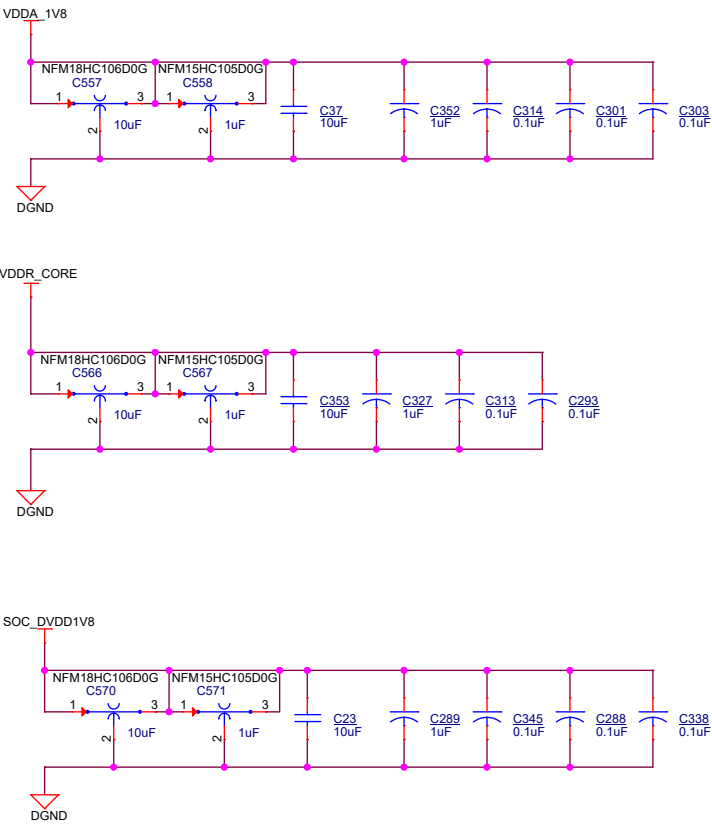
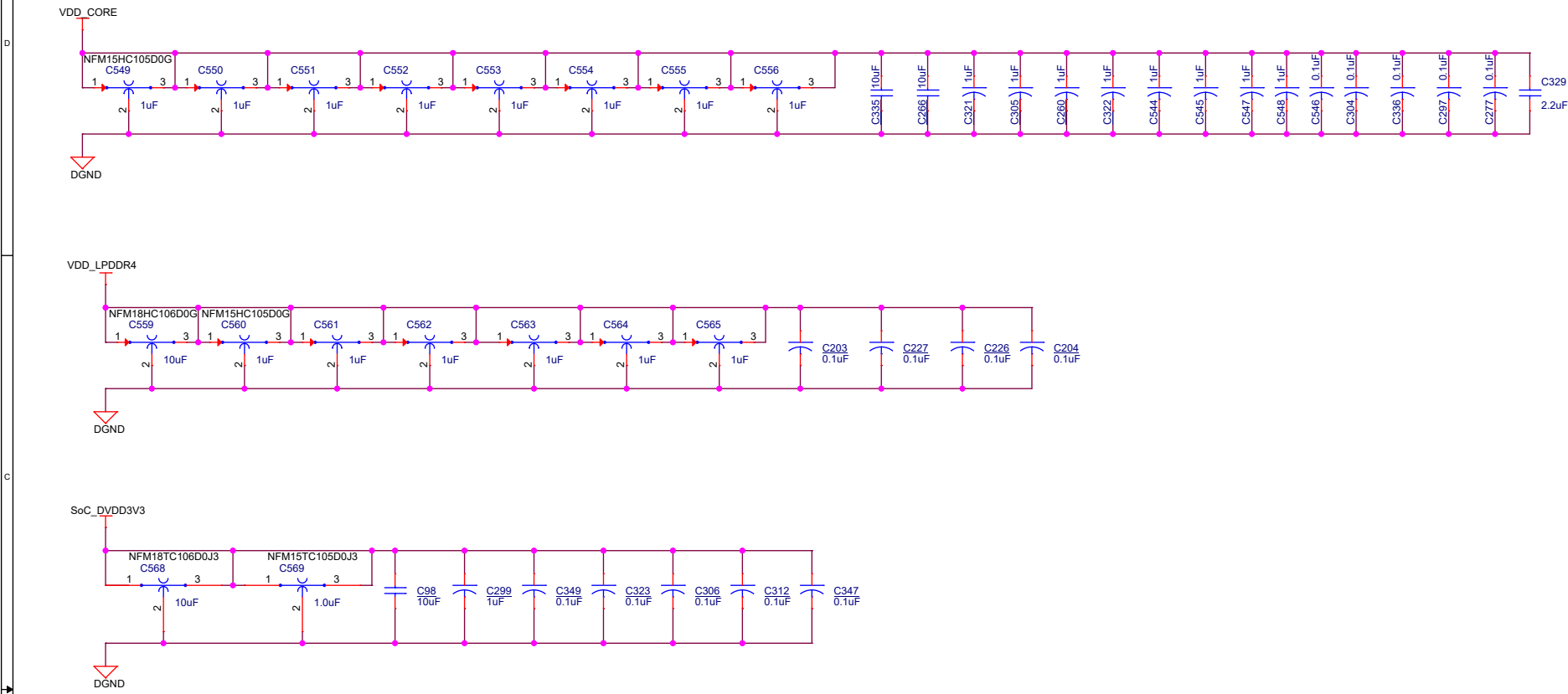
Size	PROC164E1
C	

Date: Monday, June 26, 2023

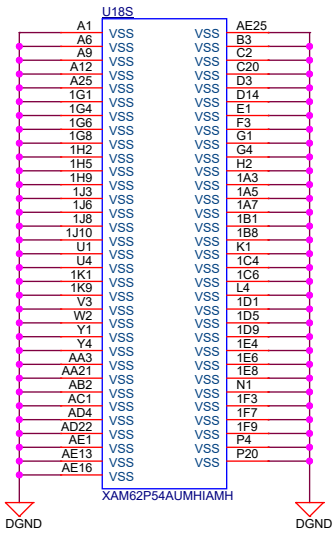
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SOC POWER DECAPS

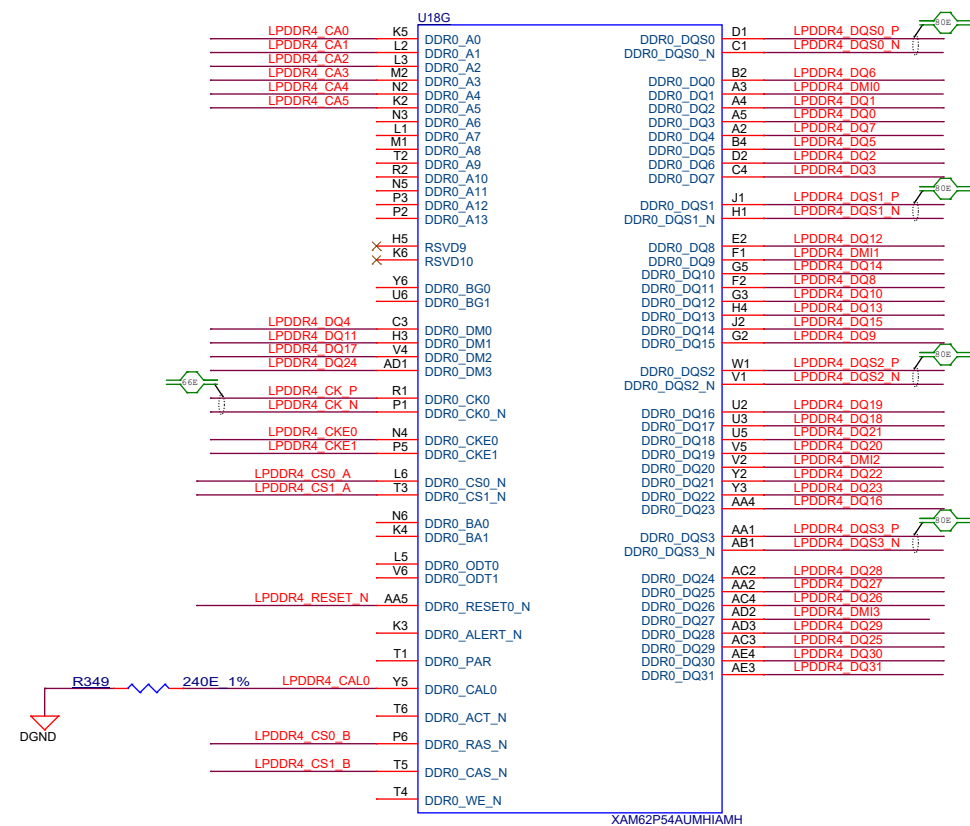


SOC VSS

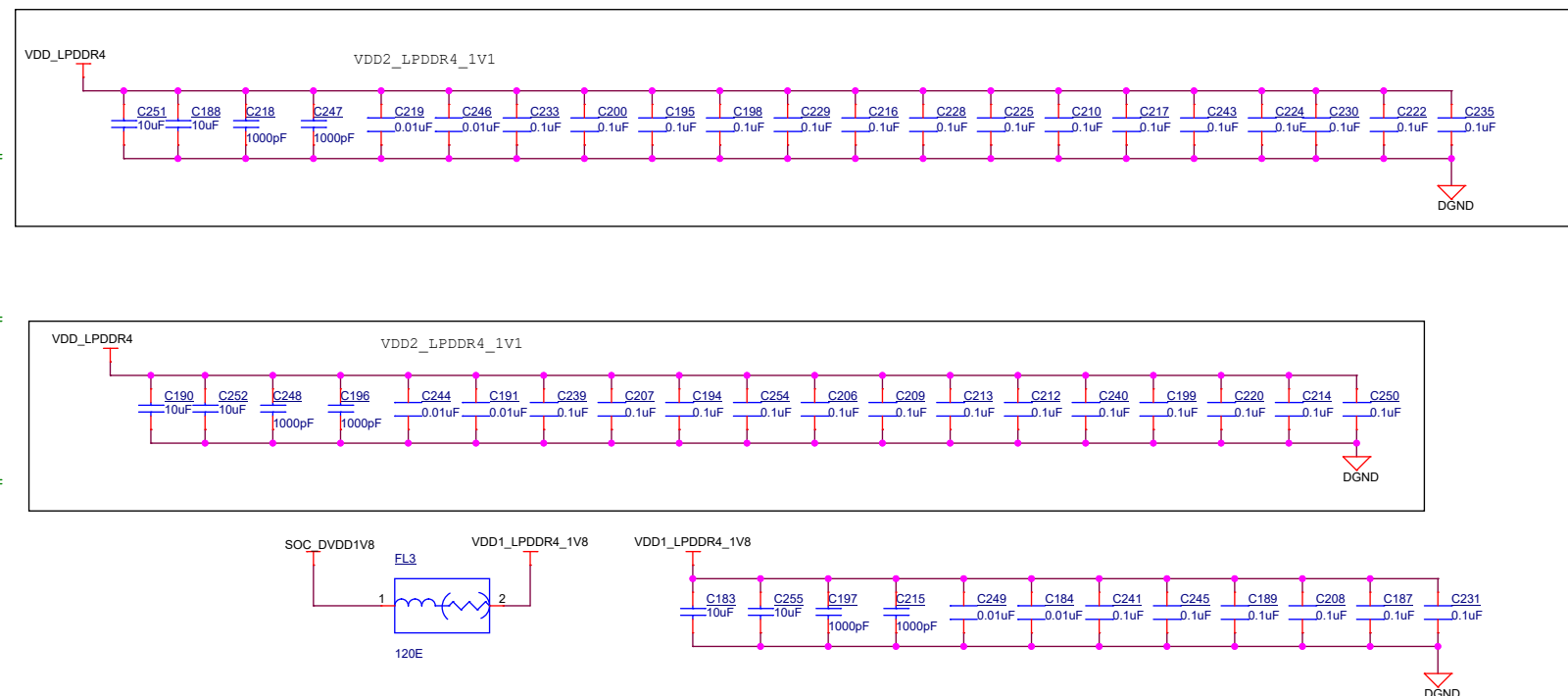




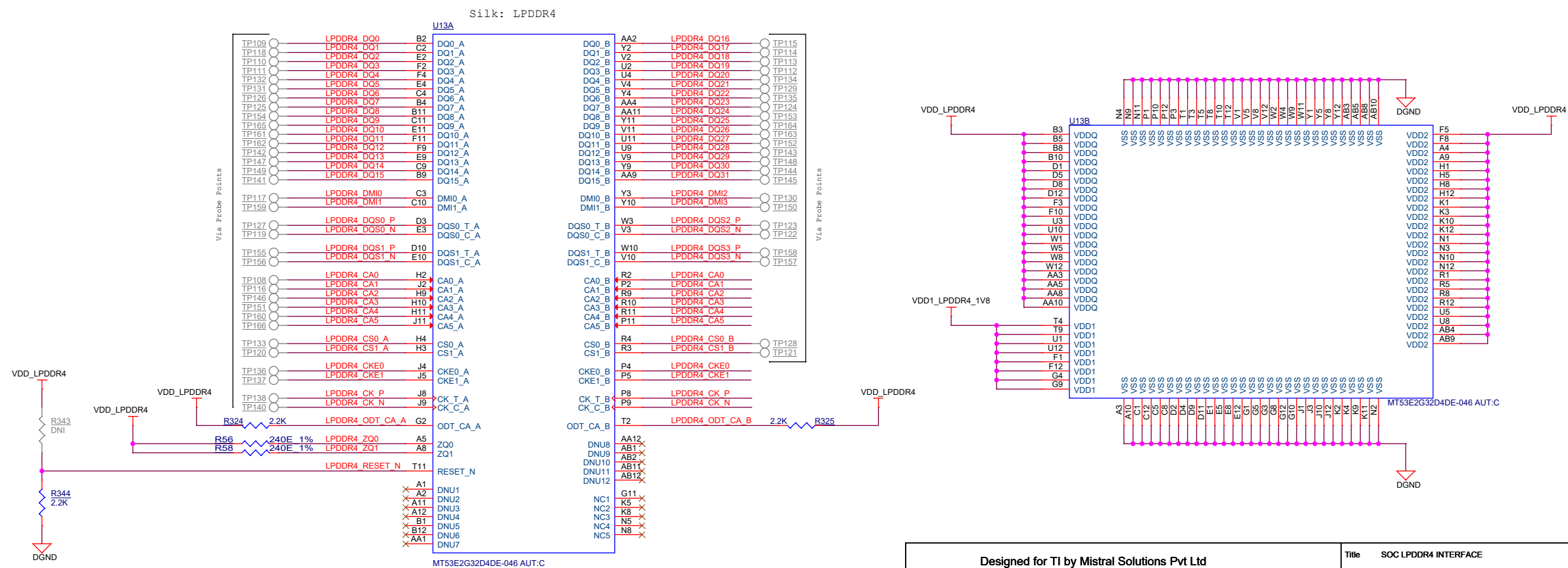
## SOC LPDDR4 INTERFACE



## LPDDR4 POWER DECAPS



## LPDDR4 DEVICE



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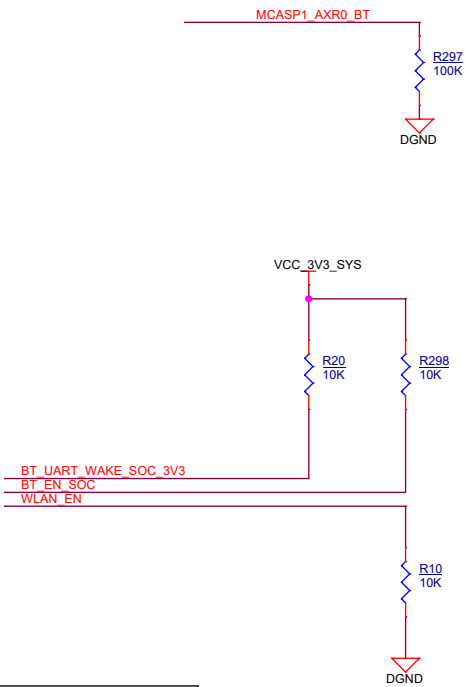
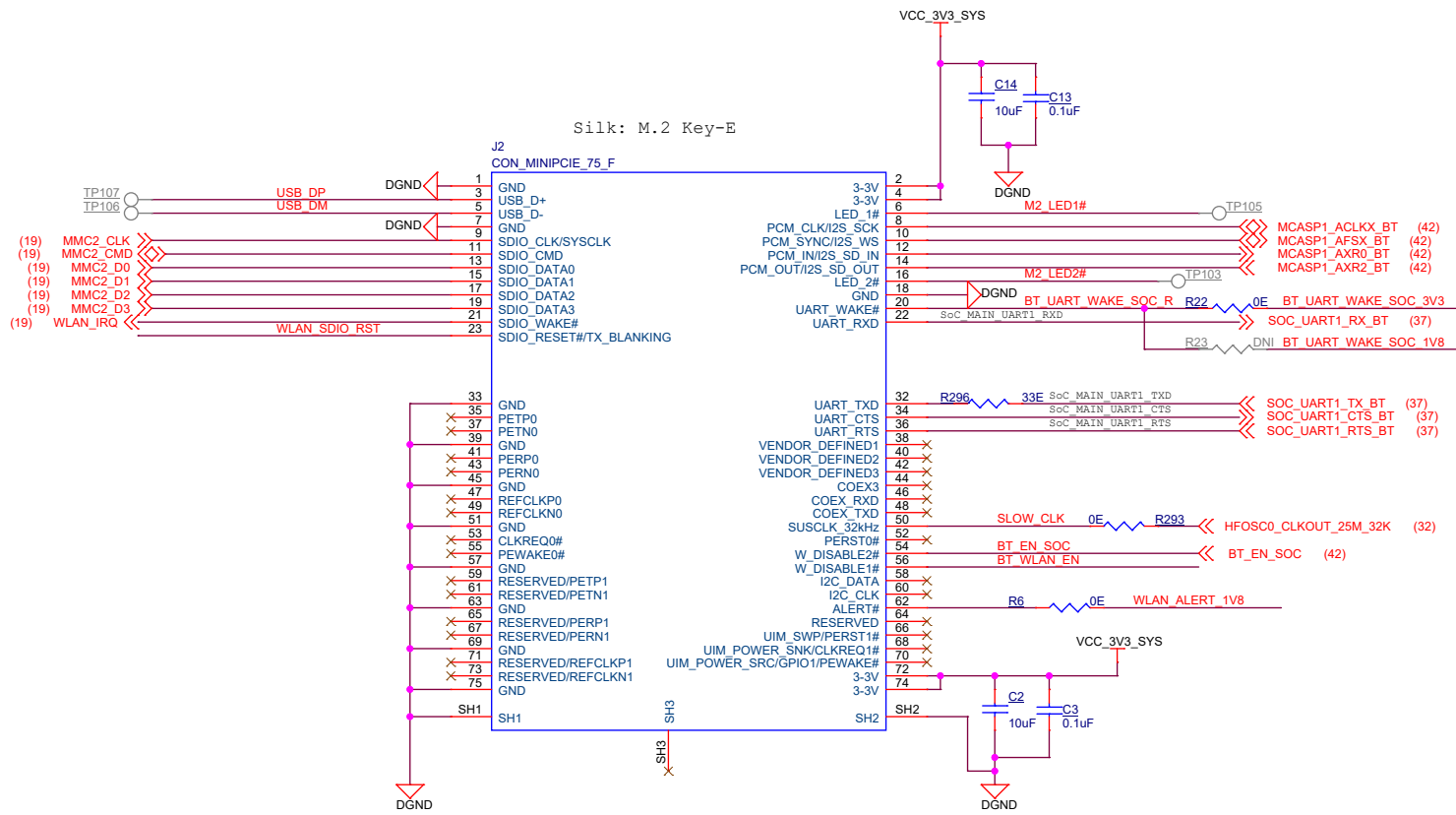
Title	SOC LPDDR4 INTERFACE
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Size	PROC164E1
C	

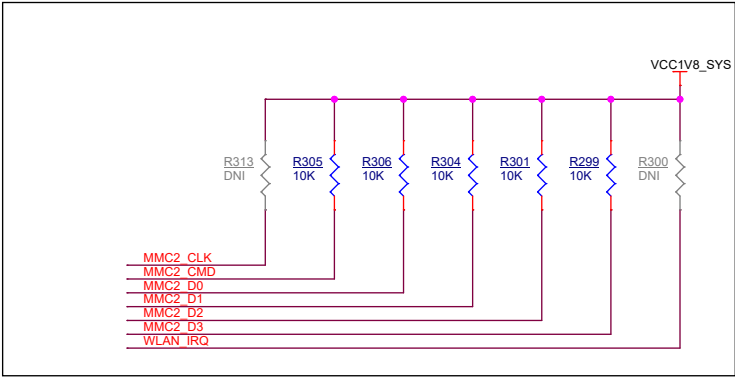
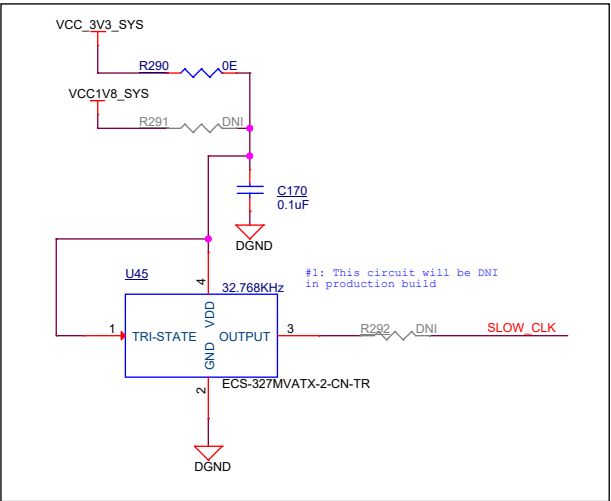
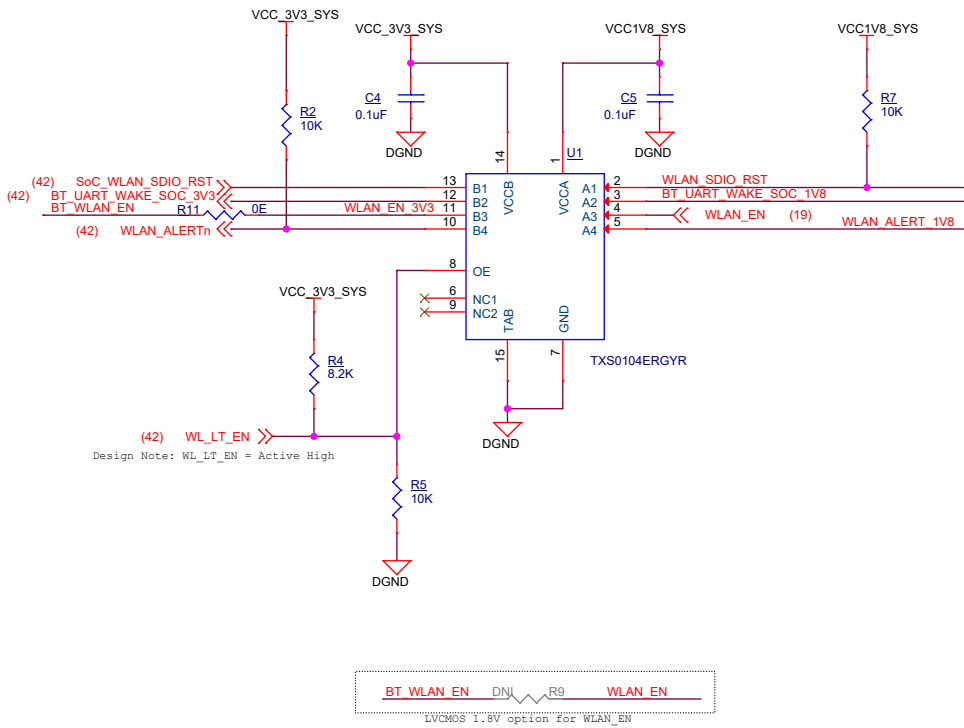

Date: Monday, June 26, 2023

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M.2 INTERFACE - SDIO



M.2 LEVEL TRANSLATOR



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Title M.2 CONNECTOR V/F

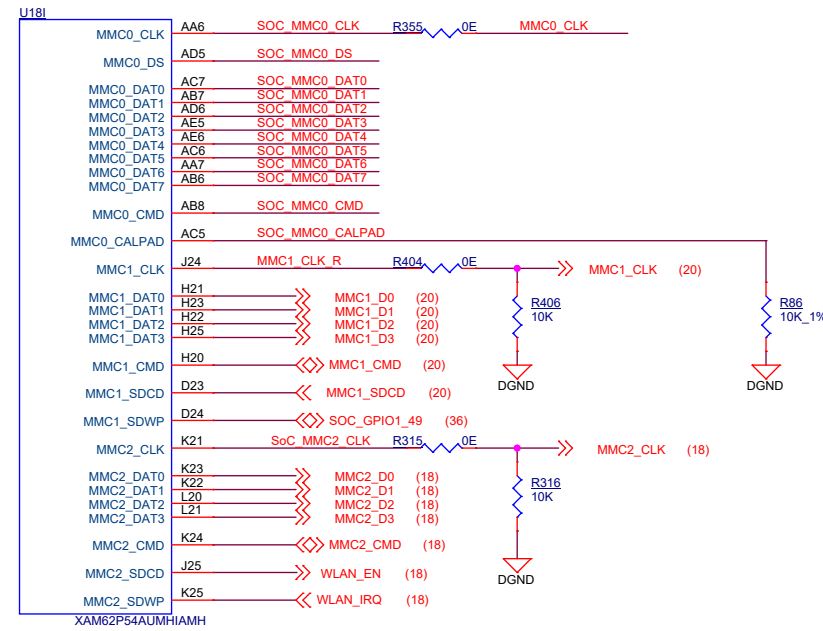
Size C

Date: Monday, June 26, 2023

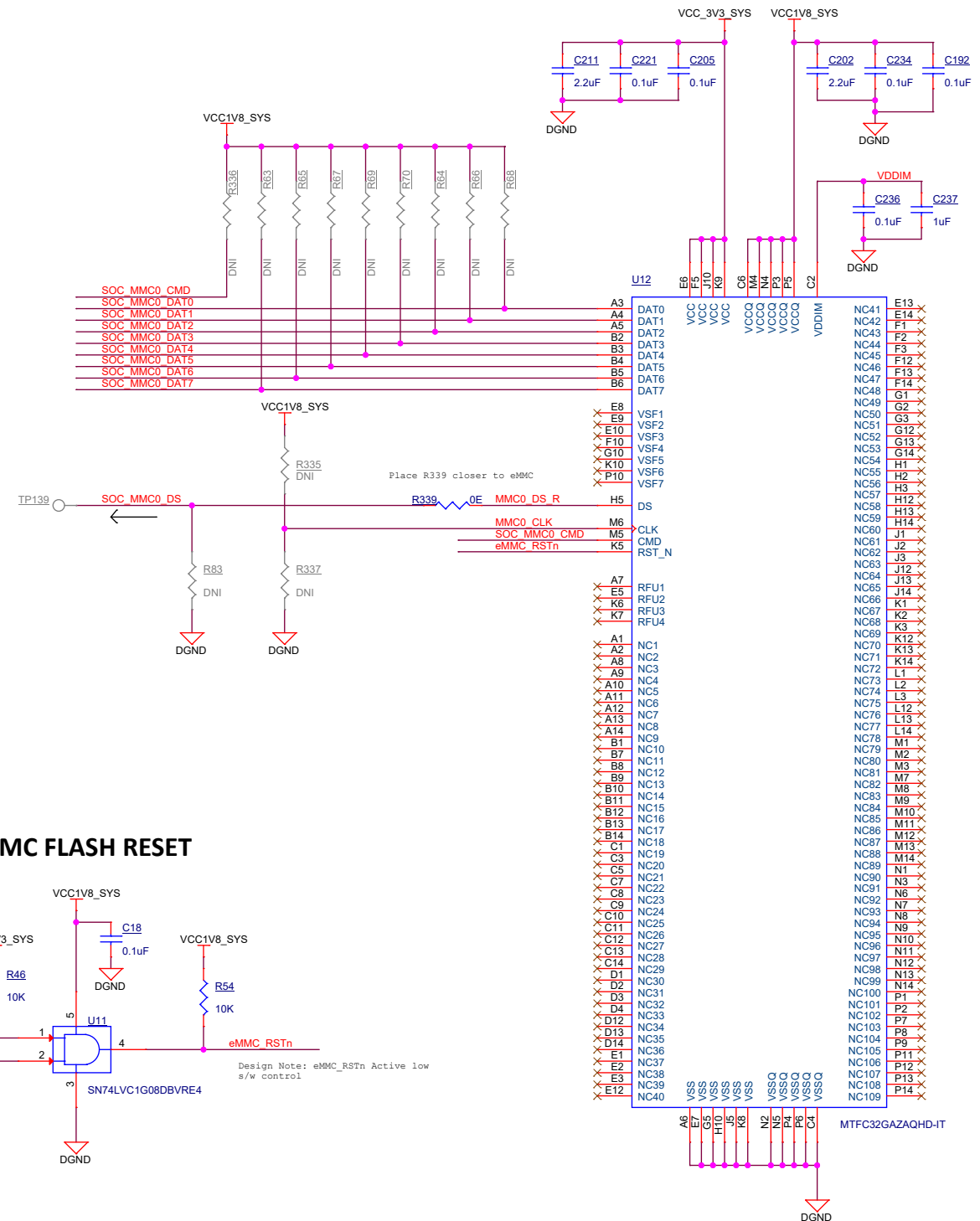
Sheet 18 of 47

Rev E1

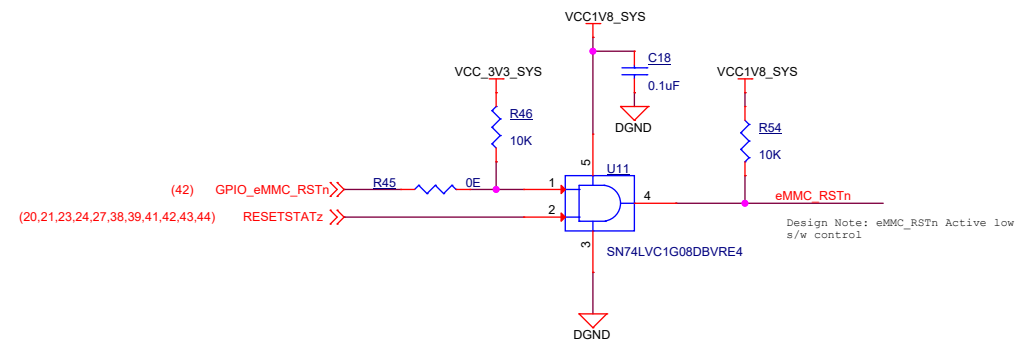
## SOC - MMC Interface



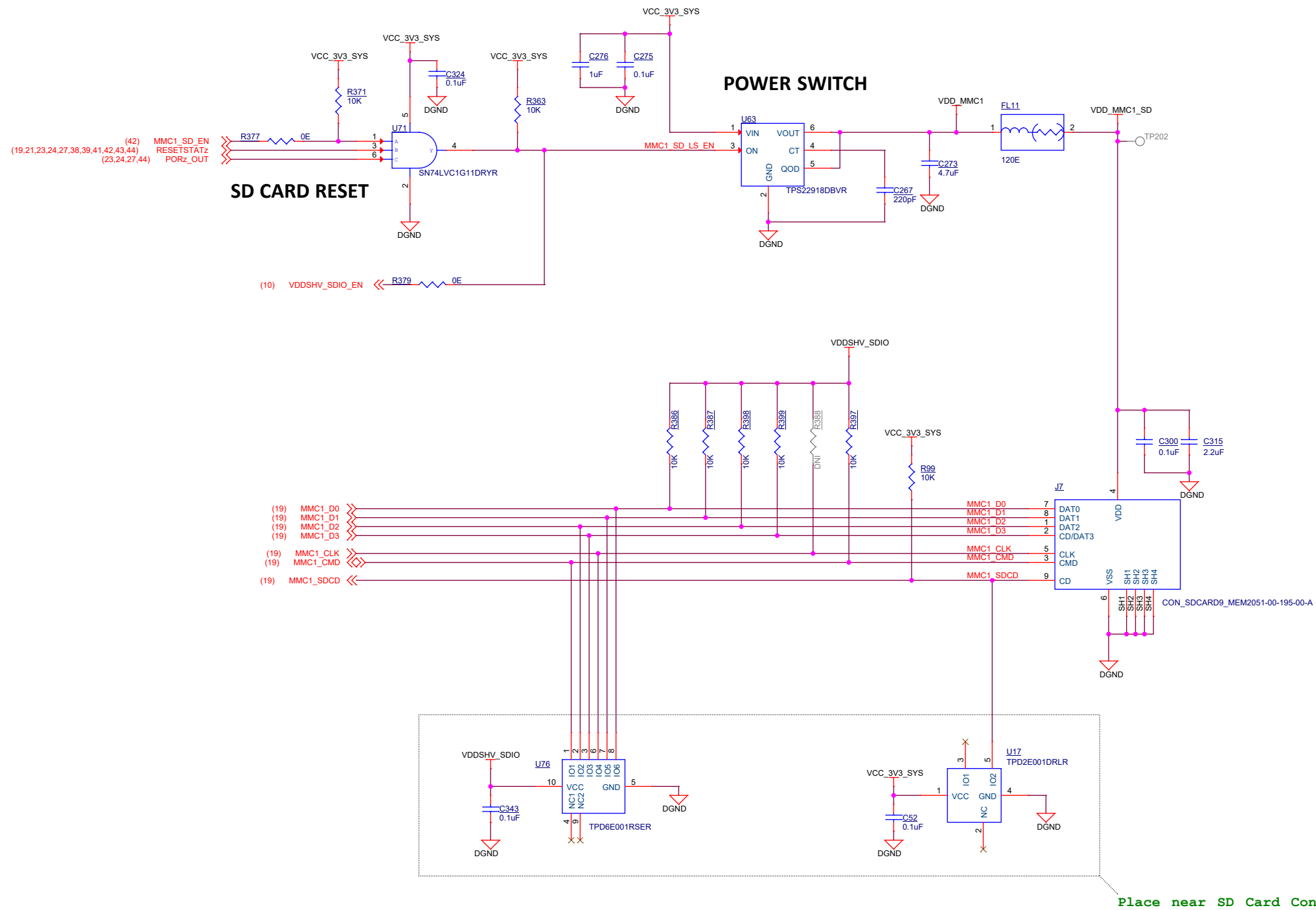
## eMMC FLASH



## eMMC FLASH RESET



## SD CARD INTERFACE

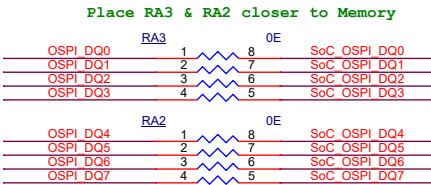
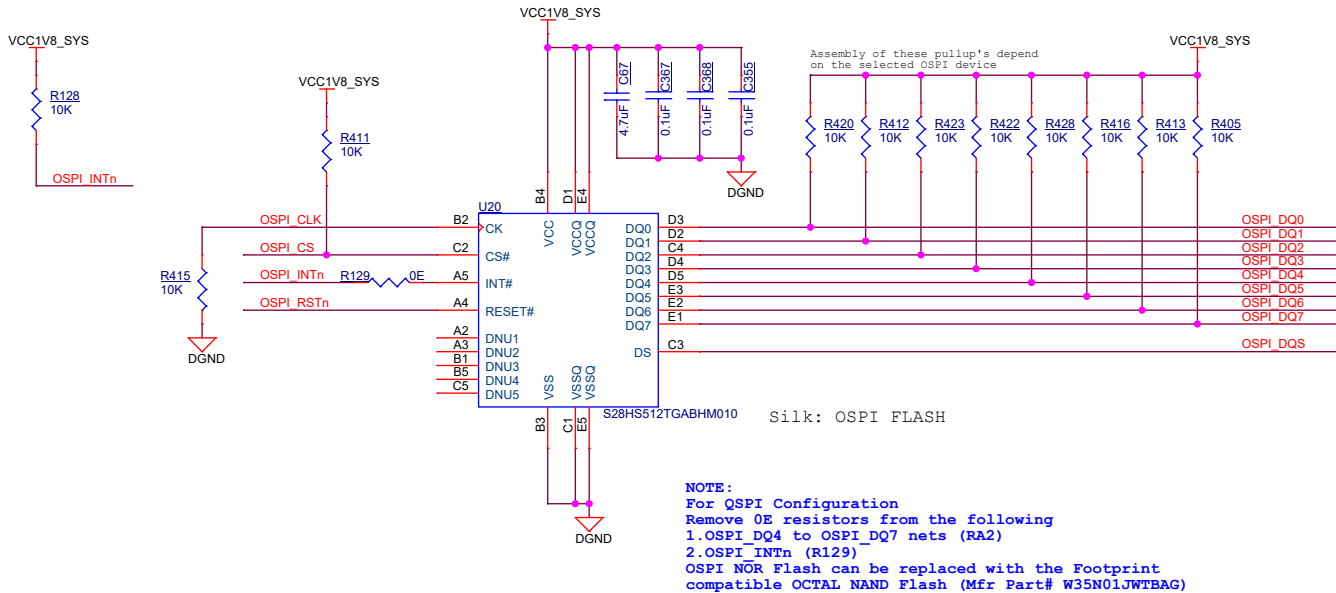


Place near SD Card Connector



OSPI FLASH

SOC OSPI INTERFACE

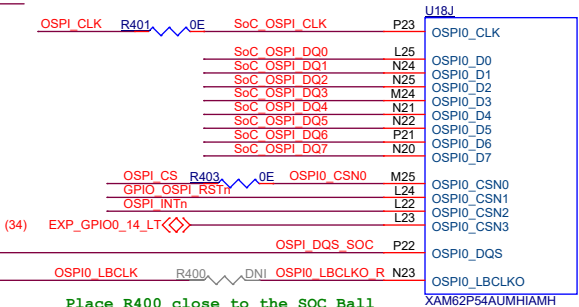


Place R417 close to the Memory

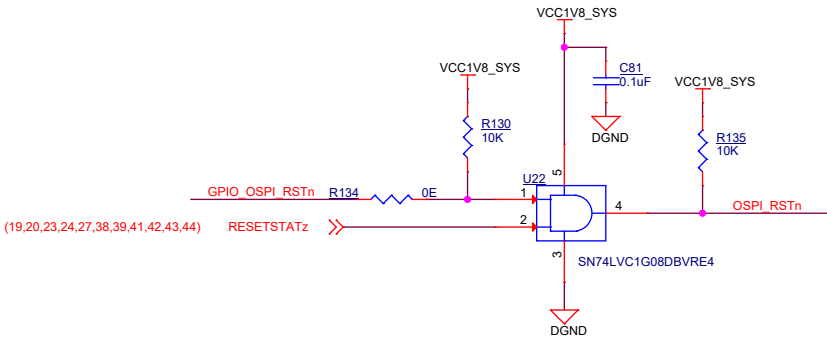
Place R396 closer to the SoC

Tripad R421 & R417 to avoid stubs

Place R400 close to the SOC Ball with as little trace as possible



OSPI FLASH RESET

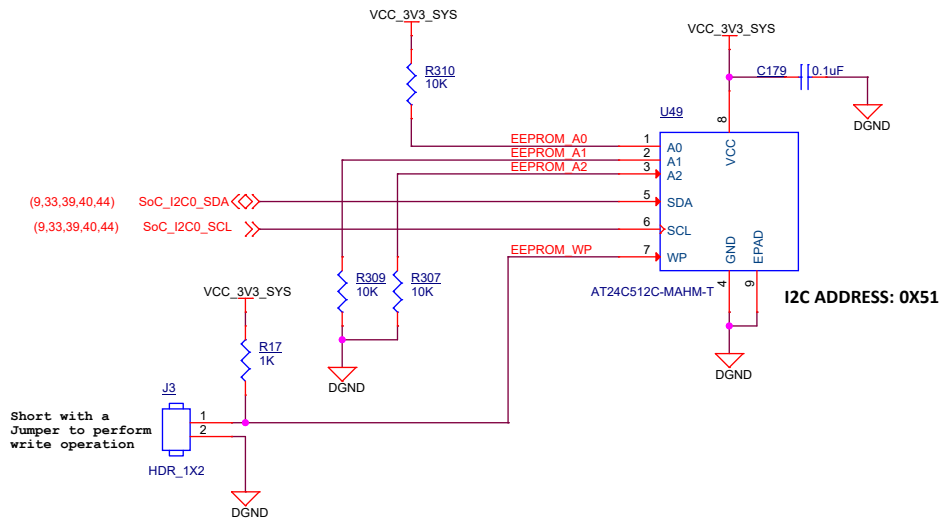


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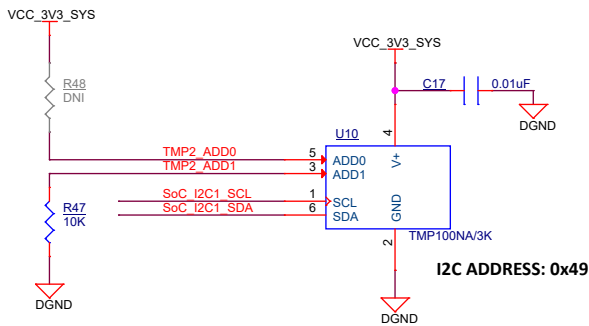
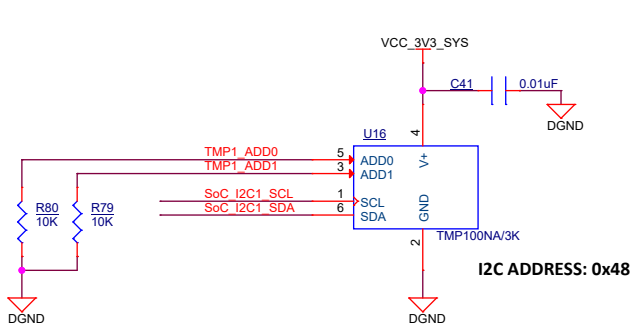


Title OSPI INTERFACE		
Size	PROC164E1	Rev
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BOARD ID EEPROM



TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR U16 CLOSE TO SoC

CAD NOTE: PLACE TEMP SENSOR U10 CLOSE TO LPDDR4

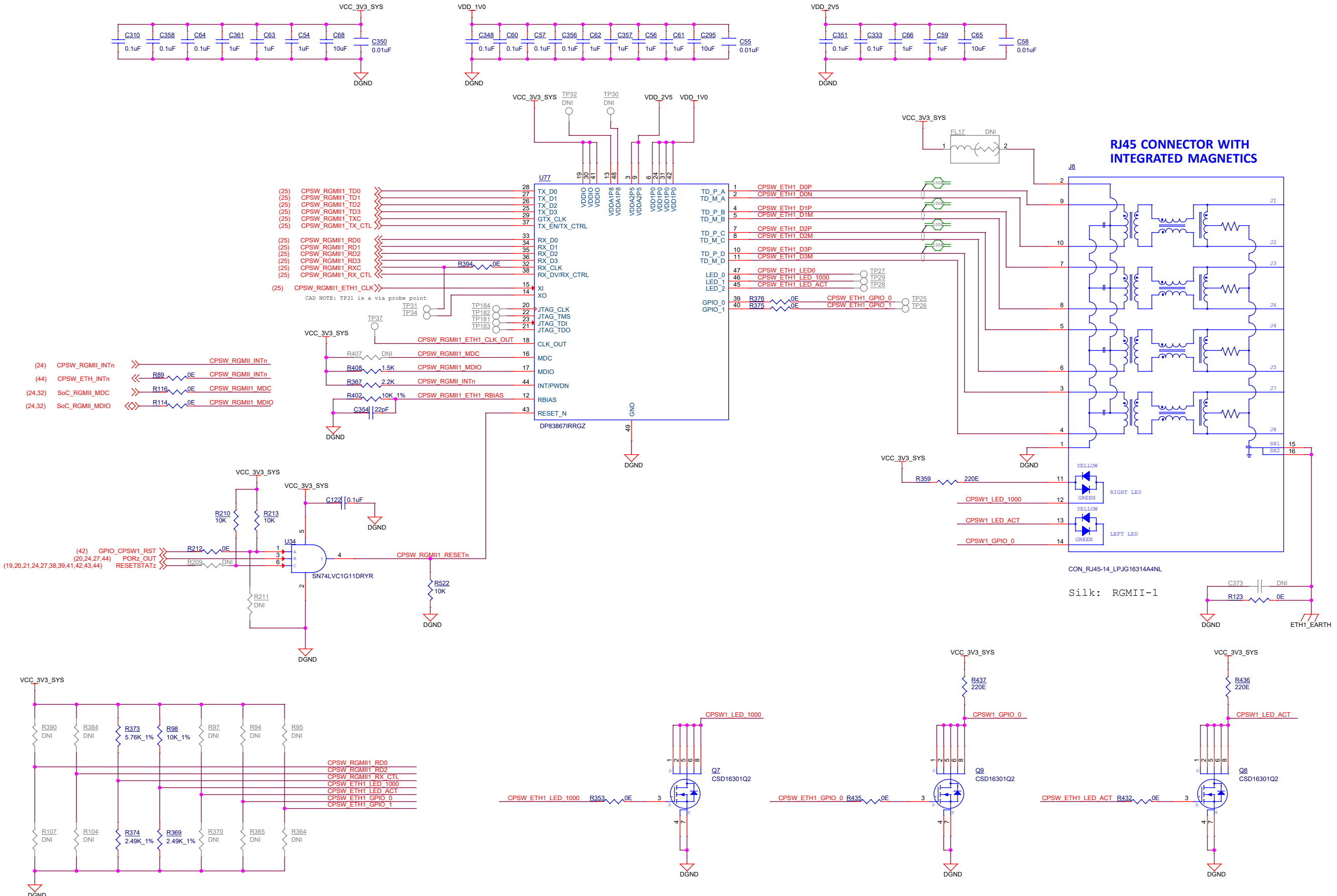
(13,14,26,41,42,43,44) SoC\_I2C1\_SCL >> TP63  
(13,14,26,41,42,43,44) SoC\_I2C1\_SDA >> TP64  
Silk: SOC\_I2C1

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Title BOARD ID EEPROM & TEMPERATURE SENSORS		
Size C	PROC164E1	Rev E1
Date: Monday, June 26, 2023	Sheet 22 of 47	

## CPSW RGMII 1 - PHY



```
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
```

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Title	CPSW RGMII_1 ETHERNET PHY
-------	---------------------------

Size	550010154
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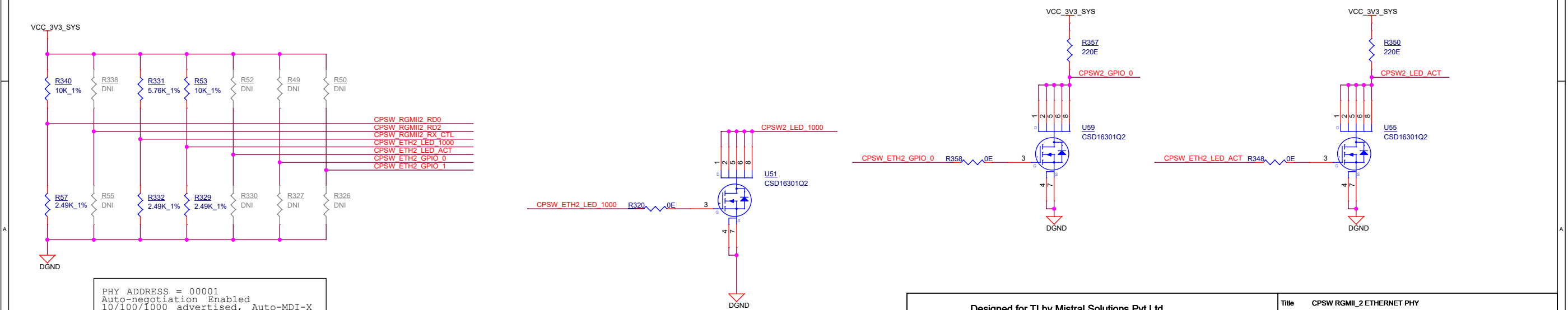
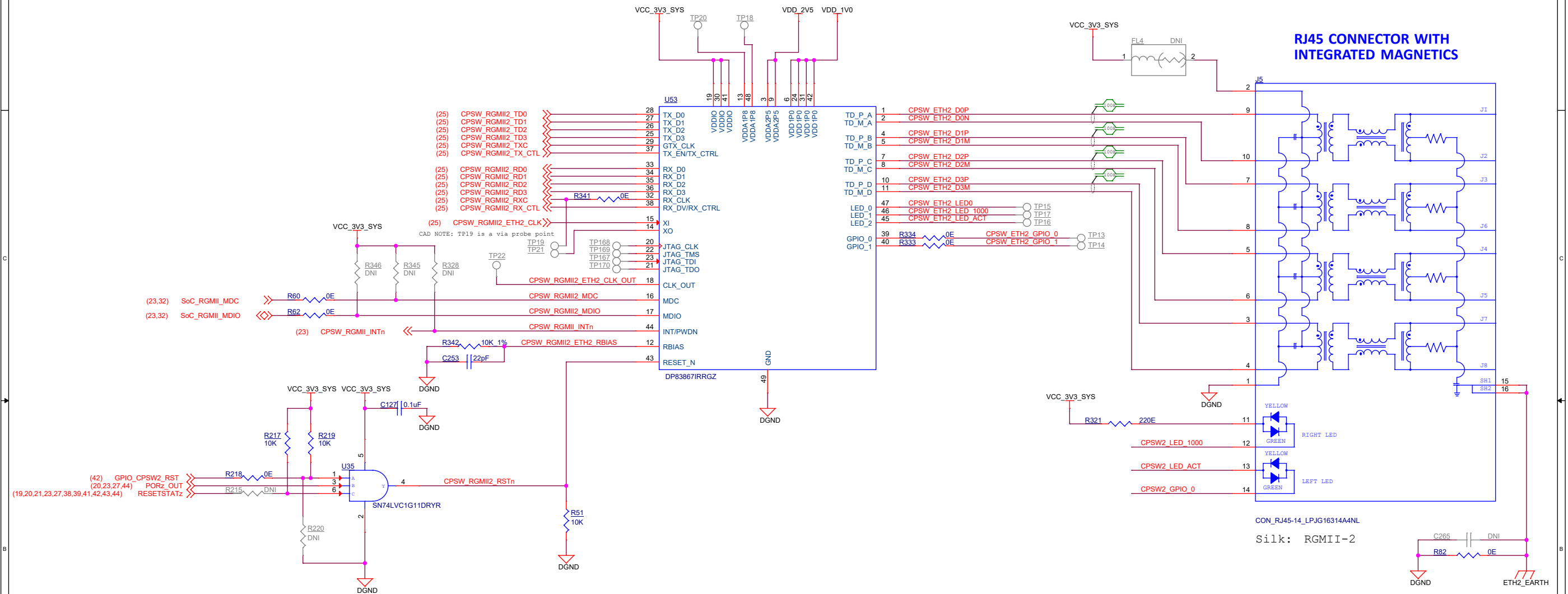
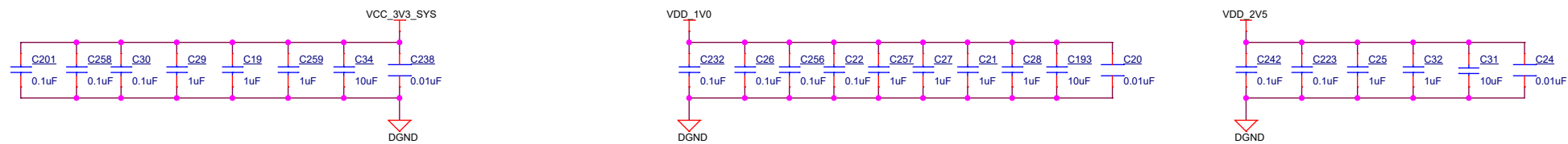
C	
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Sheet 23 of 47

## CPSW RGMII 2 - PHY



```
PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
```

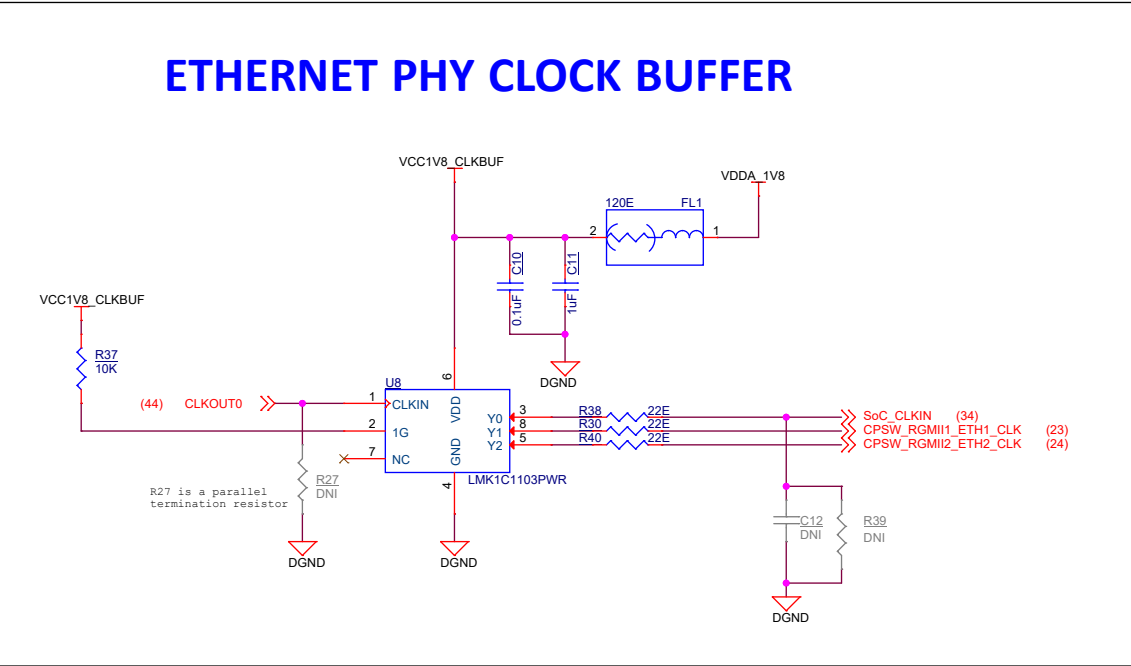
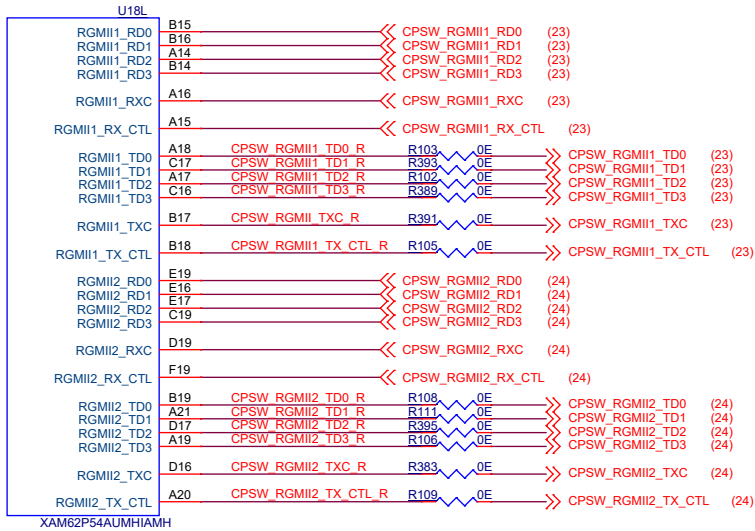
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Title	CPSW RGMII_2 ETHERNET PHY
-------	---------------------------

Size	PROC164E1	
C		
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Title ETHERNET PHY CLOCK BUFFER & LED DRIVER

Size PROC164E1

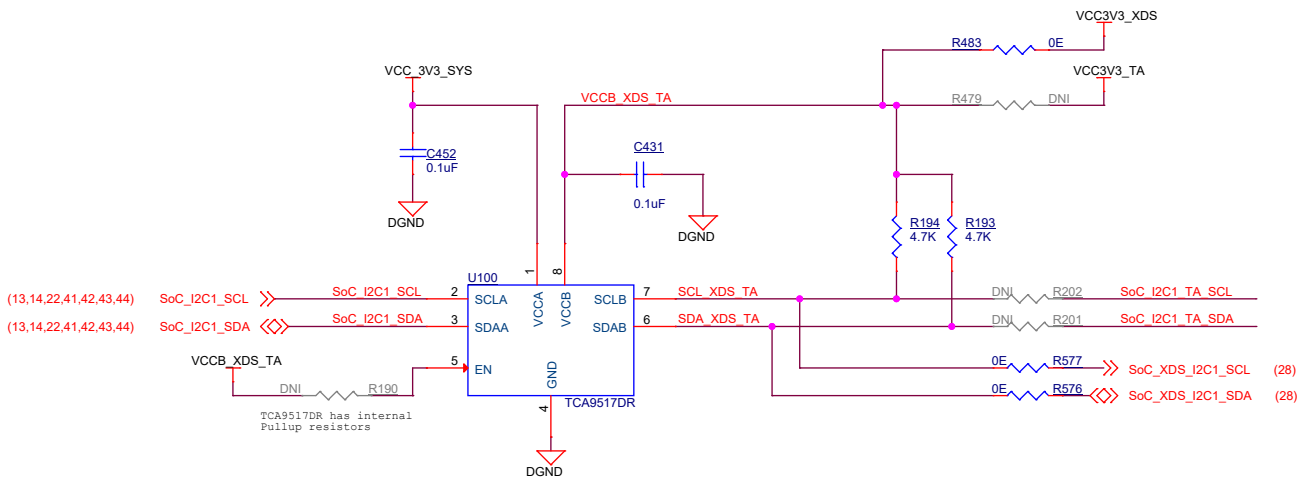
Rev

E1

Date: Monday, June 26, 2023

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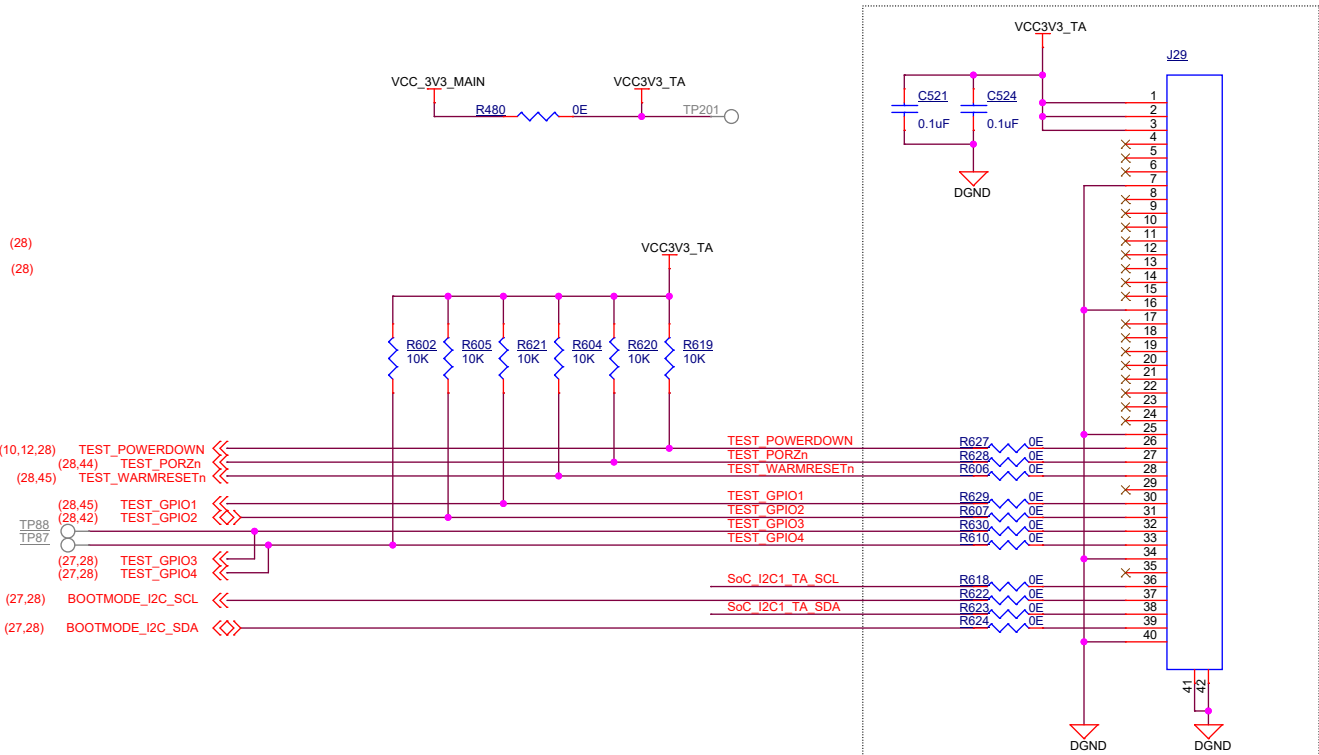
I2C BUS BUFFER



TA Header Configuration

Mount : R201, R202, R479  
Demount: R483, R576, R577

40-PIN TEST AUTOMATION HEADER



#3: The Test Automation Header  
will be DNI in the production build  
CON\_FLEX\_40X1\_FH12A-40S-0.5SH  
Silk: AUTOMATION HDR

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

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Title TEST AUTOMATION

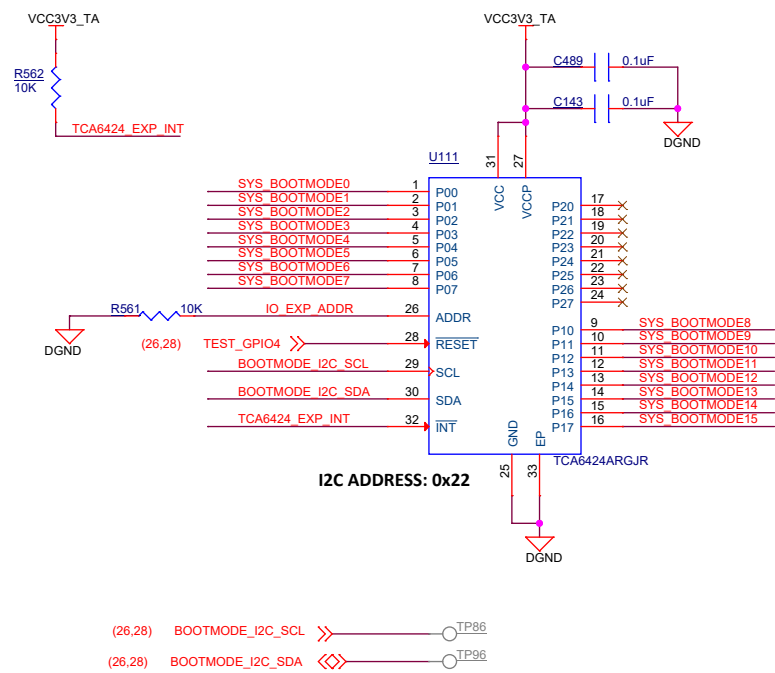
Size  
C PROC164E1

Rev  
E1

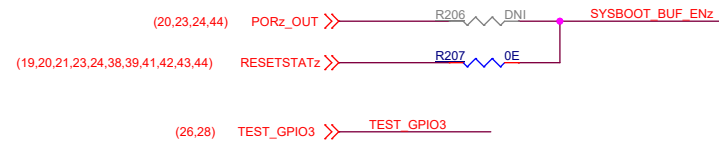
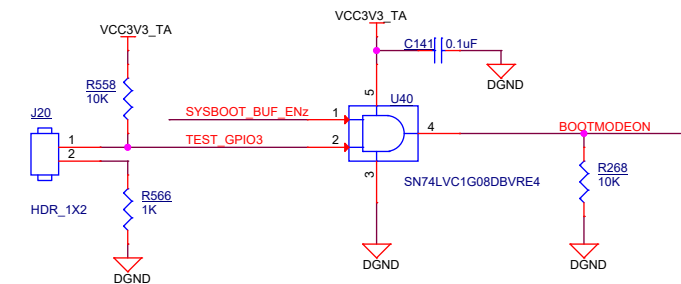
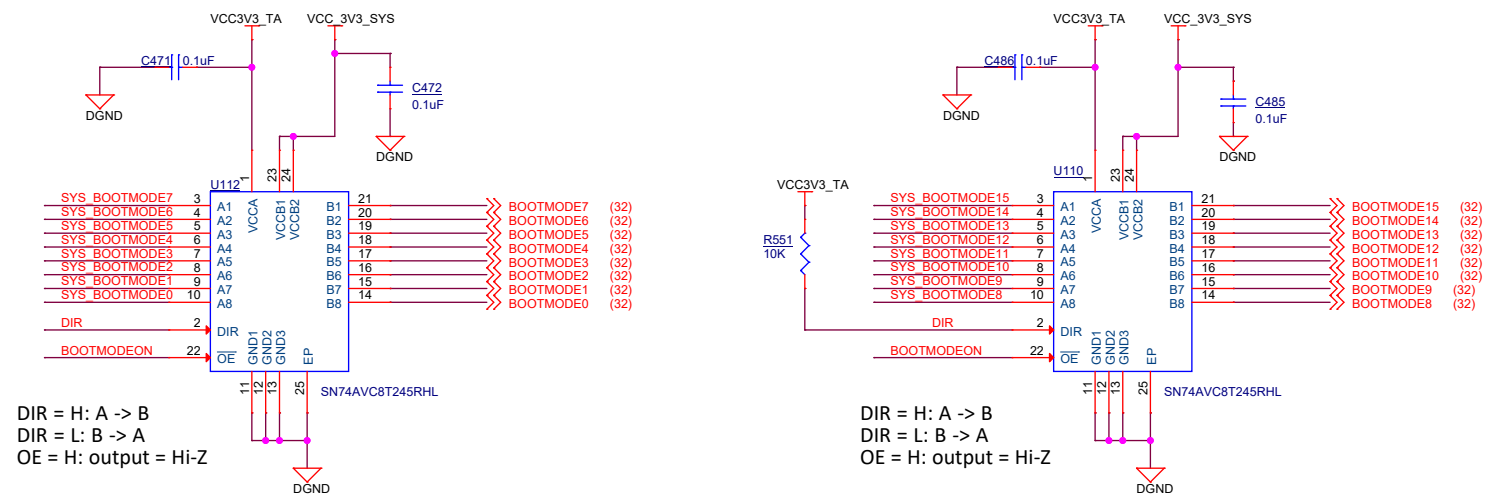
Date: Monday, June 26, 2023

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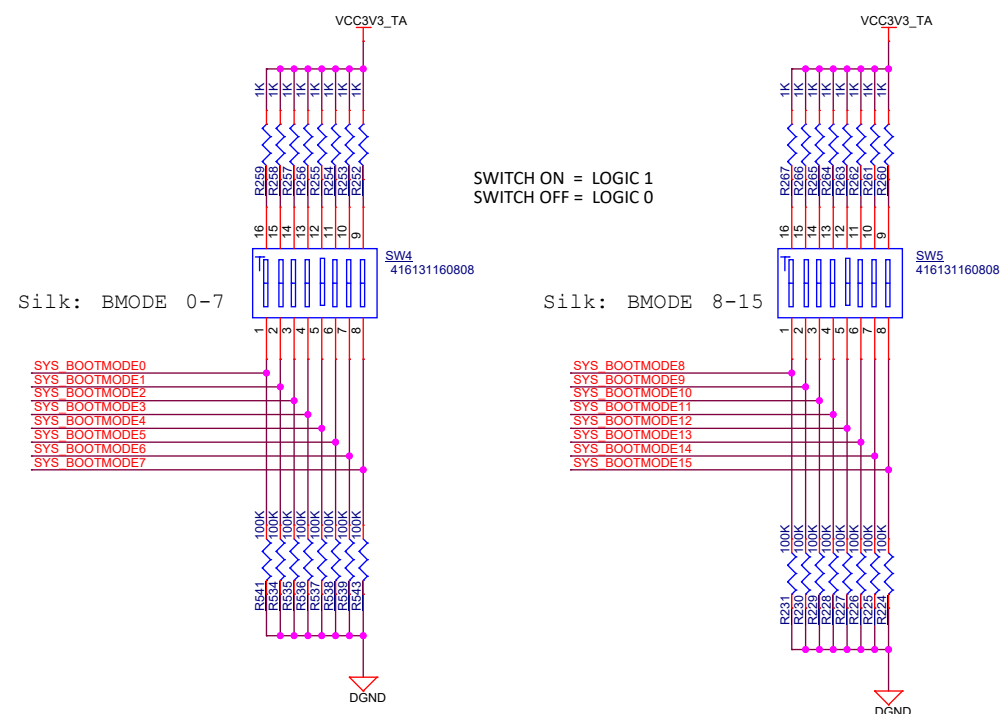
## BOOTMODE IO EXPANDER



## BOOT MODE BUFFERS



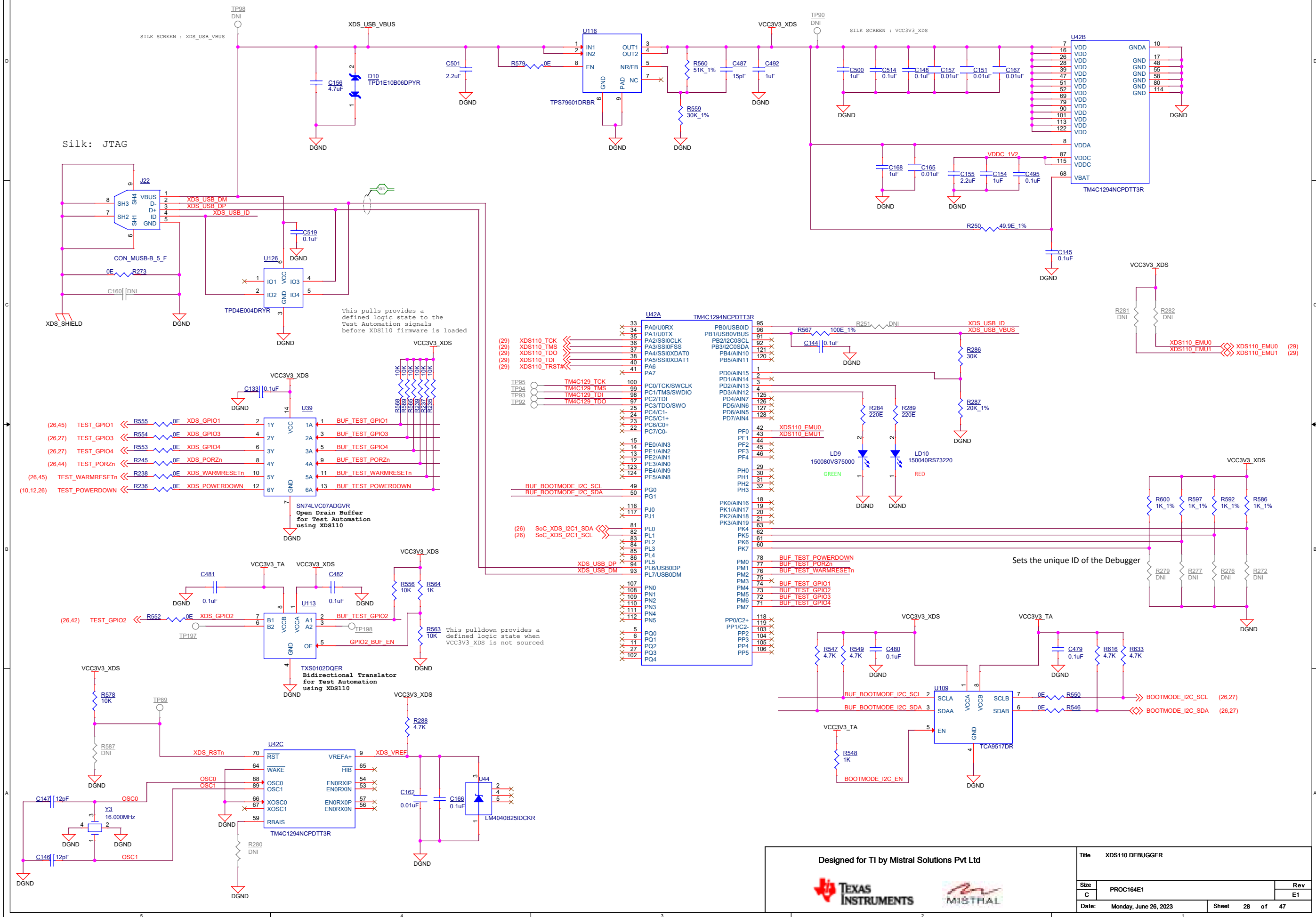
## BOOT MODE SWITCHES



## BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

# XDS110 DEBUGGER



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Title XDS110 DEBUGGER

Size PROC164E1

C

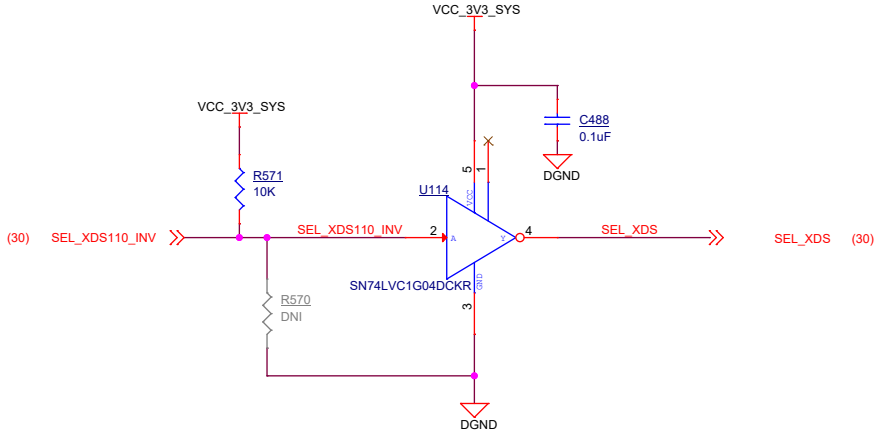
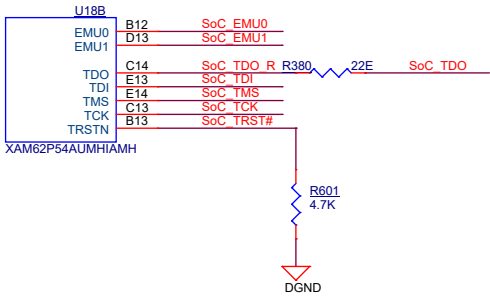
Date: Monday, June 26, 2023

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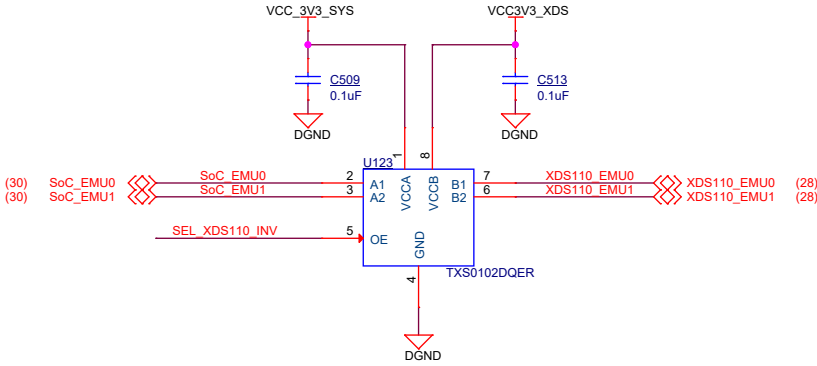
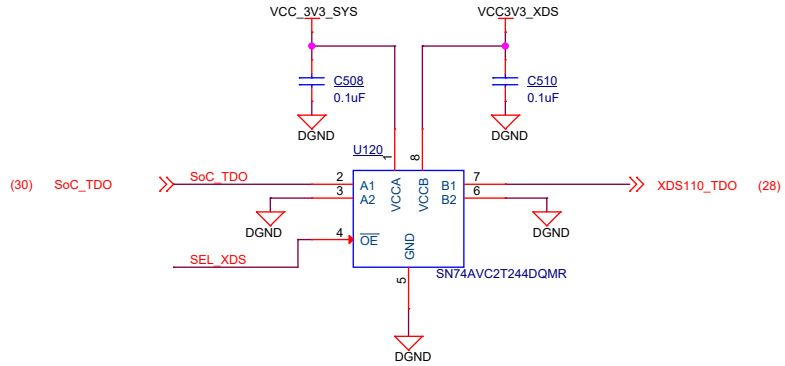
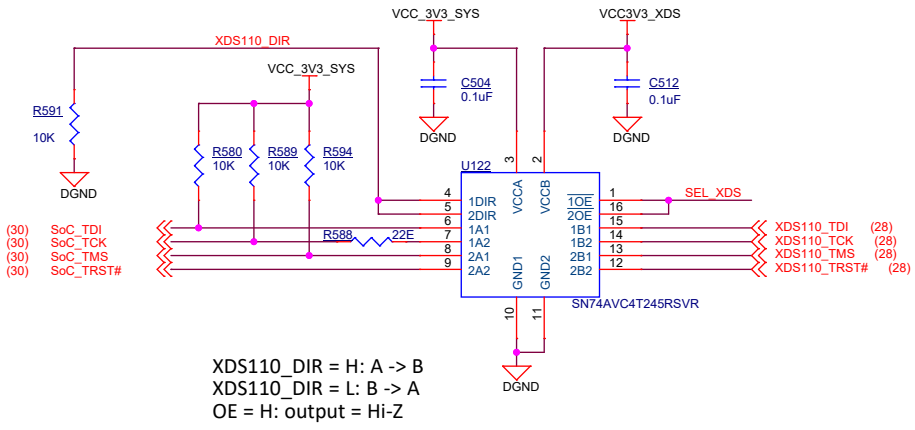
Rev

E1

JTAG SOC SECTION



BUFFER XDS110



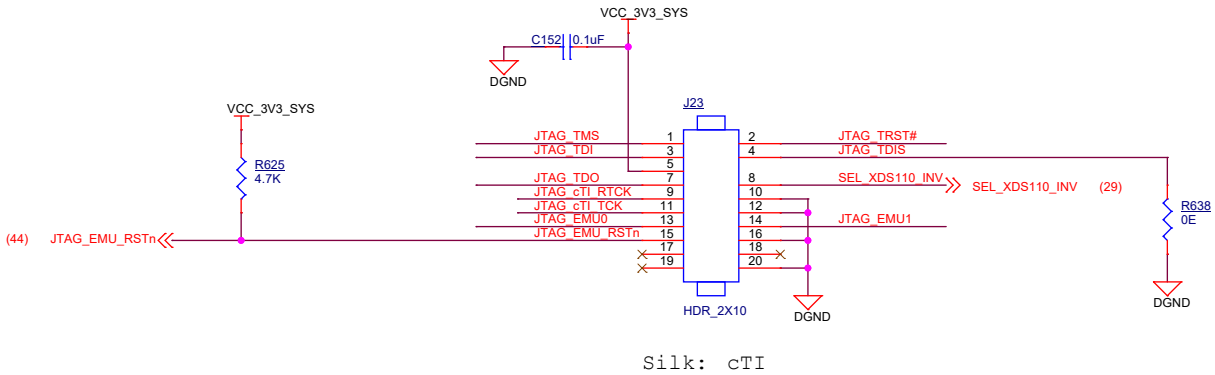
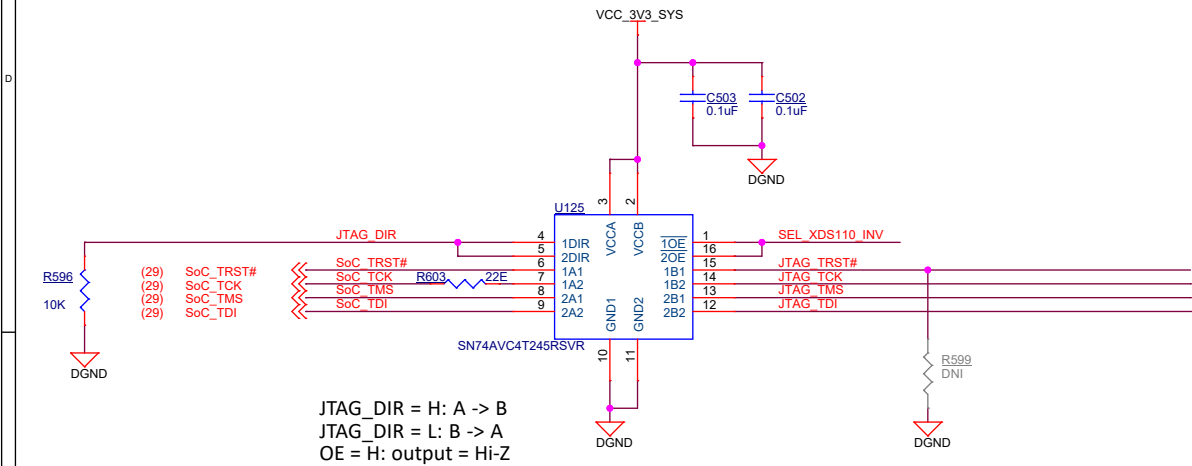
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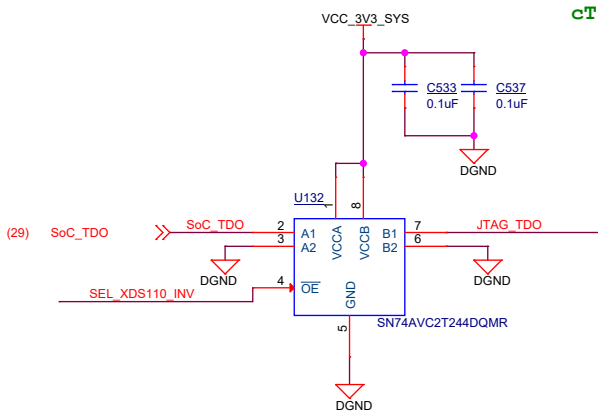
Title JTAG BUFFER		
Size	PROC164E1	Rev
C		E1
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cTI20 JTAG BUFFERS

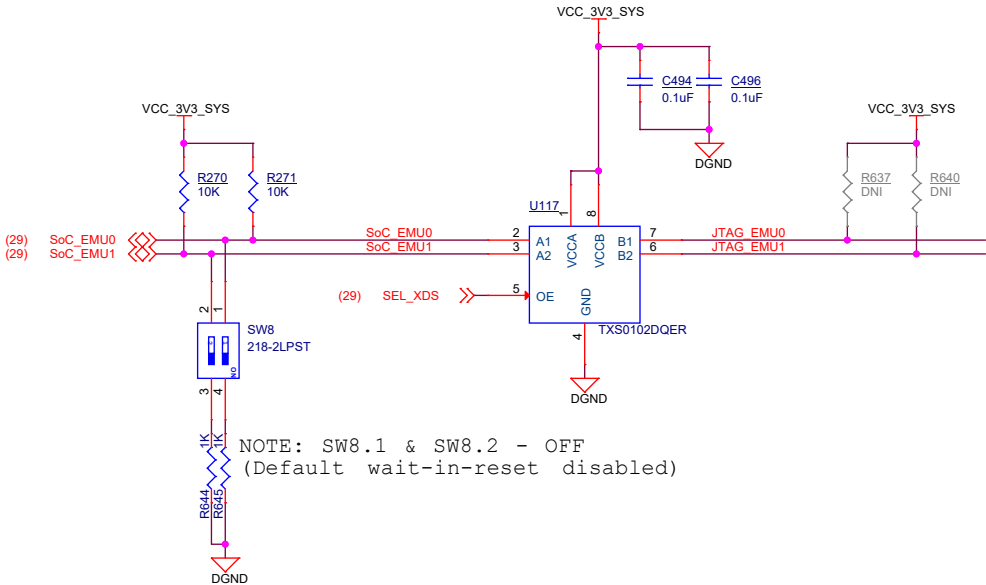
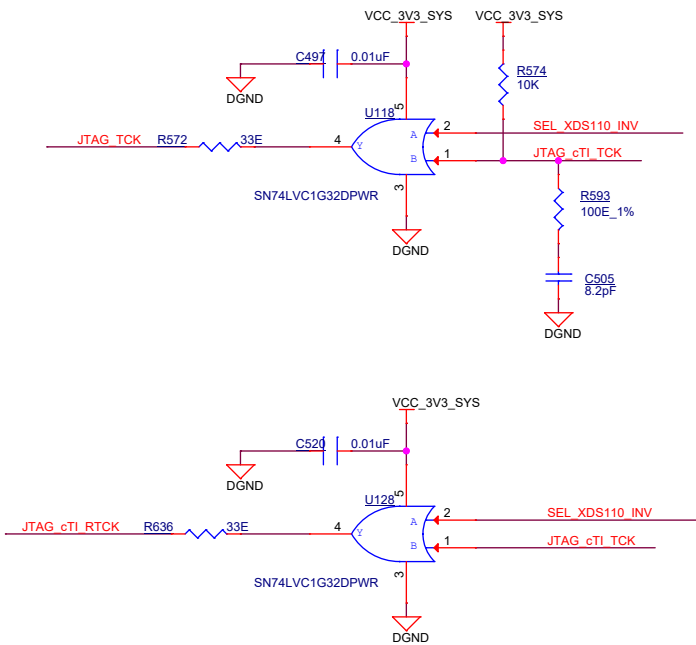
JTAG 20 PIN cTI CONNECTOR



CAD NOTE: Buffers U125 and U132 need to be placed closer to the cTI-20pin connector J23 to reduce Stub length of the JTAG signals.

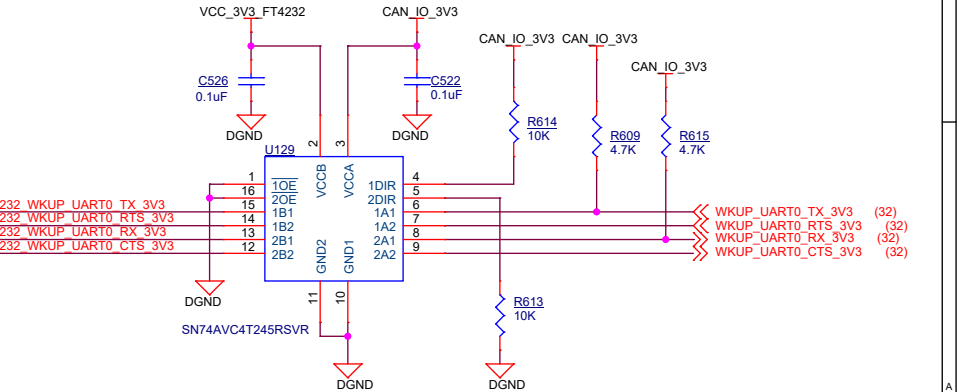
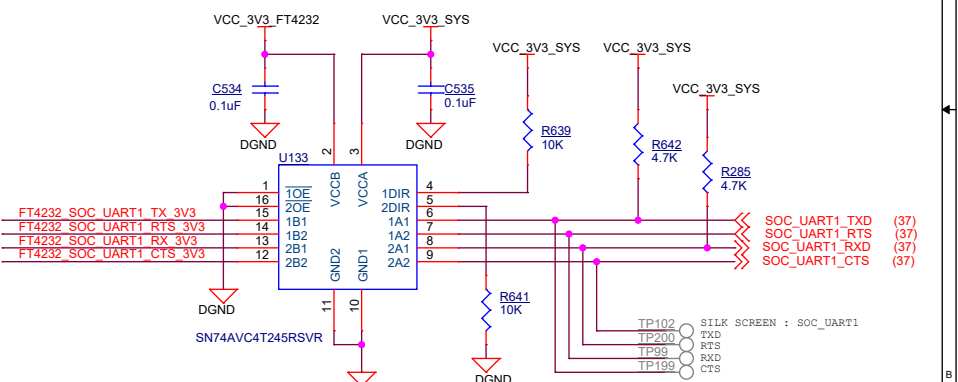
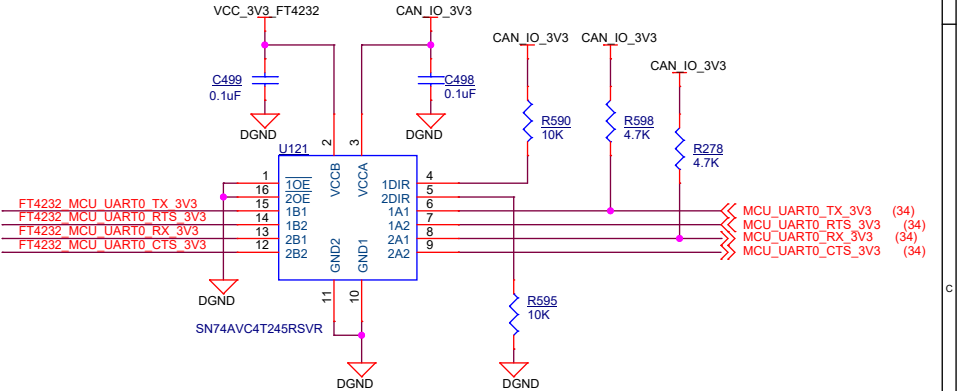
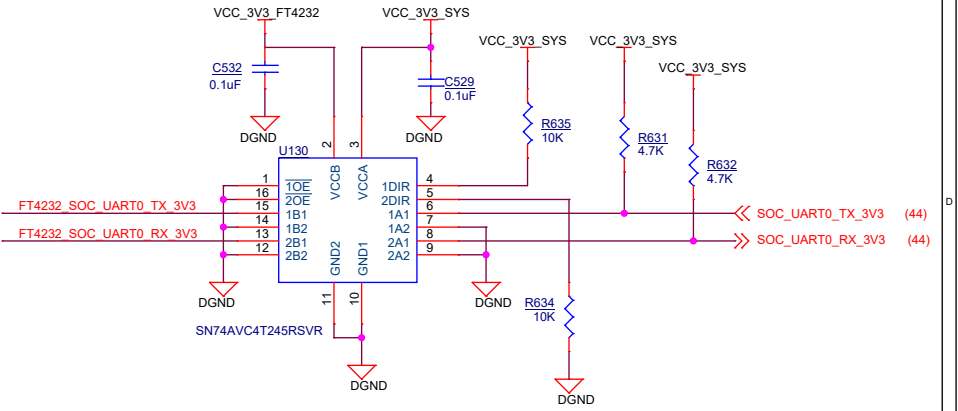
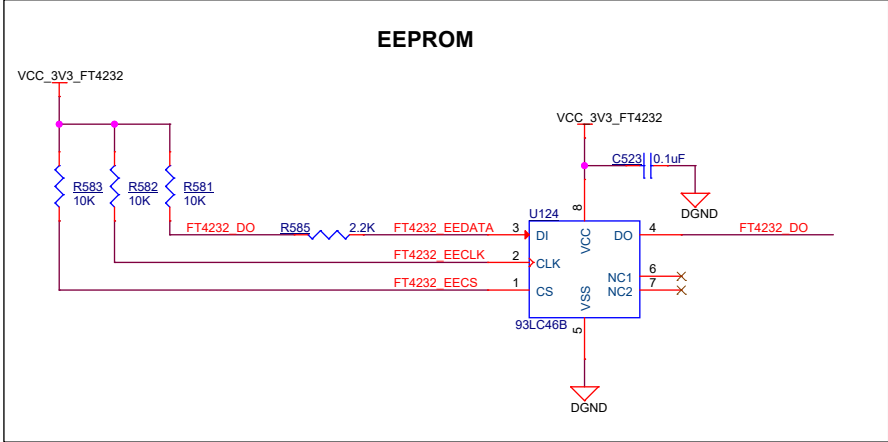
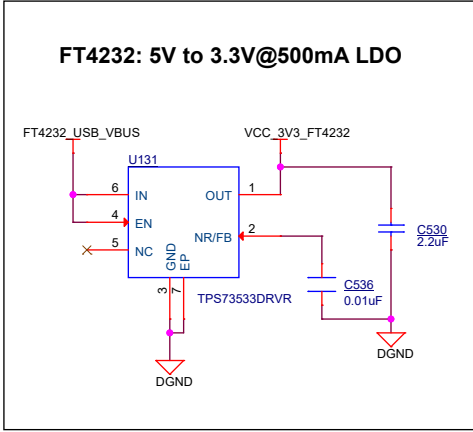
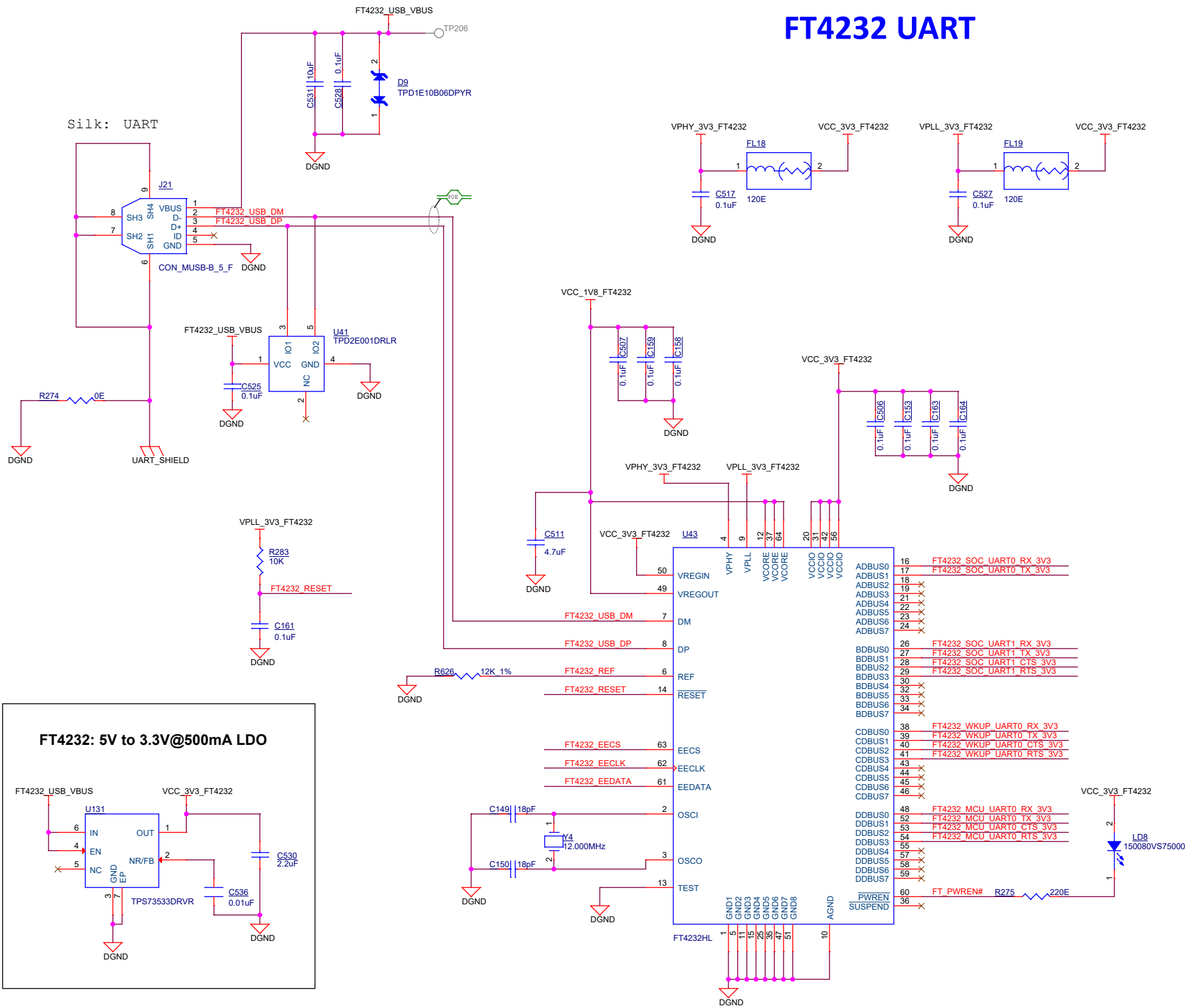


JTAG CLOCK BUFFER



NOTE: SW8.1 & SW8.2 - OFF (Default wait-in-reset disabled)

FT4232 UART

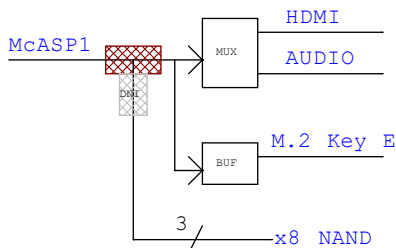
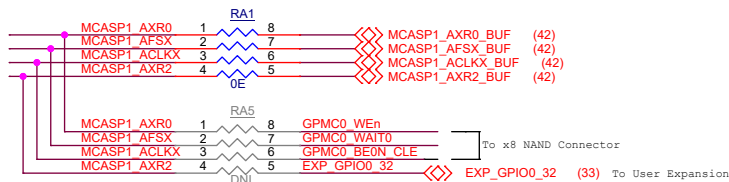
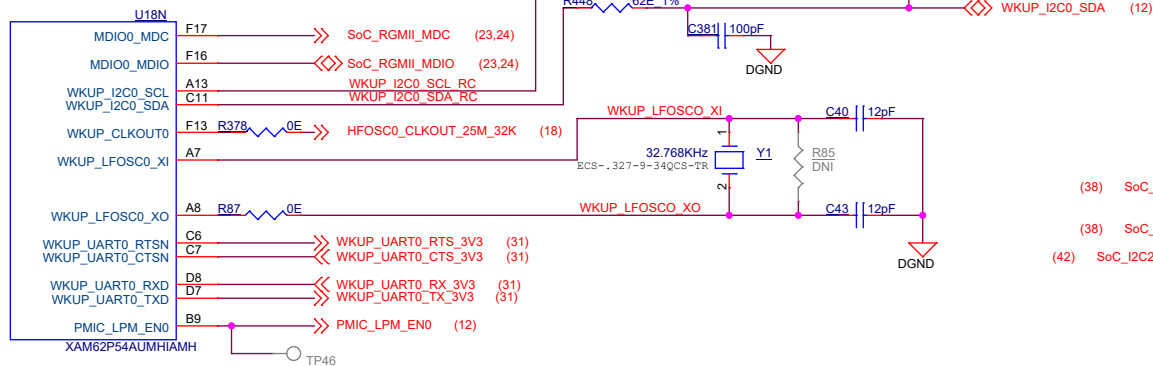


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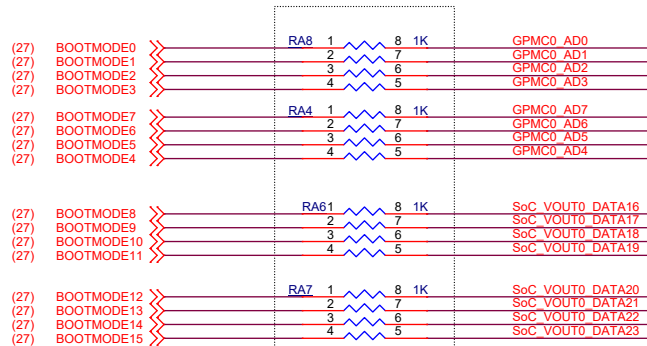


Title FT4232 UART TO USB BRIDGE		
Size	PROC164E1	Rev
C		E1
Date:	Monday, June 26, 2023	Sheet 31 of 47

## SOC WKUP DOMAIN

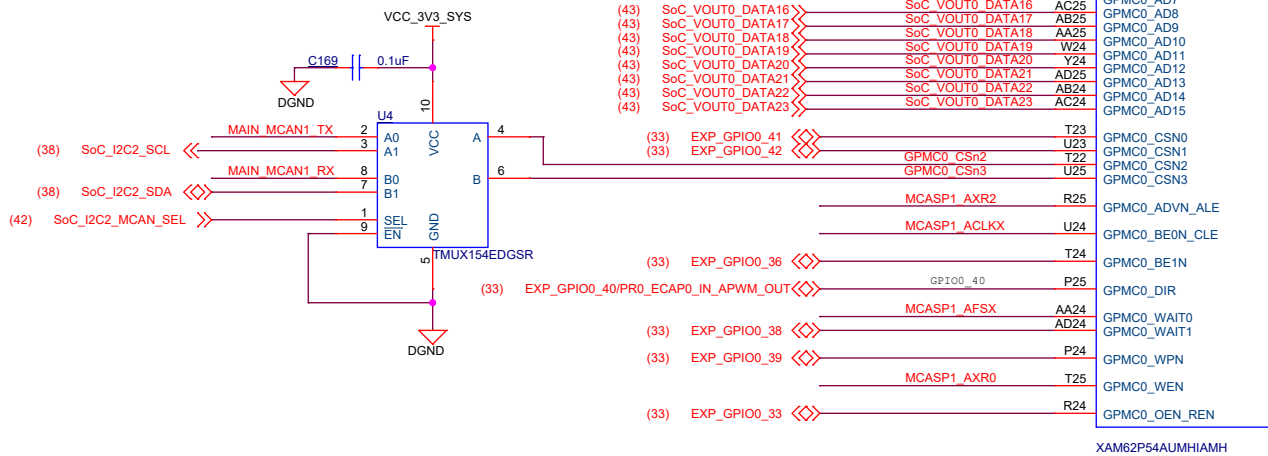


## BOOTMODE PINS

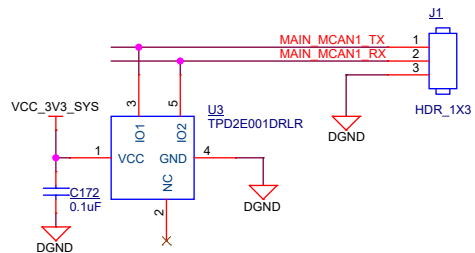


NOTE: 1K Resistors are used to isolate the BOOTMODE control logic after the value is latched

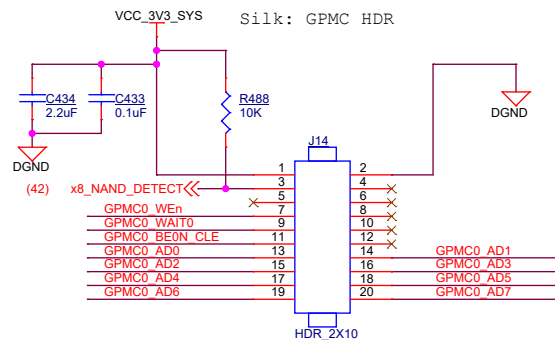
## SOC GPMC



## MCAN1 HDR



## GPMC NAND (x8)



NOTE: J4, J11 & J14 will be used together when plugging in GPMC NAND (x8) Board

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Title SOC WKUP & GPMC

Size PROC164E1

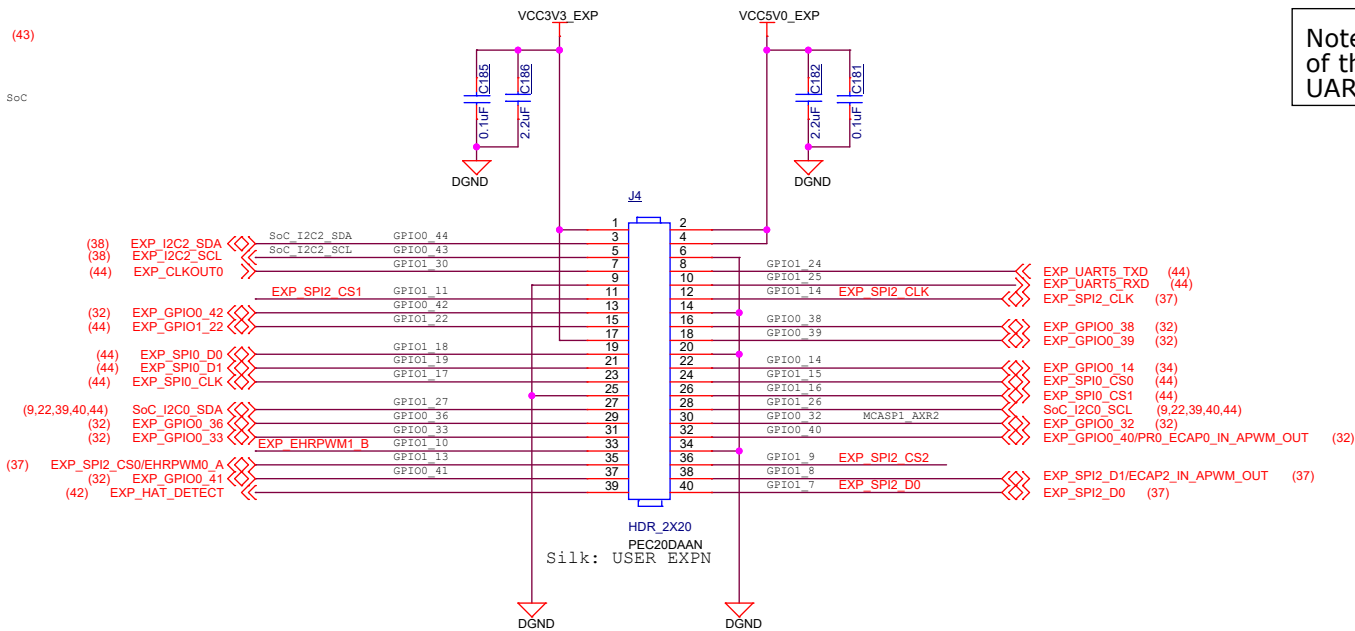
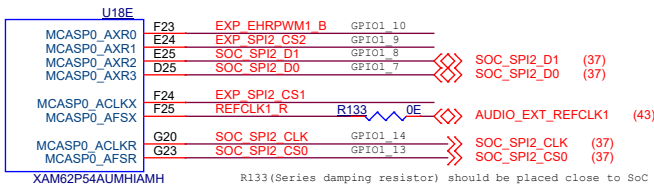
Rev E1

Date: Monday, June 26, 2023

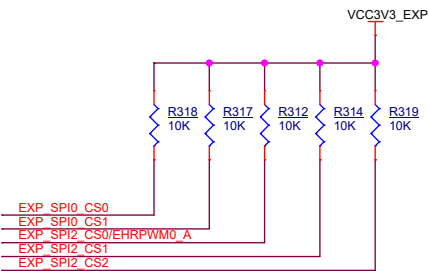
Sheet 32 of 47



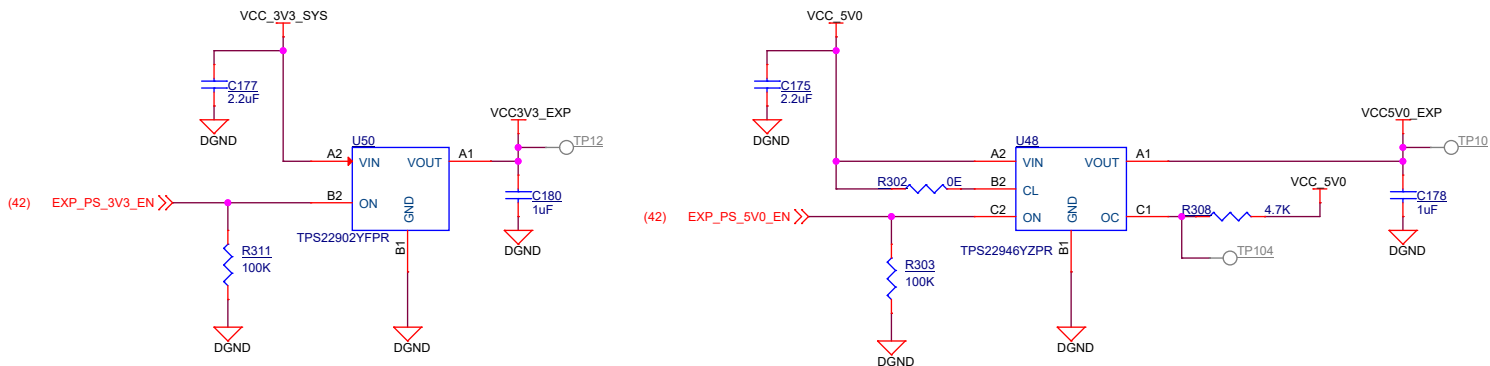
USER EXPANSION CONNECTOR



Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



POWER SWITCHES FOR USER EXPANSION CONNECTOR



NOTE:

AM62P Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62P Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

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Title USER EXPANSION CONNECTOR

Size PROC164E1

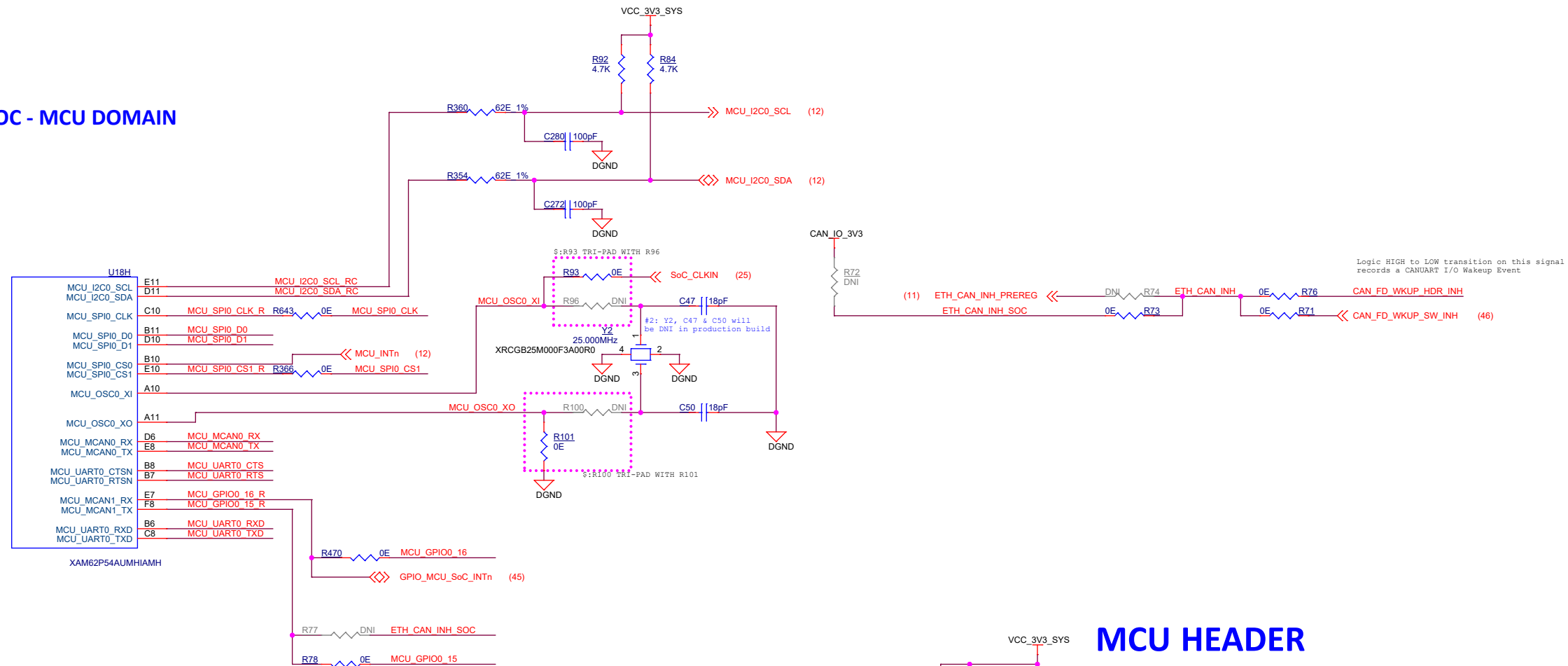
Rev

E1

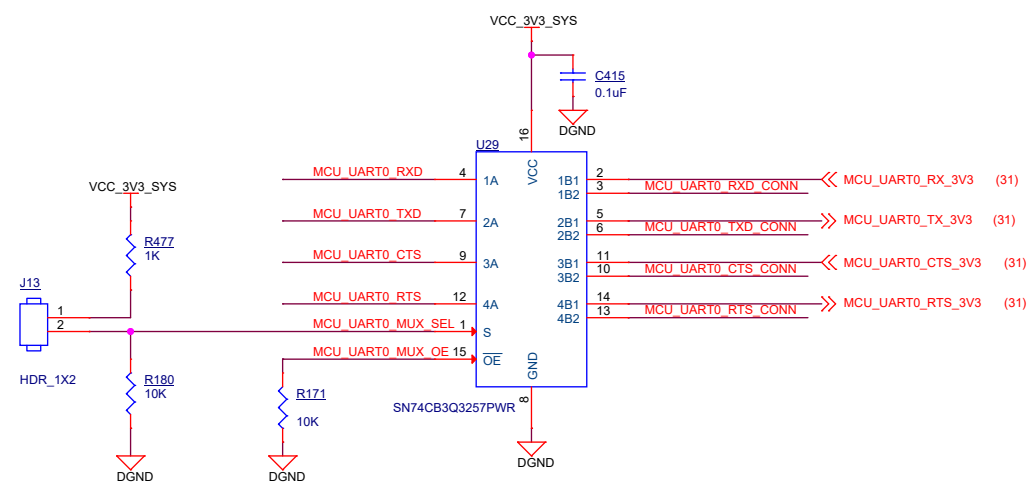
Date: Monday, June 26, 2023

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## SOC - MCU DOMAIN

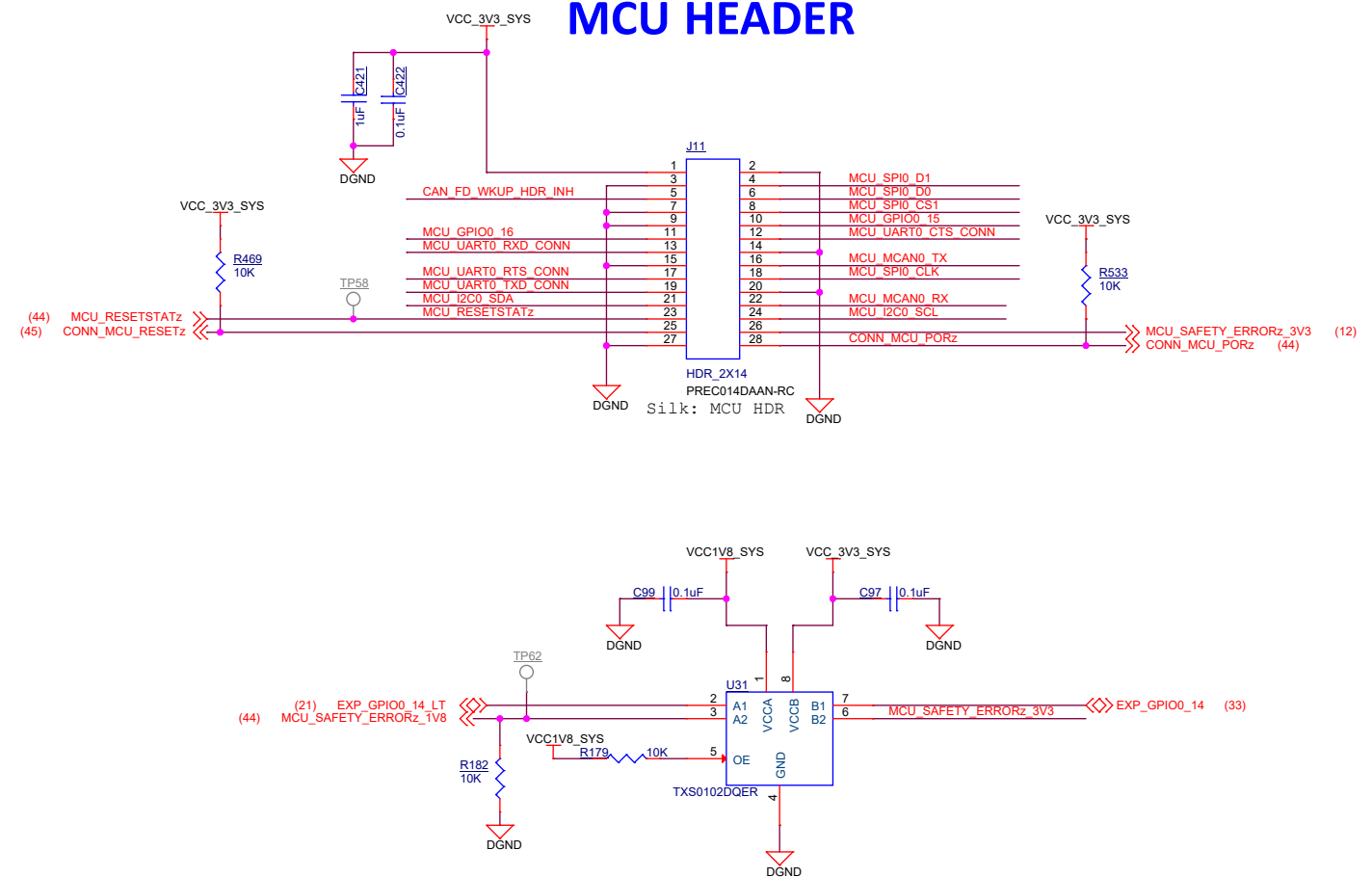


## SoC MCU UART0 FET SWITCH



OEn	SEL	INPUT/OUTPUT An	
L	L (DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

## MCU HEADER



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Title	MCU HEADER
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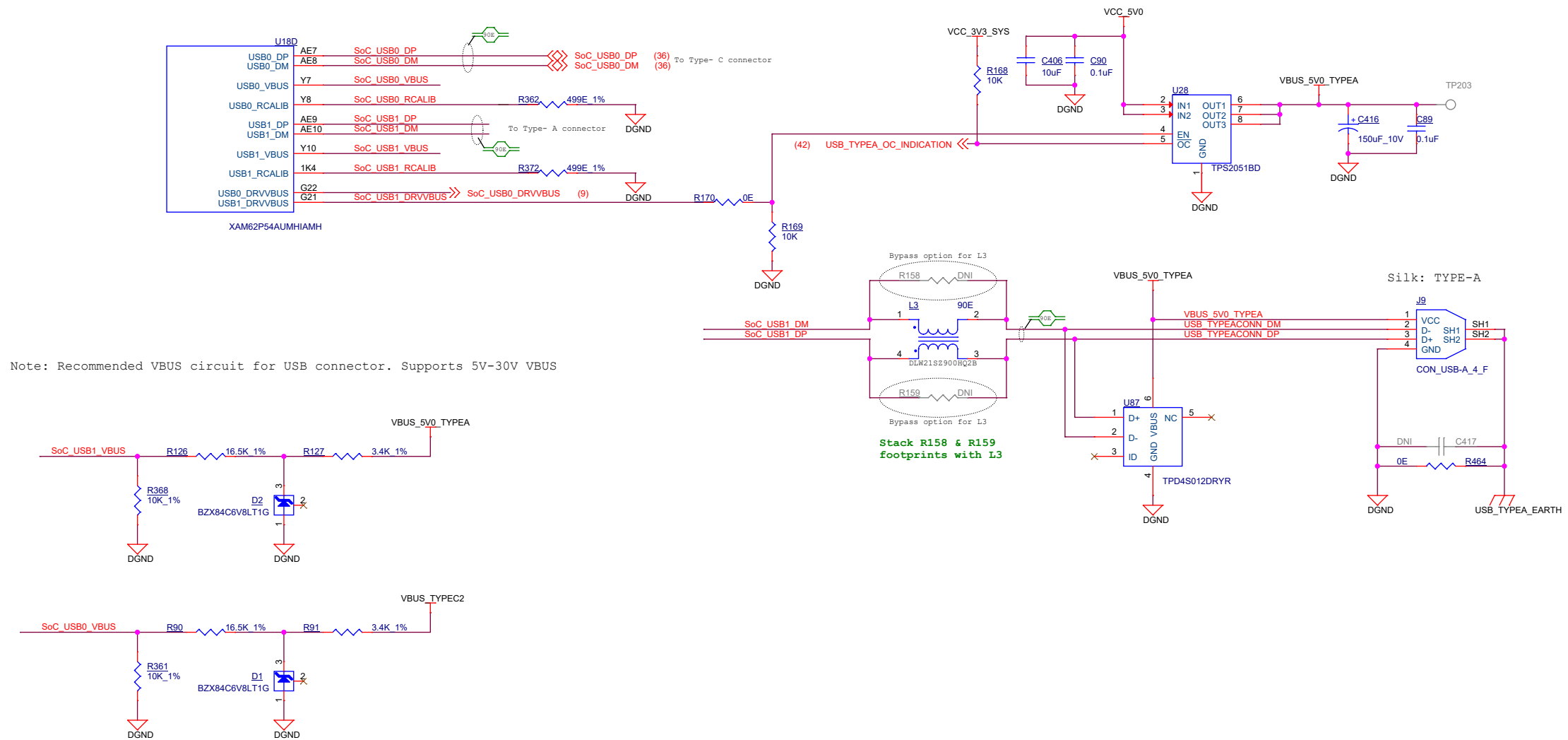
Size	PROC164E1
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C	PROJECT
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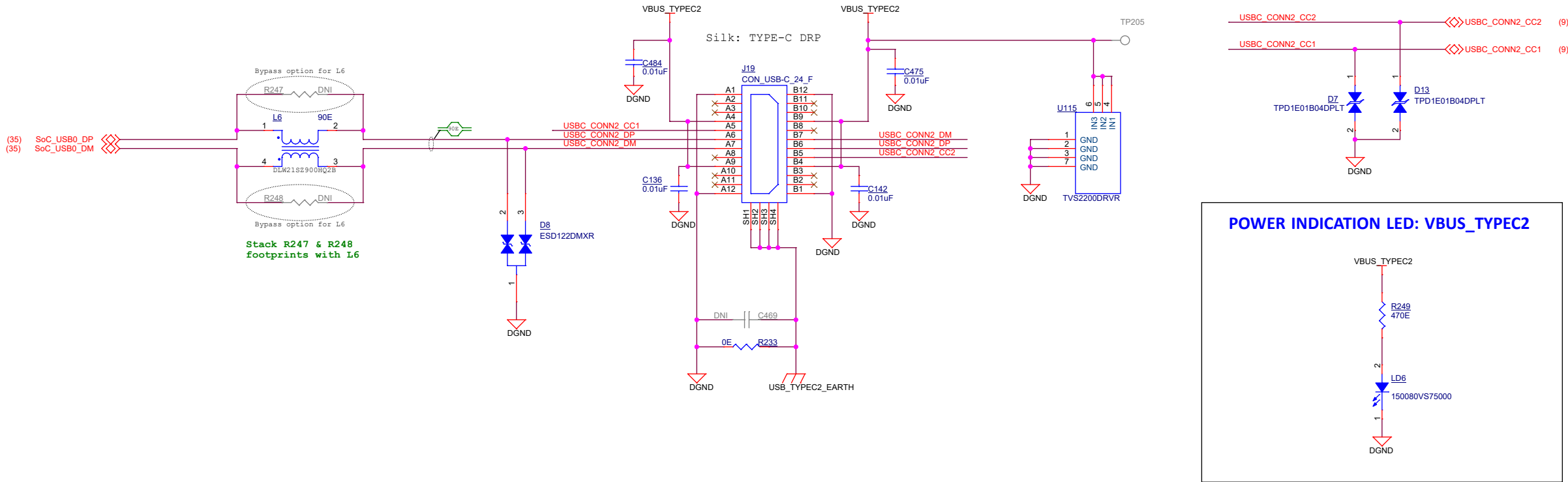
	Rev
--	-----

E1
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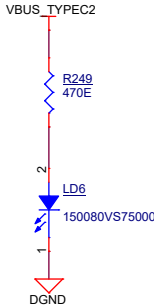
## USB1 TYPE-A



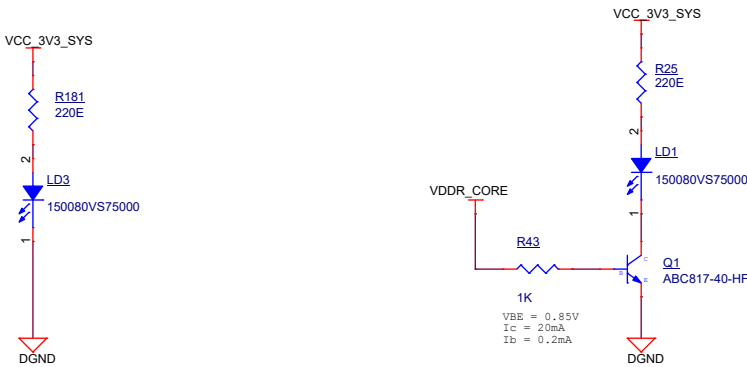
USB0 TYPE-C DRP



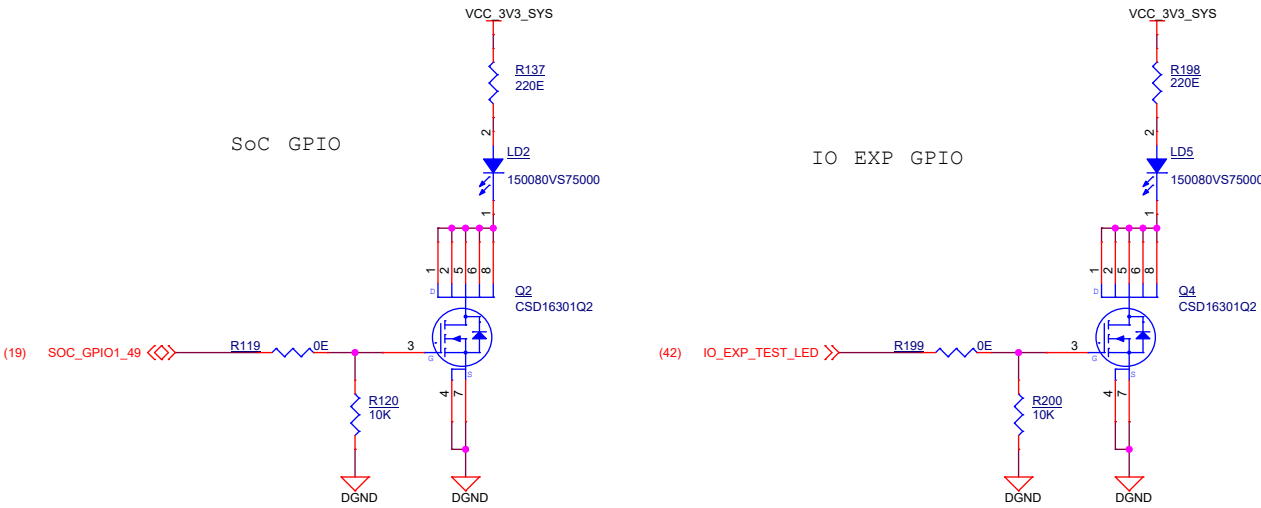
POWER INDICATION LED: VBUS\_TYPEC2



POWER RAIL LEDS



USER TEST LEDS



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Title USB0 TYPE-C DRP & USER TEST LED

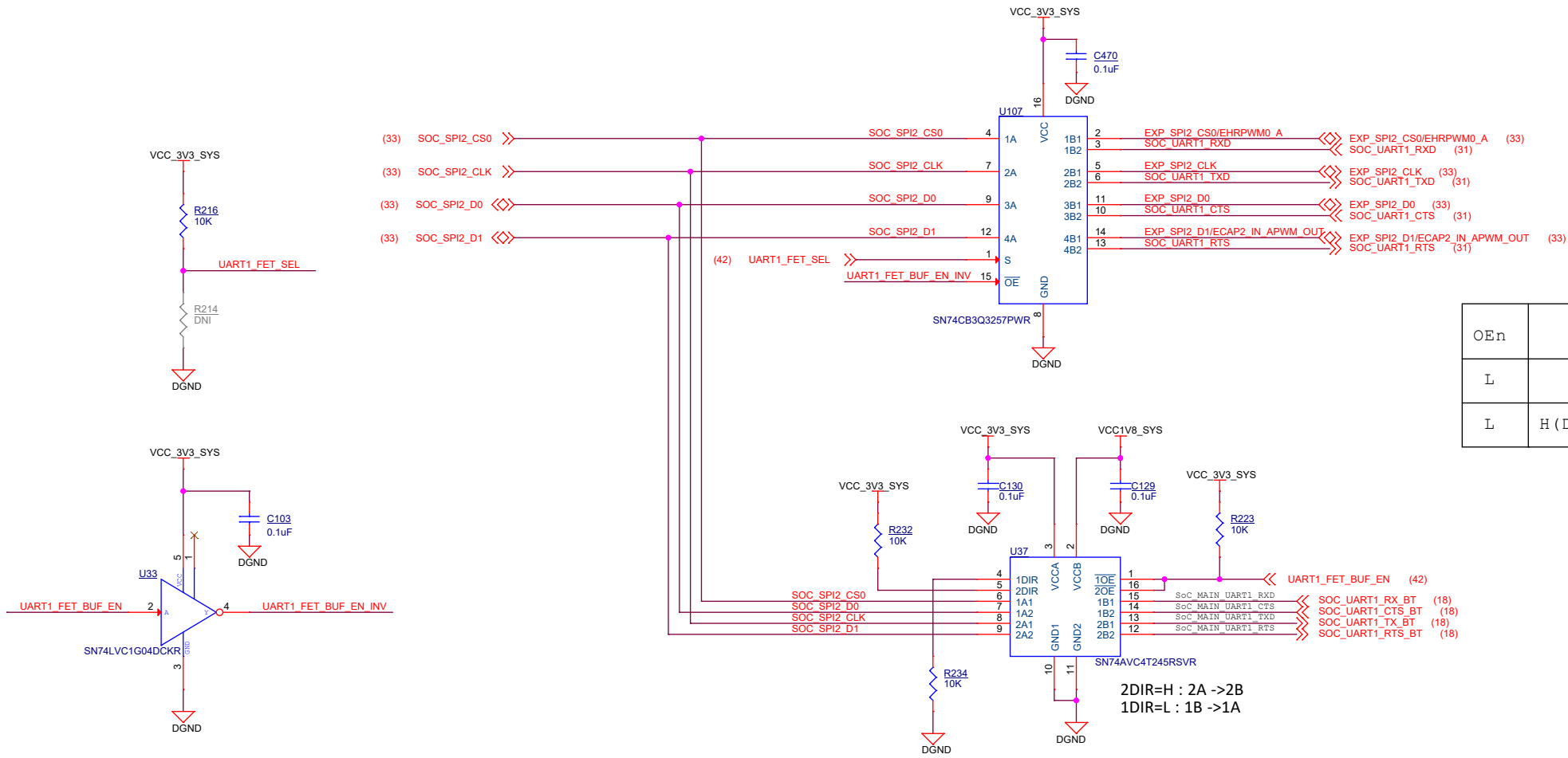
Size PROC164E1

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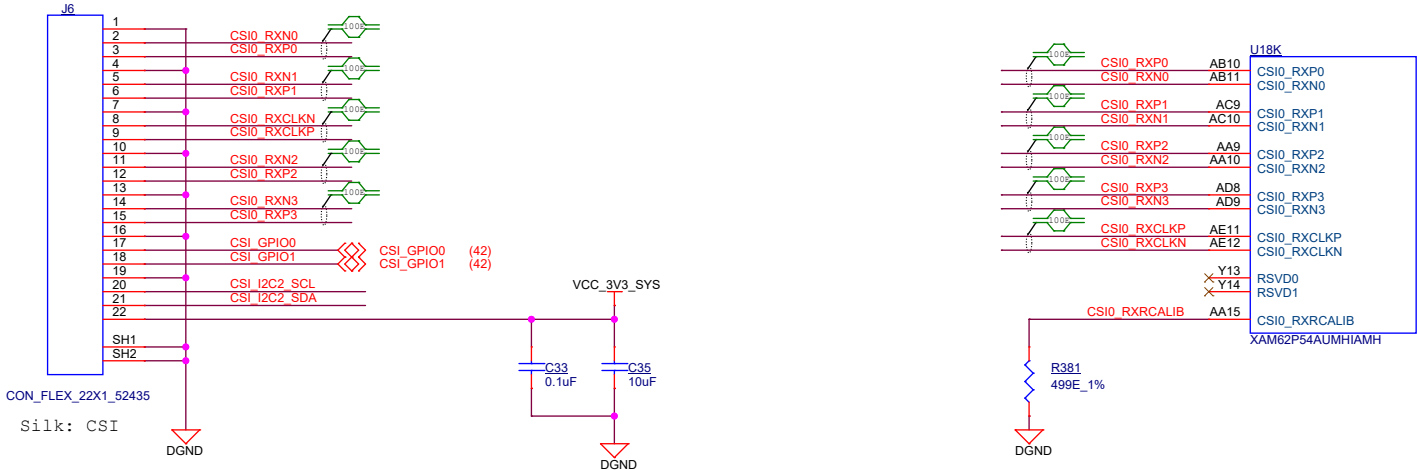
SoC UART1 FET SWITCH & BUFFER



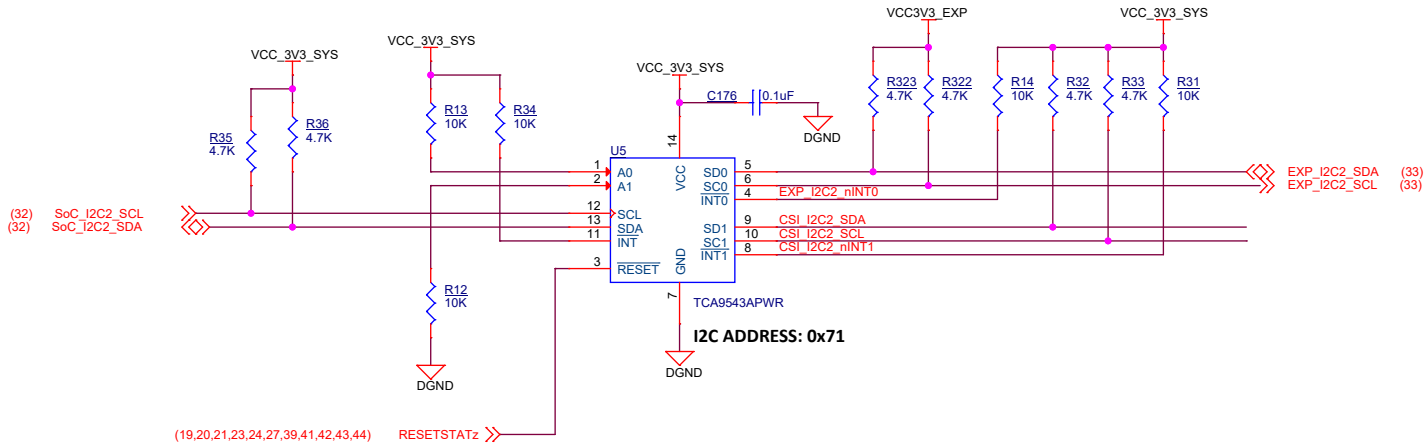
OEn	SEL	INPUT/OUTPUT	
		An	
L	L	An=nB1	SOC - EXP CONN
L	H (DEFAULT)	An=nB2	SOC - FT4232

2DIR=H : 2A ->2B  
1DIR=L : 1B ->1A

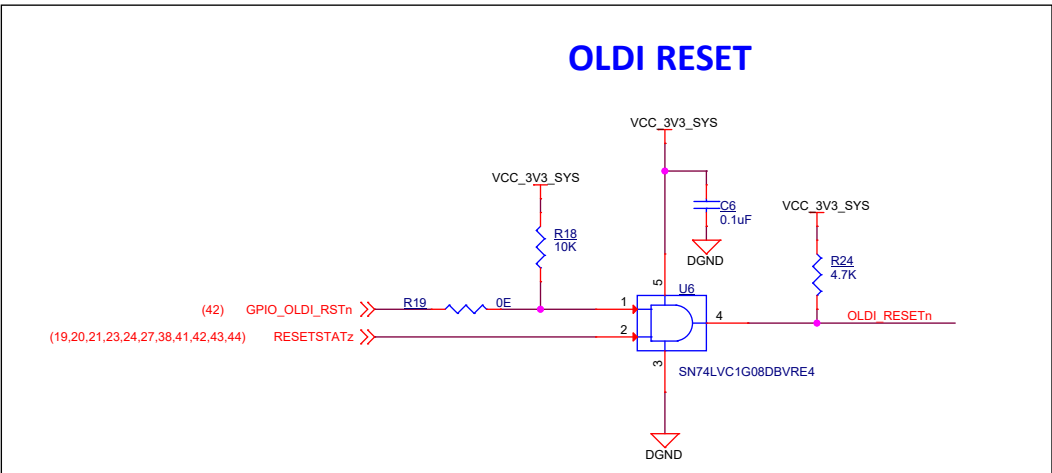
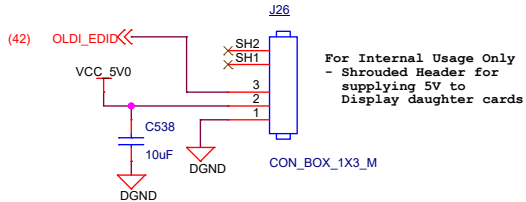
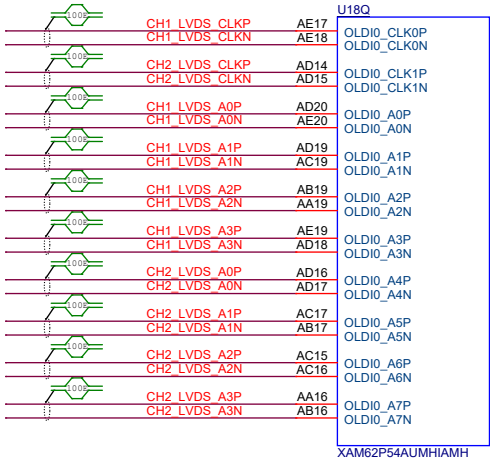
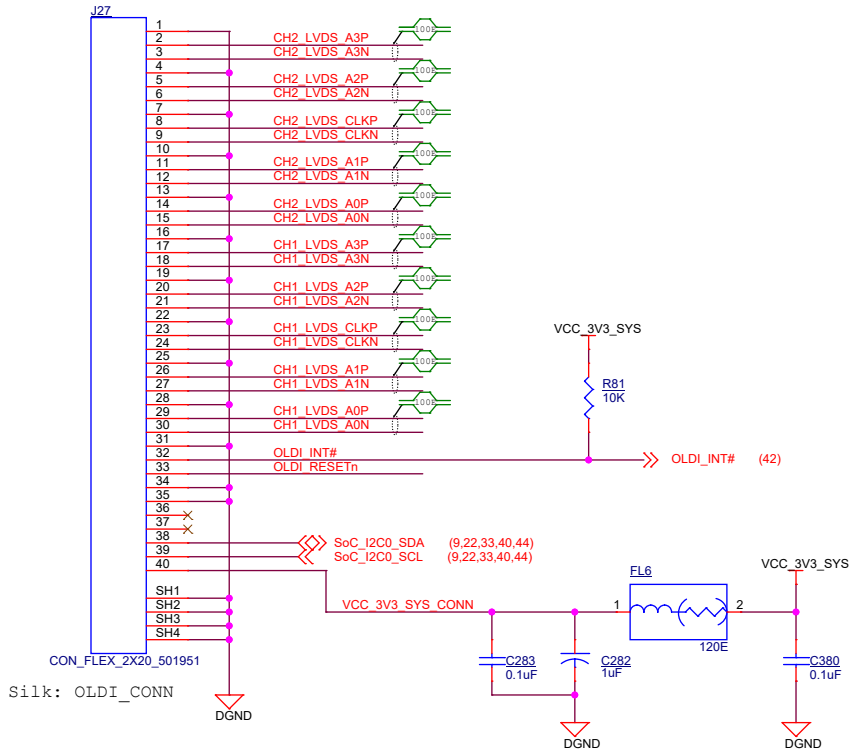
## CSI SECTION



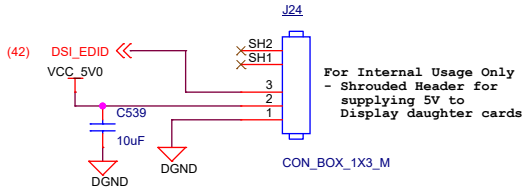
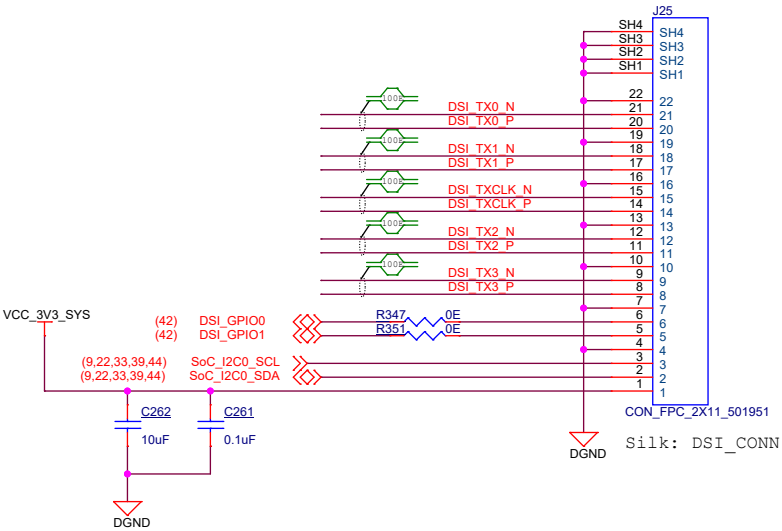
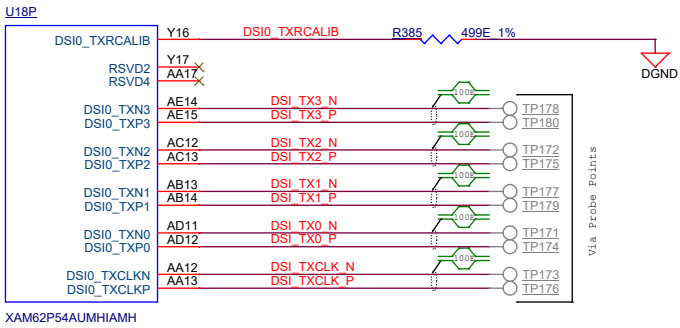
## I2C SWITCH FOR SoC\_I2C2



## OLDI SECTION

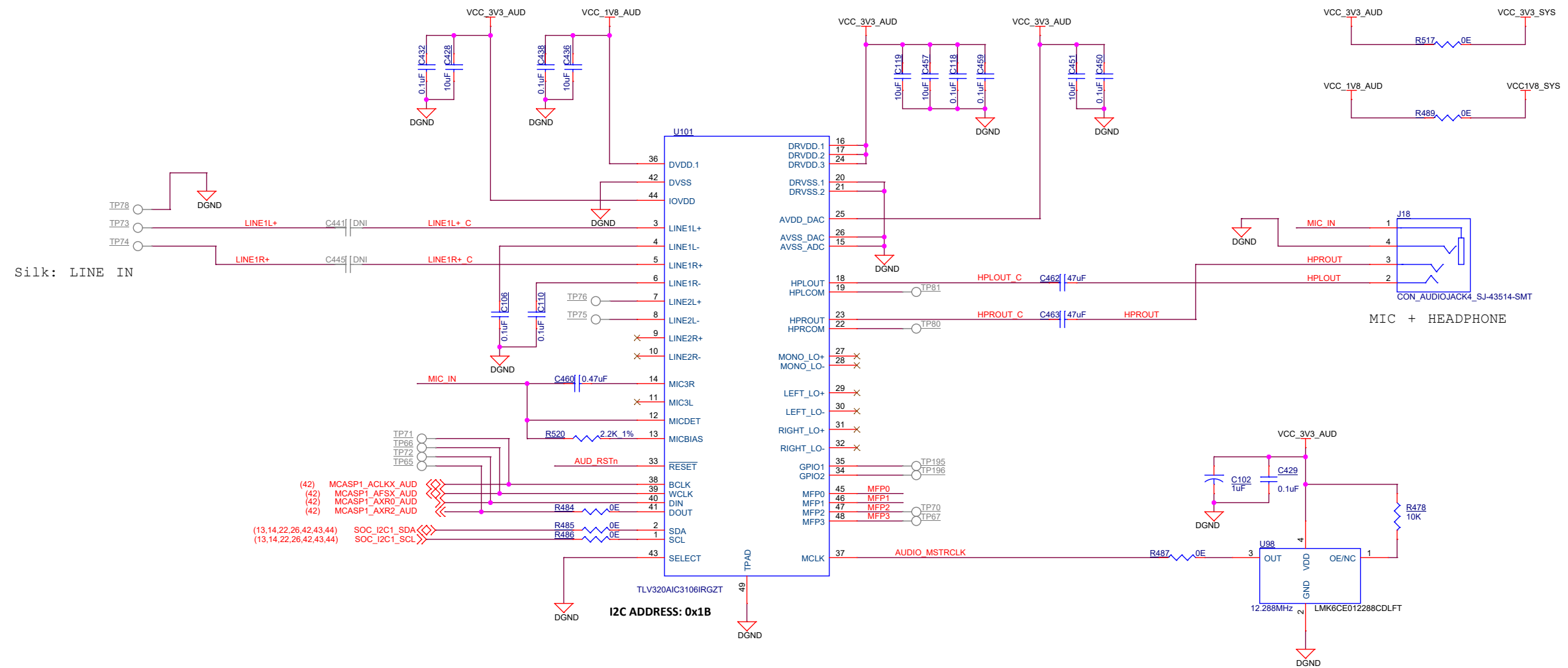


DSI SECTION

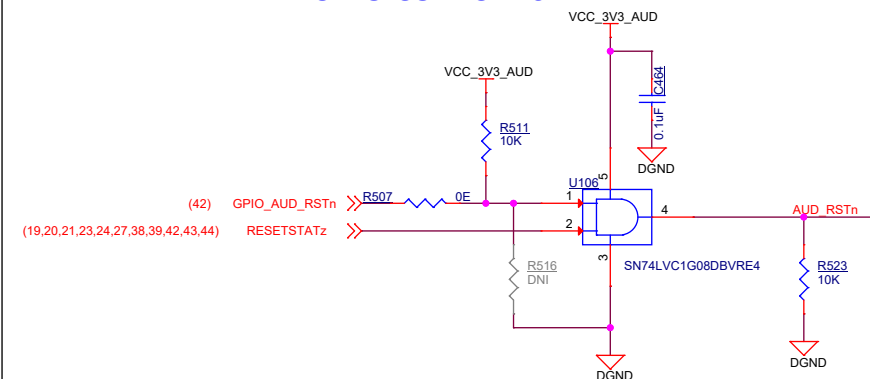




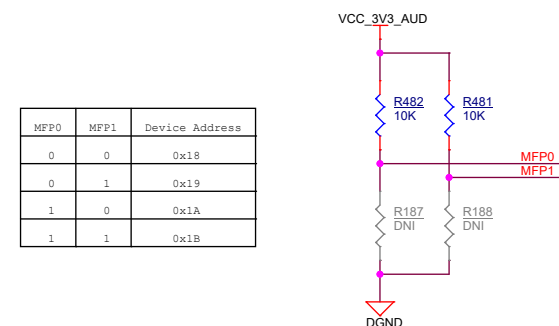
## AUDIO CODEC



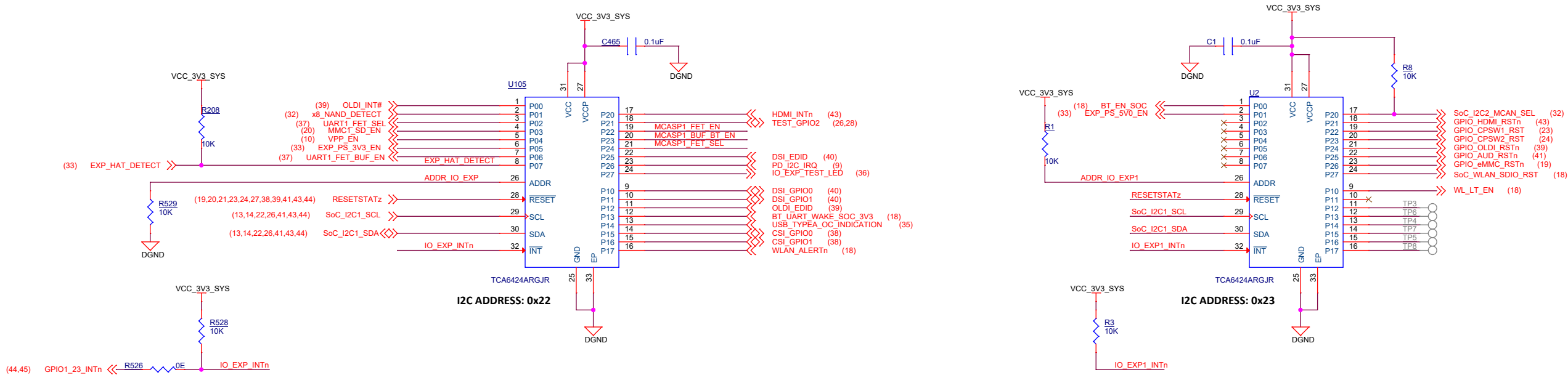
## AUDIO CODEC RESET



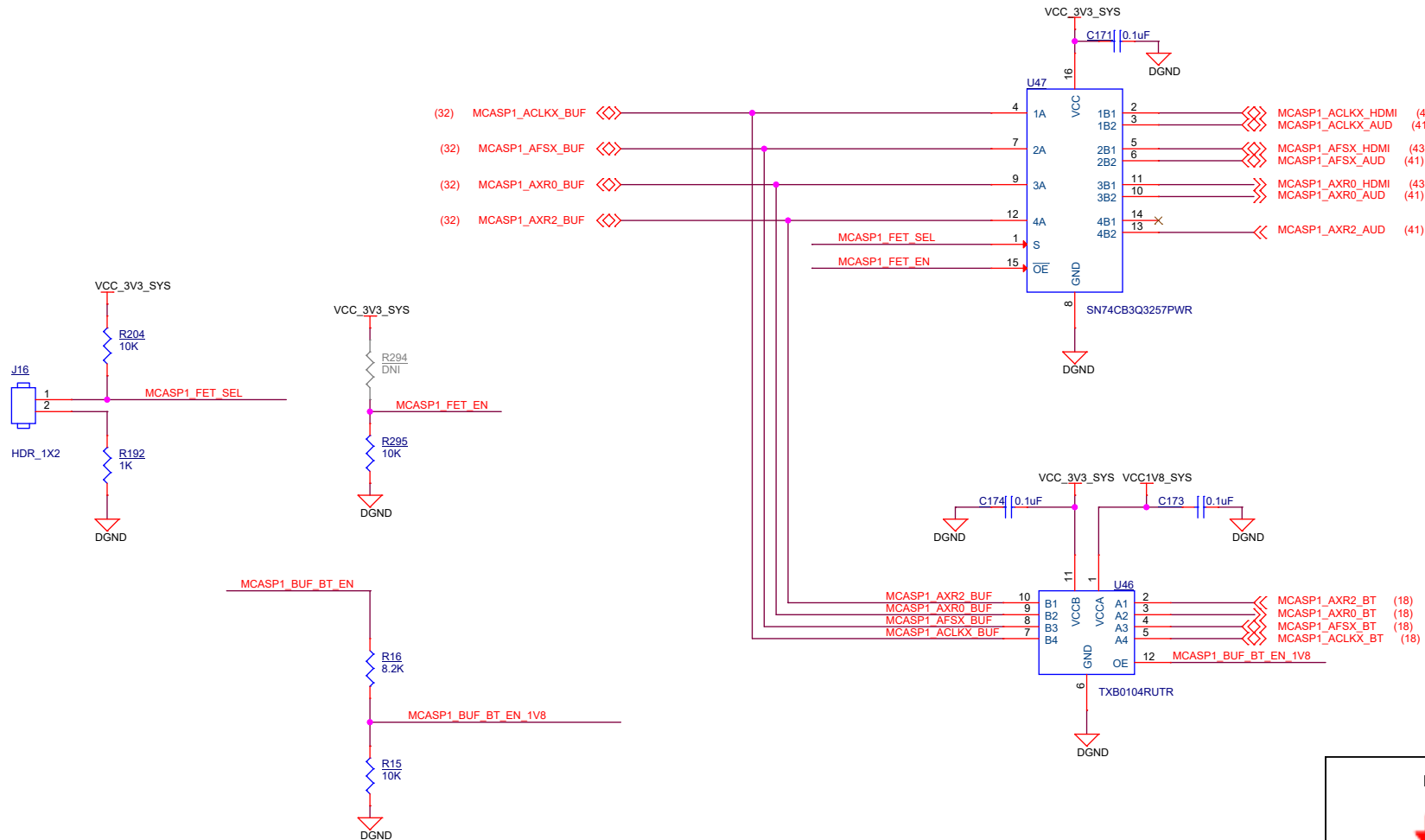
## CODEC I2C ADDRESS SELECTION



IO EXPANDER



McASP1 FET SWITCH & BUFFER



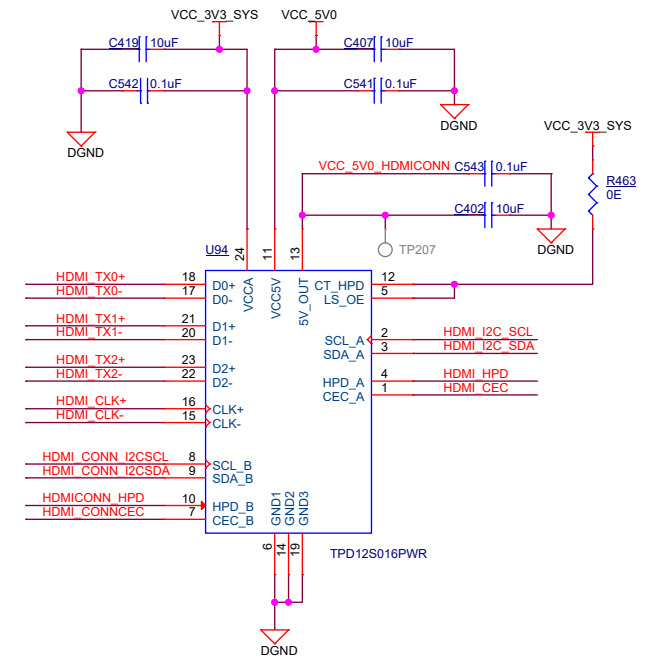
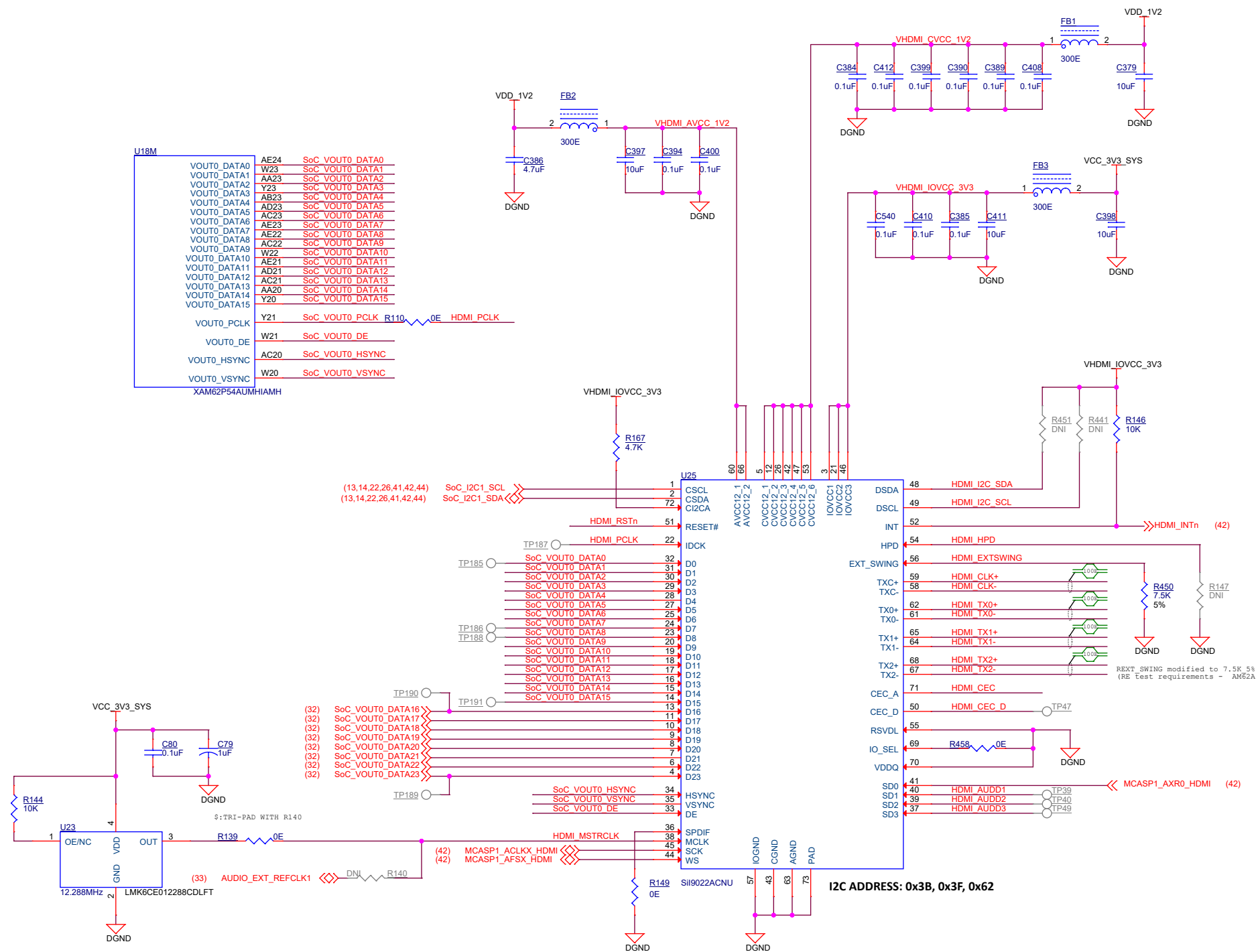
OEn	SEL	INPUT/OUTPUT	
		An=nB2	An
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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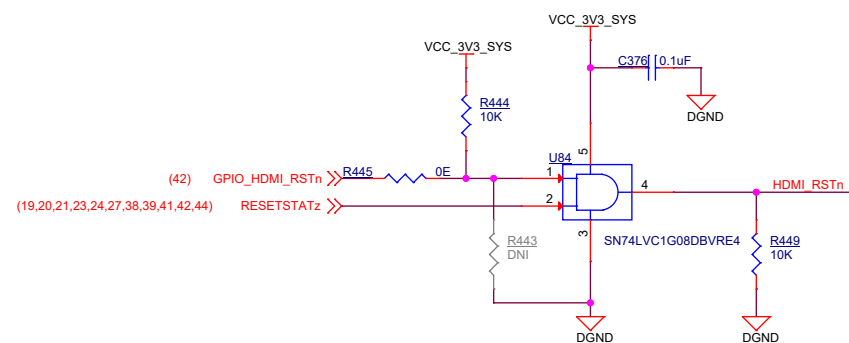
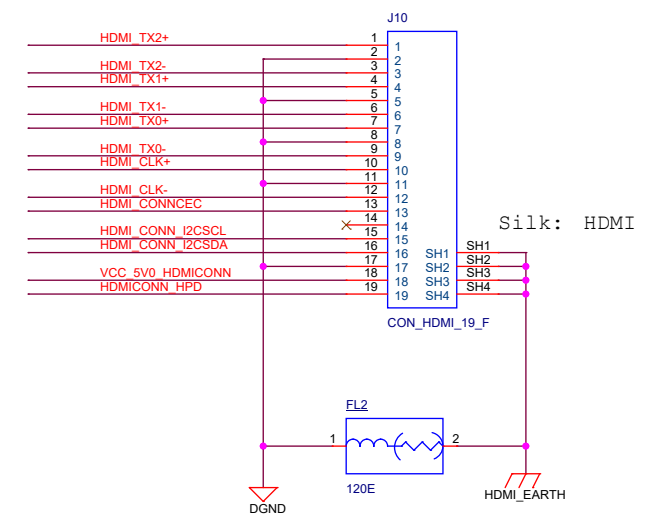


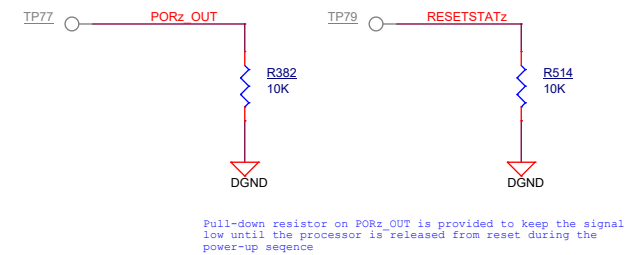
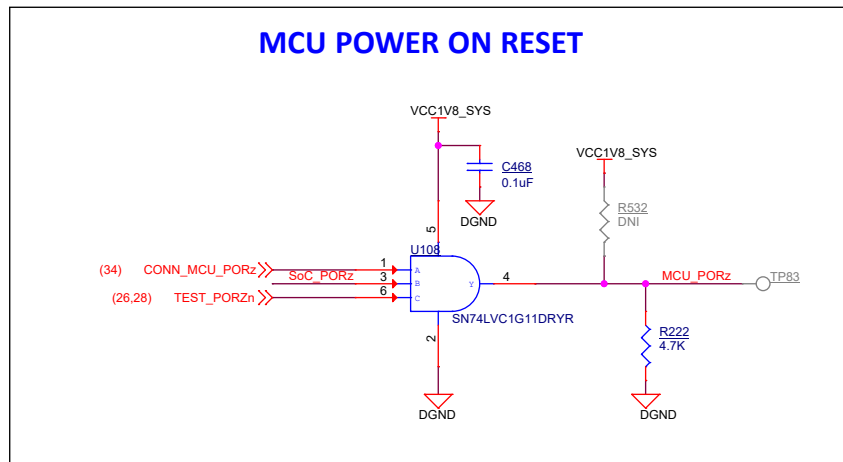
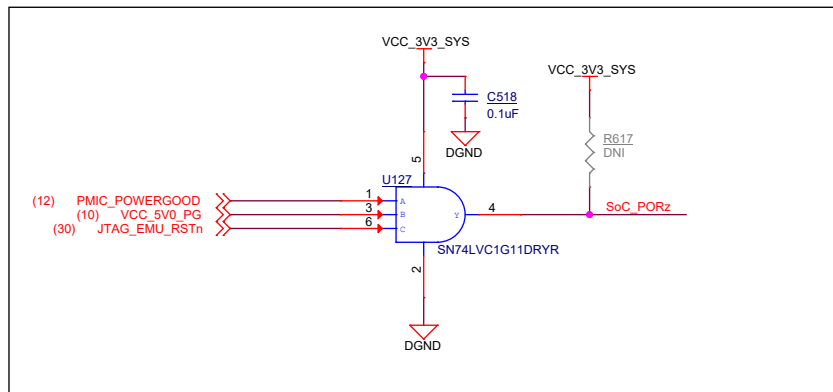
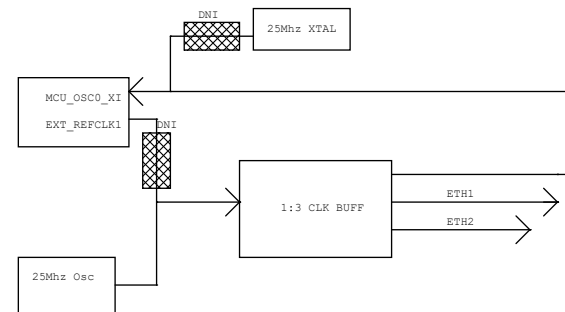
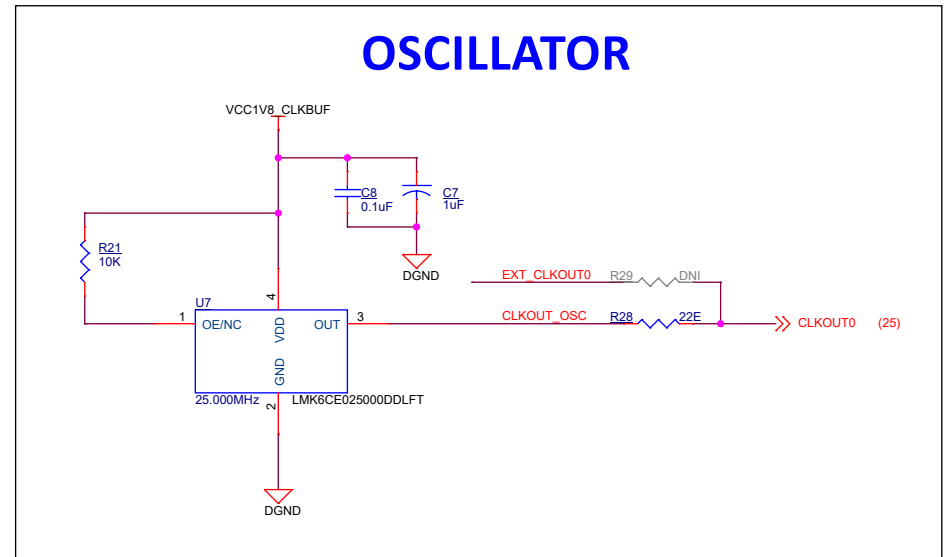
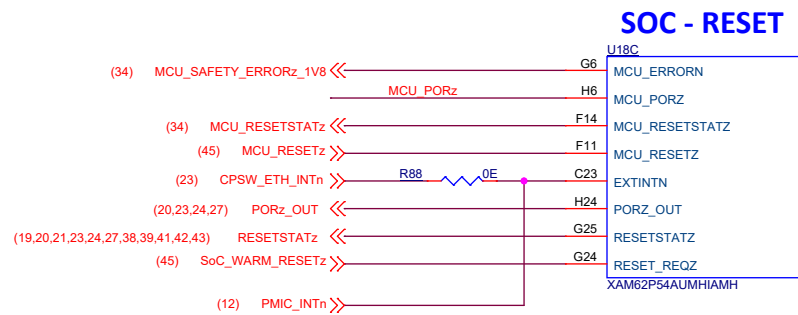
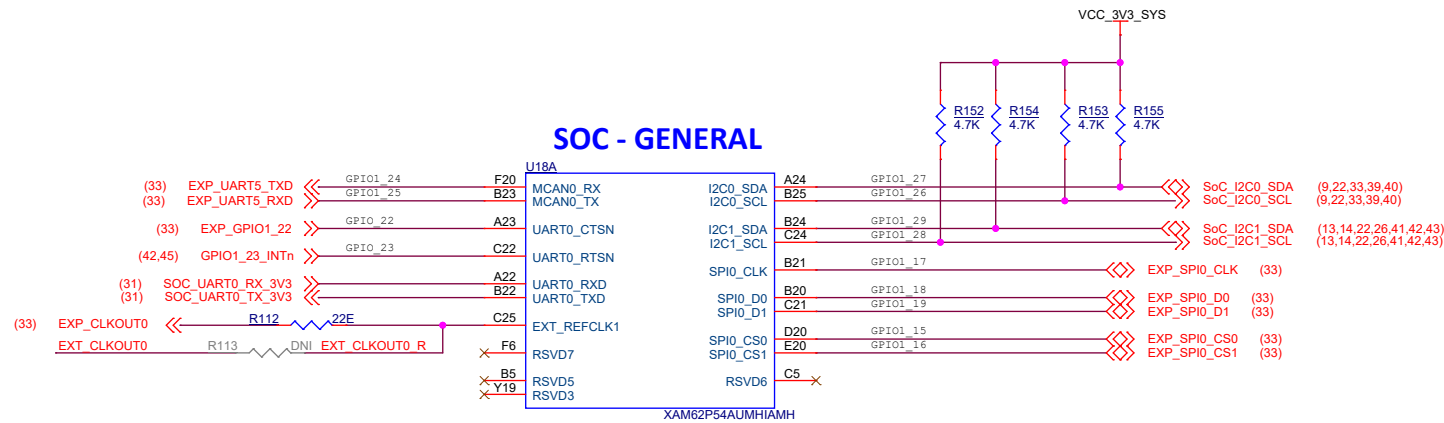
Title IO EXPANDER		
Size C	PROC164E1	Rev E1
Date: Monday, June 26, 2023	Sheet 42 of 47	

# HDMI INTERFACE



NOTE:  
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.





Full-down resistor on PORz\_OUT is provided to keep the signal low until the processor is released from reset during the power-up sequence

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Title OSCILLATOR

Size PROC164E1

C

Date: Monday, June 26, 2023

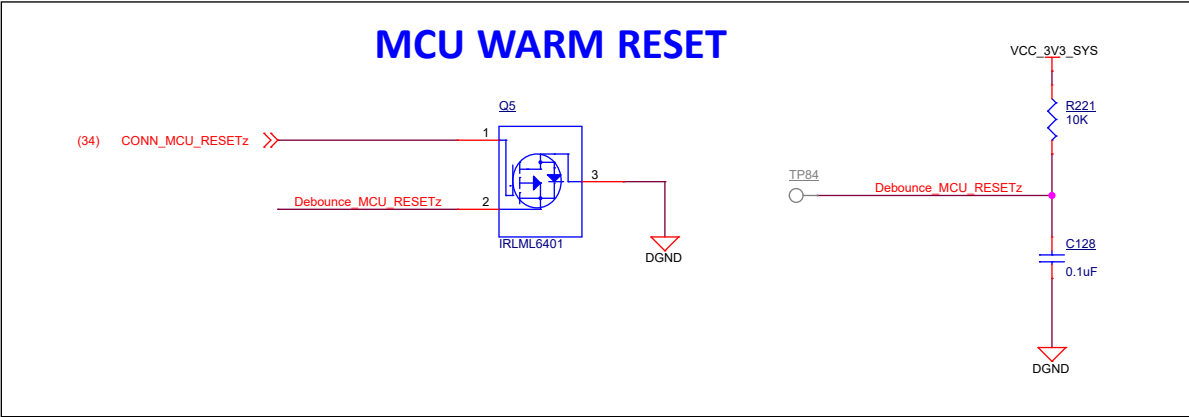
Sheet 44 of 47

Rev

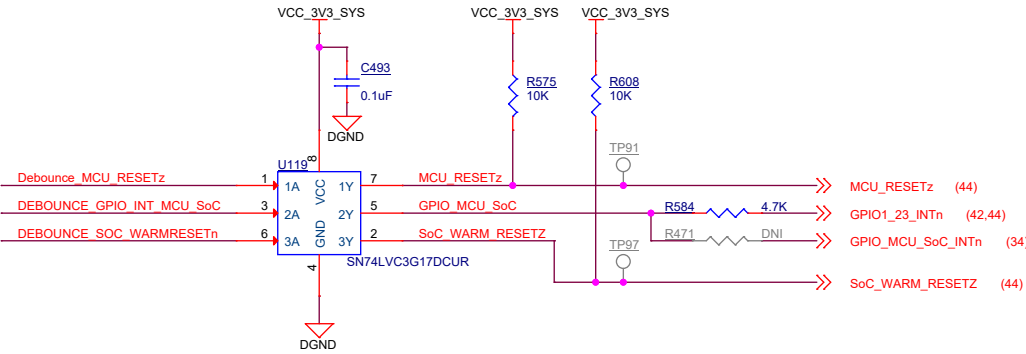
E1

RESET

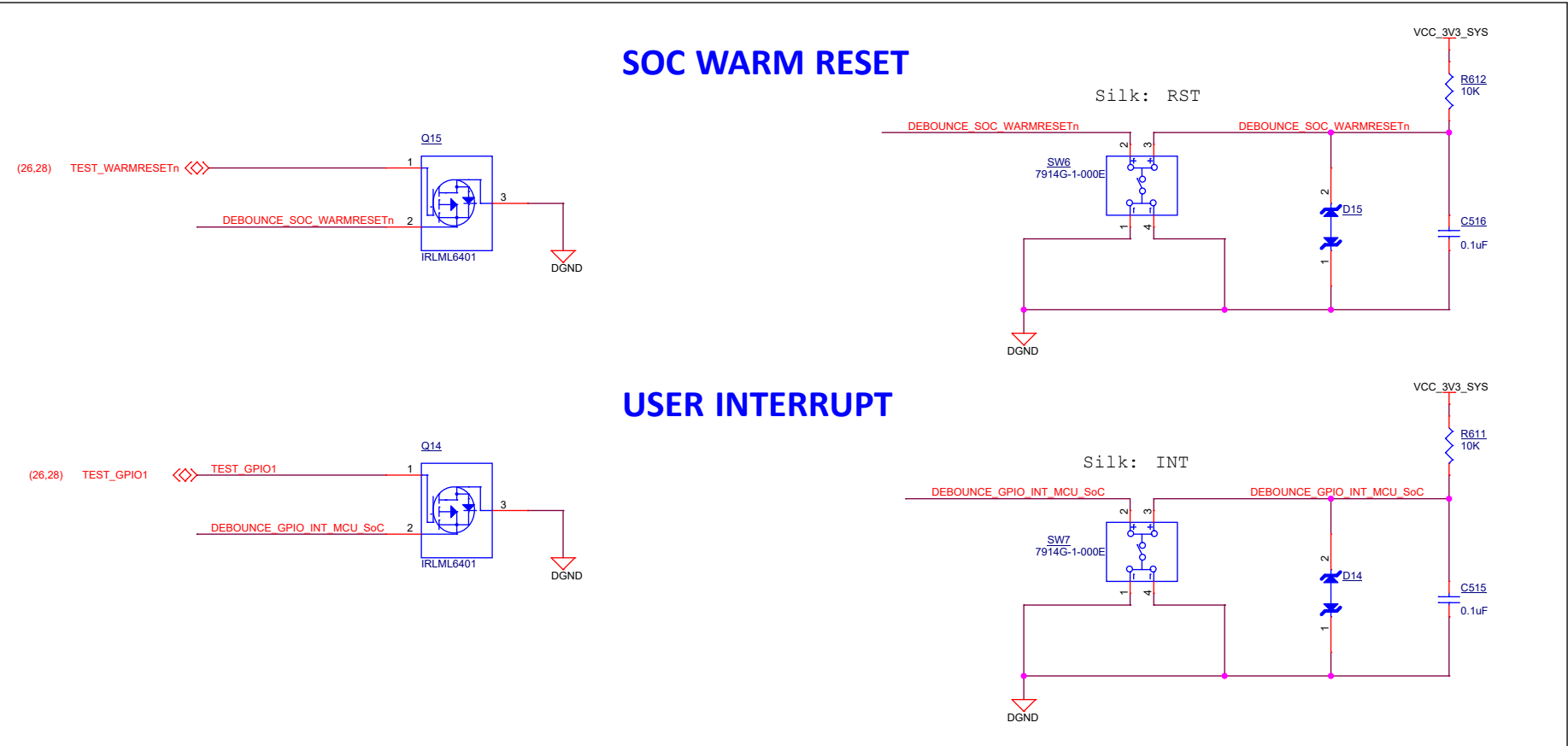
MCU WARM RESET



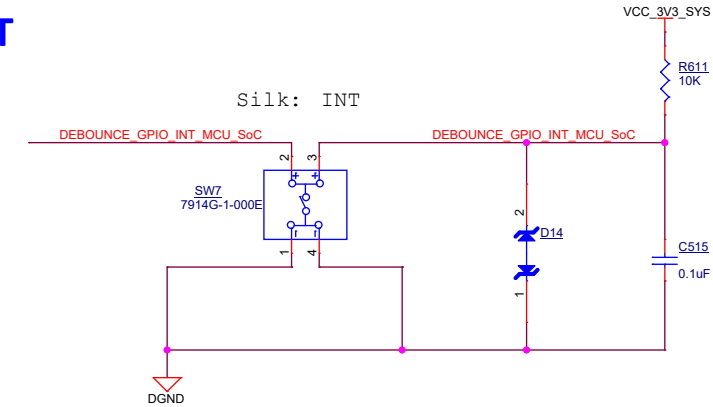
DEBOUNCE CIRCUIT



SOC WARM RESET



USER INTERRUPT

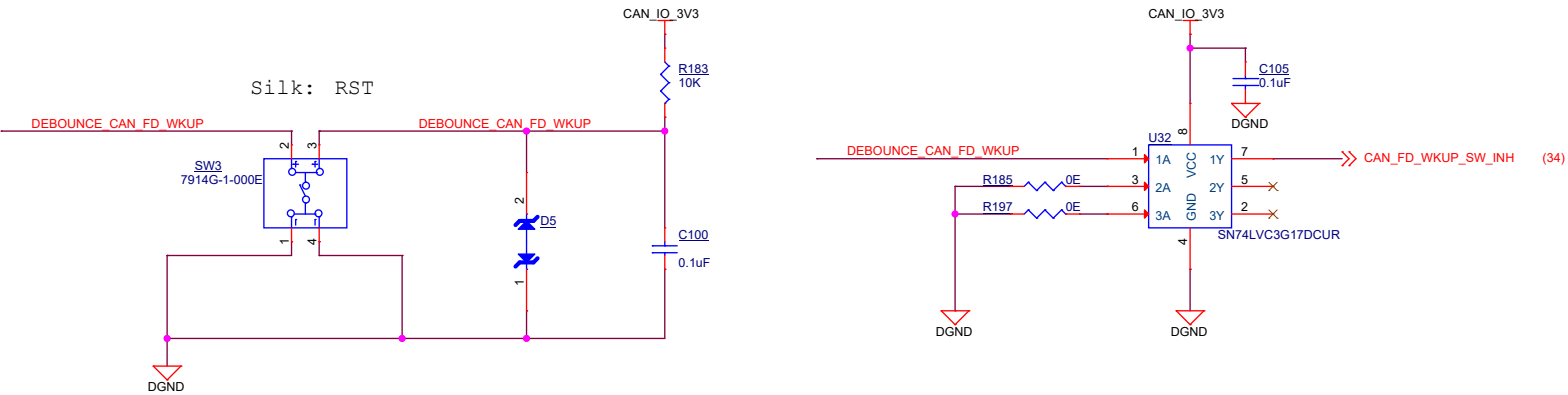


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Title			RESET
Size	PROC164E1		Rev
C			E1
Date:	Monday, June 26, 2023	Sheet	45 of 47

CAN-FD FAST WAKE UP SW



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Title CAN FD WKUP SW

Size C  
PROC164E1

Rev

E1

Date: Monday, June 26, 2023

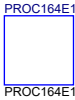
Sheet 46 of 47

HARDWARE SCHEMATICS

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

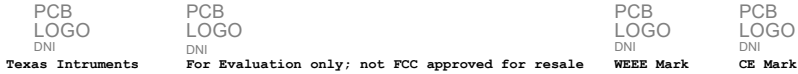
BARE PCB



AM62P SOCKET



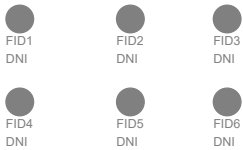
LOGOs



JUMPERS



FIDUCIALS



LABELS

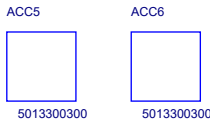
Board Serial No.      Assembly Revision



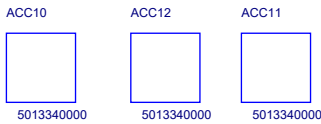
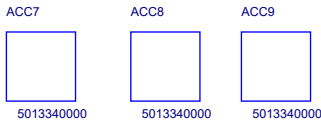
SCREW & WASHER FOR PCIe M.2



HOUSING & CRIMP FOR DSI AND OLDI HEADER



HOUSING



CRIMP

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Title      HARDWARE SCHEMATICS

Size      PROC164E1

C      Date:      Monday, June 26, 2023

Rev      E1

Sheet      47      of      47