User's Guide

J784S4, TDA4VH, TDA4AH, TDA4VP, TDA4AP, AM69 Power Estimation Tool User's Guide

1 Abstract

The Excel-based tool allows users to estimate their thermal power based upon specified loadings for different components (compute cores and peripherals) of the system-on-chip (SoC). The tool allows the user to pre-populate the various fields (which components are used, and utilization of the major components) from a set of representative use cases. This gives a starting point from which a new use case can be customized to judge the power and loadings of their own use case. The tool provides a breakdown of thermal power at the junction temperature (Tj) entered, and it also provides a table of power delivery network (PDN) currents computed for this defined use case at Tj = 125°C or 105°C.[1]

The tool gives two power estimates:

Thermal power estimate

- The time constant for heating or cooling an SoC is on the order of seconds or minutes. Because this is the primary use for the tool, the loadings should represent the average activity over a duration of seconds or minutes.

Peak / PDN estimate

- The time constant for peak current (power) is on the order of a microsecond. Though a use case (on average) may utilize a given component for say 70%, for windows of time that component will be at 100% utilization. The tool's calculation for Peak / Power Delivery Network (PDN) estimates automatically increases the loading on key intellectual property (IP) that is enabled in order to create the PDN requirements.

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Trademarks

[1] If the user selects a junction temperature less than or equal to 105°C, the Peak / PDN estimate is computed for 105°C. If the user-selected junction temperature is greater than 105°C, then the Peak / PDN estimate is carried out at 125°C.

2 Contributions to Power

The SoC power is typically considered to have two different components – dynamic power and leakage.[2]

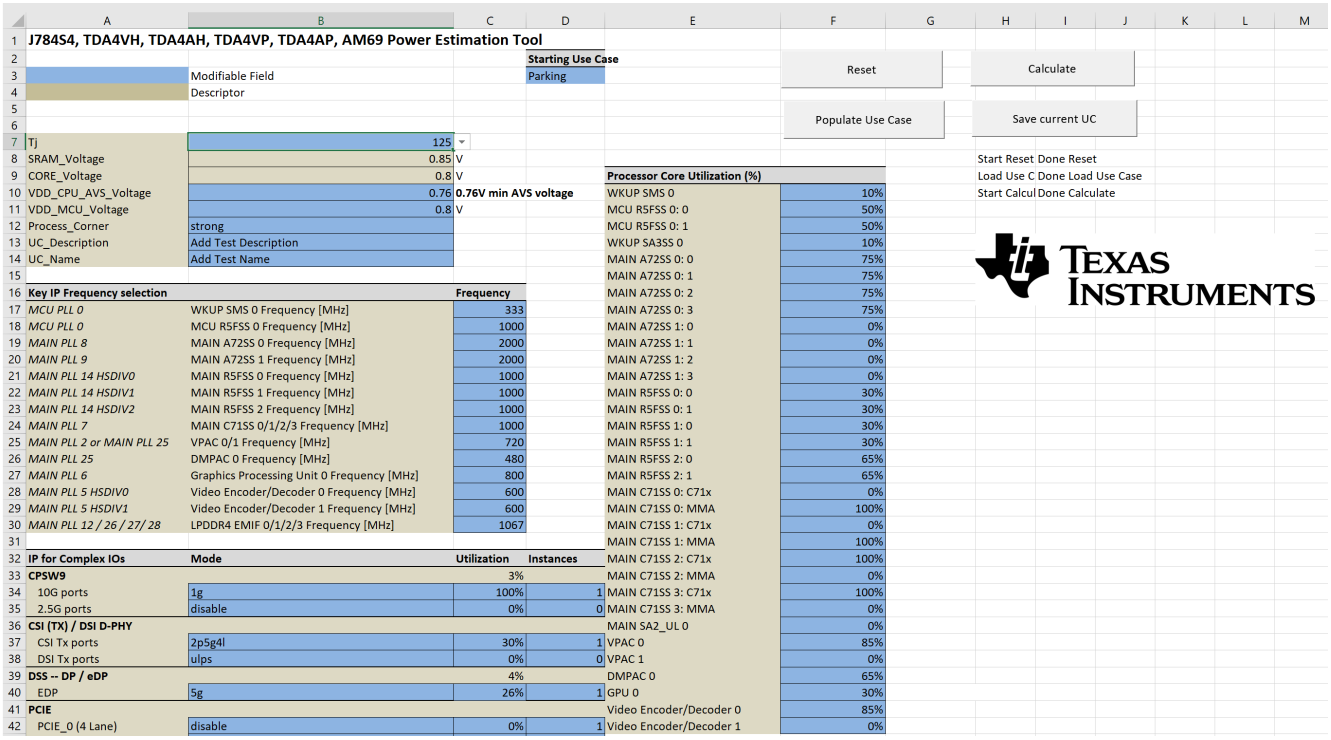
- The dynamic power is computed based upon two numbers for the IP – max power and idle power (both scaled to the voltage). The dynamic power is computed as the weighted average of the max and idle power: $P_{dyn}=P_{max}\times Utilization+P_{idle}\times(1-Utilization)$
  - For background: Dynamic power is typically computed as fCV^2. Consider a clock signal on a pcb that is driven from a CMOS output to a CMOS input. Dynamic power is computed based upon the (a) frequency of the signal – f; (b) the capacitance of the input load and the pcb trace capacitance – C; and (c) the voltage swing of the signal – V.
  - Within the tool, the user can select the frequency for some IP as well as the IP's utilization. The frequency and utilization are obviously linked; as the frequency decreases, the utilization will need to increase to maintain the same activity. Therefore, a function that requires 40% loading on an IP will have nearly the same power if the frequency is cut in half and the utilization doubles to 80%.
- The leakage power is computed based upon voltage, junction temperature, and manufacturing process variation. While the process and voltage have strong effects on the leakage power, the leakage power increases exponentially with T_j.
  - For background, a CMOS transistor is considered to have two states: (a) ON in which the channel between source and drain is conducting; and (b) OFF in which the channel is non-conductive between the source and the drain. Leakage power arises because the OFF state can allow a trickle of current to cross the channel.

[2] There is a third component of the SoC power – that is, analog or bias currents. These currents are not considered in this tool because in almost all cases the power contributed from these sources is negligible to the overall power.

3 How to Use the Tool

The tool has two pages:

1. Use Case (tab in the Excel workbook) contains many different components that the user can configure to represent their use case; the top portion of this worksheet is shown in Figure 3-1. (The individual largest contributors to the power are in column E.) This sheet also contains 4 buttons that initialize different phases of the estimate.
2. Results is a blank sheet into which the results are populated.



J784S4, TDA4VH, TDA4AH, TDA4VP, TDA4AP, AM69 Power Estimation Tool

Starting Use Case: Parking

Reset | Calculate | Populate Use Case | Save current UC

Start Reset Done Reset
Load Use C Done Load Use Case
Start Calcul Done Calculate

TJ	125		
SRAM_Voltage	0.85	V	
CORE_Voltage	0.8	V	
VDD_CPU_AVS_Voltage	0.76	0.76V min AVS voltage	
VDD_MCU_Voltage	0.8	V	
Process_Corner	strong		
UC_Description	Add Test Description		
UC_Name	Add Test Name		

Key IP Frequency selection		Frequency
MCU PLL 0	WKUP SMS 0 Frequency [MHz]	333
MCU PLL 0	MCU R5FSS 0 Frequency [MHz]	1000
MAIN PLL 8	MAIN A72SS 0 Frequency [MHz]	2000
MAIN PLL 9	MAIN A72SS 1 Frequency [MHz]	2000
MAIN PLL 14 HSDIV0	MAIN R5FSS 0 Frequency [MHz]	1000
MAIN PLL 14 HSDIV1	MAIN R5FSS 1 Frequency [MHz]	1000
MAIN PLL 14 HSDIV2	MAIN R5FSS 2 Frequency [MHz]	1000
MAIN PLL 7	MAIN C71SS 0/1/2/3 Frequency [MHz]	1000
MAIN PLL 2 or MAIN PLL 25	VPAC 0/1 Frequency [MHz]	720
MAIN PLL 25	DMPAC 0 Frequency [MHz]	480
MAIN PLL 6	Graphics Processing Unit 0 Frequency [MHz]	800
MAIN PLL 5 HSDIV0	Video Encoder/Decoder 0 Frequency [MHz]	600
MAIN PLL 5 HSDIV1	Video Encoder/Decoder 1 Frequency [MHz]	600
MAIN PLL 12 / 26 / 27/ 28	LPDDR4 EMIF 0/1/2/3 Frequency [MHz]	1067

IP for Complex IOs	Mode	Utilization	Instances
CPSW9		3%	
10G ports	1g	100%	1
2.5G ports	disable	0%	0
CSI (TX) / DSI D-PHY			
CSI Tx ports	2p5g4l	30%	1
DSI Tx ports	ulps	0%	0
DSS -- DP / eDP		4%	
EDP	5g	26%	1
PCIE			
PCIE_0 (4 Lane)	disable	0%	1

Processor Core Utilization (%)	
WKUP SMS 0	10%
MCU R5FSS 0: 0	50%
MCU R5FSS 0: 1	50%
WKUP SA3SS 0	10%
MAIN A72SS 0: 0	75%
MAIN A72SS 0: 1	75%
MAIN A72SS 0: 2	75%
MAIN A72SS 0: 3	75%
MAIN A72SS 1: 0	0%
MAIN A72SS 1: 1	0%
MAIN A72SS 1: 2	0%
MAIN A72SS 1: 3	0%
MAIN R5FSS 0: 0	30%
MAIN R5FSS 0: 1	30%
MAIN R5FSS 1: 0	30%
MAIN R5FSS 1: 1	30%
MAIN R5FSS 2: 0	65%
MAIN R5FSS 2: 1	65%
MAIN C71SS 0: C71x	0%
MAIN C71SS 0: MMA	100%
MAIN C71SS 1: C71x	0%
MAIN C71SS 1: MMA	100%
MAIN C71SS 2: C71x	100%
MAIN C71SS 2: MMA	0%
MAIN C71SS 3: C71x	100%
MAIN C71SS 3: MMA	0%
MAIN SA2_UL 0	0%
VPAC 0	85%
VPAC 1	0%
DMPAC 0	65%
GPU 0	30%
Video Encoder/Decoder 0	85%
Video Encoder/Decoder 1	0%

Figure 3-1. Top of Use Case Tab of AM69PowerEstimationTool

	A	B	C	D	E	F	G	H	I	J	K
1	UC_Name:	Add Test Name		**Caution:**							
2	UC_Description:	Add Test Description		This power estimation spreadsheet is subject to change. SoC power estimates provide approximate power and c							
3	Based on Loaded Use Case:	Parking		they are provided "as is" and are not guaranteed within a specified precision. Power consumption depends on el							
4	Internal Reference Date:	8/28/2023		environmental conditions, and uses cases running on the processor during operation. Actual power consumptior							
5	Internal Reference Revision:	1.4		SoC power, PDN integrity & thermal performance can vary depending on final use cases, features supported, s							
6	Date:	11/13/2023		**Conditions: Strong Process, AVS enabled**							
7	Tool Revision / Date	1 / 14-Sep-2023									
8		J784S4_PowerEstimationTool_v0p8_mine.xlsm									
9	**Thermal Power**										
10	**Tj [C]**	**Leakage Power [mW]**	**Dynamic Power [mW]**	**Total Power [mW]**				**125C**			
11	125	11980	17889	29869				**IP**	**Total Power [mW]**		
12	120	10595	17889	28484				A72	2952		
13	115	9343	17889	27232				C7x / MMA	7048		
14	110	8234	17889	26123				Pulsar (Main)	748		
15	105	7224	17889	25113				GPU	575		
16	100	6336	17889	24225				Wave Encoder / Decoder	693		
17	95	5540	17889	23429				VPAC3	879		
18	90	4832	17889	22721				DMPAC	1		
19	85	4198	17889	22087				Rest of chip	16973		
20	80	3655	17889	21544							
21	75	3177	17889	21066							
22	50	1516	17889	19405				**PD**	**PSC**	**State**	
23	25	701	17889	18590				GP_CORE_CTL_wkup		ON	
24	0	348	17889	18237				GP_Core_CTL (CC)		ON	
25	-20	211	17889	18100				GP_Core_CTL		ON	
26	-40	154	17889	18043				PD_Pulsar_MCU		ON	
27								PD_C7_0	14	ON	
28	**Tj = 125C**							PD_C7_1	15	ON	
29	**Thermal Power**		not suitable for designing a PDN					PD_A72_Cluster_0	16	ON	
30		**Leakage Power [mW]**	**Dynamic Power [mW]**	**Total Power [mW]**	**Voltage [V]**	**Total Current [mA]**		PD_A72_0	17	ON	
31	VDD_CORE	5160	5630	10790	0.8	13490		PD_A72_1	18	ON	
32	VDD_CPU	5250	10690	15940	0.76	20980		PD_A72_Cluster_1	19	OFF	
33	VDD_MCU	260	430	690	0.8	870		PD_A72_4	20	OFF	
34	VDDAR_CORE	380	0	380	0.85	450		PD_A72_5	21	OFF	
35	VDDAR_CPU	720	0	720	0.85	850		PD_GPUCOM	22	ON	
36	VDDAR_MCU	52	0	52	0.85	62		PD_C7_2	24	ON	
37								PD_C7_3	25	ON	

Figure 3-2. Top of Results Tab of AM69PowerEstimationTool

3.1 Use Case

The use case page is shown in Figure 3-1. This sheet has 10 different sections that must be completed.

Core Processor Utilization:

Processor Core Utilization (%)	
WKUP SMS 0	10%
MCU R5FSS 0: 0	50%
MCU R5FSS 0: 1	50%
WKUP SA3SS 0	10%
MAIN A72SS 0: 0	75%
MAIN A72SS 0: 1	75%
MAIN A72SS 0: 2	75%
MAIN A72SS 0: 3	75%
MAIN A72SS 1: 0	0%
MAIN A72SS 1: 1	0%
MAIN A72SS 1: 2	0%
MAIN A72SS 1: 3	0%
MAIN R5FSS 0: 0	30%
MAIN R5FSS 0: 1	30%
MAIN R5FSS 1: 0	30%
MAIN R5FSS 1: 1	30%
MAIN R5FSS 2: 0	65%
MAIN R5FSS 2: 1	65%
MAIN C71SS 0: C71x	0%
MAIN C71SS 0: MMA	100%
MAIN C71SS 1: C71x	0%
MAIN C71SS 1: MMA	100%
MAIN C71SS 2: C71x	100%
MAIN C71SS 2: MMA	0%
MAIN C71SS 3: C71x	100%
MAIN C71SS 3: MMA	0%
MAIN SA2_UL 0	0%
VPAC 0	85%
VPAC 1	0%
DMPAC 0	65%
GPU 0	30%
Video Encoder/Decoder 0	85%
Video Encoder/Decoder 1	0%

This block allows the user to assign a utilization to each major core IP.

WKUP domain:

- SMS 0 – Arm Cortex-M4F based Security Management Subsystem
- SA3SS 0 – a collection of essential hardware accelerators supporting cryptography

MCU domain:

- Dual-R5F MCU Subsystem

Main domain:

- 2x Quad-A72 MPU Subsystem
- 3x Dual-R5F MCU Subsystems
- 4x C71x DSP Subsystem that includes a Matrix Multiplication Accelerator (MMA)
- SA2_UL is a collection of hardware accelerators supporting cryptography
- 2x Vision Preprocessing Accelerator (VPAC)
- Depth and Motion Processing Accelerator (DMPAC)
- Graphics Processing Unit (GPU)
- 2x Combination Video Encoder and Decoder

Key IP Frequency selection:

Key IP Frequency selection		Frequency
MCU PLL 0	WKUP SMS 0 Frequency [MHz]	333
MCU PLL 0	MCU R5FSS 0 Frequency [MHz]	1000
MAIN PLL 8	MAIN A72SS 0 Frequency [MHz]	2000
MAIN PLL 9	MAIN A72SS 1 Frequency [MHz]	2000
MAIN PLL 14 HSDIV0	MAIN R5FSS 0 Frequency [MHz]	1000
MAIN PLL 14 HSDIV1	MAIN R5FSS 1 Frequency [MHz]	1000
MAIN PLL 14 HSDIV2	MAIN R5FSS 2 Frequency [MHz]	1000
MAIN PLL 7	MAIN C71SS 0/1/2/3 Frequency [MHz]	1000
MAIN PLL 2 or MAIN PLL 25	VPAC 0/1 Frequency [MHz]	720
MAIN PLL 25	DMPAC 0 Frequency [MHz]	480
MAIN PLL 6	Graphics Processing Unit 0 Frequency [MHz]	800
MAIN PLL 5 HSDIV0	Video Encoder/Decoder 0 Frequency [MHz]	600
MAIN PLL 5 HSDIV1	Video Encoder/Decoder 1 Frequency [MHz]	600
MAIN PLL 12 / 26 / 27/ 28	LPDDR4 EMIF 0/1/2/3 Frequency [MHz]	1067

This block allows the user to select the frequency for the key blocks in the core utilization block (+DDR).

- One special note involves PLL25. Since the internal frequency of the PLL is limited to ~3GHz, the VPAC and DMPAC cannot simultaneously run at the highest frequency (720MHz and 520MHz, respectively) for both IPs from the same PLL.

Memory Interfaces:

Memory Interfaces	Mode	Utilization
DDRSS 0	lpddr4_4267_32	40%
DDRSS 1	lpddr4_4267_32	40%
DDRSS 2	lpddr4_4267_32	40%
DDRSS 3	sleep	0%
GPMC / ELM	unused	0%

The AM69x device has 4 Double Data Rate (DDR) SDRAM controllers and associated physical layer interfaces (PHYs) as well as a General-Purpose Memory Controller (GPMC) with Error Location Module (ELM).

PHYs:

PHYs	Mode	Utilization	Instances
CSI2.0 D_PHY 4L Rx	2p5g4l	100%	1
CSI2.0 / DSI D_PHY 4L Tx	ulps	0%	0
MAIN MMCSD0	off	0%	0
UFS M_PHY 2L	sleep	0%	1
USB2.0	sleep	0%	1

The AM69x device has several PHYs; for the PHYs with multiple instances, in addition to the mode and the utilization, the user should also select how many of the instances are used:

- 3x Camera Stream Interface (CSI) 2.0 Receive PHYs each with 4 Lanes
- 2x CSI2.0 Transmit PHYs each with 4 Lanes
  - 2x Display Subsystem Display Serial Interface (DSI) Transmit interface (using the CSI2.0 Tx PHY)
- 1x Multi Media Card Interface (MMC) for eMMC only
- 1x Universal Flash Storage PHY with 2 lanes
- 1x Universal Serial Bus (USB) 2.0 PHY

High Speed Serial Interface:

High Speed Serial Interfaces	Mode	Utilization
SerDes 0 (PCIE_3, PCIE_1, USB_0, Hyperlink_0)		
Lane0	disable	0%
Lane1	disable	0%
Lane2	disable	0%
Lane3	disable	0%
SerDes 1 (CPSW9_0, PCIE_0, PCIE_2, n/a)		
Lane0	1g	100%
Lane1	disable	0%
Lane2	disable	0%
Lane3	disable	0%
SerDes 2 (CPSW9_0, CPSW9_0, n/a, n/a)		
Lane0	disable	0%
Lane1	disable	0%
Lane2	disable	0%
Lane3	disable	0%
SerDes 3 (eDP_0, CPSW9_0, USB_0, Hyperlink_0)		
Lane0	5g	100%
Lane1	5g	100%
Lane2	5g	100%
Lane3	5g	100%

There are four high speed serializing / deserializing (SerDes) interface on this device. Each SerDes has 4 lanes for which the mode, utilization and IP should be selected.

- The IP loading (utilization) is required to be configured in the IP Utilization for High Speed IO
- Because the SerDes constantly transmit (e.g. SGMII sends /I1/ and /I2/ ordered sets when not sending data), the utilization should likely be set to 100%.

IP Utilization for High Speed IO

IP for Complex IOs	Mode	Utilization	Instances
CPSW9		3%	
10G ports	1g	100%	1
2.5G ports	disable	0%	0
CSI (TX) / DSI D-PHY			
CSI Tx ports	2p5g4l	30%	1
DSI Tx ports	ulps	0%	0
DSS -- DP / eDP		4%	
EDP	5g	26%	1
PCIE			
PCIE_0 (4 Lane)	disable	0%	1
PCIE_1 (4 Lane)	disable	0%	1
PCIE_2 (2 Lane)	disable	0%	1
PCIE_3 (2 Lane)	disable	0%	1
Hyper Link			
Lanes	disable	0%	1
USB			
3.0	disable	0%	1

The tool cannot determine the loading of the IP from the SerDes loading. Therefore, it is required that the user enter the IP loading in this table as well as entering the SerDes loading.

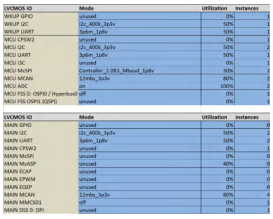
Environmental:

Tj	125	C
SRAM_Voltage	0.85	V
CORE_Voltage	0.8	V
VDD_CPU_AVS_Voltage	0.76	0.76V min AVS voltage
VDD_MCU_Voltage	0.8	V
Process_Corner	strong	
UC_Description	Add Test Description	
UC_Name	Add Test Name	

The environmental section allows the user to define junction temperature (T_j), VDD_CPU_AVS voltage, VDD_MCU voltage, the process corner, and a use case name and description.

- The PDN / Peak estimate will be run with Strong silicon and at either 105°C or 125°C; see Footnote 1.
- To save the use case, the user must supply a name for the use case.

LVCMOS IOs



Like the PHY section, the user enters Mode, utilization, and instances for each LVCMOS.

There is only one mode and utilization allowed per IP (customization is not supported since the corresponding IP blocks do not contribute significantly to the overall power). If a system uses multiple modes for an IP type, the highest power mode should be used.

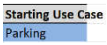
Buttons:

The buttons initialize different phases of the power estimation.

- Reset clears and resets the form as well as clearing Results
- Populate Use Case – It is recommended to start any power estimate by using one of the pre-configured representative use cases. This helps to highlight how the tool can be used in a reasonable way (i.e., it is usually not appropriate to enter 100% for all of the IP on the SoC).
- Calculate – once the form is completed, calculate in order to populate data into Results
- Save current UC – once the user gets a test case competed, it can be saved if a UC Name has been supplied. Once a use case is saved it will be part of the “Starting Use Case” list and be re-populated with the Populate use case button.

When each button is pushed, the cells underneath the button (H8:I11) record that it was started and then record when the step completes.

Starting Use Case:



This drop down selects the use case to pre-populate.

This set of use cases is supplemented when the user saves the current UC (with the buttons described above).

The pre-populated use cases are intended to provide TI-generated starting points for the customer’s use case. In the final section of this user guide, some of the pre-populated use cases will be discussed.

4 Results Sheet

The Results sheet gives a lot of information based upon the use case entered.

Thermal power estimate:

- The primary output of the estimation is shown in cells A10 to D26; this table gives the total power of the device at various temperatures.
  - Because the leakage power is very nearly exponential, the leakage component can be interpolated between any two consecutive temperatures: $P_{LKG}=10^{mT\_j+b}$
- Cells A1 to B8 contain reference information about the tool and the use case.
- Some users find it helpful to have the power breakdown by rail, and those results are provided in cell A30 to F114.
- Cells H52 to J146 provide information – utilization and frequencies -- on the use case estimated.
- Cells H22 to J49 show how the device's power domains have been configured.

Note

In the Environmental section of the Use Case tab, the user selects the voltage for configurable voltage domains. Within a voltage domain (e.g. VDD_CPU_AVS), some circuitry is placed within a power domain (e.g. C7x_0 and MMA are within PD_C7_0); the power domain can break the connection to the voltage domain if-and-only-if all of the IP within the power domain is unused. Circuitry within an off power domain, do not contribute power – leakage or dynamic – to the power budget. Within the power domain, IP is controlled by a local power sleep controller (LPSC) which controls the clock and reset to the IP. IP which is not clocked does not contribute dynamic power to the overall device power but it will contribute leakage power unless it resides in an unpowered power domain.

Note that a voltage domain typically has some IP that is within a power domain and other IP that is not within a power domain.

  - When possible, the tool powers OFF the power domain; if the user wants to keep the domain ON, it is recommended to load IP utilization within the domain at 0.1%
  - The user should configure their software to match the expectations defined in the power estimate.
- Cells H11 to I19 show a breakdown of power by block; this table shows that significant power is present in the back-plane of the device.

Peak / PDN power estimate:

- Cells M30 to R117 contain the by-rail Peak / PDN estimate; this estimate is derived from the entered use case.
  - Column U creates a label V_G1 through V_G18 (i.e. voltage group). These are just labels and can be modified by the user.
  - The same labels are present in cells N8 to N25; if the user modifies the labels in column U, the labels should also be modified in this range. Cells O2 to O19 sum the current for this voltage group.

4.1 Some Specific Pre-loaded Use Case Results

The three use cases below are intended to span the expected range of thermal power for this device; it is possible for a use case to fall outside of this range. (And the Peak / PDN power will certainly fall outside of this range.)

Table 4-1. 125°C Thermal Power

Use case	Leakage [mW]	Dynamic [mW]	Total [mW]
ARM only (x4)	9290	5700	14990
Superset	13910	29050	42960
Compute	13450	24110	37560

Table 4-2. 105°C Thermal Power

Use case	Leakage [mW]	Dynamic [mW]	Total [mW]
ARM only (x4)	5650	5700	11350
Superset	8410	29050	37460
Compute	8150	24110	32260

Comments:

- As noted, the exponential behavior of the leakage with junction temperature causes a significant decrease in leakage between 125°C and 105°C.

4.1.1 ARM Only (x4)

A minimum use case for this class of processors relies upon using the A72 cores and the PCIe and ethernet switch; in this case, the A72 cores are reduced from 2GHz to 1GHz.

In this configuration, many of the power domains are disabled.

Table 4-3. ARM-only Power Domain States

PD	State
GP_CORE_CTL_wkup	ON
GP_Core_CTL (CC)	ON
GP_Core_CTL	ON
PD_Pulsar_MCU	ON
PD_C7_0	OFF
PD_C7_1	OFF
PD_A72_Cluster_0	ON
PD_A72_0	ON
PD_A72_1	ON
PD_A72_Cluster_1	OFF
PD_A72_4	OFF
PD_A72_5	OFF
PD_GPUCOM	OFF
PD_C7_2	OFF
PD_C7_3	OFF
PD_Pulsar_0	OFF
PD_decode	OFF
PD_Pulsar_1	OFF
PD_DMPAC	OFF
PD_VPAC	OFF
PD_A72_2	ON
PD_A72_3	ON
PD_A72_6	OFF
PD_A72_7	OFF
PD_VPAC2	OFF
PD_encode2	OFF
PD_Pulsar_2	OFF

The device loading is shown in the following table.

Table 4-4. ARM-only Device Configuration

Tj	125	
VDD_CORE_SRAM_Voltage	0.85	
VDD_CORE_Voltage	0.8	

Table 4-4. ARM-only Device Configuration (continued)

VDD_CPU_SRAM_Voltage	0.85	
VDD_CPU_Voltage	0.76	
VDD_MCU_SRAM_Voltage	0.85	
VDD_MCU_Voltage	0.85	
Process_Corner	strong	
UC_Description		
A72 CPU	70%	1000
A72 CPU	70%	1000
A72 CPU	70%	1000
A72 CPU	70%	1000
A72 CPU	0%	1000
A72 CPU	0%	1000
A72 CPU	0%	1000
A72 CPU	0%	1000
Pulsar Main	0%	1000
Pulsar Main	0%	1000
Pulsar Main	0%	1000
C711 512k 1.1	0%	1000
MMA2p1	0%	1000
C711 512k 1.1	0%	1000
MMA2p1	0%	1000
C711 512k 1.1	0%	1000
MMA2p1	0%	1000
C711 512k 1.1	0%	1000
MMA2p1	0%	1000
SMS	10%	333
Pulsar MCU	50%	1000
DSS7L_eDP_DSI	0%	600
GPU	0%	800
CSI_3RX_2TX	0%	720
DPHY 1.2 RX - 4L	0%	upls
DPHY 1.2 RX - 4L	0%	upls
DPHY 1.2 RX - 4L	0%	upls
DPHY 1.2 TX - 4L	0%	upls
DPHY 1.2 TX - 4L	0%	upls
DMPAC	0%	480
VPAC3	0%	720
VPAC3	0%	720
WAVE521CL Video Codec	0%	600
WAVE521CL Video Codec	0%	600
CPSW2X eAVB	0%	
CPSW9x eAVB	23%	
PCIE_G3 4L	0%	
PCIE_G3 4L	20%	
PCIE_G3 4L	0%	
PCIE_G3 4L	0%	
Hyperlink x2	0%	

Table 4-4. ARM-only Device Configuration (continued)

USB3P0TCx1	0%	
EMMC 4	0%	
SDIO 1 bit	0%	unused
EMMC 8	20%	
Arasan HS400 8 bit	20%	hs400
UFSHCI21	0%	
MPHY - 2L	0%	sleep
DDR 0	35%	1067
LPDDR4-32 PHY 4267	39%	lpddr4_4267_32
DDR 1	35%	1067
LPDDR4-32 PHY 4267	39%	lpddr4_4267_32
DDR 2	0%	1067
LPDDR4-32 PHY 4267	0%	sleep
DDR 3	0%	1067
LPDDR4-32 PHY 4267	0%	sleep
SerDes 10G Common	100%	1pll
Lane 0	20%	8g
Lane 1	20%	8g
Lane 2	20%	8g
Lane 3	20%	8g
SerDes 10G Common	100%	2pll
Lane 0	50%	5g
Lane 1	50%	5g
Lane 2	50%	1g
Lane 3	50%	1g
SerDes 10G Common	100%	1pll
Lane 0	50%	1g
Lane 1	50%	1g
Lane 2	50%	1g
Lane 3	50%	1g
SerDes 10G Common	0%	suspend
Lane 0	0%	disable
Lane 1	0%	disable
Lane 2	0%	disable
Lane 3	0%	disable

The thermal power for the device is shown in the following table.

Table 4-5. ARM-only Thermal Power

Tj	Leakage [mW]	Dynamic [mW]	Total [mW]
125	9283	5698	14981
120	8247	5698	13945
115	7276	5698	12974
110	6427	5698	12125
105	5649	5698	11347
100	4955	5698	10653
95	4347	5698	10045
90	3808	5698	9506

Table 4-5. ARM-only Thermal Power (continued)

Tj	Leakage [mW]	Dynamic [mW]	Total [mW]
85	3330	5698	9028
80	2894	5698	8592
75	2519	5698	8217
50	1228	5698	6926
25	596	5698	6294
0	293	5698	5991
-20	193	5698	5891
-40	147	5698	5845

4.1.2 Superset

On the other end of the spectrum is a superset use case in which A72s, Pulsars, C71x and MMAs, GPU, DMPAC and VPAC are effectively maximized. In this example, the SerDes is also loaded.

In this configuration, none of the power domains are disabled.

Table 4-6. Superset Power Domain States

PD	State
GP_CORE_CTL_wkup	ON
GP_Core_CTL (CC)	ON
GP_Core_CTL	ON
PD_Pulsar_MCU	ON
PD_C7_0	ON
PD_C7_1	ON
PD_A72_Cluster_0	ON
PD_A72_0	ON
PD_A72_1	ON
PD_A72_Cluster_1	ON
PD_A72_4	ON
PD_A72_5	ON
PD_GPUCOM	ON
PD_C7_2	ON
PD_C7_3	ON
PD_Pulsar_0	ON
PD_decode	ON
PD_Pulsar_1	ON
PD_DMPAC	ON
PD_VPAC	ON
PD_A72_2	ON
PD_A72_3	ON
PD_A72_6	ON
PD_A72_7	ON
PD_VPAC2	ON
PD_encode2	ON
PD_Pulsar_2	ON

The device loading is shown in the following table.

Table 4-7. Superset Device Configuration

Tj	125	

Table 4-7. Superset Device Configuration (continued)

VDD_CORE_SRAM_Voltage	0.85	
VDD_CORE_Voltage	0.8	
VDD_CPU_SRAM_Voltage	0.85	
VDD_CPU_Voltage	0.76	
VDD_MCU_SRAM_Voltage	0.85	
VDD_MCU_Voltage	0.8	
Process_Corner	Strong	
UC_Description		
A72 CPU	90%	2000
A72 CPU	90%	2000
A72 CPU	90%	2000
A72 CPU	90%	2000
A72 CPU	90%	2000
A72 CPU	90%	2000
A72 CPU	90%	2000
A72 CPU	10%	2000
Pulsar Main	80%	1000
Pulsar Main	80%	1000
Pulsar Main	80%	1000
C711 512k 1.1	0%	1000
MMA2p1	100%	1000
C711 512k 1.1	0%	1000
MMA2p1	100%	1000
C711 512k 1.1	0%	1000
MMA2p1	100%	1000
C711 512k 1.1	20%	1000
MMA2p1	80%	1000
SMS	10%	333
Pulsar MCU	80%	1000
DSS7L_eDP_DSI	63%	600
GPU	100%	800
CSI_3RX_2TX	64%	720
DPHY 1.2 RX - 4L	80%	2p5g4l
DPHY 1.2 RX - 4L	80%	2p5g4l
DPHY 1.2 RX - 4L	80%	2p5g4l
DPHY 1.2 TX - 4L	80%	2p5g4l
DPHY 1.2 TX - 4L	0%	upls
DMPAC	79%	480
VPAC3	72%	720
VPAC3	83%	720
WAVE521CL Video Codec	75%	600
WAVE521CL Video Codec	75%	600
CPSW2X eAVB	100%	
CPSW9x eAVB	50%	
PCIE_G3 4L	80%	
PCIE_G3 4L	80%	
PCIE_G3 4L	0%	

Table 4-7. Superset Device Configuration (continued)

PCIE_G3 4L	0%	
Hyperlink x2	0%	
USB3P0TCx1	80%	
EMMC 4	0%	
SDIO 1 bit	0%	unused
EMMC 8	50%	
Arasan HS400 8 bit	50%	hs400
UFSHCI21	0%	
MPHY - 2L	0%	sleep
DDR 0	40%	1067
LPDDR4-32 PHY 4267	44%	lpddr4_4267_32
DDR 1	40%	1067
LPDDR4-32 PHY 4267	44%	lpddr4_4267_32
DDR 2	40%	1067
LPDDR4-32 PHY 4267	44%	lpddr4_4267_32
DDR 3	40%	1067
LPDDR4-32 PHY 4267	44%	lpddr4_4267_32
SerDes 10G Common	100%	2pll
Lane 0	100%	8g
Lane 1	100%	8g
Lane 2	0%	disable
Lane 3	100%	5g
SerDes 10G Common	100%	1pll
Lane 0	100%	8g
Lane 1	100%	8g
Lane 2	100%	8g
Lane 3	100%	8g
SerDes 10G Common	100%	2pll
Lane 0	100%	10g
Lane 1	100%	3g
Lane 2	100%	3g
Lane 3	100%	3g
SerDes 10G Common	100%	1pll
Lane 0	66%	5g
Lane 1	66%	5g
Lane 2	66%	5g
Lane 3	66%	5g

The thermal power for the device is shown in the following table.

Table 4-8. Superset Thermal Power

Tj [C]	Leakage Power [mW]	Dynamic Power [mW]	Total Power [mW]
125	13910	29046	42956
120	12305	29046	41351
115	10853	29046	39899
110	9554	29046	38600
105	8404	29046	37450
100	7376	29046	36422

Table 4-8. Superset Thermal Power (continued)

Tj [C]	Leakage Power [mW]	Dynamic Power [mW]	Total Power [mW]
95	6440	29046	35486
90	5622	29046	34668
85	4894	29046	33940
80	4251	29046	33297
75	3690	29046	32736
50	1752	29046	30798
25	807	29046	29853
0	381	29046	29427
-20	228	29046	29274
-40	161	29046	29207

4.1.3 Compute

A use case representative of the vision analytics features of the device – camera input run through deep learning algorithms:

Again, in this configuration, none of the power domains are disabled.

Table 4-9. Compute Power Domain States

PD	State
GP_CORE_CTL_wkup	ON
GP_Core_CTL (CC)	ON
GP_Core_CTL	ON
PD_Pulsar_MCU	ON
PD_C7_0	ON
PD_C7_1	ON
PD_A72_Cluster_0	ON
PD_A72_0	ON
PD_A72_1	ON
PD_A72_Cluster_1	ON
PD_A72_4	ON
PD_A72_5	ON
PD_GPUCOM	OFF
PD_C7_2	ON
PD_C7_3	ON
PD_Pulsar_0	ON
PD_decode	ON
PD_Pulsar_1	ON
PD_DMPAC	OFF
PD_VPAC	ON
PD_A72_2	ON
PD_A72_3	ON
PD_A72_6	ON
PD_A72_7	ON
PD_VPAC2	ON
PD_encode2	OFF
PD_Pulsar_2	ON

The device loading is shown in the following table.

Table 4-10. Compute Device Configuration

Tj	125	
VDD_CORE_SRAM_Voltage	0.85	
VDD_CORE_Voltage	0.8	
VDD_CPU_SRAM_Voltage	0.85	
VDD_CPU_Voltage	0.76	
VDD_MCU_SRAM_Voltage	0.85	
VDD_MCU_Voltage	0.8	
Process_Corner	strong	
UC_Description		
A72 CPU	75%	2000
A72 CPU	75%	2000
A72 CPU	75%	2000
A72 CPU	75%	2000
A72 CPU	75%	2000
A72 CPU	75%	2000
A72 CPU	75%	2000
A72 CPU	75%	2000
Pulsar Main	80%	1000
Pulsar Main	80%	1000
Pulsar Main	80%	1000
C711 512k 1.1	0%	1000
MMA2p1	100%	1000
C711 512k 1.1	0%	1000
MMA2p1	100%	1000
C711 512k 1.1	0%	1000
MMA2p1	100%	1000
C711 512k 1.1	0%	1000
MMA2p1	100%	1000
SMS	25%	333
Pulsar MCU	80%	1000
DSS7L_eDP_DSI	0%	600
GPU	0%	800
CSI_3RX_2TX	45%	720
DPHY 1.2 RX - 4L	75%	2p5g4l
DPHY 1.2 RX - 4L	75%	2p5g4l
DPHY 1.2 RX - 4L	75%	2p5g4l
DPHY 1.2 TX - 4L	0%	upls
DPHY 1.2 TX - 4L	0%	upls
DMPAC	0%	480
VPAC3	60%	720
VPAC3	60%	720
WAVE521CL Video Codec	80%	600
WAVE521CL Video Codec	0%	600
CPSW2X eAVB	20%	
CPSW9x eAVB	0%	
PCIE_G3 4L	50%	
PCIE_G3 4L	0%	

Table 4-10. Compute Device Configuration (continued)

PCIE_G3 4L	0%	
PCIE_G3 4L	0%	
Hyperlink x2	0%	
USB3P0TCx1	0%	
EMMC 4	0%	
SDIO 1 bit	0%	unused
EMMC 8	0%	
Arasan HS400 8 bit	0%	off
UFSHCI21	0%	
MPHY - 2L	0%	sleep
DDR 0	50%	1067
LPDDR4-32 PHY 4267	55%	lpddr4_4267_32
DDR 1	50%	1067
LPDDR4-32 PHY 4267	55%	lpddr4_4267_32
DDR 2	50%	1067
LPDDR4-32 PHY 4267	55%	lpddr4_4267_32
DDR 3	0%	1067
LPDDR4-32 PHY 4267	0%	sleep
SerDes 10G Common	0%	suspend
Lane 0	0%	disable
Lane 1	0%	disable
Lane 2	0%	disable
Lane 3	0%	disable
SerDes 10G Common	100%	2pll
Lane 0	100%	8g
Lane 1	100%	8g
Lane 2	0%	disable
Lane 3	0%	disable
SerDes 10G Common	0%	suspend
Lane 0	0%	disable
Lane 1	0%	disable
Lane 2	0%	disable
Lane 3	0%	disable
SerDes 10G Common	0%	suspend
Lane 0	0%	disable
Lane 1	0%	disable
Lane 2	0%	disable
Lane 3	0%	disable

The thermal power for the device is shown in the following table.

Table 4-11. Compute Thermal Power

Tj [C]	Leakage Power [mW]	Dynamic Power [mW]	Total Power [mW]
125	13450	24107	37557
120	11905	24107	36012
115	10513	24107	34620
110	9254	24107	33361
105	8144	24107	32251

Table 4-11. Compute Thermal Power (continued)

Tj [C]	Leakage Power [mW]	Dynamic Power [mW]	Total Power [mW]
100	7146	24107	31253
95	6250	24107	30357
90	5462	24107	29569
85	4760	24107	28867
80	4138	24107	28245
75	3591	24107	27698
50	1715	24107	25822
25	784	24107	24891
0	380	24107	24487
-20	226	24107	24333
-40	160	24107	24267

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2023	*	Initial Release

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