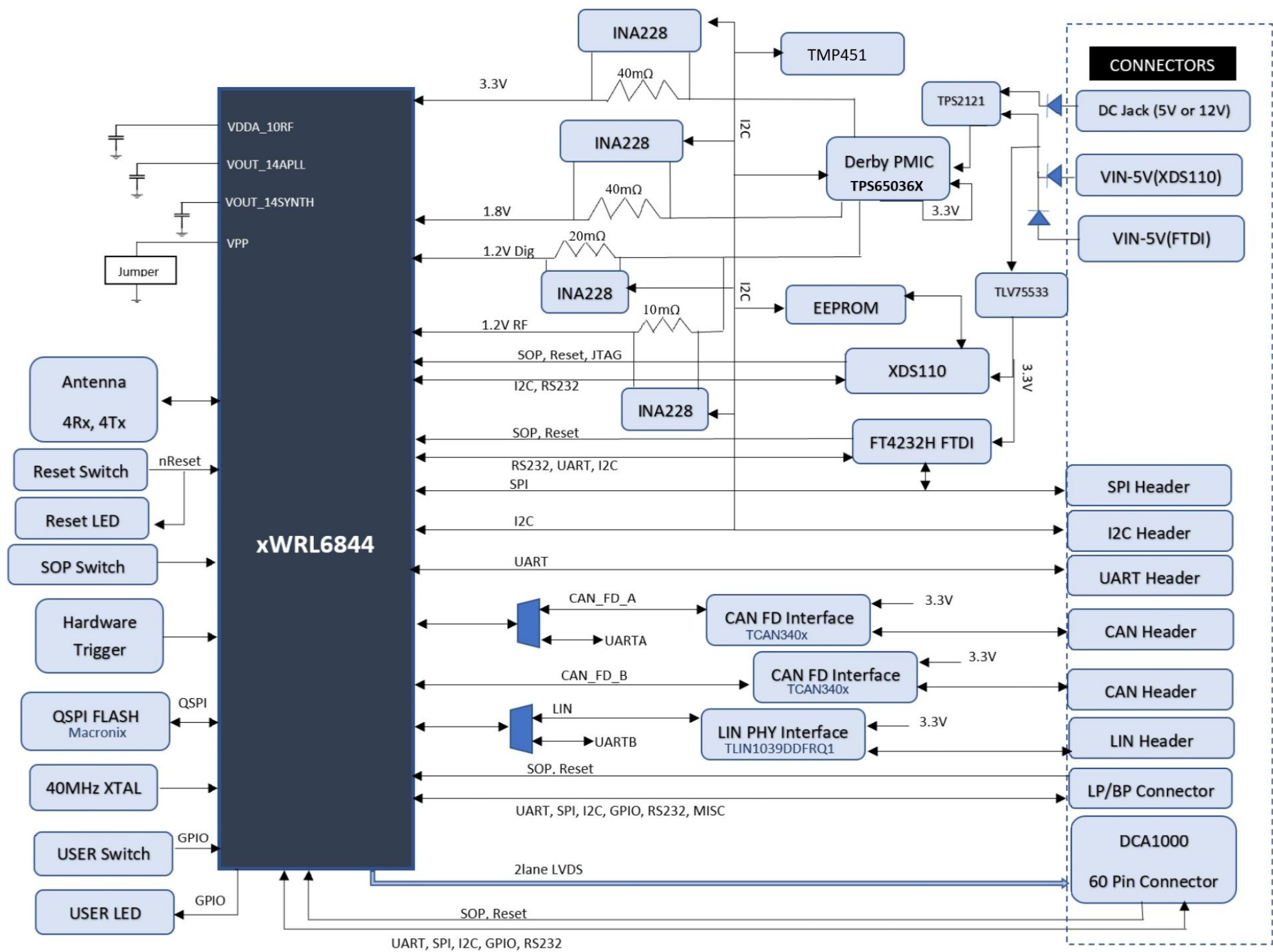


BLOCK DIAGRAM



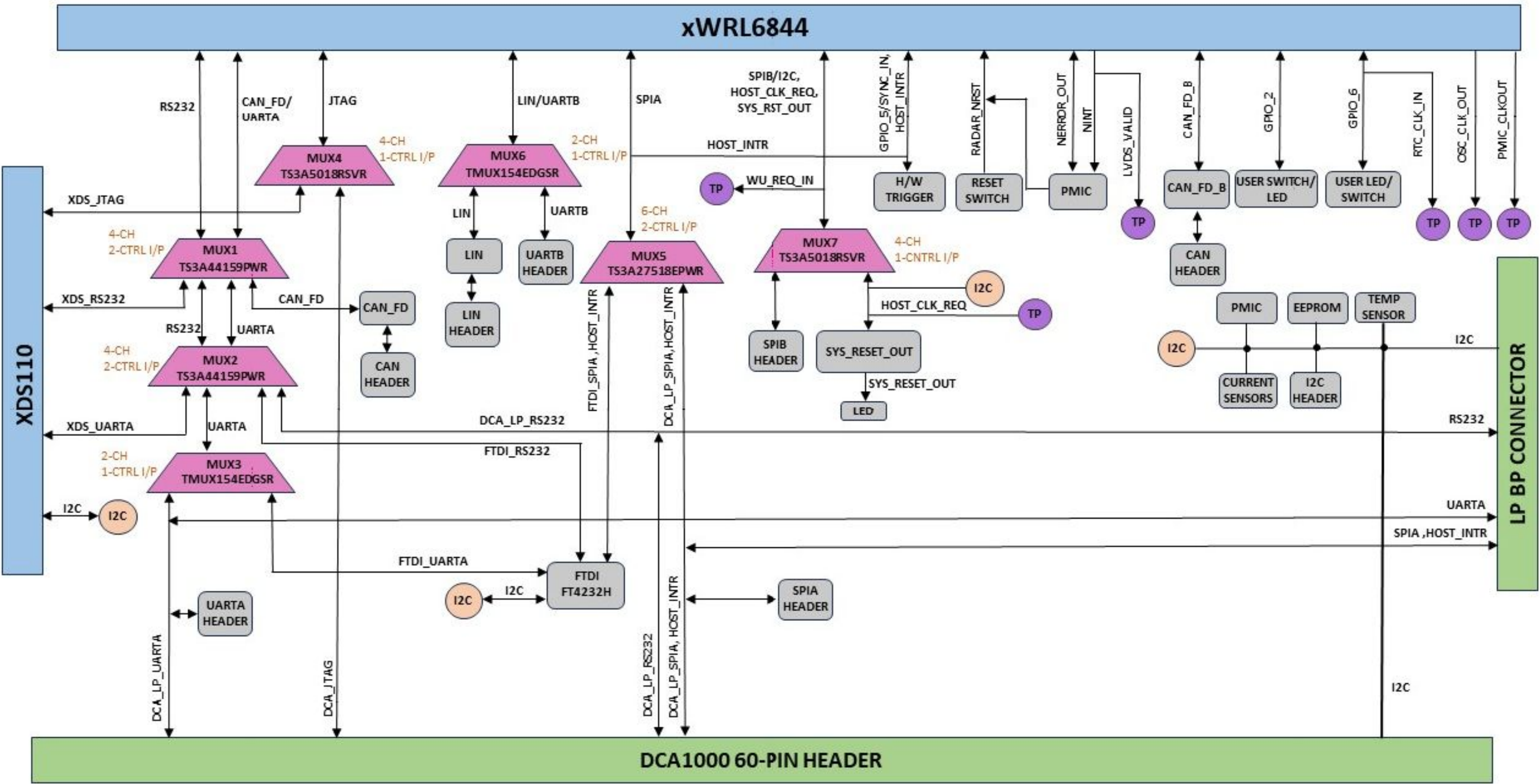
Revision History				
Rev	ECN #	Approved Date	Approved by	Notes

S.No	DESCRIPTION	I2C ADDRESS
1	CURRENT SENSOR 3.3V	100 0101
2	CURRENT SENSOR 1.8V	100 0000
3	CURRENT SENSOR 1.2V	100 0001
4	CURRENT SENSOR RF_1.2V	100 0100
5	TEMPERATURE SENSOR	1001 100
6	EEPROM	1010 0XX

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: <a href="#">AWRL6844EVM</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 25-11-2024
TID #: <a href="#">N/A</a>	Project Title: <a href="#">xWRL6844 EVM</a>	
Number: <a href="#">PROC182</a>	Rev: <a href="#">A</a>	Sheet Title: <a href="#">BLOCK DIAGRAM</a>
SVN Rev: <a href="#">Not in version control</a>	Assembly Variant: <a href="#">01_AWR</a>	Sheet: <a href="#">1</a> of <a href="#">17</a>
Drawn By: <a href="#">Mistral</a>	File: <a href="#">PROC182A_Block_Diagram.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">Mistral</a>	Contact: <a href="#">http://www.ti.com/support</a>	

MUX BLOCK DIAGRAM



Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: <a href="#">AWRL6844EVM</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 25-11-2024
TID #: <a href="#">N/A</a>	Project Title: <a href="#">xWRL6844 EVM</a>	
Number: <a href="#">PROC182</a>	Rev: <a href="#">A</a>	Sheet Title: <a href="#">MUX BLOCK DIAGRAM</a>
SVN Rev: <a href="#">Not in version control</a>	Assembly Variant: <a href="#">01_AWR</a>	Sheet: <a href="#">2</a> of <a href="#">17</a>
Drawn By: <a href="#">Mistral</a>	File: <a href="#">PROC182A_MUX_Block_Diagram.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">Mistral</a>	Contact: <a href="#">http://www.ti.com/support</a>	

1	2	3	4	5	6
A					A
B					B
C					C
D					D

TABLE OF CONTENTS

SHEET NO.	SHEET NAME
1	BLOCK DIAGRAM
2	MUX BLOCK DIAGRAM
3	TABLE OF CONTENTS
4	USB_PWR_DC_JACK_SWITCH
5	PMIC
6	xWRL6844_CHIP
7	DECOUPLING_CAPS-QSPI_FLASH_
8	TEMP_CURRENT_SENSORS_EEPROM
9	ANALOG_MUX_SOP_CTRL
10	ANALOG_MUX_SPI_DCA/FTDI
11	XDS110_INTERFACE
12	MUX_CAN_FD
13	CAN_LIN_PHY_INTERFACE
14	FTDI- USB to SPI CONVERTER
15	DCA1000_CONN_RESET
16	I2C_SPI_CONN_HEADER
17	EVM_HARDWARE

Orderable: [AWRL6844EVM](#)

TID #: [N/A](#)

Number: [PROC182](#)

SVN Rev: [Not in version control](#)

Drawn By: [Mistral](#)

Engineer: [Mistral](#)

Designed for: [Public Release](#)

Project Title: [xWRL6844 EVM](#)

Sheet Title: [TABLE OF CONTENTS](#)

Assembly Variant: [01\\_AWR](#)

File: [PROC182A\\_Table\\_Of\\_Contents.SchDoc](#)

Contact: [http://www.ti.com/support](#)

Mod. Date: [25-11-2024](#)

Sheet: [3](#) of [17](#)

Size: [B](#)

TEXAS  
INSTRUMENTS

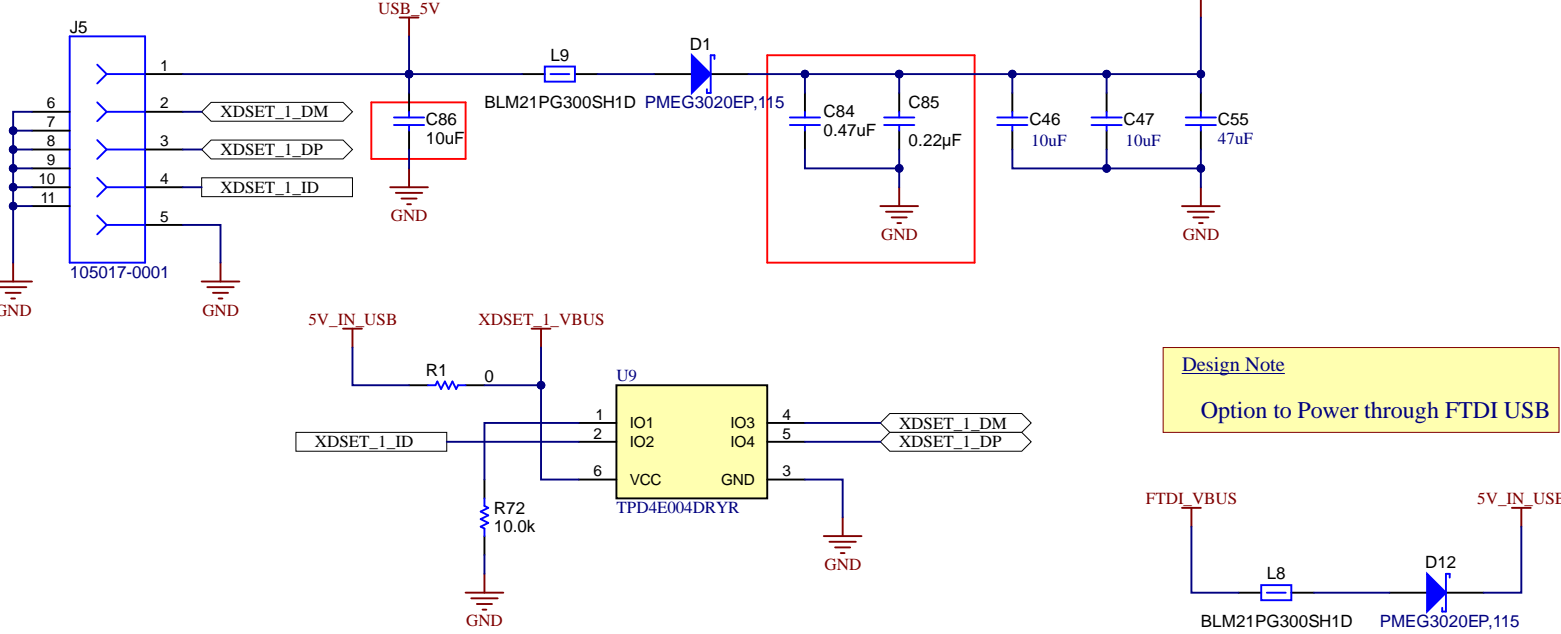
<http://www.ti.com>

© Texas Instruments [2023](#)

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

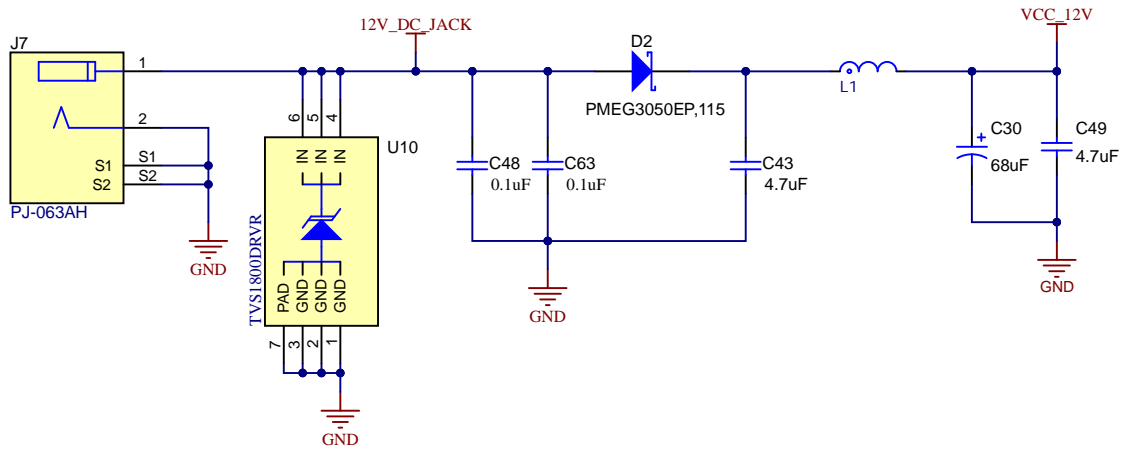
1	2	3	4	5	6
---	---	---	---	---	---

USB CONNECTOR

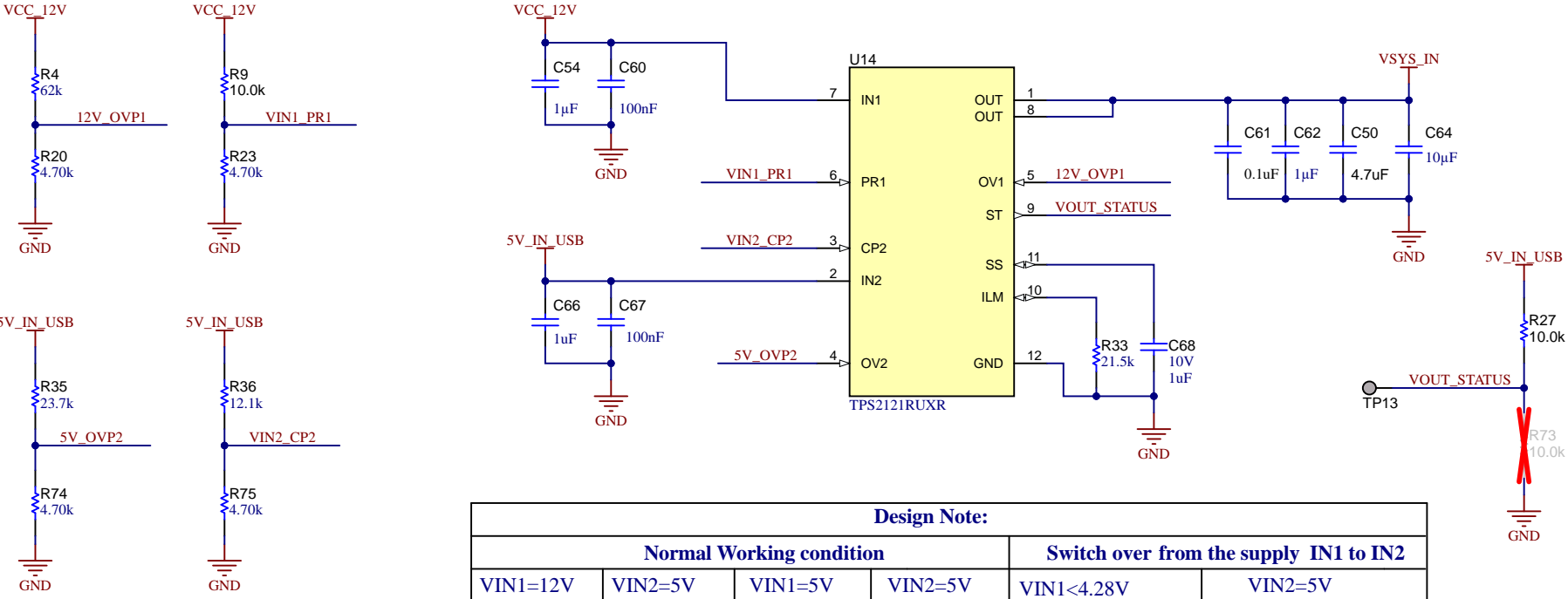


Design Note  
Option to Power through FTDI USB

DC JACK

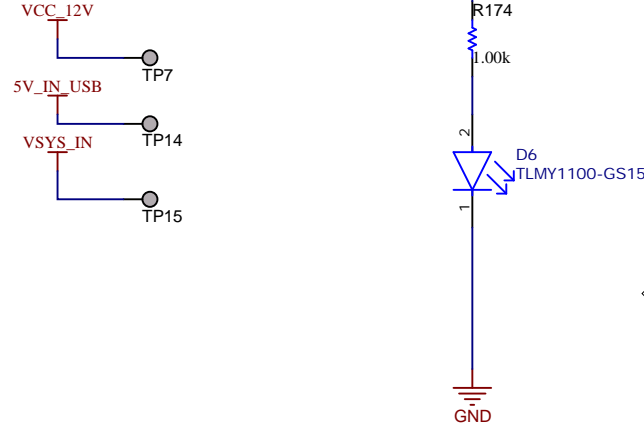


POWER LOAD SWITCH

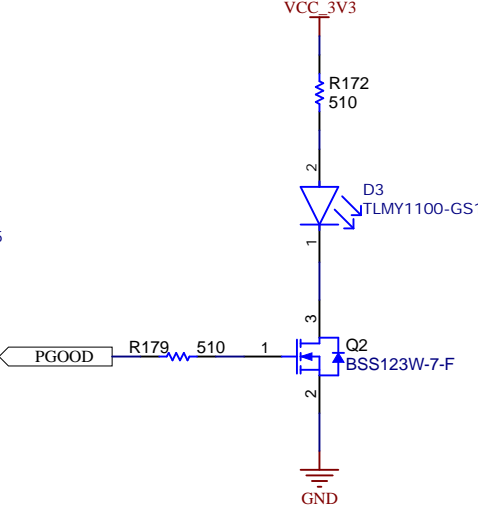


Design Note:					
Normal Working condition				Switch over from the supply IN1 to IN2	
VIN1=12V VPR1=3.83V	VIN2=5V VCP2=1.39V	VIN1=5V VPR1=1.6V	VIN2=5V VCP2=1.39V	VIN1<4.28V VPR1=1.36V	VIN2=5V VCP2=1.39V
VREF(Internal)=1.06V Current Limit = 4.5A VOUT=VIN1(12V)		VREF(Internal)=1.06V Current Limit = 4.5A VOUT=VIN1 (5V)		VREF(Internal)=1.06V Current Limit = 4.5A VOUT= VIN2 (5V)	
VPR1> VCP2> VREF ==> VOUT==>VIN1				VCP2 > VPR1> VREF ==> VOUT ==> VIN2	
Over Voltage Condition					
Over Voltage Protection :15V, @ 12V for VIN1 Over Voltage Protection : 6.46V @ 5V for VIN2					

POWER ON LED INDICATION



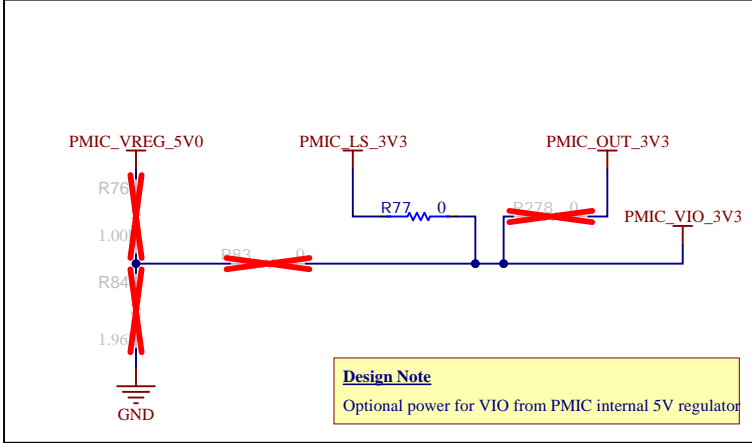
PGOOD LED



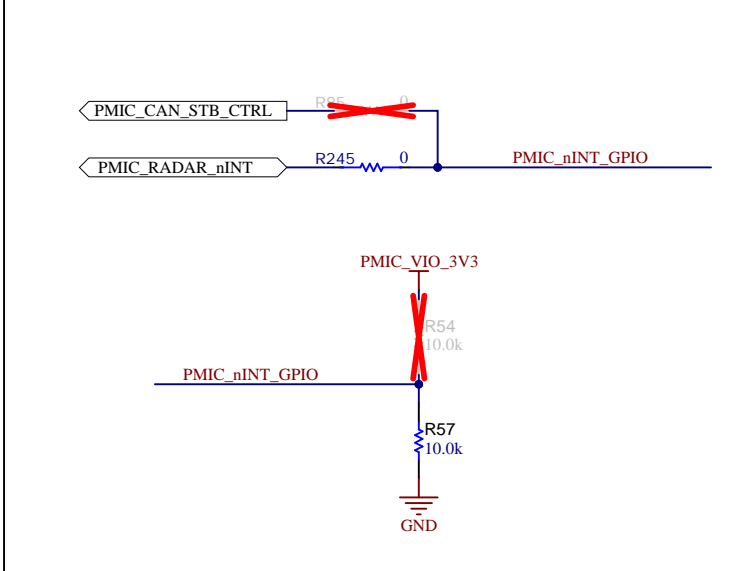
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.



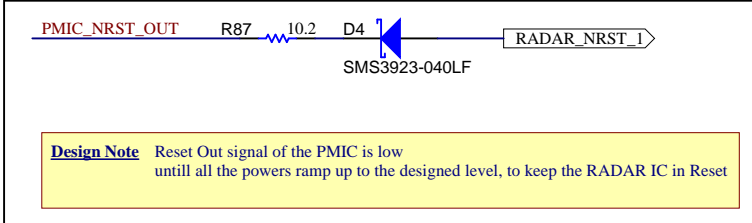
A



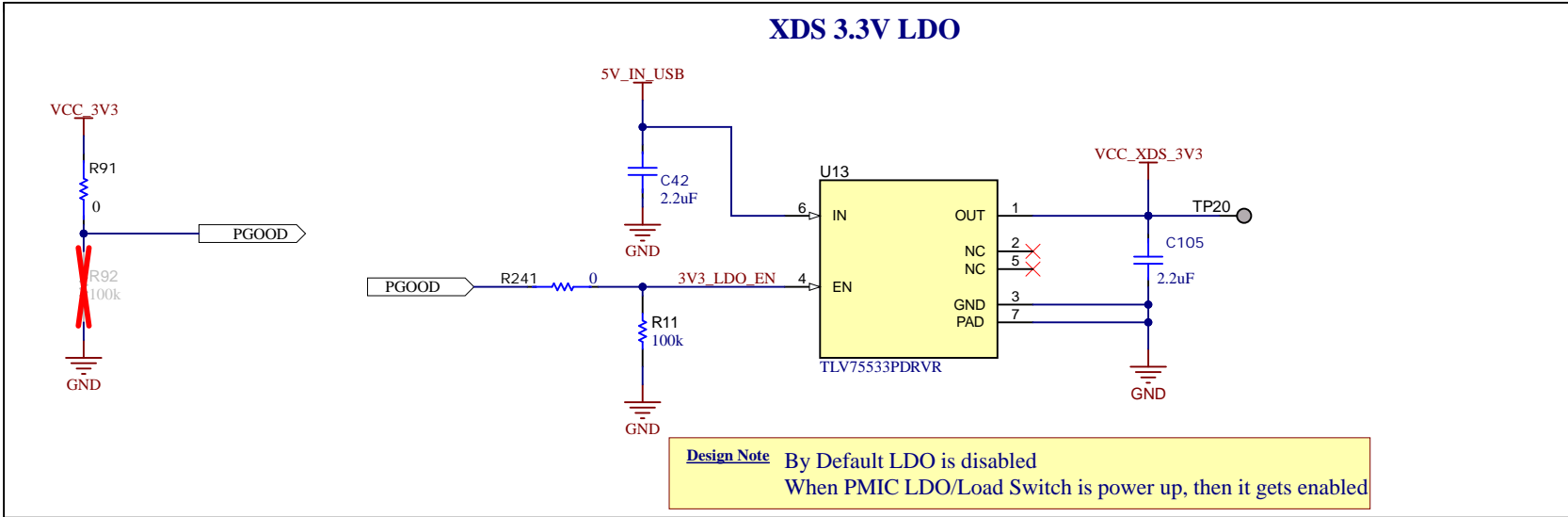
B



C

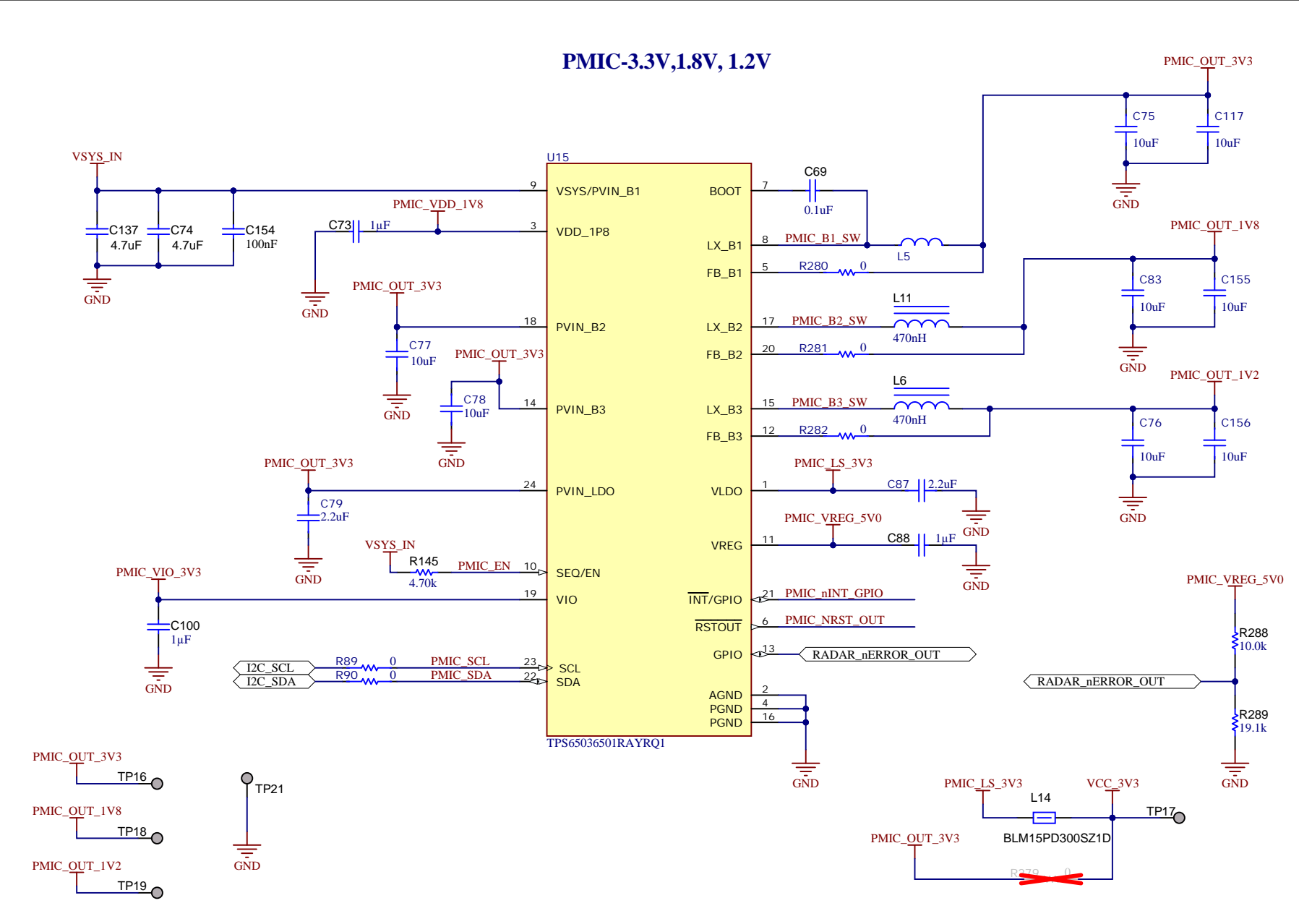


D



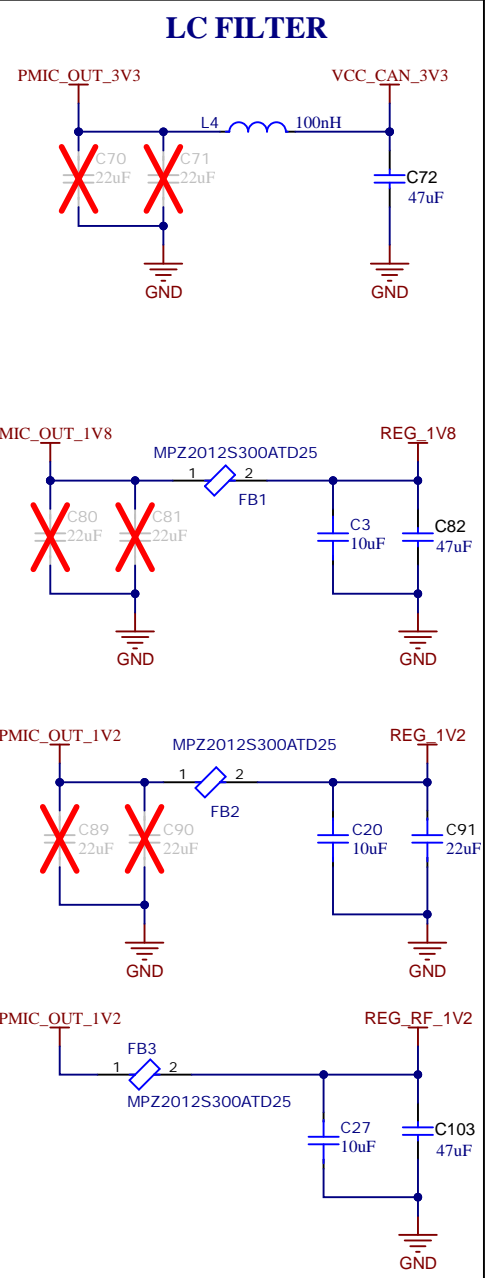
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

A

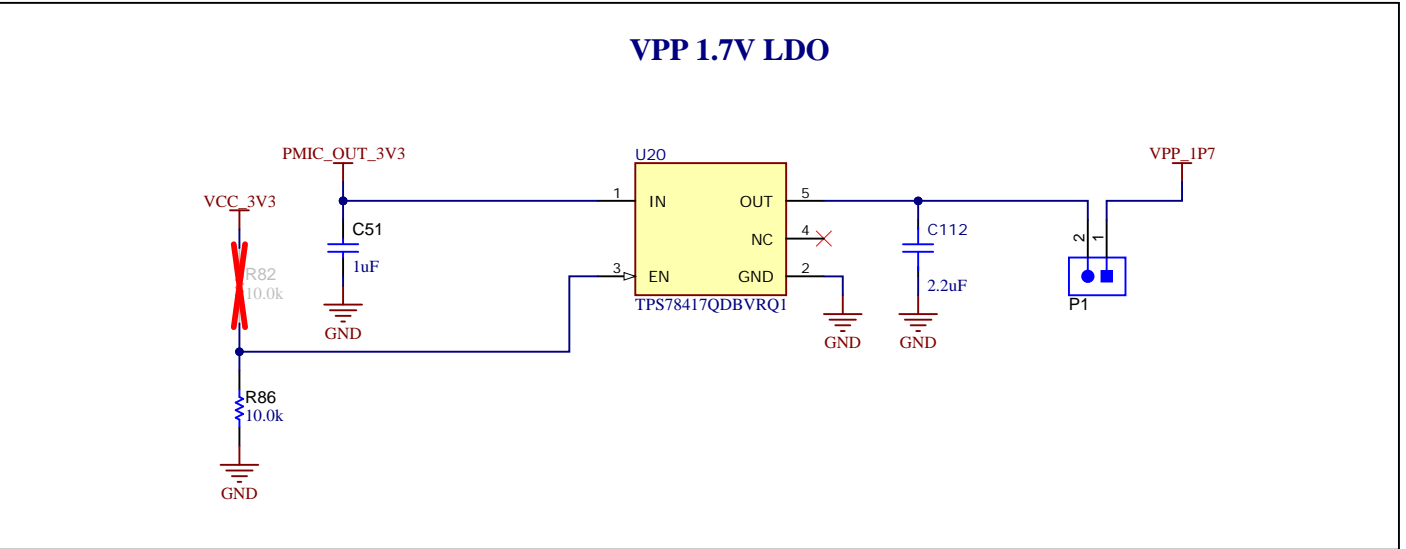


D

A



D

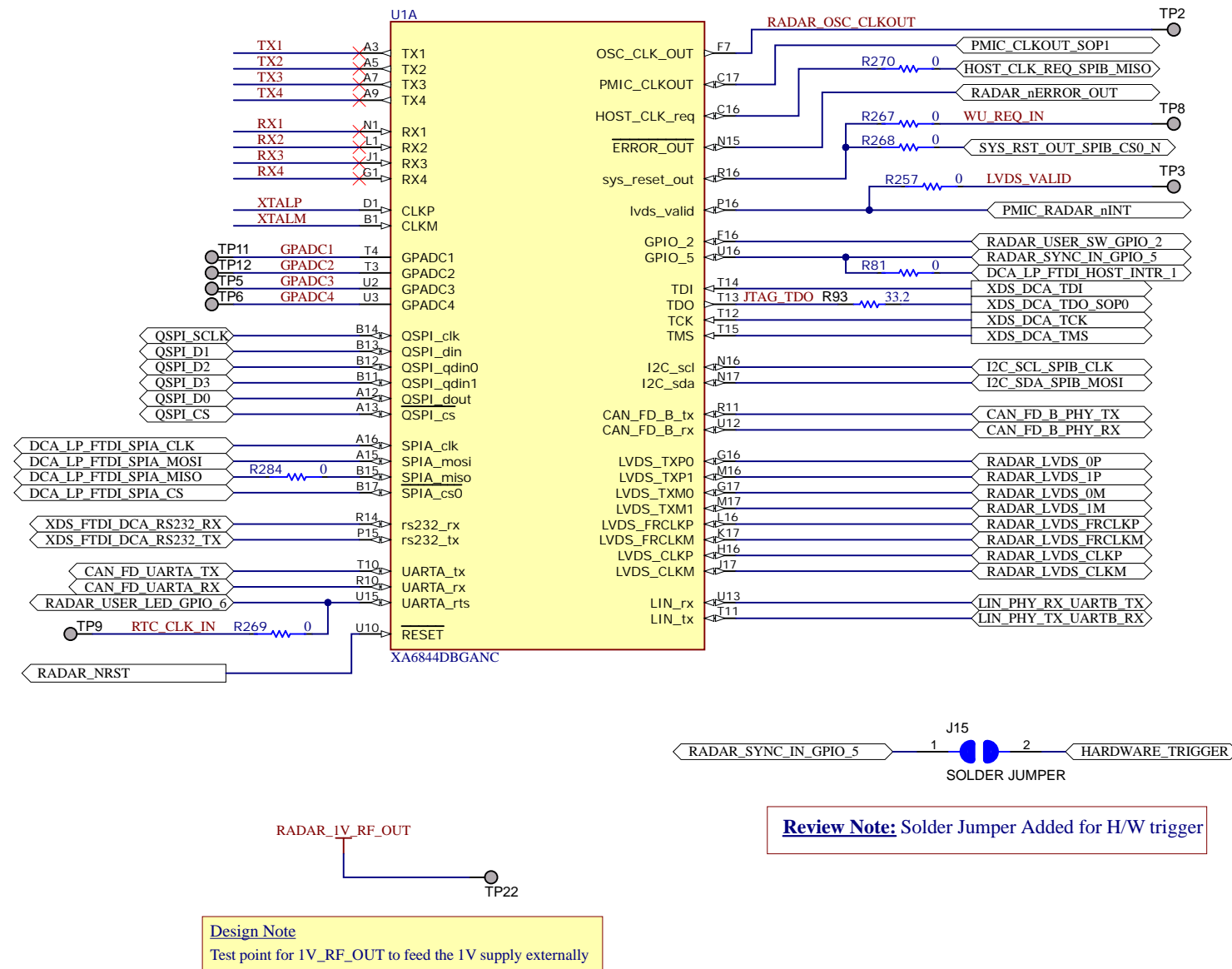


## **xWRL6844 CHIP -INTERFACE**

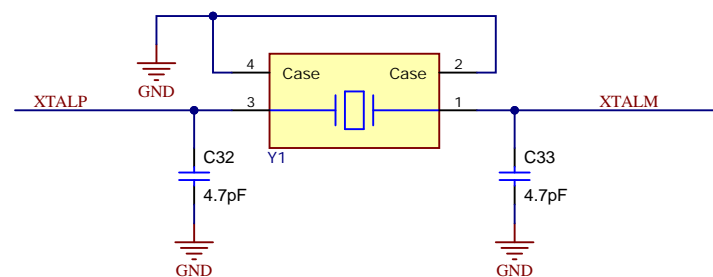
## xWRL6844 CHIP -POWER

**Design Note:**

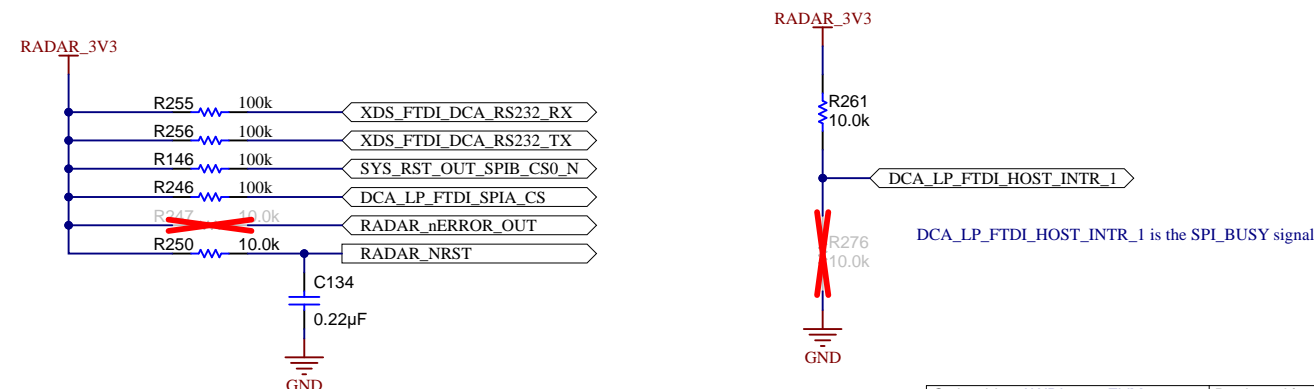
1. Antenna traces are GCPW traces
2. 'Generic No ERCs' were placed intentionally on Single Port RF Tx, Rx lines



## 40 MHz CRYSTAL OSCILLATOR



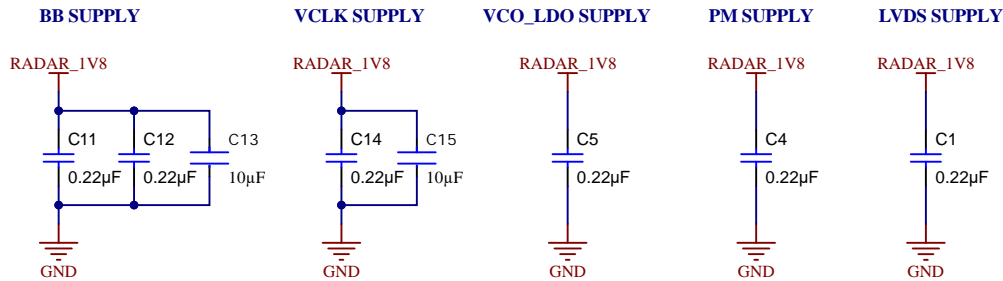
Alternate Crystal part number : CX2016SA40000D0PTWC1



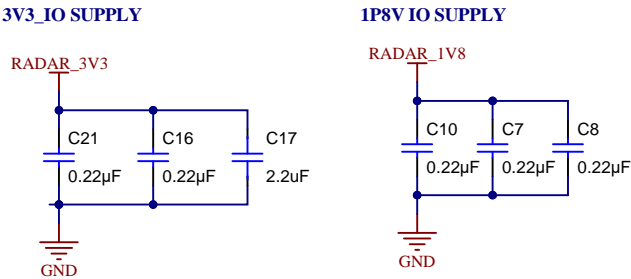
Orderable: <a href="#">AWRL6844EVM</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 25-11-2024	 <b>TEXAS INSTRUMENTS</b>  <a href="http://www.ti.com">http://www.ti.com</a> © Texas Instruments 2023
TID #: <a href="#">N/A</a>	Project Title: <a href="#">xWRL6844 EVM</a>		
Number: <a href="#">PROC182</a>	Rev: <a href="#">A</a>	Sheet Title: <a href="#">xWRL6844_CHIP</a>	
SVN Rev: Not in version control	Assembly Variant: <a href="#">01_AWR</a>	Sheet: <a href="#">6</a> of <a href="#">17</a>	
Drawn By: <a href="#">Mistral</a>	File: <a href="#">PROC182A_Chip.SchDoc</a>	Size: B	
Engineer: <a href="#">Mistral</a>	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>		

SUPPLY\_DECOUPLING\_CAPS

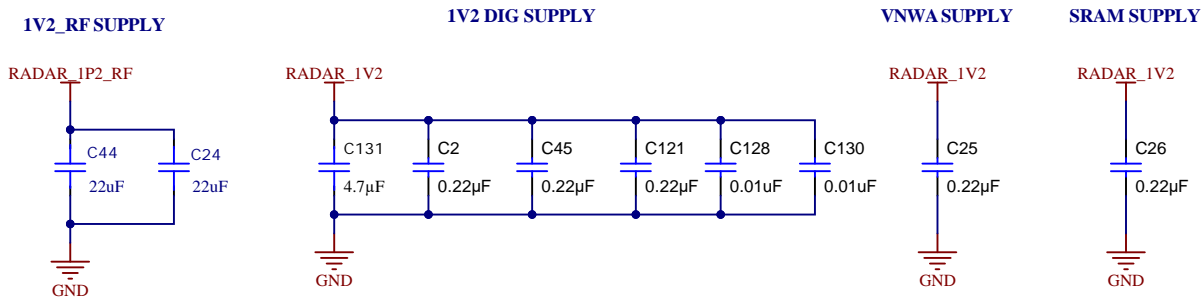
1.8V POWER SUPPLY VOLTAGE RAILS



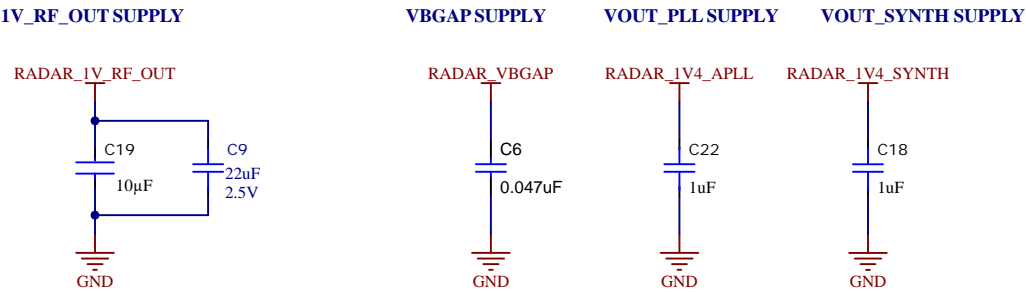
I/O SUPPLY VOLTAGE RIALS



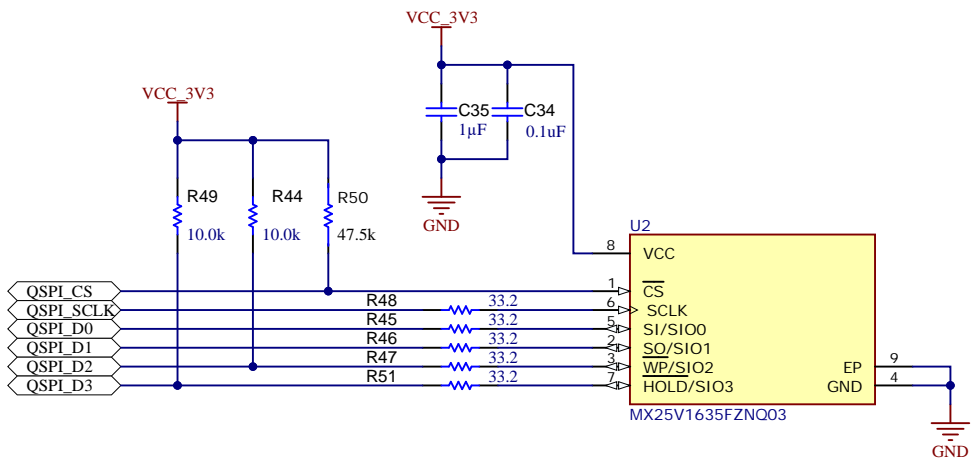
1.2V POWER SUPPLY VOLTAGE RAILS



INTERNAL GENERATED VOLTAGE RAILS



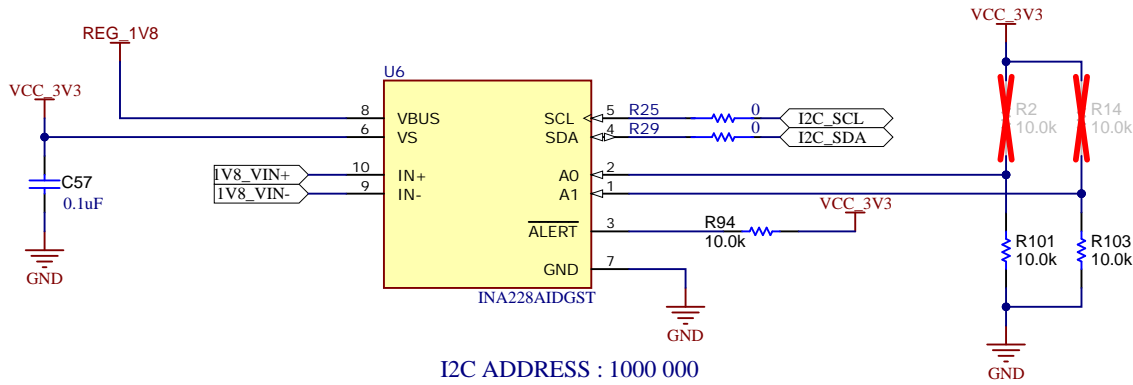
QSPI FLASH



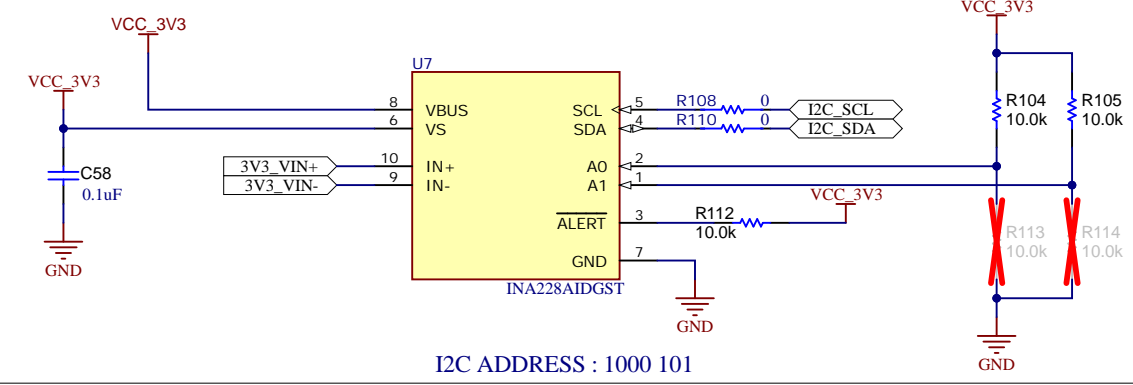
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: <a href="#">AWRL6844EVM</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 25-11-2024
TID #: N/A	Project Title: <a href="#">xWRL6844 EVM</a>	
Number: <a href="#">PROC182</a>	Rev: <a href="#">A</a>	Sheet Title: <a href="#">DECOUPLING_CAPS</a>
SVN Rev: Not in version control	Assembly Variant: <a href="#">01_AWR</a>	Sheet: <a href="#">7</a> of <a href="#">17</a>
Drawn By: <a href="#">Mistral</a>	File: <a href="#">PROC182A_Decoupling_caps-QSPI Flash.Sch</a>	Size: <a href="#">B</a>
Engineer: <a href="#">Mistral</a>	Contact: <a href="#">http://www.ti.com/support</a>	

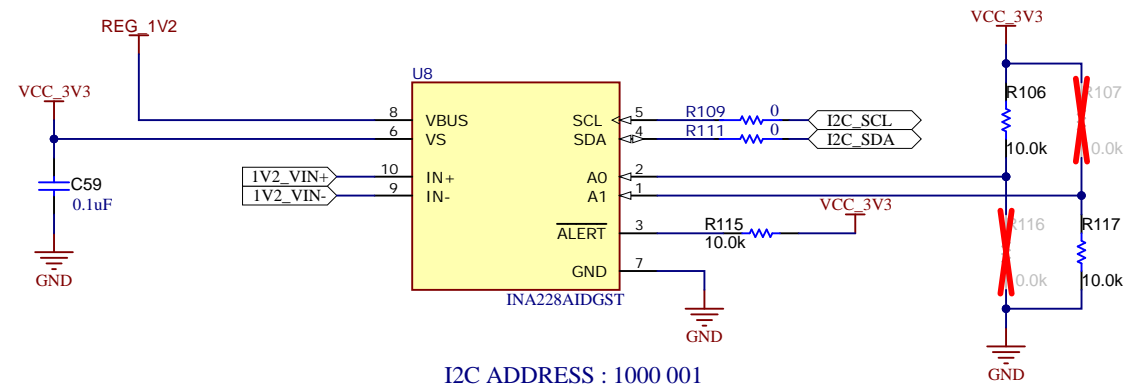
CURRENT SENSOR- 1V8



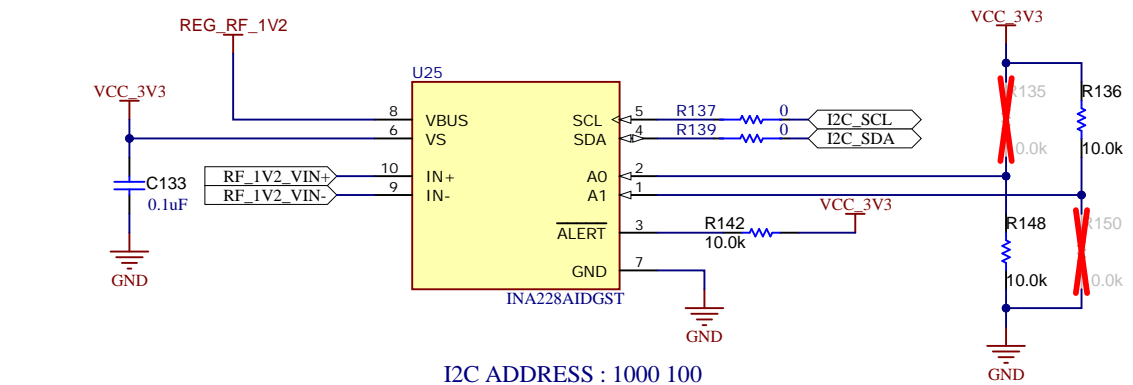
CURRENT SENSOR- 3V3



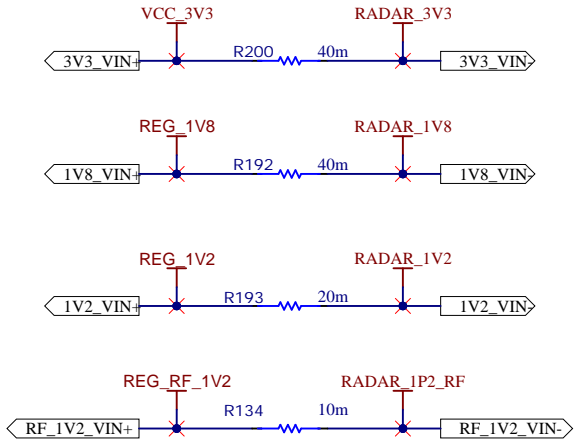
CURRENT SENSOR- 1V2



CURRENT SENSOR- RF\_1V2

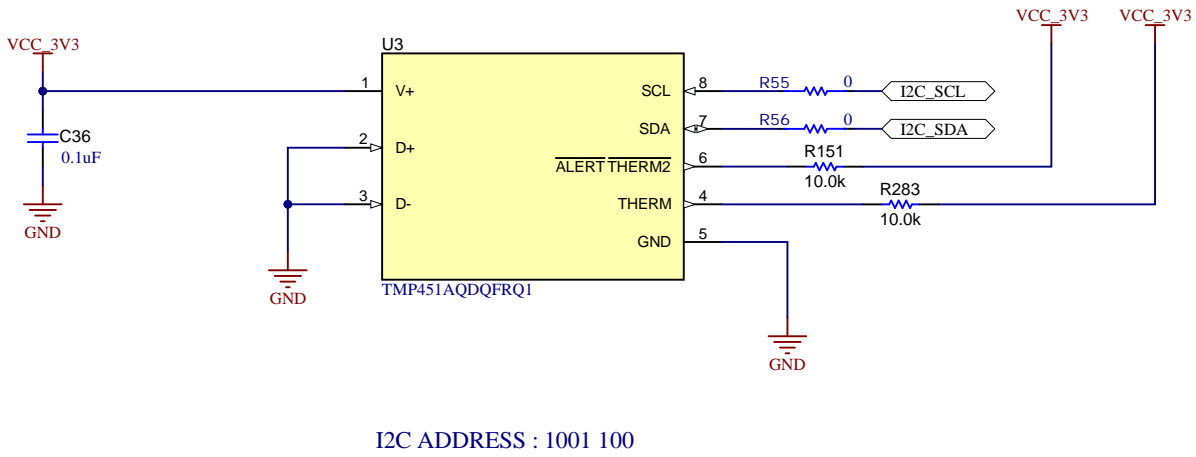


CURRENT SENSE RESISTORS

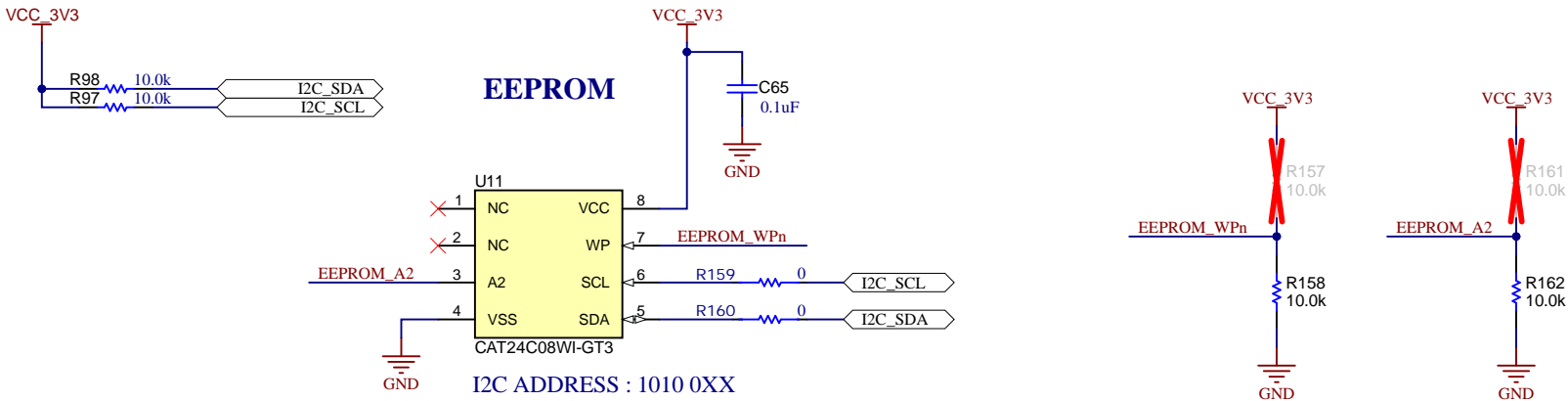


Design Note: 'Generic No ERCs' were placed intentionally on either sides of Current sense resistors

TEMPERATURE SENSOR



EEPROM





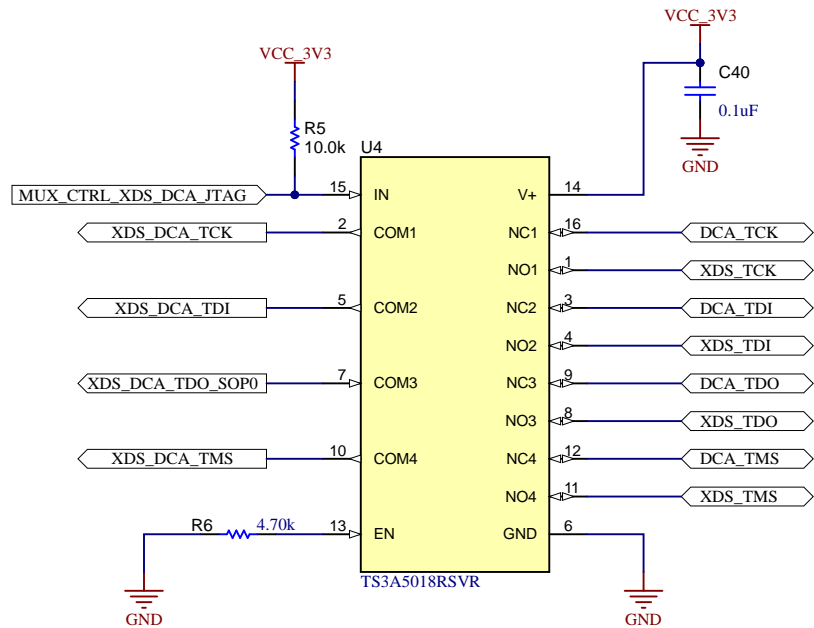
A

B

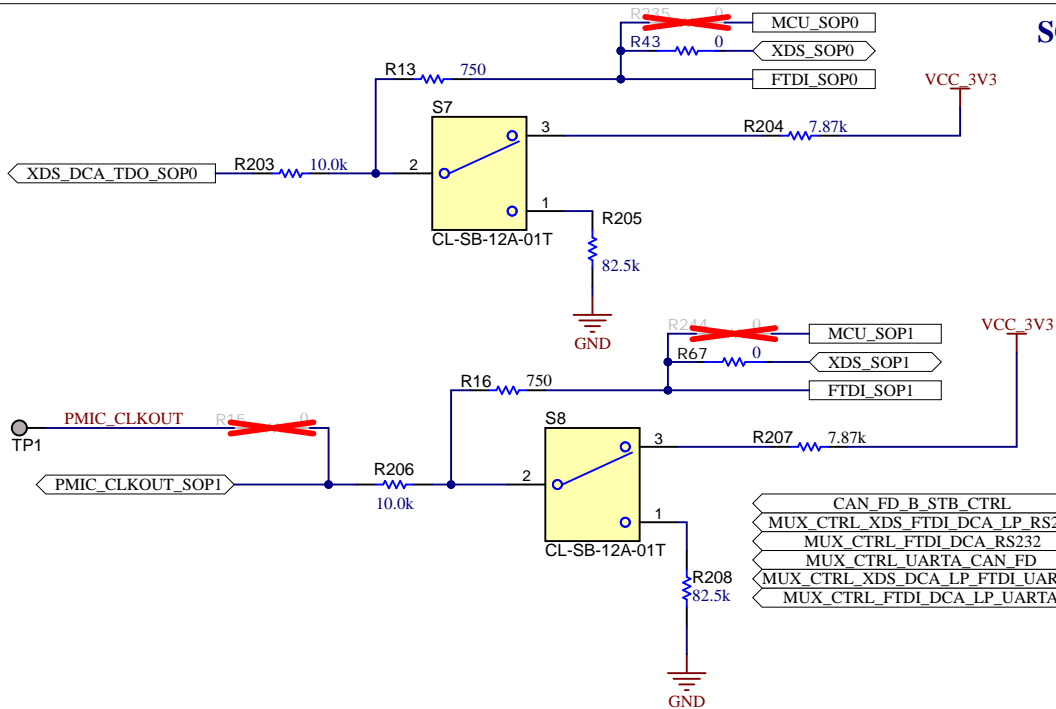
A

B

### JTAG-ANALOG MUX



### SOP & MUX CONTROL



MUX / CONTROL TABLE

	Switch Position OFF	Switch Position ON
S4.1	CAN PHY : Stand-by Mode Disable	CAN PHY : Stand-by Mode Enable
S4.2	LIN PHY : Enable	LIN PHY : Disable
S4.3	FTDI SPI	DCA SPI
S4.4	XDS_JTAG	DCA_JTAG
S4.5	UARTB	LIN
S4.6	SPIB	I2C/ HOST_CLK_REQ/SYS_RST_OUT

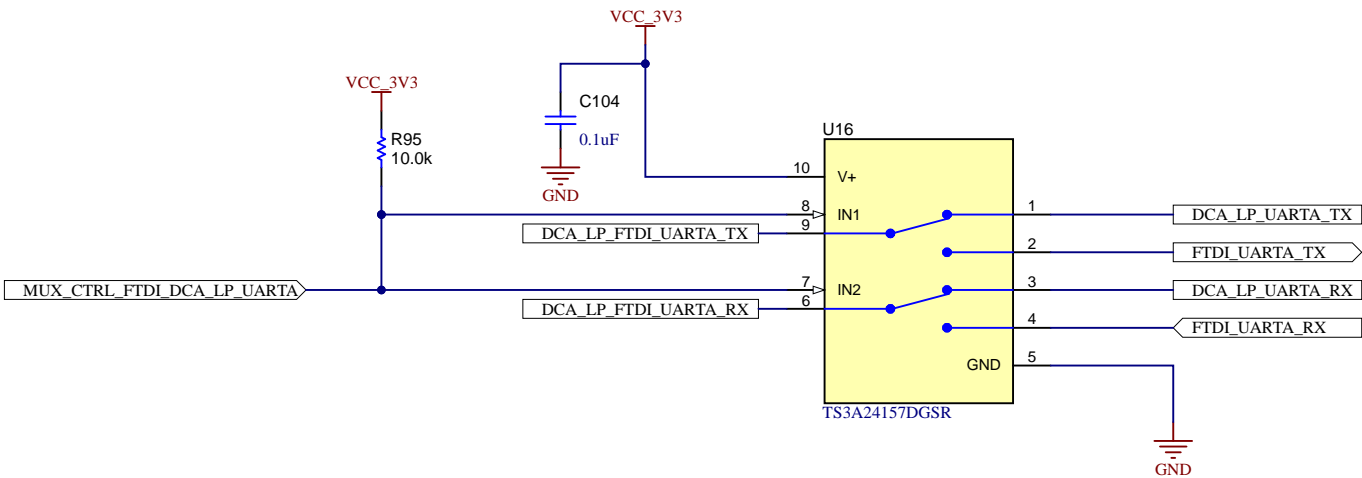
MUX / CONTROL TABLE

	Switch Position OFF	Switch Position ON
S1.1	CAN B PHY : Stand-by Mode Disable	CAN B PHY : Stand-by Mode Enable
S1.2	XDS_RS232	FTDI_DCA_LP/BP_RS232
S1.3	FTDI_RS232	DCA_LP/BP_RS232
S1.4	CAN_FD	XDS_DCA_LP/BP_FTDI_UARTA
S1.5	DCA_LP/BP_FTDI_UARTA	XDS_UARTA
S1.6	FTDI_UARTA	DCA_LP/BP_UART

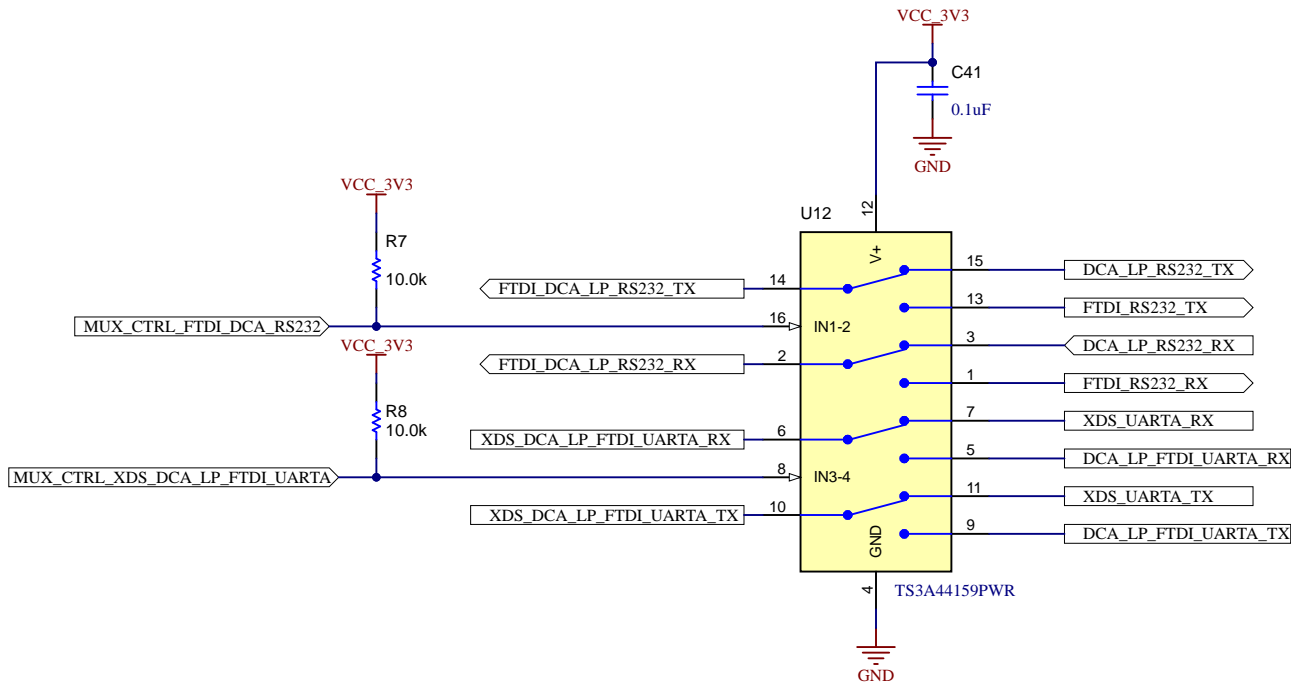
SOP CONFIGURATION

SOP Mode	PMIC_CLK_OUT, TDO	Combination	S8(SOP1)	S7(SOP0)
SOP_MODE1	Device management mode / QSPI Flashing mode	0 0	2-1	2-1
SOP_MODE2	Application mode / Functional mode	0 1	2-1	2-3
SOP_MODE4	Debug mode / mmWave studio connectivity mode	1 1	2-3	2-3

### ANALOG MUX - FTDI UARTA / DCA\_LP UARTA



### UARTA, RS232-ANALOG SWITCH



A

B

C

D

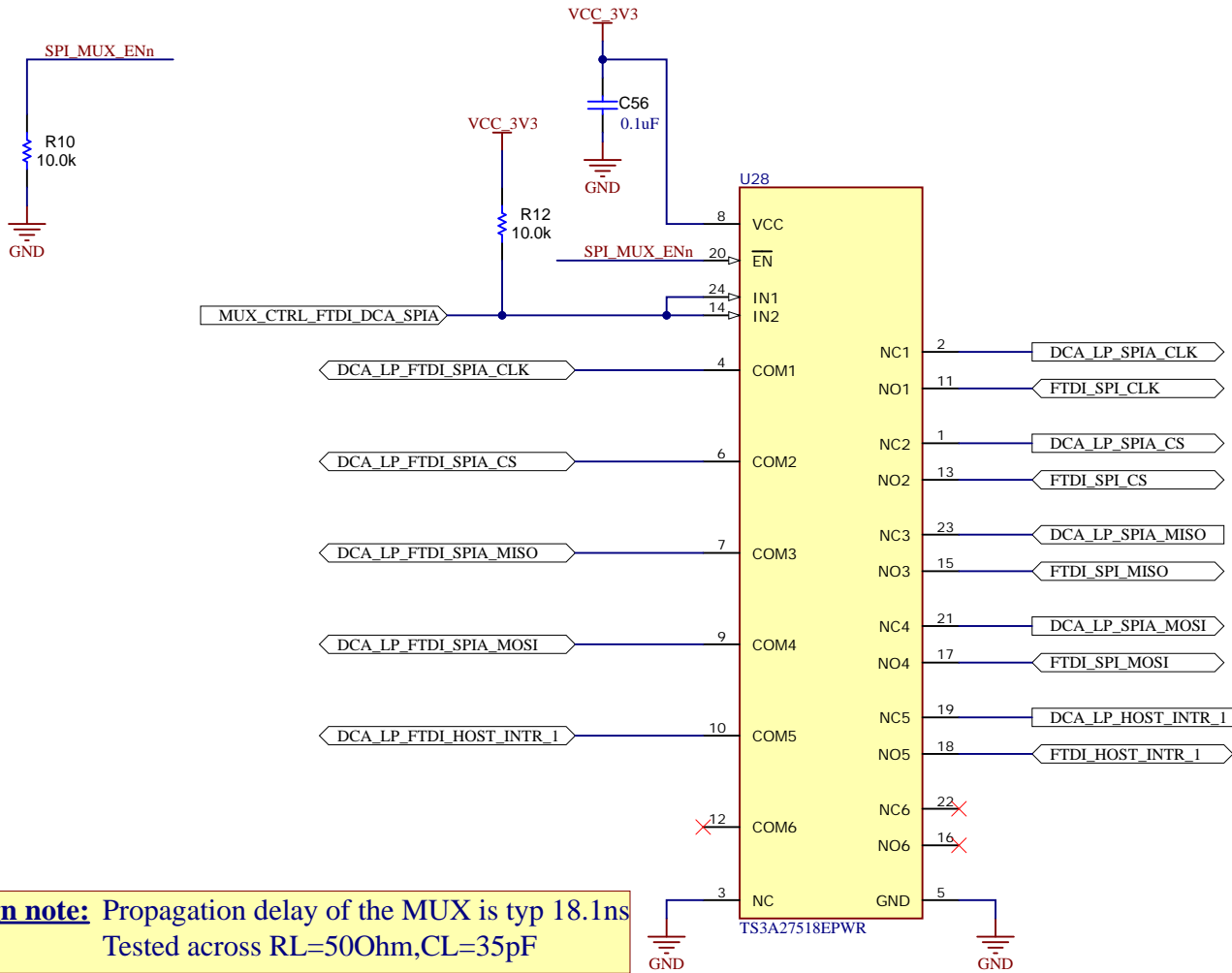
A

B

C

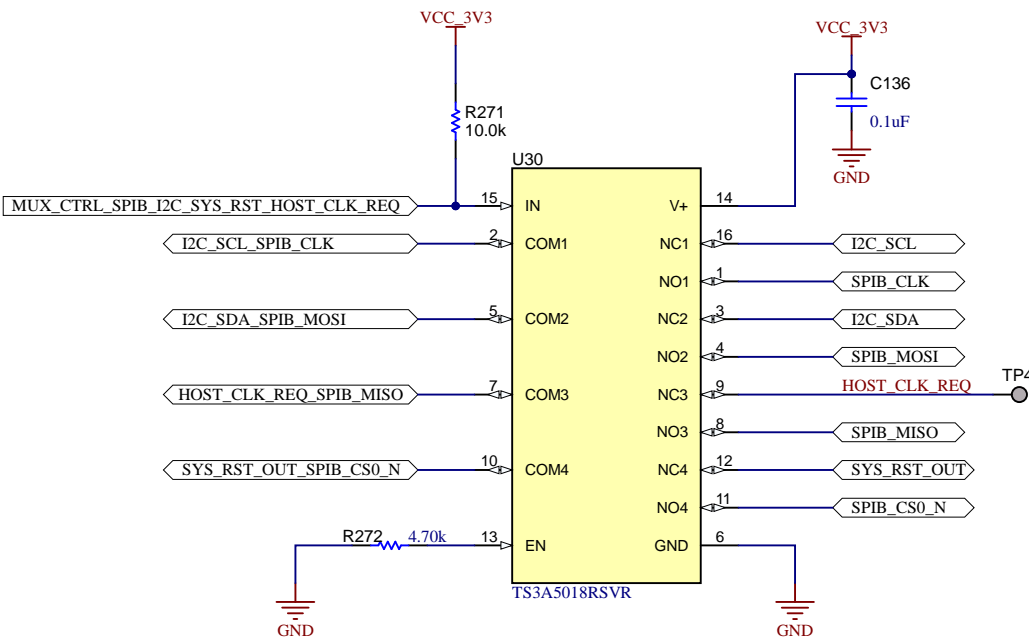
D

ANALOG MUX SPIA- DCA/FTDI

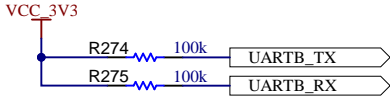
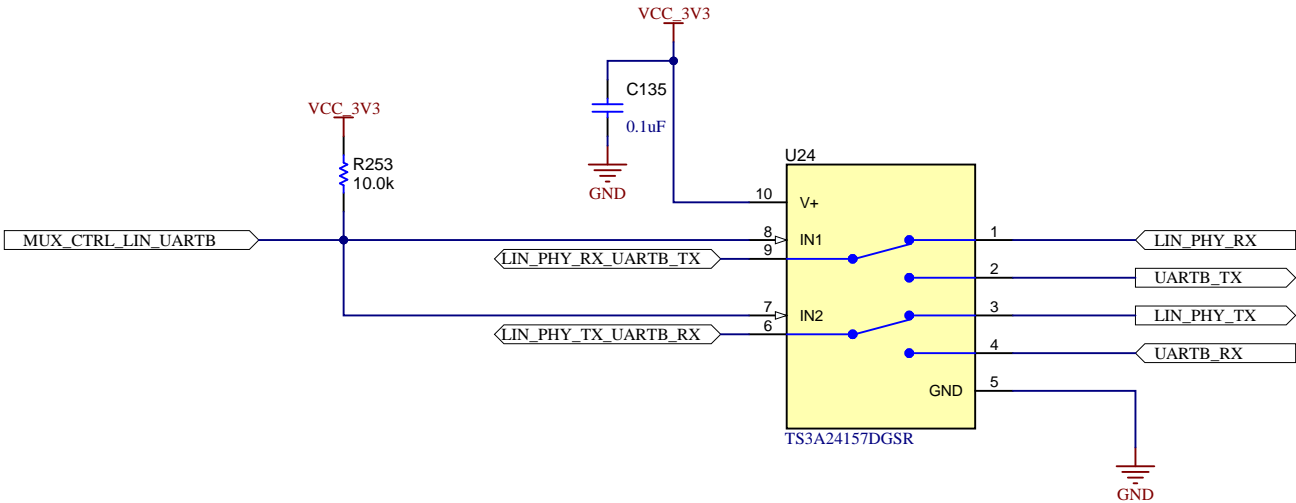


**Design note:** Propagation delay of the MUX is typ 18.1ns  
Tested across RL=50Ohm,CL=35pF

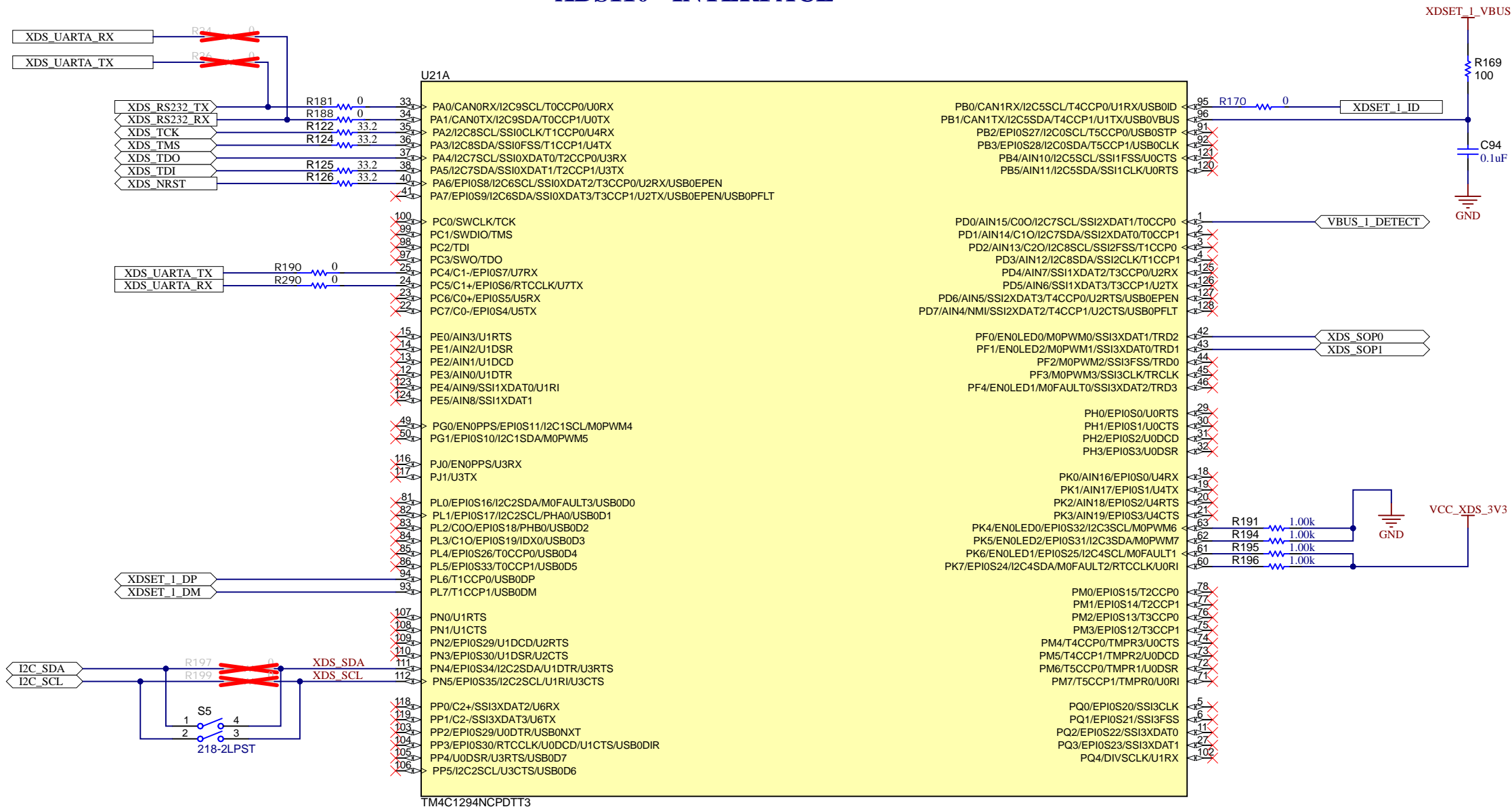
ANALOG MUX- SPI B/ I2C, LVDS VALID, SYS RESET OUT (OPTIONAL)



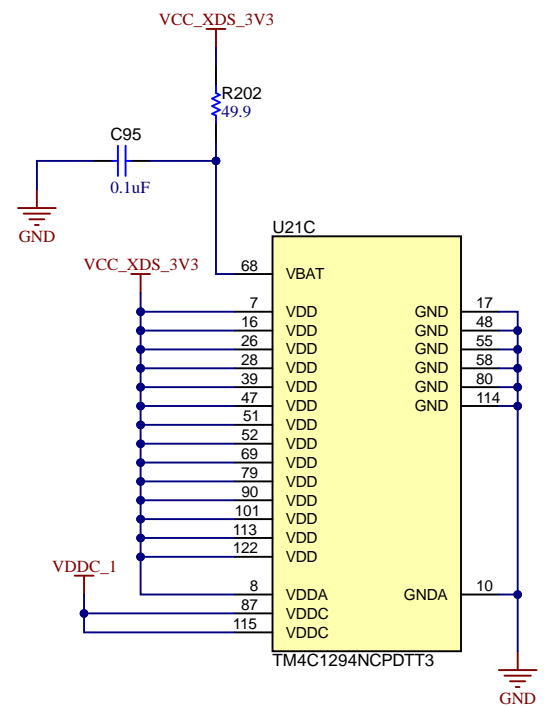
ANALOG MUX - LIN/UARTB



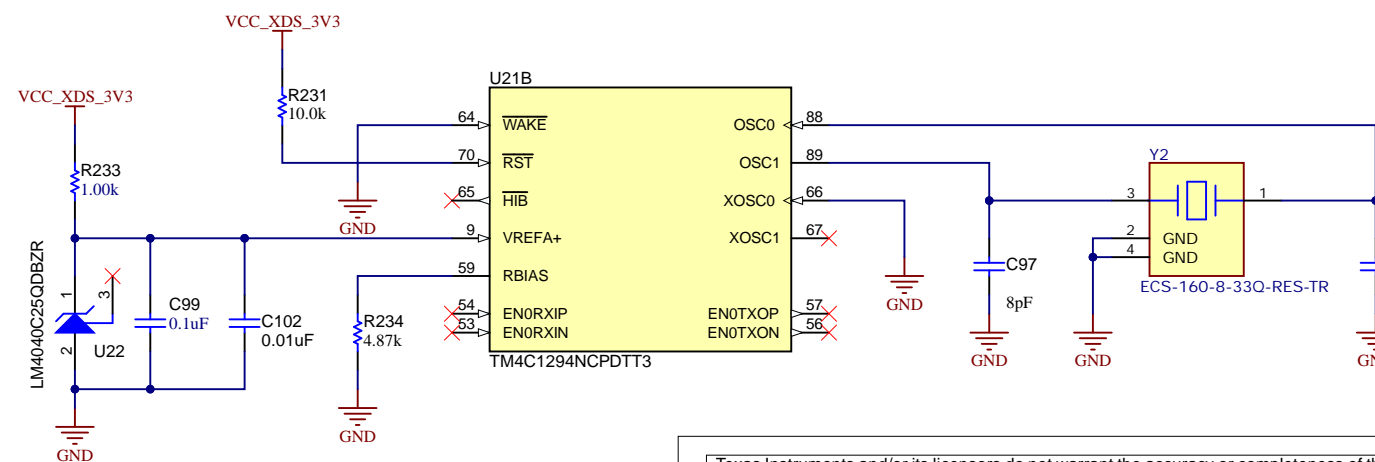
## XDS110 - INTERFACE



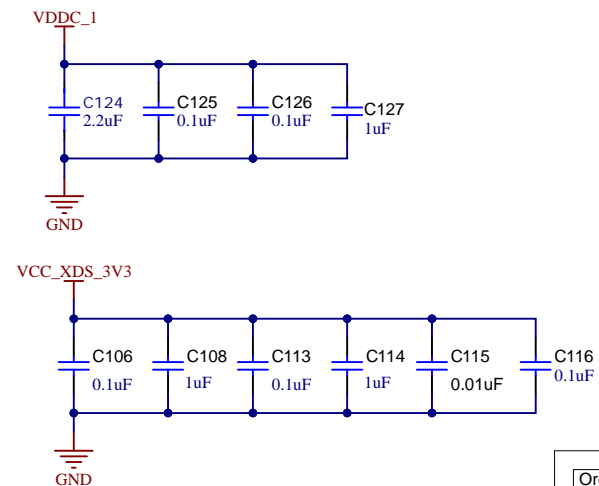
## XDS110 - POWER



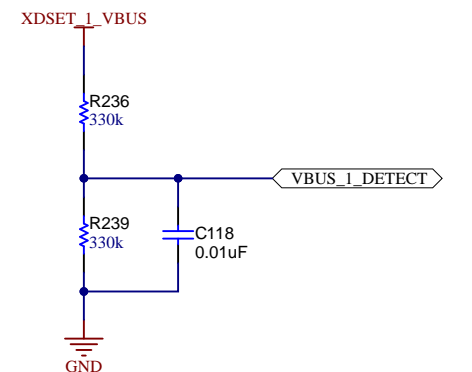
## XDS110 - XTAL



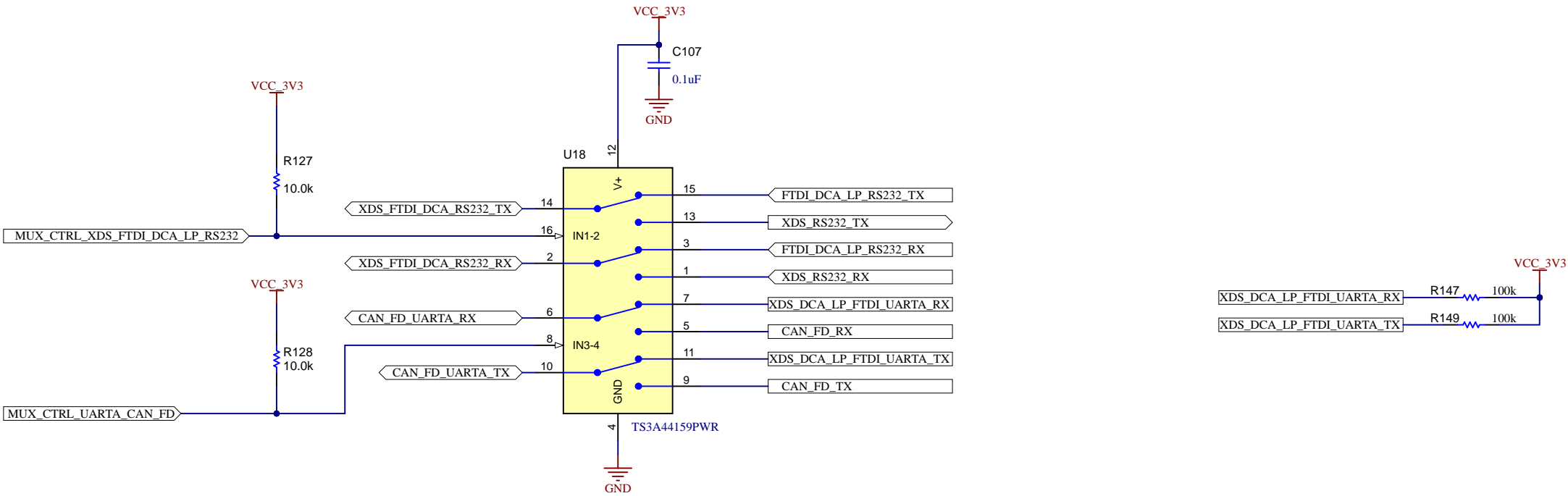
## DECOUPLING CAPS - XDS



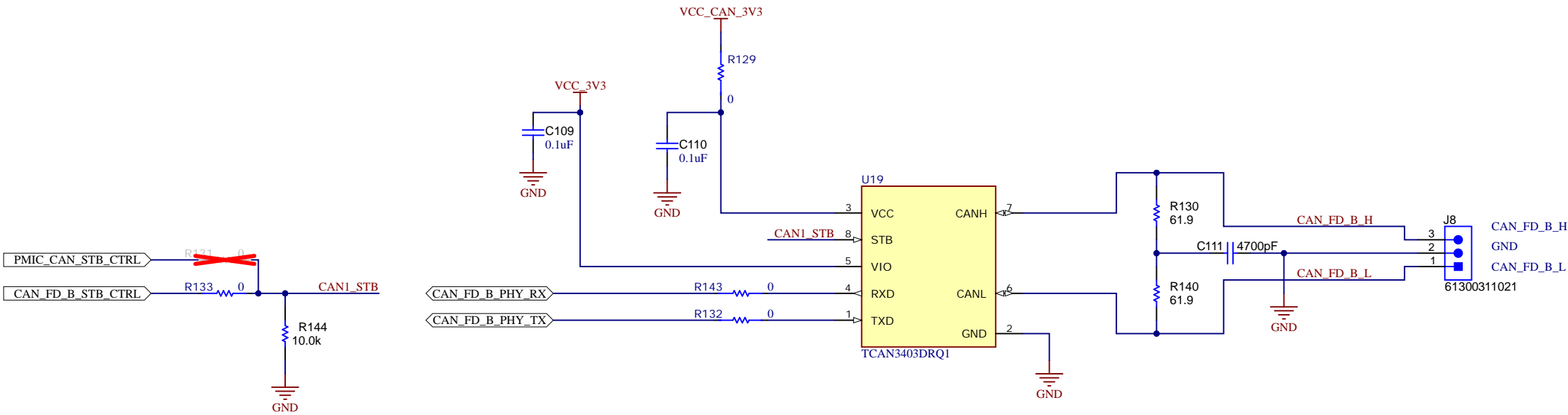
## VBUS\_DETECT



ANALOG MUX -XDS /FTDI, DCA RS232, CAN\_FD / UART A



CAN\_FD\_B\_TRANSCEIVER



Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: <a href="#">AWRL6844EVM</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: 25-11-2024
TID #: <a href="#">N/A</a>	Project Title: <a href="#">xWRL6844 EVM</a>	
Number: <a href="#">PROC182</a>	Rev: <a href="#">A</a>	Sheet Title: <a href="#">ANALOG MUX AND CAN_FD_B</a>
SVN Rev: <a href="#">Not in version control</a>	Assembly Variant: <a href="#">01_AWR</a>	Sheet: <a href="#">12 of 17</a>
Drawn By: <a href="#">Mistral</a>	File: <a href="#">PROC182A_MUX_CAN_FD.SchDoc</a>	Size: <a href="#">B</a>
Engineer: <a href="#">Mistral</a>	Contact: <a href="#">http://www.ti.com/support</a>	

A

B

C

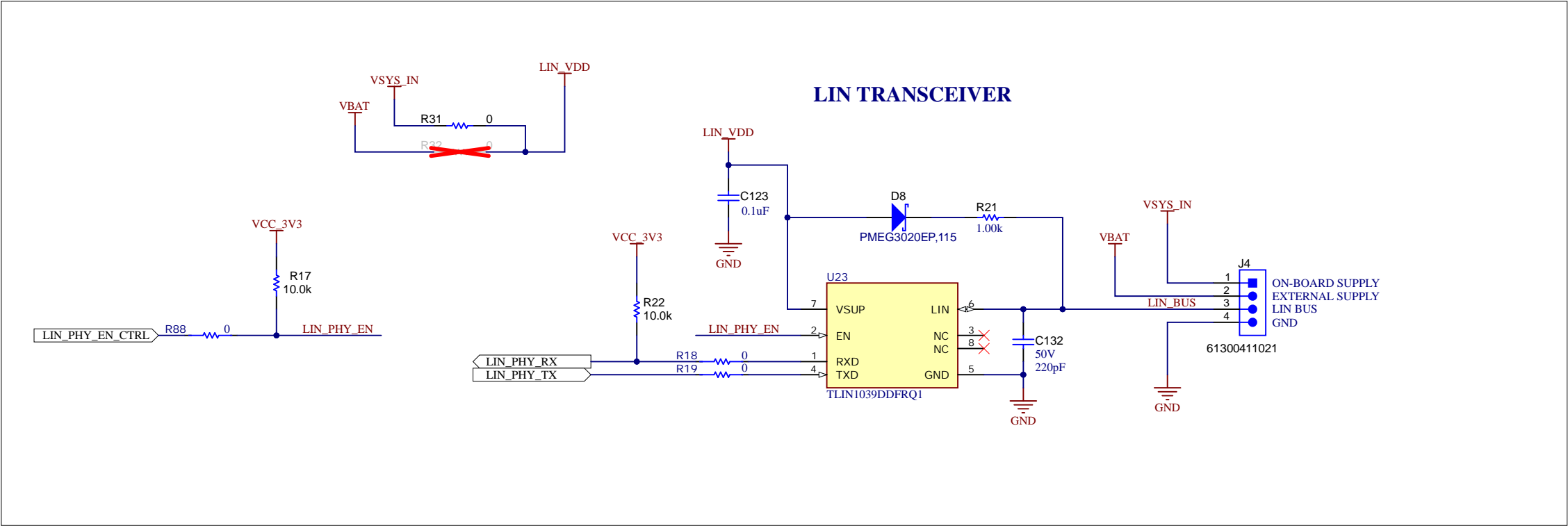
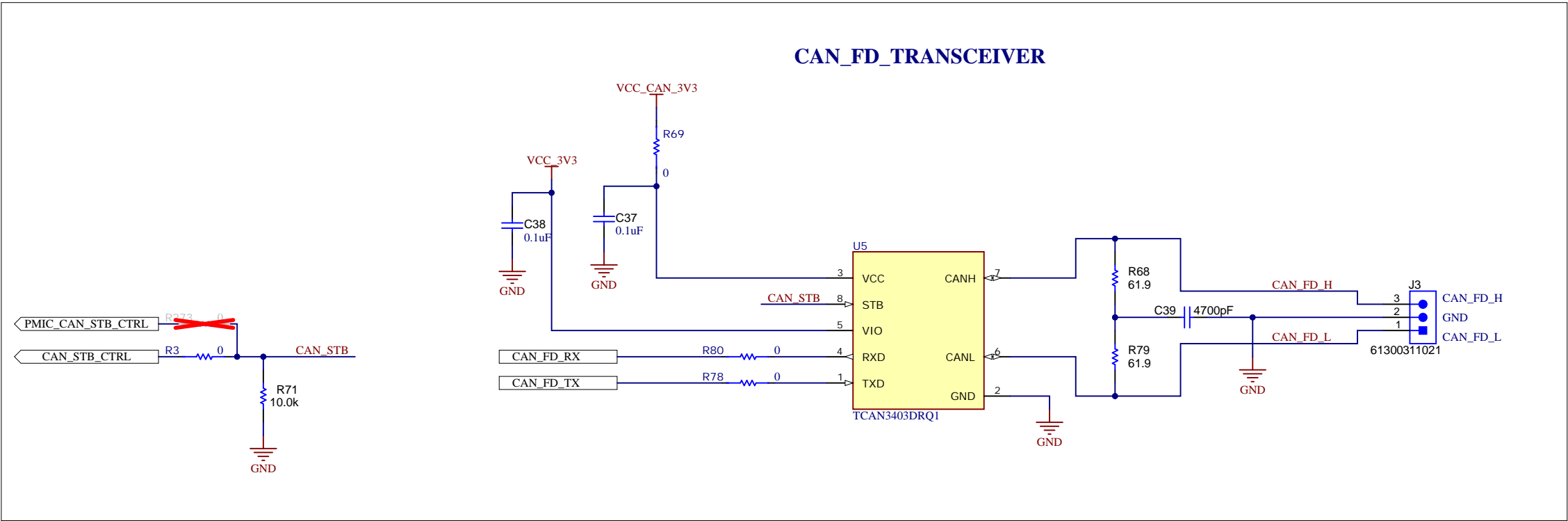
D

A

B

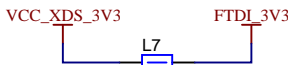
C

D





# FTDI - USB to SPI CONVERTER

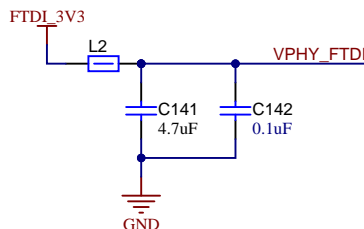
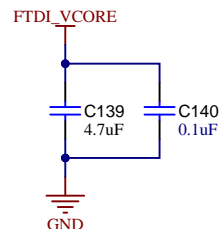


Review Note

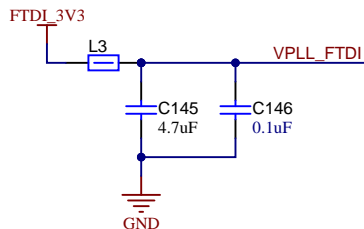
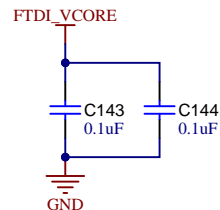
FTDI\_3V3 Power from XDS LDO 3V3

## FTDI SUPPLY DECAPS

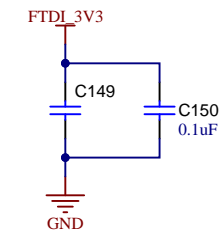
VCORE DECAPS



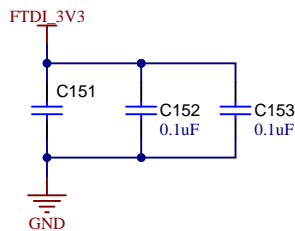
VREGOUT DECAPS



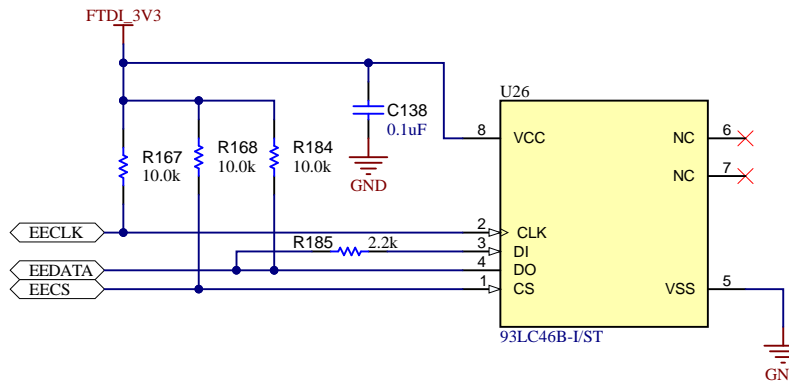
VREGIN DECAPS



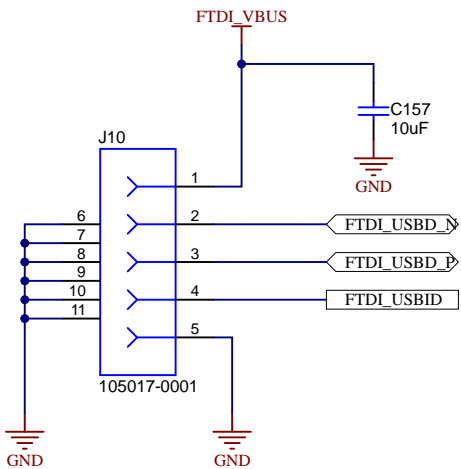
VCCIO DECAPS



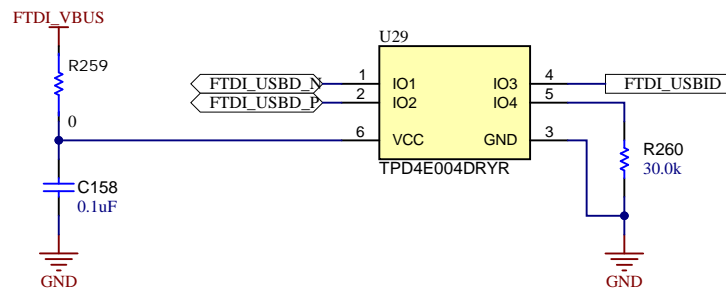
## FTDI EEPROM



## FTDI USB PORT



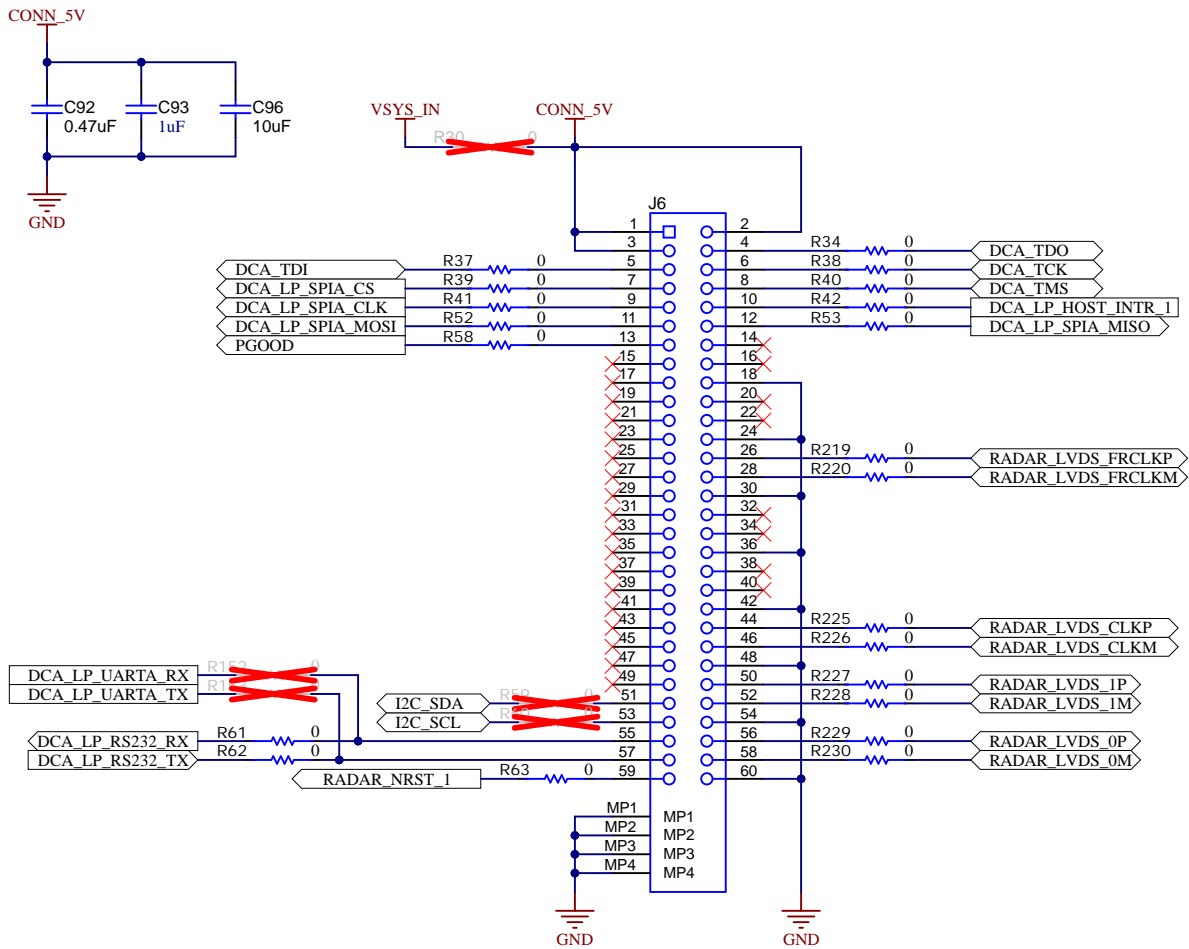
## FTDI USB - ESD PROTECTION



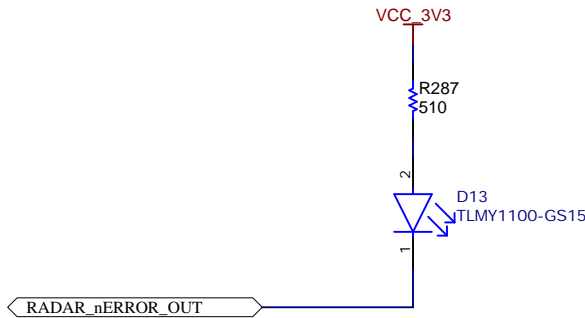
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: <b>AWRL6844EVM</b>	Designed for: <b>Public Release</b>	Mod. Date: <b>25-11-2024</b>
TID #: <b>N/A</b>	Project Title: <b>xWRL6844 EVM</b>	
Number: <b>PROC182</b>	Rev: <b>A</b>	Sheet Title: <b>FTDI_USB to SPI/12C/UART_Converter</b>
SVN Rev: <b>Not in version control</b>	Assembly Variant: <b>01_AWR</b>	Sheet: <b>14 of 17</b>
Drawn By: <b>Mistral</b>	File: <b>PROC182A_FTDI.SchDoc</b>	Size: <b>B</b>
Engineer: <b>Mistral</b>	Contact: <b>http://www.ti.com/support</b>	

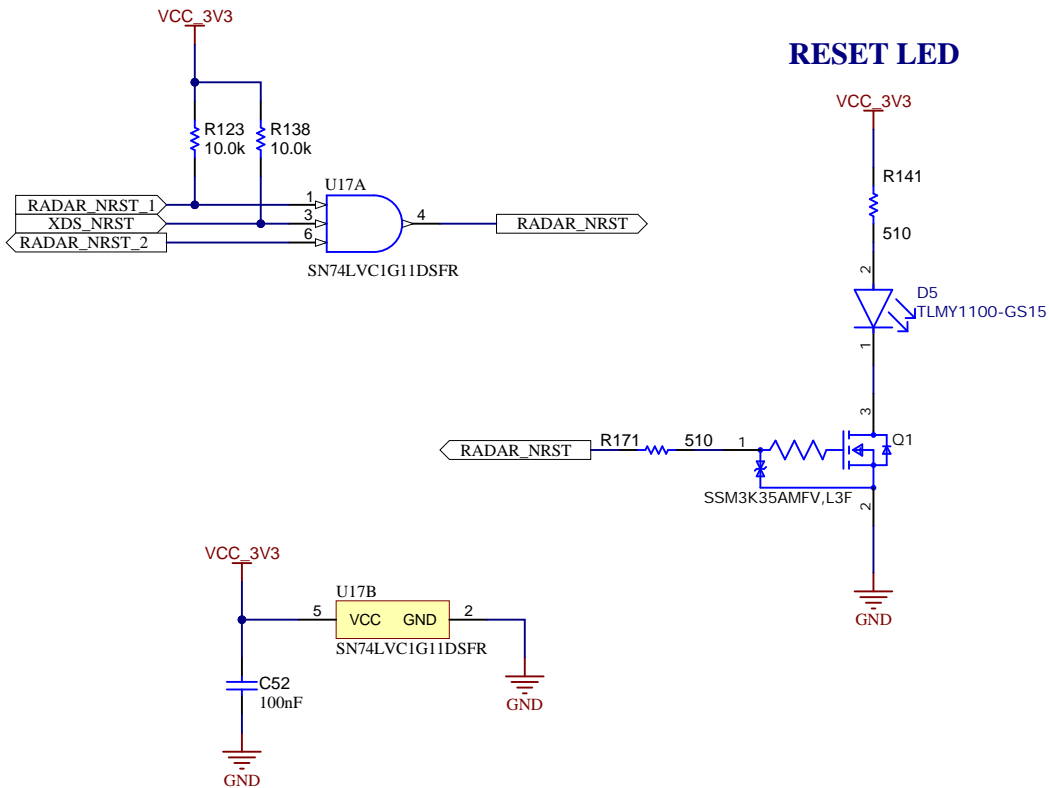
# 60-PIN HD CONNECTOR FOR DCA1000



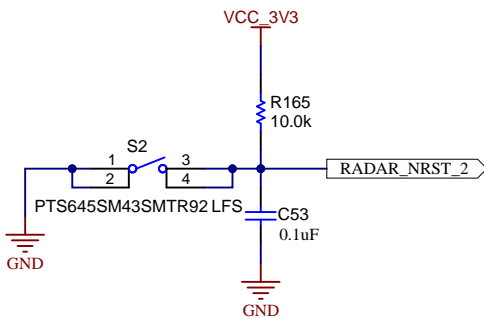
## nERROR LED



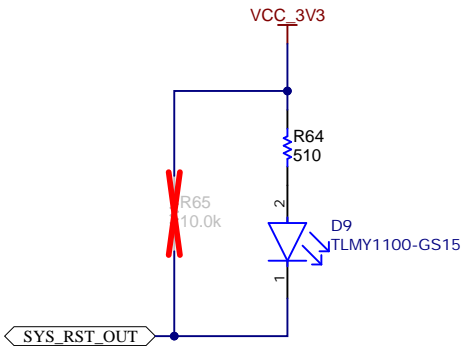
## RESET SCHEME



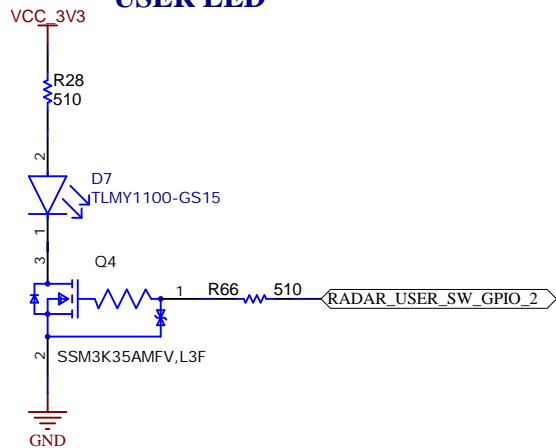
## RESET SWITCH



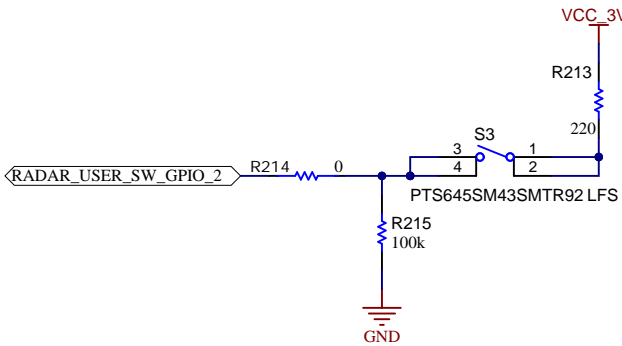
## RESET OUT LED



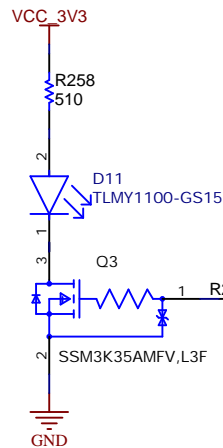
## USER LED



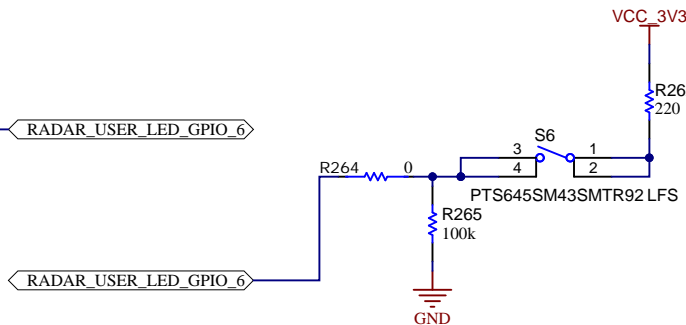
## USER SWITCH



## USER LED



## USER SWITCH

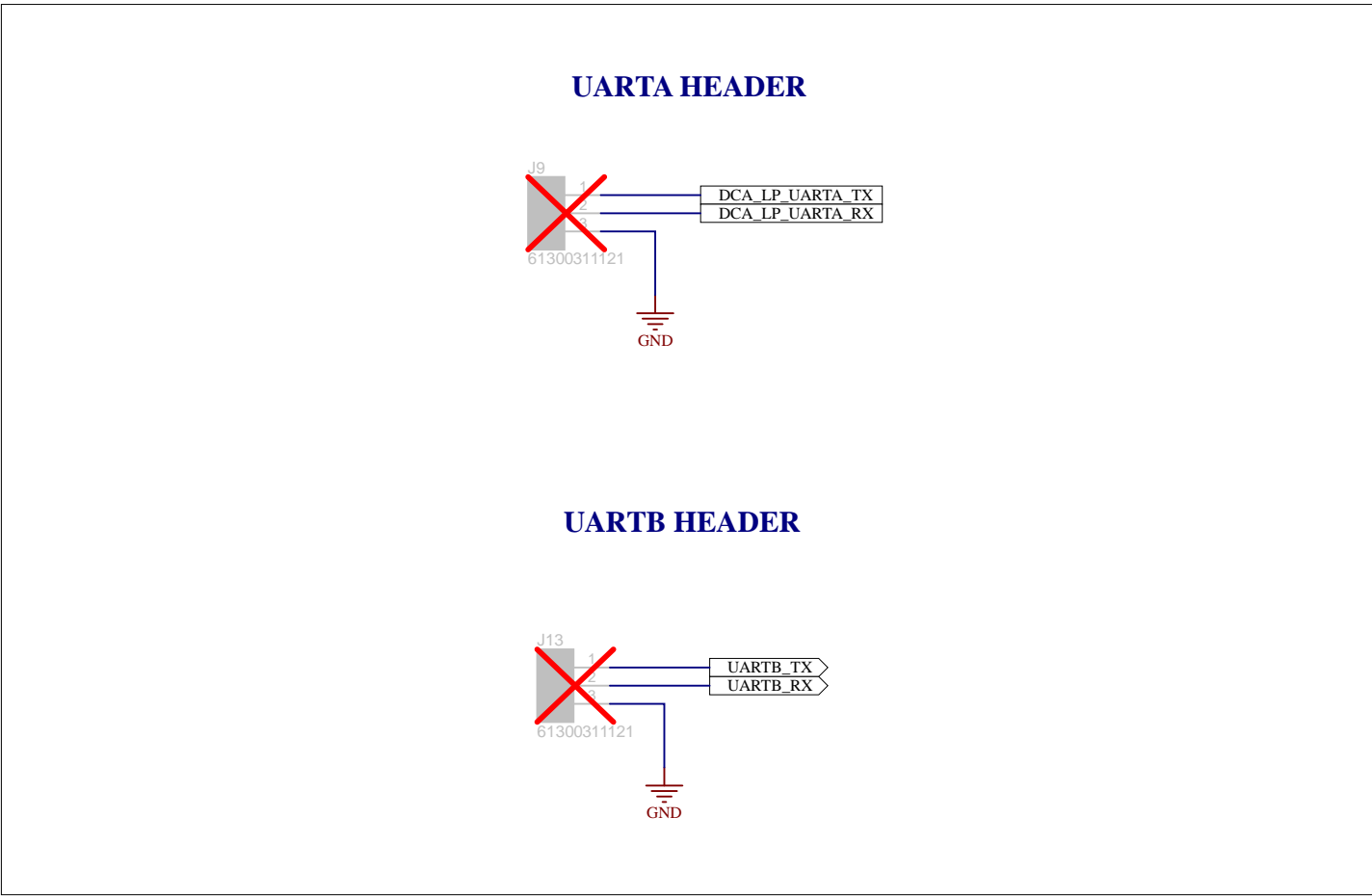
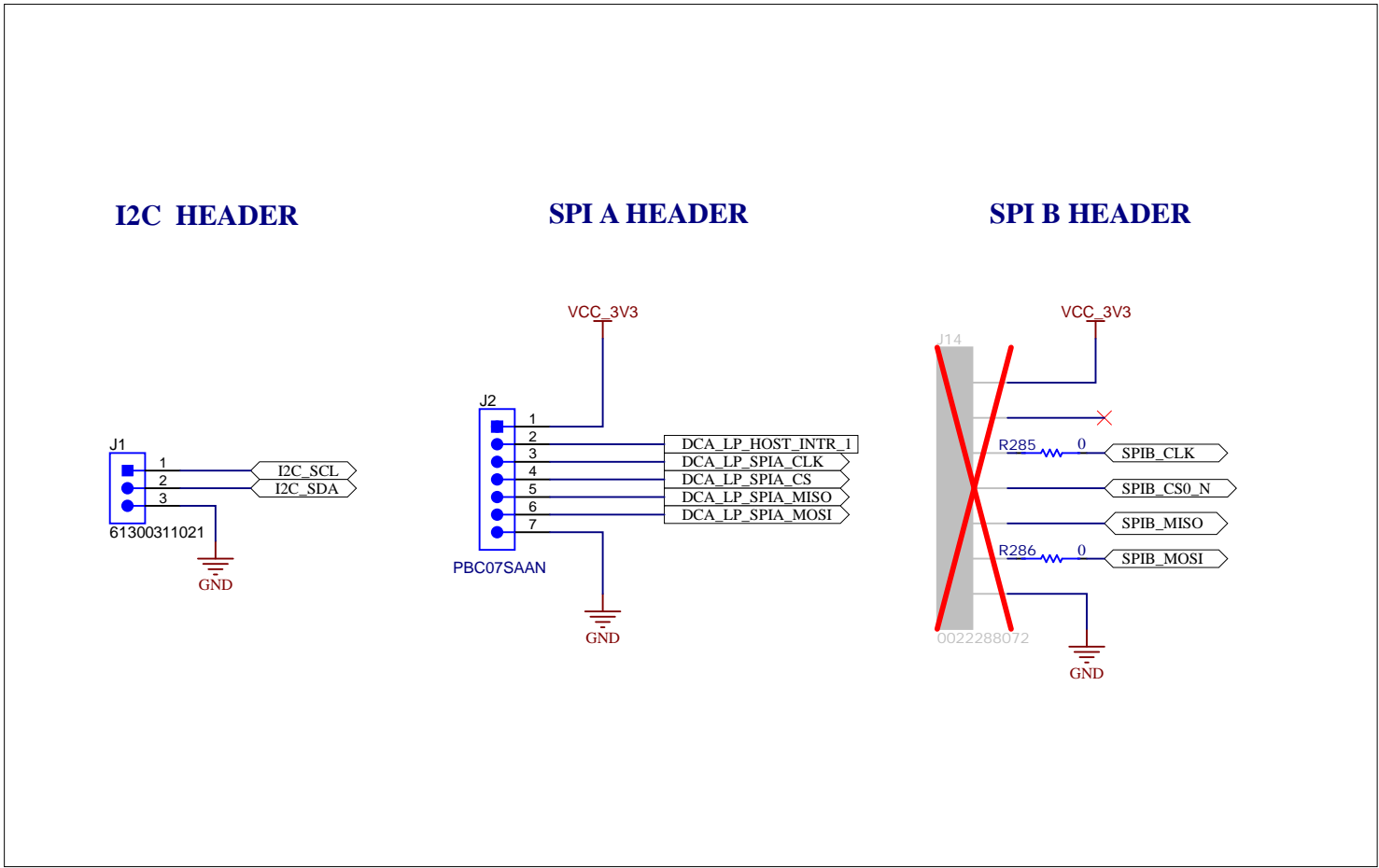


A

B

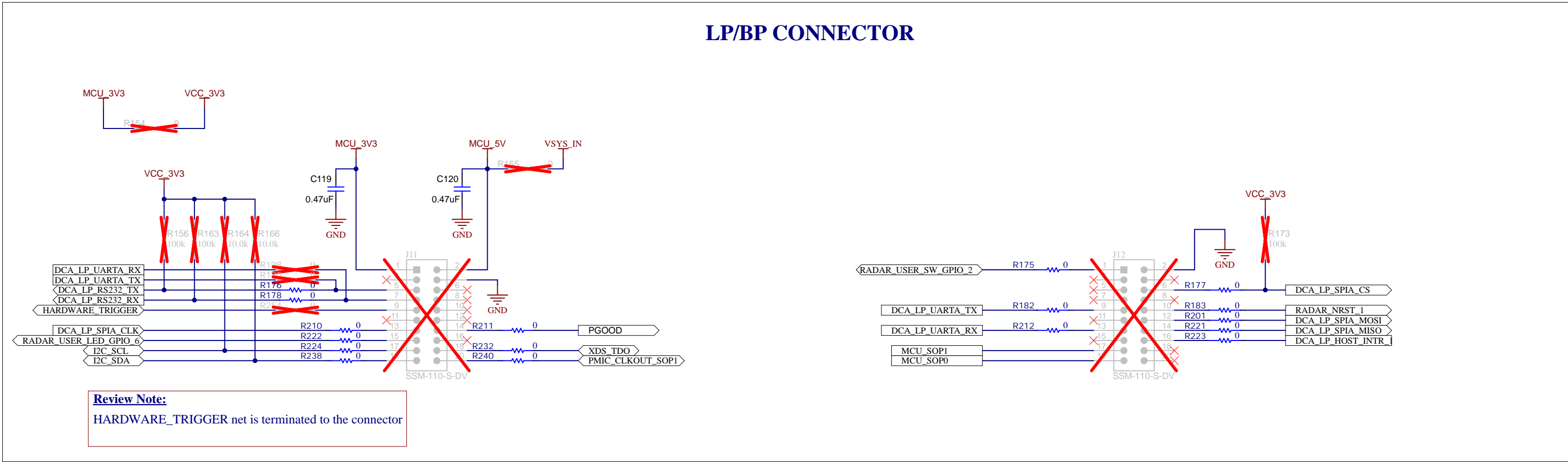
A

B



C

D





PCB Number: PROC182  
PCB Rev: A

PCB  
LOGO  
Texas Instruments



PCB  
LOGO  
FCC disclaimer

PCB  
LOGO  
WEEE logo

CAUTION HOT SURFACE1



CAUTION HOT SURFACE

Variant/Label Table	
Variant	Label Text
001_AWR	
002_IWR	

LBL1

PCB Label

THT-14-423-10  
Size: 0.65" x 0.20 "

CAPACITORS HIGHLIGHTED IN THE RED COLOR BOXES ARE ADDED FOR IMPROVEMENT AND THOSE ARE NOT MANDATORY.

ZZ1

Label Assembly Note

This Assembly Note is for PCB labels only

ZZ2

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5

Assembly Note

INDICATION FOR COMPONENTS D\* ARE GIVEN AT THEIR CATHODE SIDE.

Orderable: <a href="#">AWRL6844EVM</a>		Designed for: <a href="#">Public Release</a>	Mod. Date: 25-11-2024
TID #: <a href="#">N/A</a>		Project Title: <a href="#">xWRL6844 EVM</a>	
Number: <a href="#">PROC182</a>	Rev: <a href="#">A</a>	Sheet Title: <a href="#">HARDWARE</a>	
SVN Rev: <a href="#">Not in version control</a>		Assembly Variant: <a href="#">01_AWR</a>	Sheet: <a href="#">17</a> of <a href="#">17</a>
Drawn By: <a href="#">Mistral</a>		File: <a href="#">PROC182A_EVM_Hardware.SchDoc</a>	Size: B
Engineer: <a href="#">Mistral</a>		Contact: <a href="#">http://www.ti.com/support</a>	

1

2

3

4

5

6