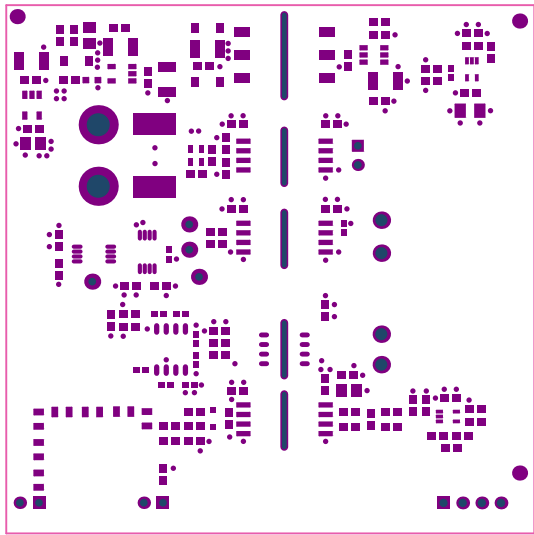
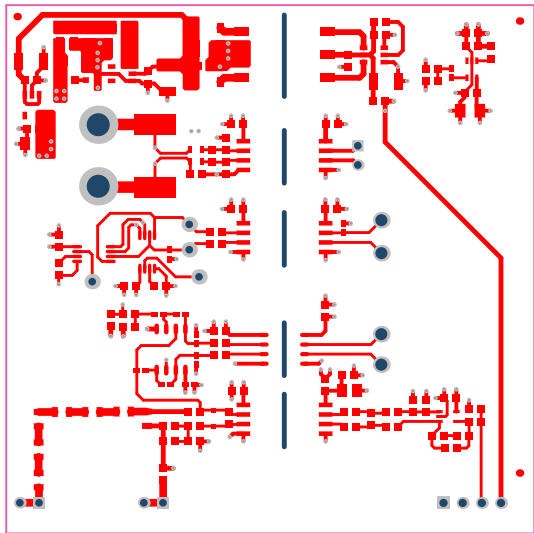


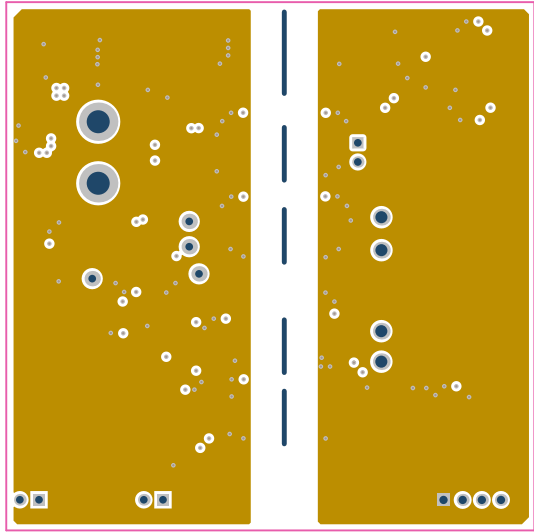
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	TIDA-010065_DC_V_I_Fault	REV: E2	SUN REV: Not In VersionControl
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PLOT NAME = Top Overlay	GENERATED	9/12/2019 11:42:38 AM	TEXAS INSTRUMENTS	



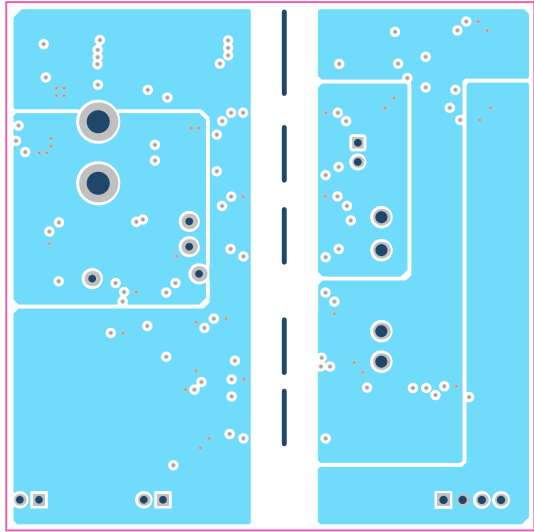
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: <small>TIDA-010065_DC_V1.1_Fault</small>	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Top Solder	TID #: TIDA-010065		
PLOT NAME = <small>Top Solder Mask</small>	GENERATED : 9/12/2019 11:42:40 AM	TEXAS INSTRUMENTS	



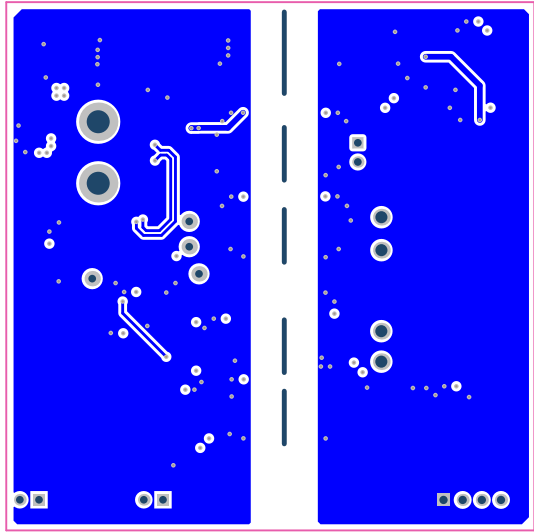
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:#TIDA-010065_DC_V1.1_Fault	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Top Layer	TID #: TIDA-010065		
PLOT NAME = Top Layer	GENERATED : 9/12/2019 11:42:41 AM	TEXAS INSTRUMENTS	



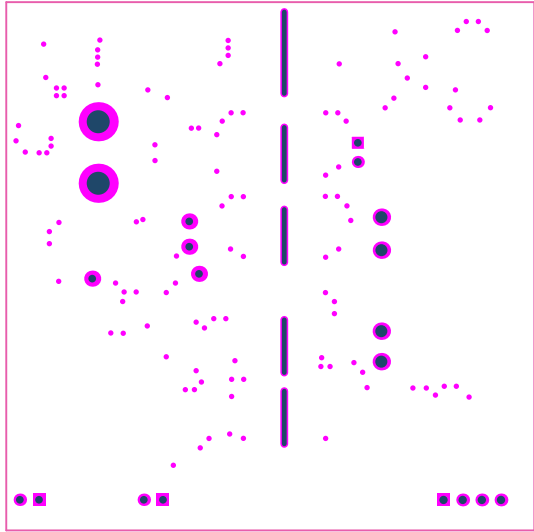
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	TIDA-010065_DC_V1.1_Fault	REV:	E2	SUN REV:	Not In VersionControl
LAYER NAME =	GND Layer	TID #:	TIDA-010065			
PLOT NAME =	GND Layer	GENERATED	:	9/12/2019	11:42:43 AM	TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: <small>TIDA-010065_DC_V1.1_Fault</small>	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = <small>Power Layer</small>	TID #: TIDA-010065		
PLOT NAME = <small>Power Layer</small>	GENERATED : 9/12/2019 11:42:44 AM	TEXAS INSTRUMENTS	



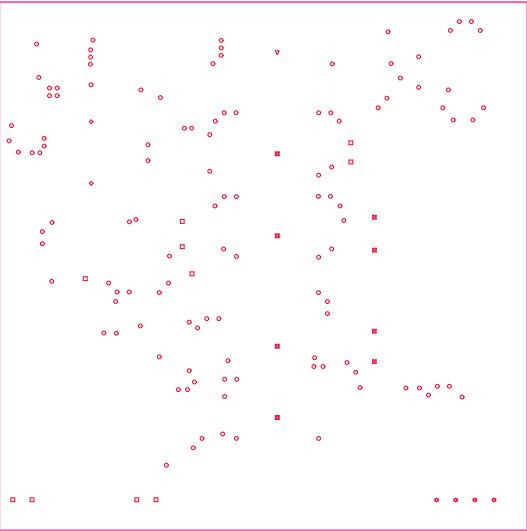
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: <small>TIDA-010065_DC_V1.1_Fault</small>	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Bottom Layer	TID #: <small> </small> TIDA-010065		
PLOT NAME = <small>Bottom Layer</small>	GENERATED : 9/12/2019 11:42:46 AM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: <small>TIDA-010065_DC_V1.1_Fault</small>	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = <small>Bottom Solder</small>	TID #: <small> TIDA-010065</small>		
PLOT NAME = <small>Bottom Solder Mask</small>	GENERATED : 9/12/2019 11:42:47 AM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: <small>TIDA-010065_DC_V.1_Fault</small>	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = <small>Bottom Overlay</small>	TID #: TIDA-010065		
PLOT NAME = <small>Bottom Overlay</small>	GENERATED : 9/12/2019 11:42:49 AM		TEXAS INSTRUMENTS

	1	2	3	4	5	6																																																																																																																																										
A																																																																																																																																																
B	DESIGN INFORMATION BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION) <div>70MM X 70MM</div> <div>Number of Layers : MIN. TRACK WIDTH: MIN. CLEARANCE: MIN. VIA DRILL SIZE:</div> <div>4 15 MIL 2.2 MIL 12 MIL</div> <div>MINIMUM ANNULAR RING 6 MIL (0.1524 mm) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C REGISTRATION TOLERANCES: METAL +/- .5 MIL, HOLES +/- .3 MIL</div> MATERIAL: <div><div>FR-408 FR-4 High Tg OTHER</div><div>THICKNESS: 63 MIL (1.6mm) +/-10% OTHER</div><div>TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2 OTHER +/-</div><div>BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2 OTHER +/-</div>COPPER THICKNESS (FINISHED):<div><div>OUTER: 1.4MIL (1oz) 2MIL (1.4oz) 2.8MIL (2oz)</div><div>INNER SIGNAL: 1.4MIL (1oz) 2.8MIL (2oz) N/A</div>DRILLING:<div><div>REFERENCE: AS SHOWN NC_DRILL FILES</div><div>PTH MIN COPPER THICKNESS: 1MIL OTHER</div>BOARD FINISH:<div><div>SILKSCREEN: TOP BOTTOM</div><div>SILKSCREEN COLOR: WHITE OTHER</div><div>SOLDER RESIST COLOR: GREEN BLUE OTHER</div>SURFACE FINISH: IMMERSSION GOLD (ENIG) ENEPIG IMM. TIN/SILVER OR EQUIV OTHERARRAY/PANEL:<div><div>CUT AND TRIM PER MECH LAYER 1 N.C. ROUTE V. SCORE</div>CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:<div><div>ANSI IPC-A-600F CLASS -> 1 2 3</div><div>UL 94V-0 RoHS OTHER PER ORDER</div>ADDITIONAL REQUIREMENTS: VIA TENTING: YES NOX MICROSECTION: YES IMPEDANCE CONTROL: YES NOX BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER MANUFACTURER'S UL: RAIL METAL SILK</div></div></div></div></div></div>																																																																																																																																															
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D	<table border="1"><thead><tr><th>Layer</th><th>Name</th><th>Material</th><th>Thickness</th><th>Constant</th><th>Board Layer Stack</th><th>Board Layer Stack</th></tr></thead><tbody><tr><td>1</td><td>Top Overlay</td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>2</td><td>Top Solder</td><td>Solder Resist</td><td>0.40mil</td><td>3.5</td><td></td><td></td></tr><tr><td>3</td><td>Top Layer</td><td>Copper</td><td>1.40mil</td><td></td><td></td><td></td></tr><tr><td>4</td><td>Dielectric1</td><td>FR-4 High Tg</td><td>13.00mil</td><td>4.8</td><td></td><td></td></tr><tr><td>5</td><td>GND Layer</td><td>Copper</td><td>1.40mil</td><td></td><td></td><td></td></tr><tr><td>6</td><td>Dielectric 2</td><td>FR-4 High Tg</td><td>30.00mil</td><td>4.2</td><td></td><td></td></tr><tr><td>7</td><td>Power Layer</td><td>Copper</td><td>1.40mil</td><td></td><td></td><td></td></tr><tr><td>8</td><td>Dielectric 3</td><td>FR-4 High Tg</td><td>13.00mil</td><td>4.2</td><td></td><td></td></tr><tr><td>9</td><td>Bottom Layer</td><td>Copper</td><td>1.40mil</td><td></td><td></td><td></td></tr><tr><td>10</td><td>Bottom Solder</td><td>Solder Resist</td><td>0.40mil</td><td>3.5</td><td></td><td></td></tr><tr><td>11</td><td>Bottom Overlay</td><td></td><td></td><td></td><td></td><td></td></tr></tbody></table> <table border="1"><thead><tr><th>Symbol</th><th>Count</th><th>Hole Size</th><th>Plated</th><th>Hole Type</th><th>Hole Length</th></tr></thead><tbody><tr><td>○</td><td>116</td><td>12.00mil (<0.305mm)</td><td>PTH</td><td>Round</td><td>-</td></tr><tr><td>◻</td><td>4</td><td>25.00mil (<0.635mm)</td><td>NPTH</td><td>Slot</td><td>300.00mil (<7.620mm)</td></tr><tr><td>▽</td><td>1</td><td>25.00mil (<0.635mm)</td><td>NPTH</td><td>Slot</td><td>450.00mil (<11.430mm)</td></tr><tr><td>□</td><td>10</td><td>40.00mil (<1.016mm)</td><td>PTH</td><td>Round</td><td>-</td></tr><tr><td>☆</td><td>4</td><td>43.31mil (<1.100mm)</td><td>PTH</td><td>Round</td><td>-</td></tr><tr><td>⊗</td><td>4</td><td>63.00mil (<1.600mm)</td><td>PTH</td><td>Round</td><td>-</td></tr><tr><td>◇</td><td>2</td><td>120.00mil (<3.048mm)</td><td>PTH</td><td>Round</td><td>-</td></tr><tr><td colspan="2">141 Total</td><td></td><td></td><td></td><td></td></tr></tbody></table> <p>Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position. Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout</p> <p>Drill Table FOR 12MIL DRILL +0/-12MIL FOR 16MIL DRILL +0/-16MIL FOR PTH DRILL +/-3MIL FOR NPTH DRILL +/-2MIL</p>						Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	1	Top Overlay						2	Top Solder	Solder Resist	0.40mil	3.5			3	Top Layer	Copper	1.40mil				4	Dielectric1	FR-4 High Tg	13.00mil	4.8			5	GND Layer	Copper	1.40mil				6	Dielectric 2	FR-4 High Tg	30.00mil	4.2			7	Power Layer	Copper	1.40mil				8	Dielectric 3	FR-4 High Tg	13.00mil	4.2			9	Bottom Layer	Copper	1.40mil				10	Bottom Solder	Solder Resist	0.40mil	3.5			11	Bottom Overlay						Symbol	Count	Hole Size	Plated	Hole Type	Hole Length	○	116	12.00mil (<0.305mm)	PTH	Round	-	◻	4	25.00mil (<0.635mm)	NPTH	Slot	300.00mil (<7.620mm)	▽	1	25.00mil (<0.635mm)	NPTH	Slot	450.00mil (<11.430mm)	□	10	40.00mil (<1.016mm)	PTH	Round	-	☆	4	43.31mil (<1.100mm)	PTH	Round	-	⊗	4	63.00mil (<1.600mm)	PTH	Round	-	◇	2	120.00mil (<3.048mm)	PTH	Round	-	141 Total					
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ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = Drill Drawing

PLOT NAME = Drill Drawing

BOARD #:#TIDA-010065_DC_U_I_Fault

TID #: TIDA-010065

GENERATED : 9/12/2019 11:42:51 AM

REV: E2

SUN REV: Not In VersionControl

TEXAS INSTRUMENTS

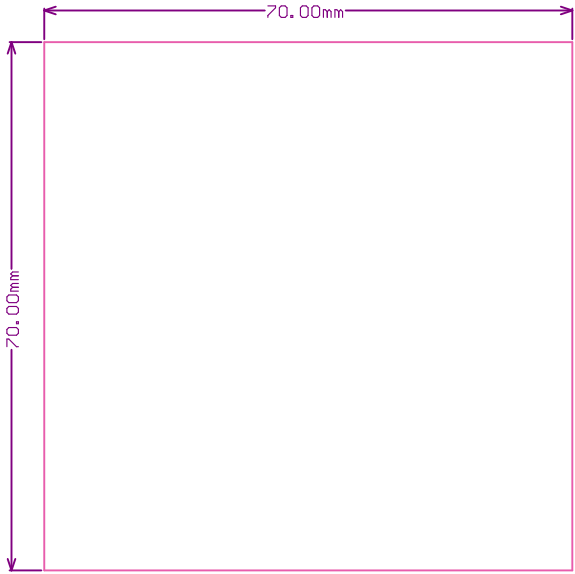
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ENGINEER: Sreenivasa kallikuppa

SCALE: 1.00

LAYOUT BY: Avinash N

ALTUM DESIGNER VERSION: 18.1.9.240



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	TIDA-010065_DC_V.1.1_Fault	REV:	E2	SUN REV:	Not In VersionControl
LAYER NAME =	TID #:	TIDA-010065				
PLOT NAME =	Board Dimensions		GENERATED	: 9/12/2019 11:42:53 AM		TEXAS INSTRUMENTS