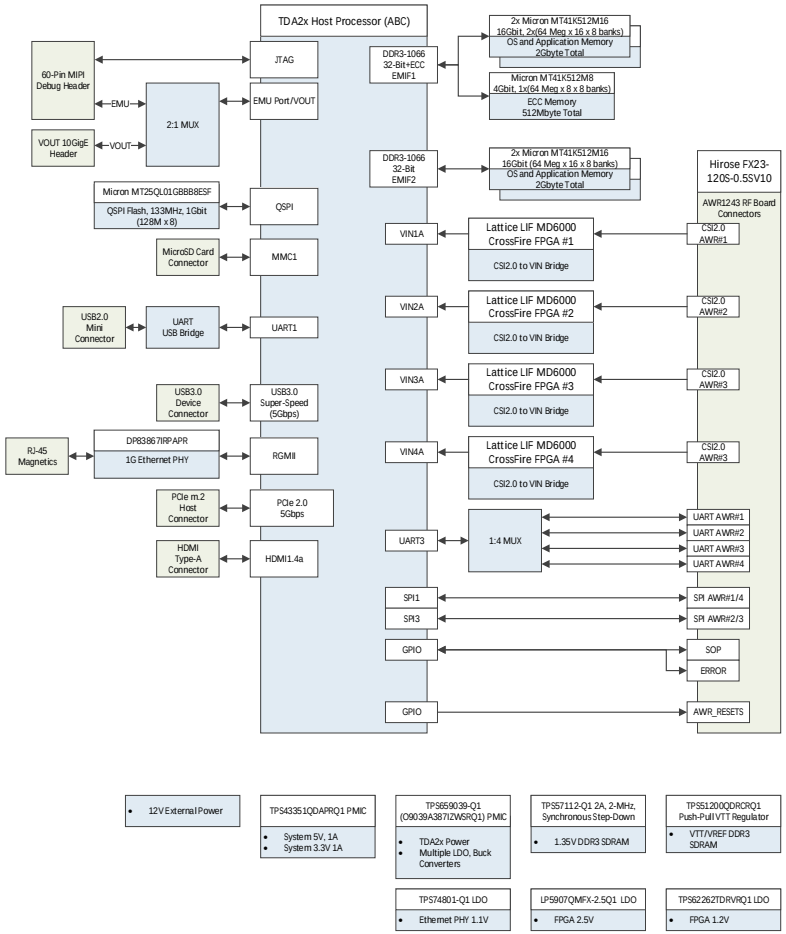
Cascade Radar Host Processor Board

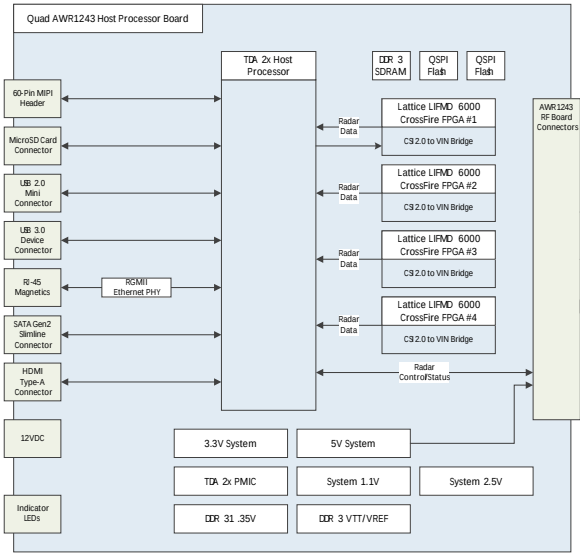
Cascade Radar Host Processor Board Block Diagram



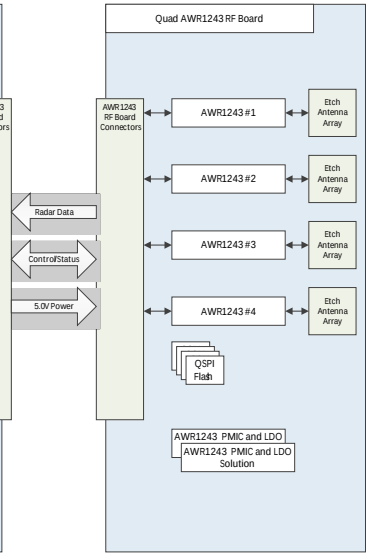
System Description

	Cascade Radar Host Board
Host Processor	TDA2SX ADAS SoC
CPU	Dual-Core ARM A15, 1176 MHz
DSP	2x C66x, 750 MHz
GPU	Dual-Core SGX544 GPU, 532 MHz
EVE Co-Processor	4x EVE Matrix Co-Processor, 532 MHz
IVA Co-Processor	2x IVA Image Co-Processor, 532 MHz
Memory	2x 32-bit, 2GByte, DDR3L-1066 SDRAM(one bank ECC capable)
USB	USB3.0 Host and USB2.0 Host
CSI2.0	4x 4-lane CSI2.0, 900 Mbps
Video Out	24-bit Digital Video Out, HDMI 1.4b
Connectivity	1 Gigabit Ethernet, USB2.0 Serial Port (TI RTOS/ Linux Console)
Data Storage	PCIe 2.0 m.2 Connector(M-Keyed), 1 Gigabit NOR Flash, MicroSD Card
Mechanical	160mm x 140mm - Two Automotive Rated Board to Board Connectors
Software	TI RTOS with Radar SDK Packages, TI Processors SDK Linux Distribution with Radar SDK Packages

Cascade Radar Host Processor Board



Cascade Radar RF Board

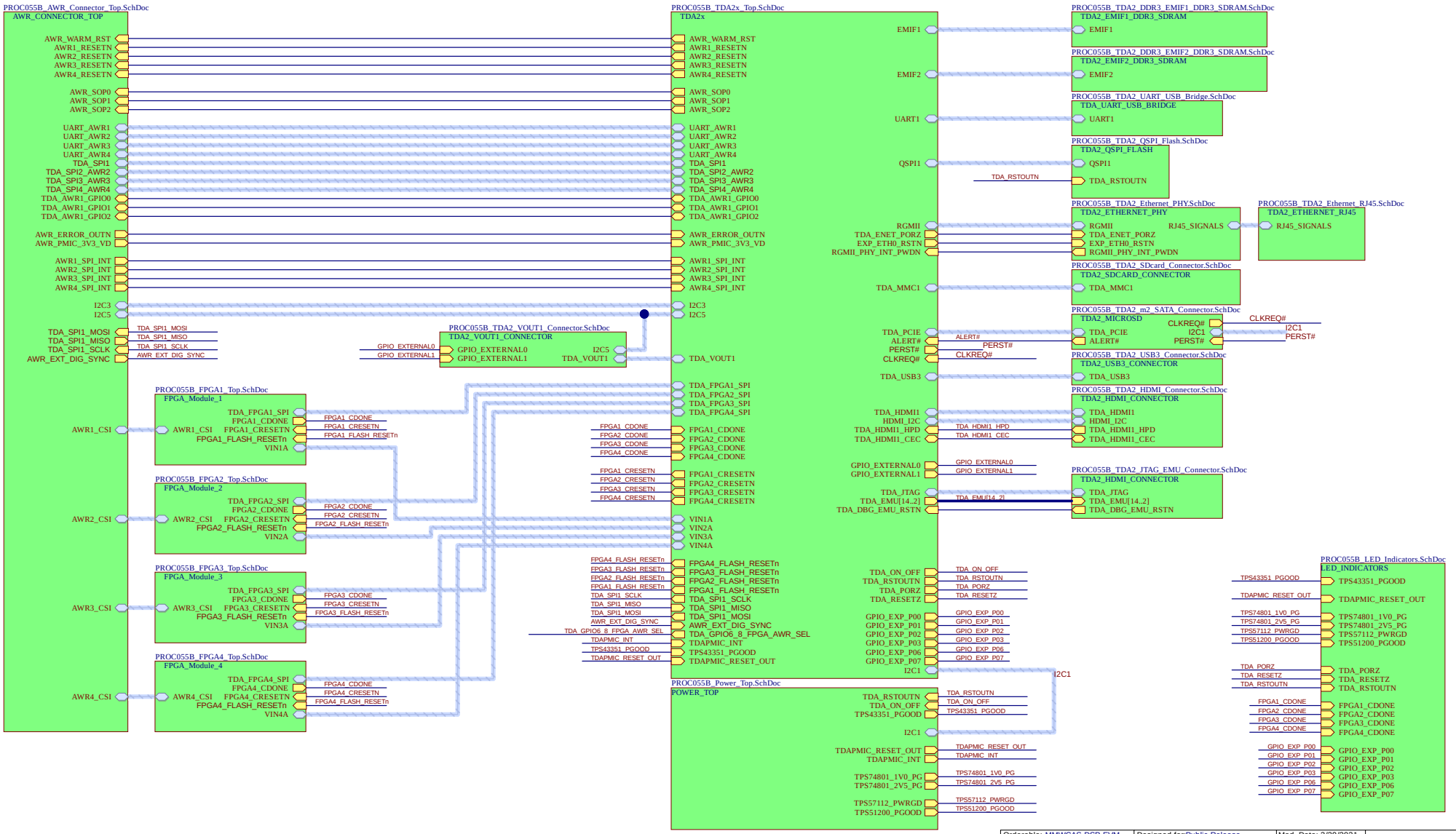


PROC055B_System_Top.SchDoc
CASCADE_HOST_PROCESSOR_BOARD
PROC055B_EVM_Hardware.SchDoc
EVM_HARDWARE

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 3/29/2021
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: Cover Sheet	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:1 of 66
Drawn By:Alec Schott		File: PROC055B_CoverSheet.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

Cascade Radar Host Processor Board - Top Level Schematic



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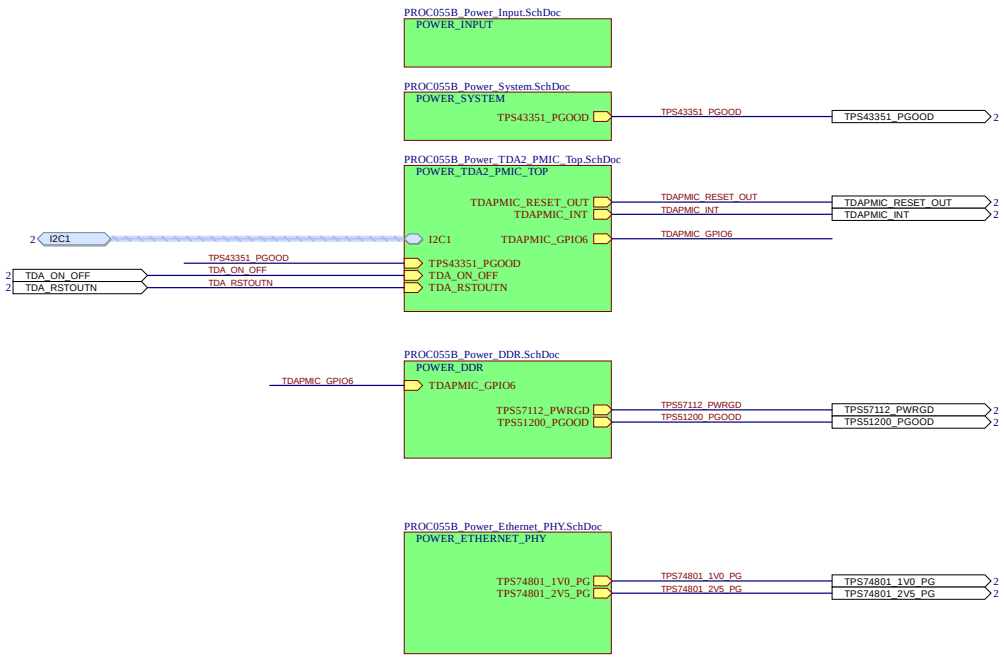
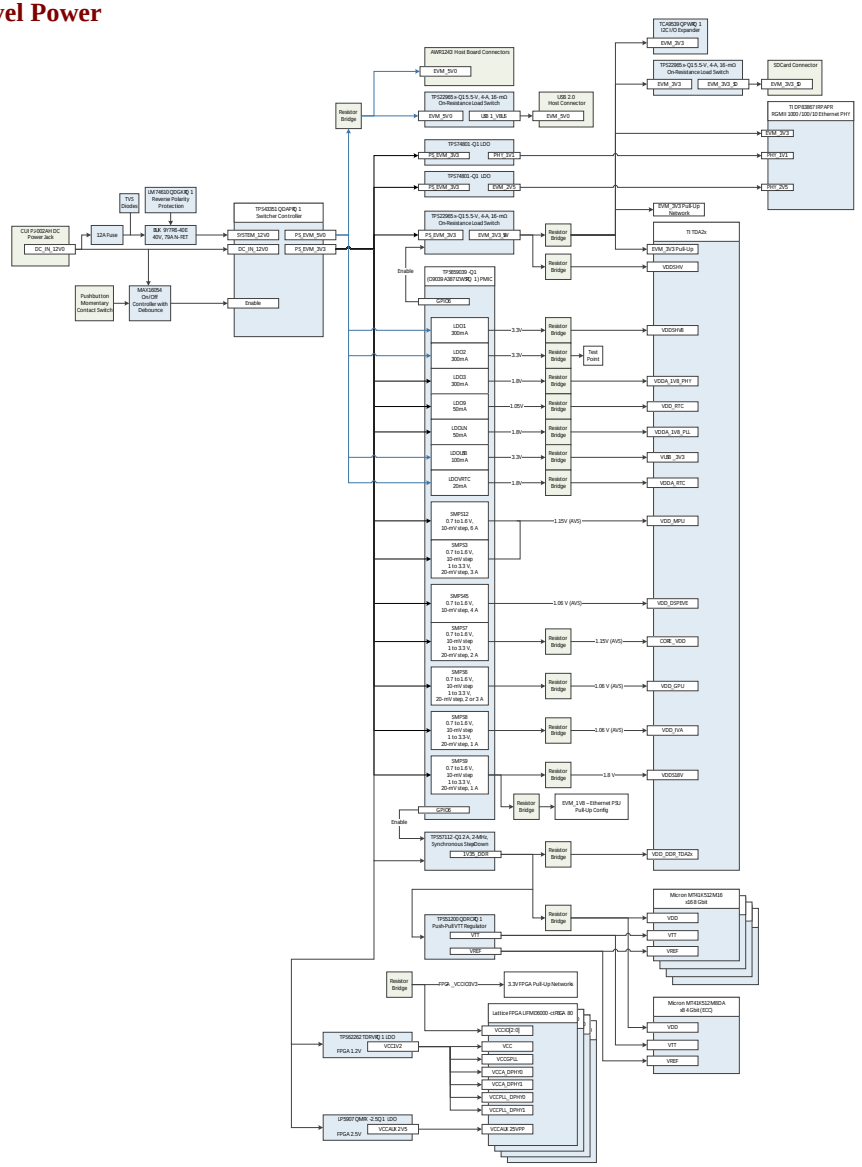
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: System Top Level	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:2 of 66
Drawn By:Alec Schott		File: PROC055B_System_Top.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

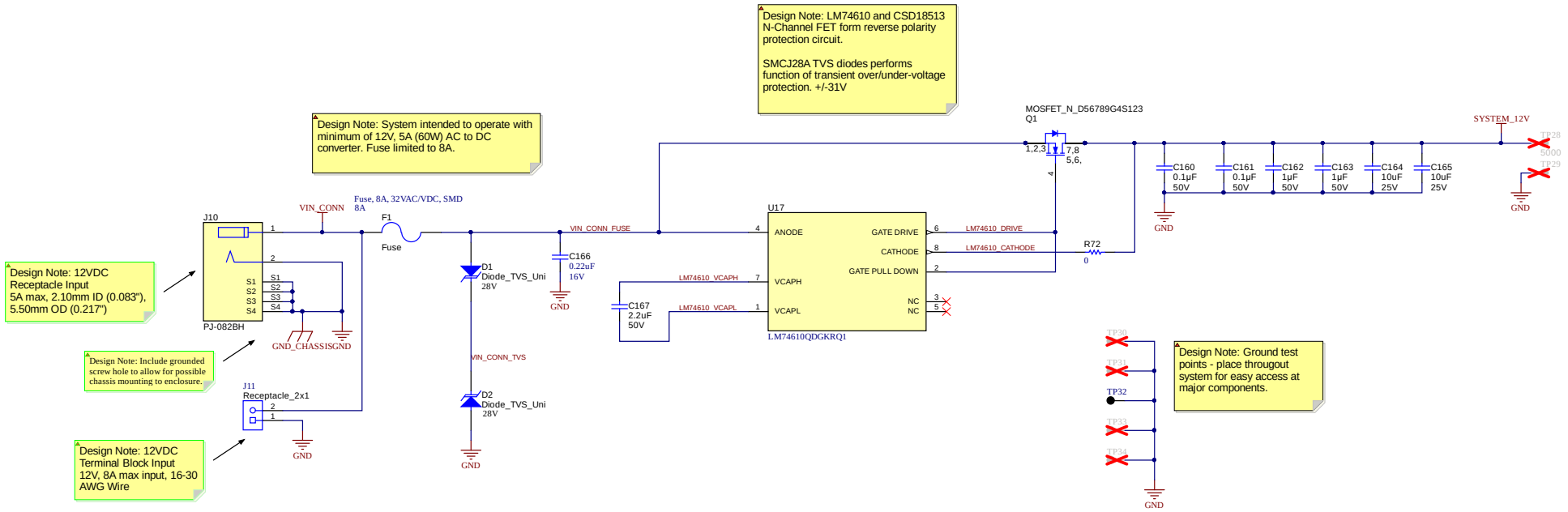
Host Processor Board - Top Level Power





Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 3/29/2021
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: System Power - Top Level	
BOM Rev: Not in version control		Assembly Variant:001	Sheet:3 of 66
Drawn By:Alec Schott		File: PROC055B_Power_Top.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

System 12VDC Power Input



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 4/5/2021
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: System Power Input	
Variant: [VariantNo]	Rev: Not in version control	Assembly Variant:001	Sheet:4 of 66
Drawn By:Alec Schott		File: PROC055B_Power_Input.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

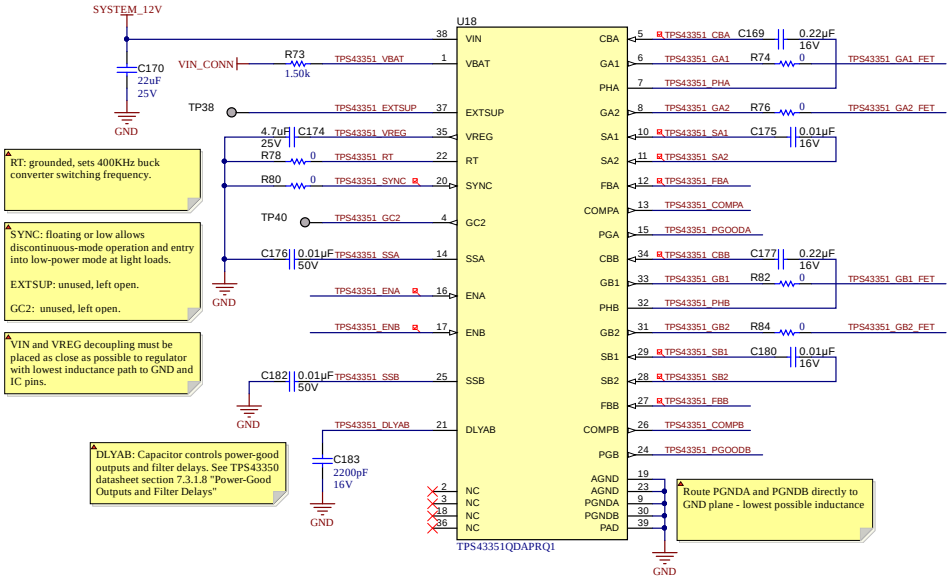
TPS43351 - System 5.0V and System 3.3V Primary Supplies

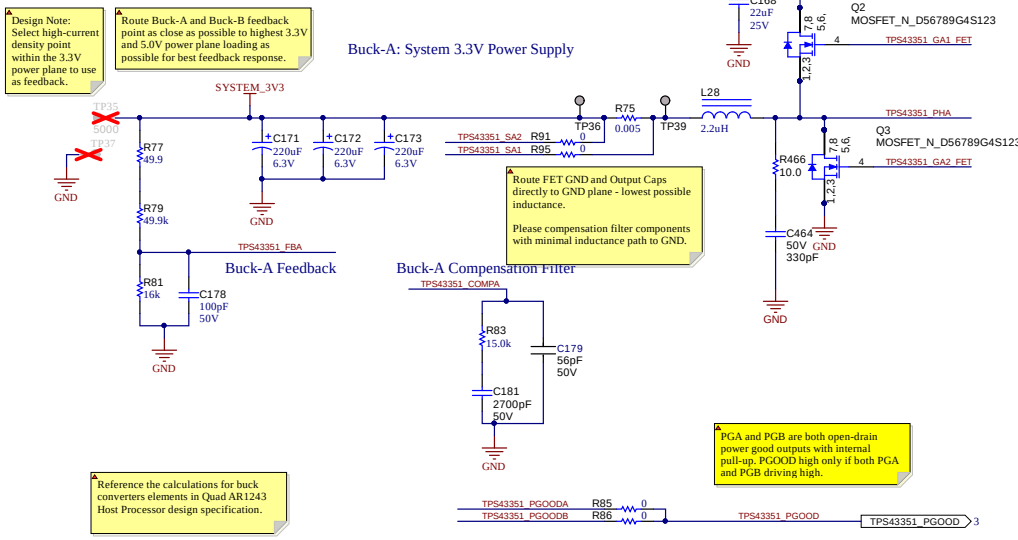
References

tps43351-q1 Datasheet

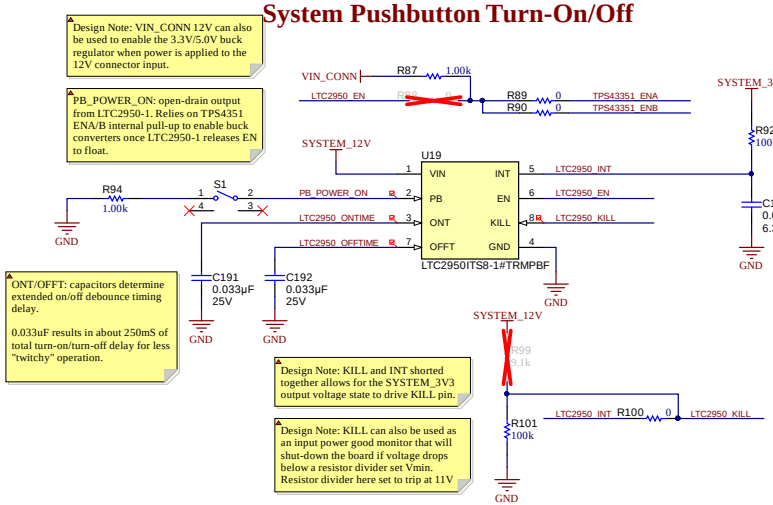
TPS43351-Q1 EVM User Guide

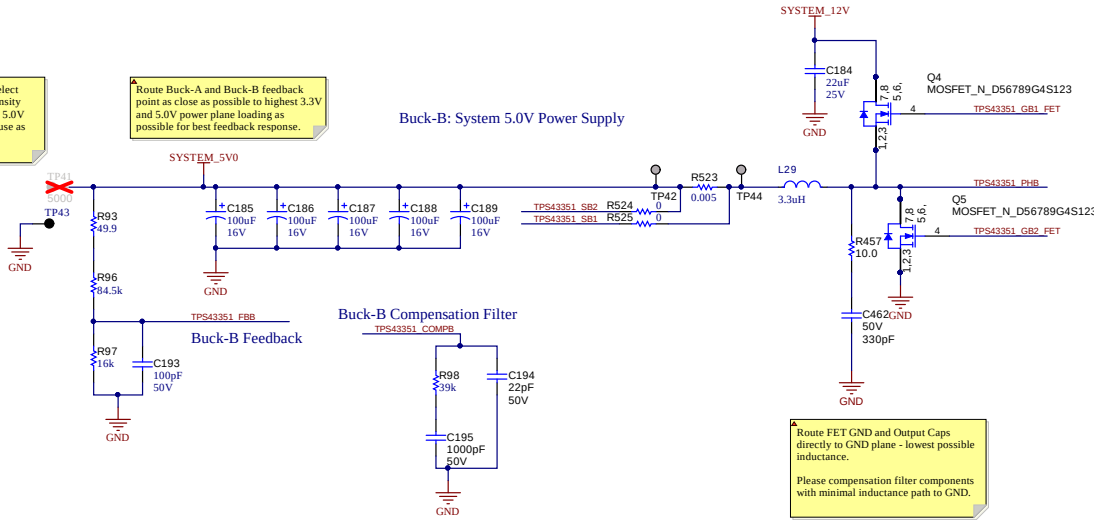
Follow all layout guidelines as presented in Chapter 10 of datasheet





System Pushbutton Turn-On/Off





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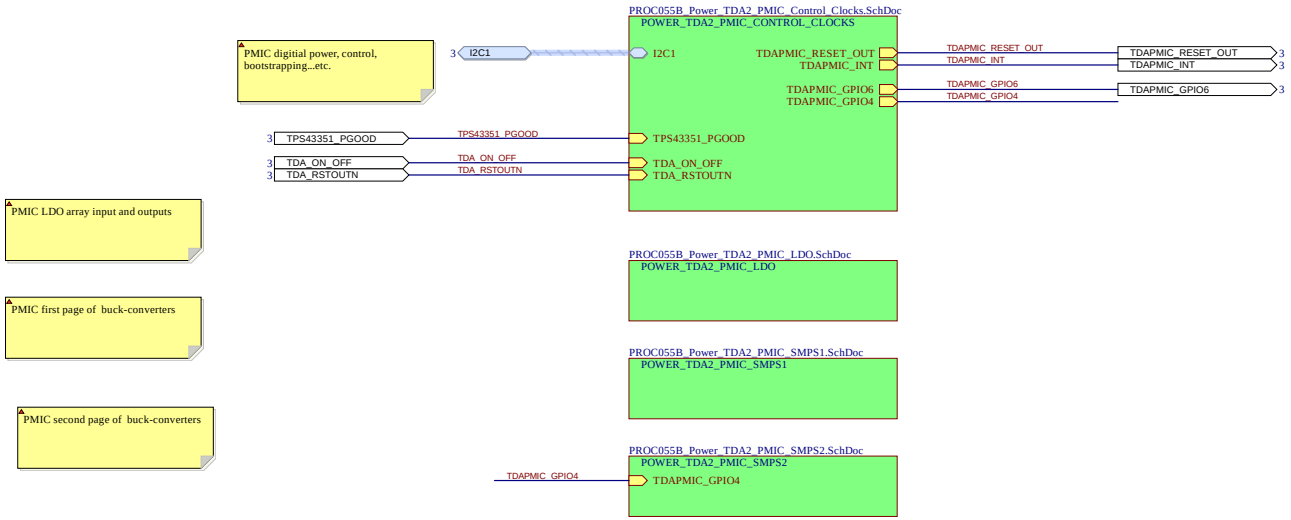
Number: PROC055	Rev: B	Sheet Title: System First Stage 3.3V and 5.0V Power	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:5 of 66
Drawn By:Alec Schott		File: PROC055B_Power_System.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

References

TPS659039-Q1 TDA2 PMIC - Top Level Schematic

Based on the TDA2x Evaluation Board Power Architecture



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Number: PROC055	Rev: B	Sheet Title: TDA2 PMIC - Top Level	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:6 of 66
Drawn By:Alec Schott		File: PROC055B_Power_TDA2_PMIC_Top.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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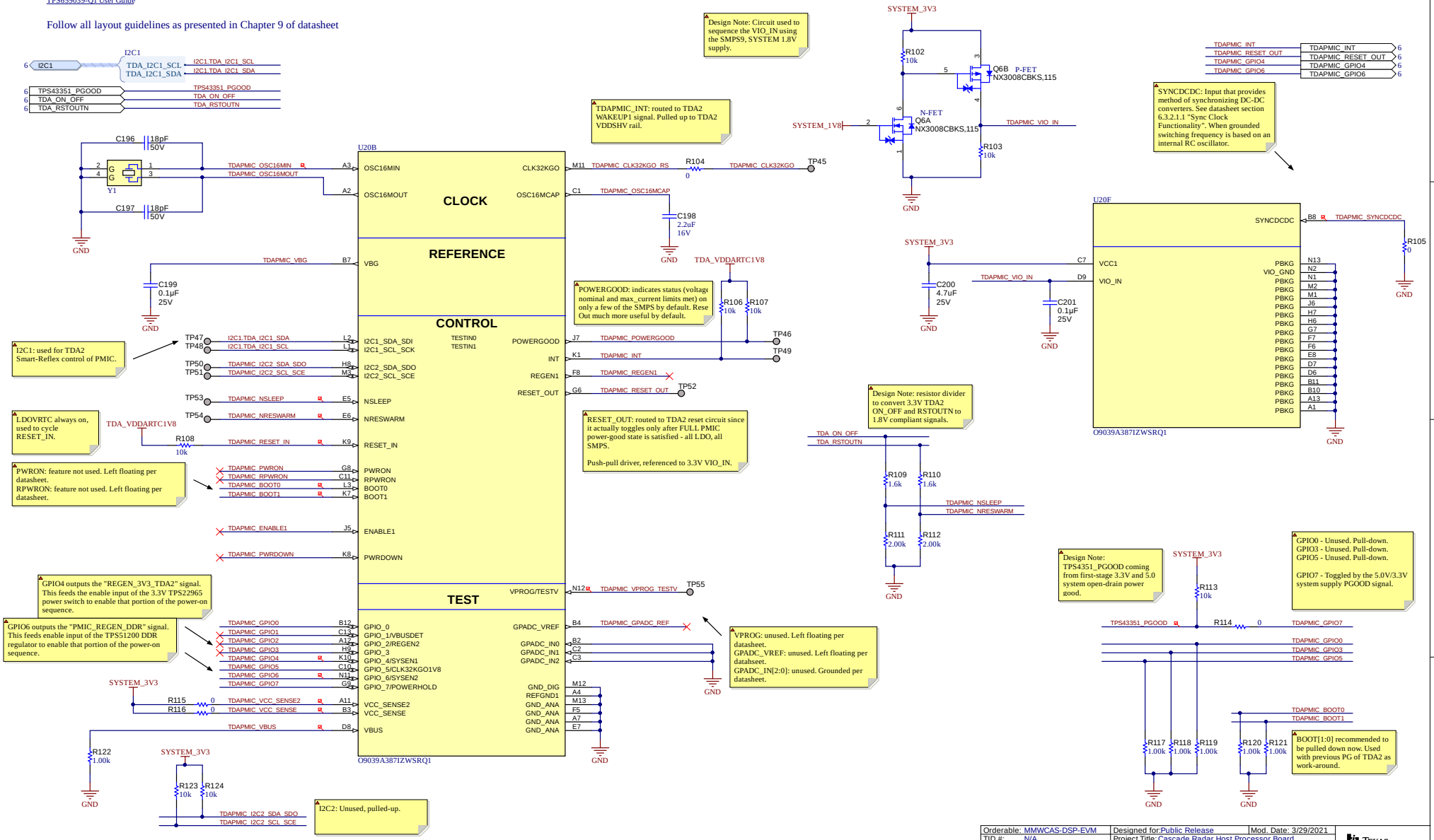
TPS659039-Q1 TDA2 PMIC - Digitial Power, Clock, Reference and Control

References
TPS659039-Q1 Datasheet
TPS659039-Q1 User Guide

Follow all layout guidelines as presented in Chapter 9 of datasheet



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TID #: N/A	Project Title: Cascade Radar Host Processor Board	
Number: PROC055 Rev: B	Sheet Title: TDA2 PMIC - Control, Clock, Power	
EVM Rev: Not in version control	Assembly Variant:001	Sheet:7 of 66
Drawn By:Alec Schott	File: PROC055B_Power_TDA2_PMIC_Control_Clock_Rst.SchDoc	
Engineer: Alec Schott	Contact: http://www.ti.com/mmwave	

http://www.ti.com

References

TPS659039-Q1 Datasheet

TPS659039-Q1 User Guide

Follow all layout guidelines as presented in Chapter 9 of datasheet

TPS659039-Q1 TDA2 PMIC - LDO Input and LDO Output

LDOUSB - TDA2 VUSB3V3 - Fixed 3.3V USB PHY Supply

LDOVRTC - TDA2 VDDARTC1V8 - Fixed 1.8V RTC Supply

LDOVANA - UNASSIGNED

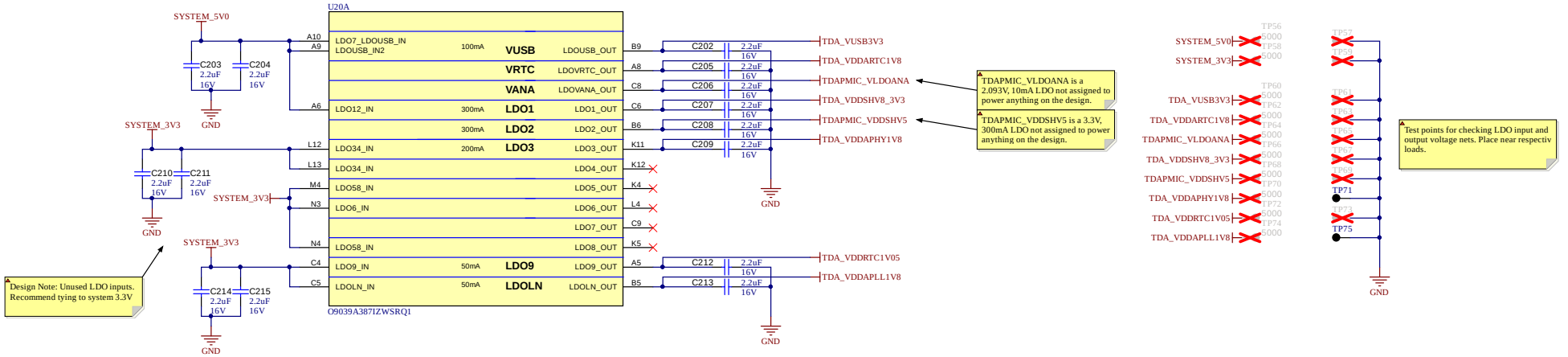
LDO1 - TDA2 VDDSHV8 - Fixed 3.3V IO Supply

LDO2 - TDA2 VDDSHV5 - Fixed 3.3V IO Supply

LDO3 - TDA2 VDDAPHY1V8 - Fixed 1.8V USB PHY Supply

LDO9 - TDA2 TDA2 VDDRTC1V05 - Fixed 1.05V RTC Supply

LDOLN - TDA2 VDDAPLL1V8 - Fixed 1.8V PLL Supply



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TDA2 PMIC - LDO Input and Output	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:8 of 66
Drawn By:Alec Schott		File: PROC055B_Power_TDA2_PMIC_LDO.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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References

TPS659039-Q1 Datasheet

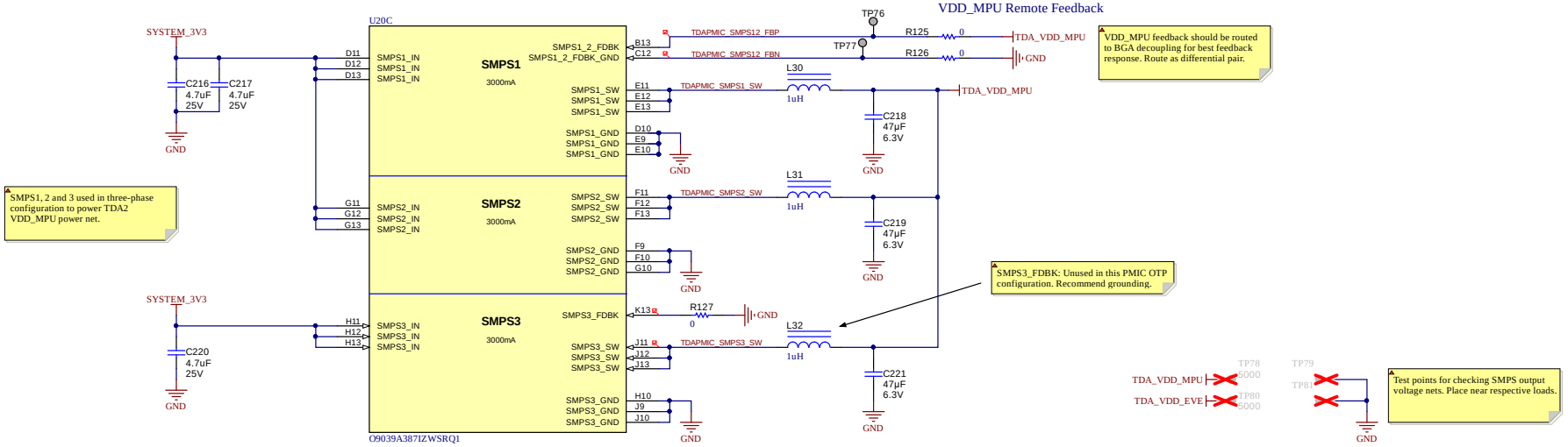
TPS659039-Q1 User Guide

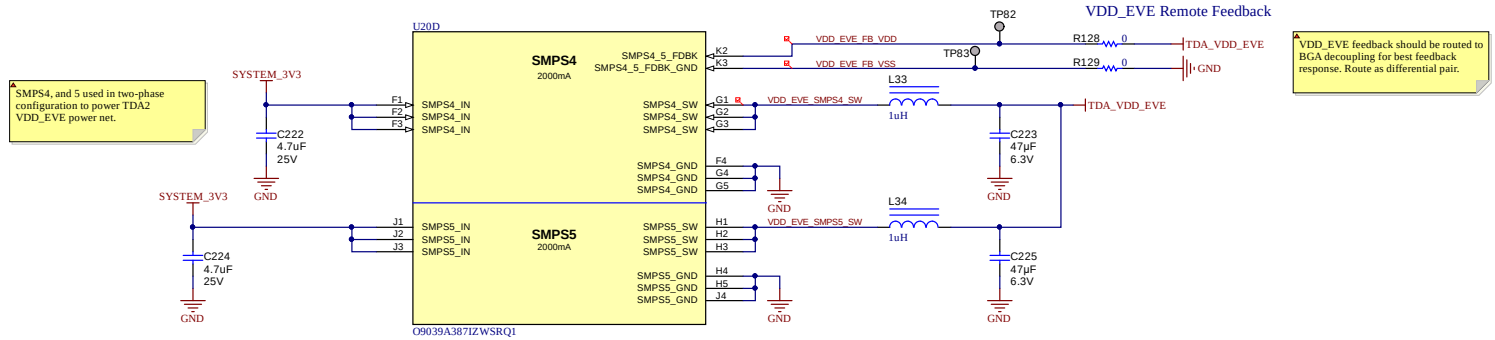
TPS659039-Q1 TDA2 PMIC - SMPS Buck Converters: SMPS1, SMPS2, SMPS3, SMPS4 and SMPS5

Follow all layout guidelines as presented in Chapter 9 of datasheet

SMPS[3:1] - TDA2 VDD_MPU - AVS Supply

SMPS[5:4] - TDA2 VDD_EVE - AVS Supply





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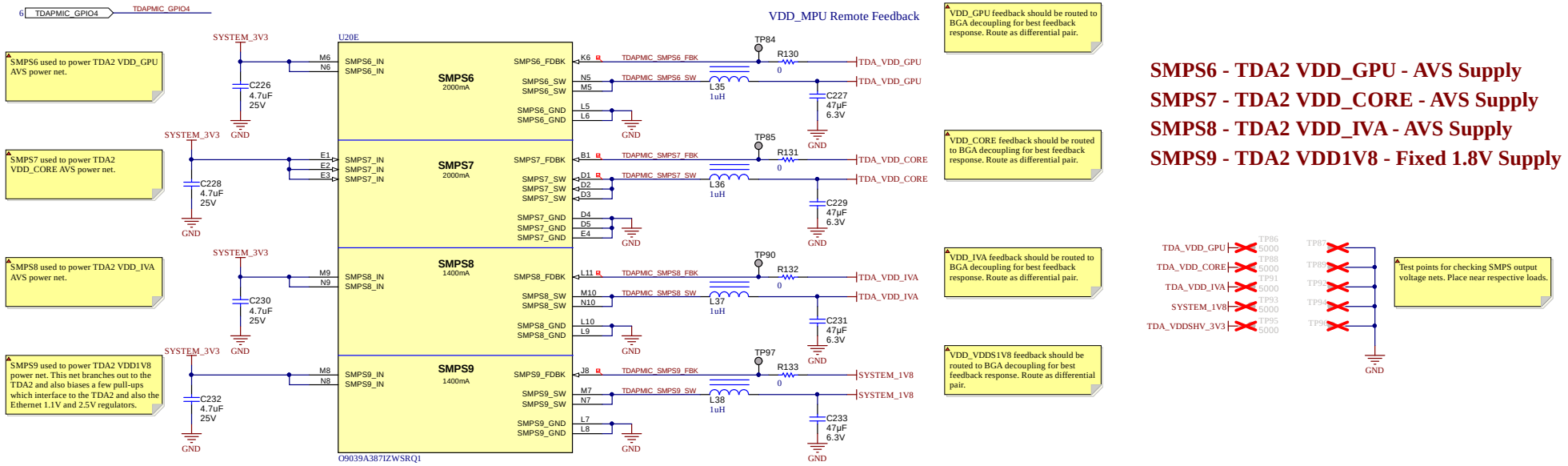
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TDA2 PMIC - SMPS1/2/3/4/5	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:9 of 66
Drawn By:Alec Schott		File: PROC055B_Power_TDA2_PMIC_SMPS1.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

References

TPS659039-Q1 Datasheet
TPS659039-Q1 User Guide
TPS22965-Q1 User Guide

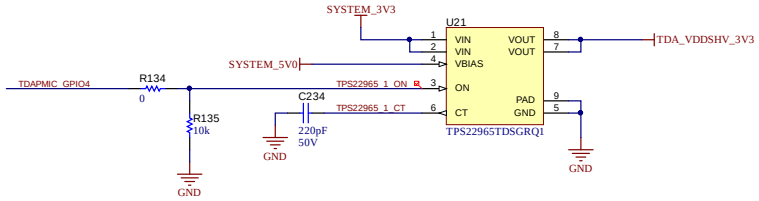
Follow all layout guidelines as presented in datasheets

TPS659039-Q1 TDA2 PMIC - SMPS Buck Converters: SMPS6, SMPS7, SMPS9 and SMPS9 and TDA/System 3.3V Switch



SMPS6 - TDA2 VDD_GPU - AVS Supply
SMPS7 - TDA2 VDD_CORE - AVS Supply
SMPS8 - TDA2 VDD_IVA - AVS Supply
SMPS9 - TDA2 VDD1V8 - Fixed 1.8V Supply

TPS22965-Q1 Load Switch - TDA2 and System Fixed 3.3V Supply



TDA2 - Fixed 3.3V I/O Supply

A load switch is used to allow the primary TDA2 PMIC to control when its 3.3V I/O supply is sequenced as well as all 3.3V I/O peripheral IC and pull-ups attached to the TDA2 device to prevent leakage during power-on/off

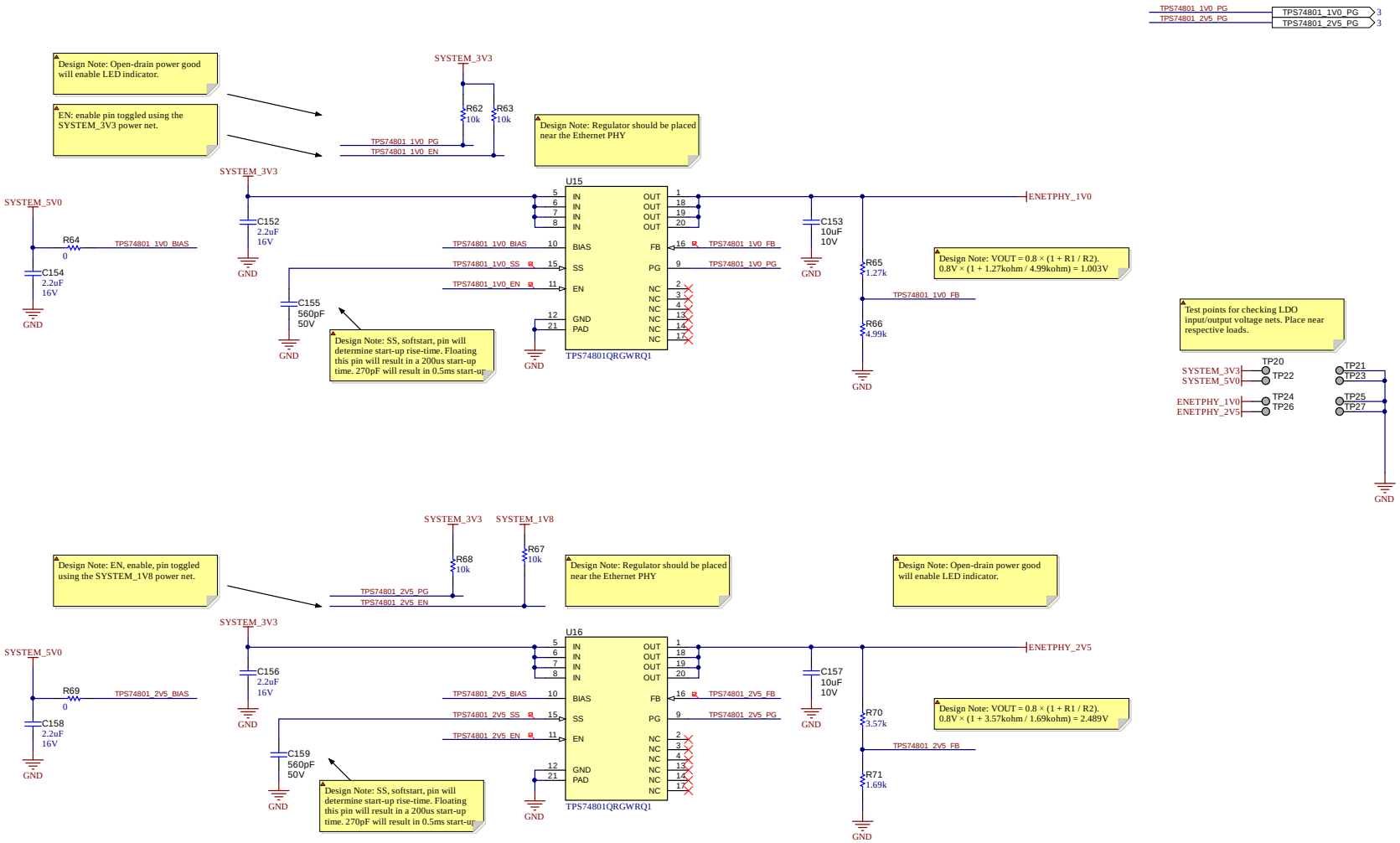
Also used to power the Lattice CrossFire FPGA 3.3V I/O Power

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TDA2 PMIC - SMPS6/7/8/9	
BOM Rev: Not in version control		Assembly Variant:001	Sheet:10 of 66
Drawn By:Alec Schott		File: PROC055B_Power_TDA2_PMIC_SMPS2.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

References
TPS74801QRGWRQ1 Datasheet

TPS74801QRGWRQ1 - Ethernet PHY 1.1V and 2.5V LDO Supplies

Follow all layout guidelines as presented in the device datasheet.



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: Ethernet PHY 1.2V and 2.5V Supplies	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:11 of 66
Drawn By:Alec Schott		File: PROC055B_Power_Ethernet_PHY.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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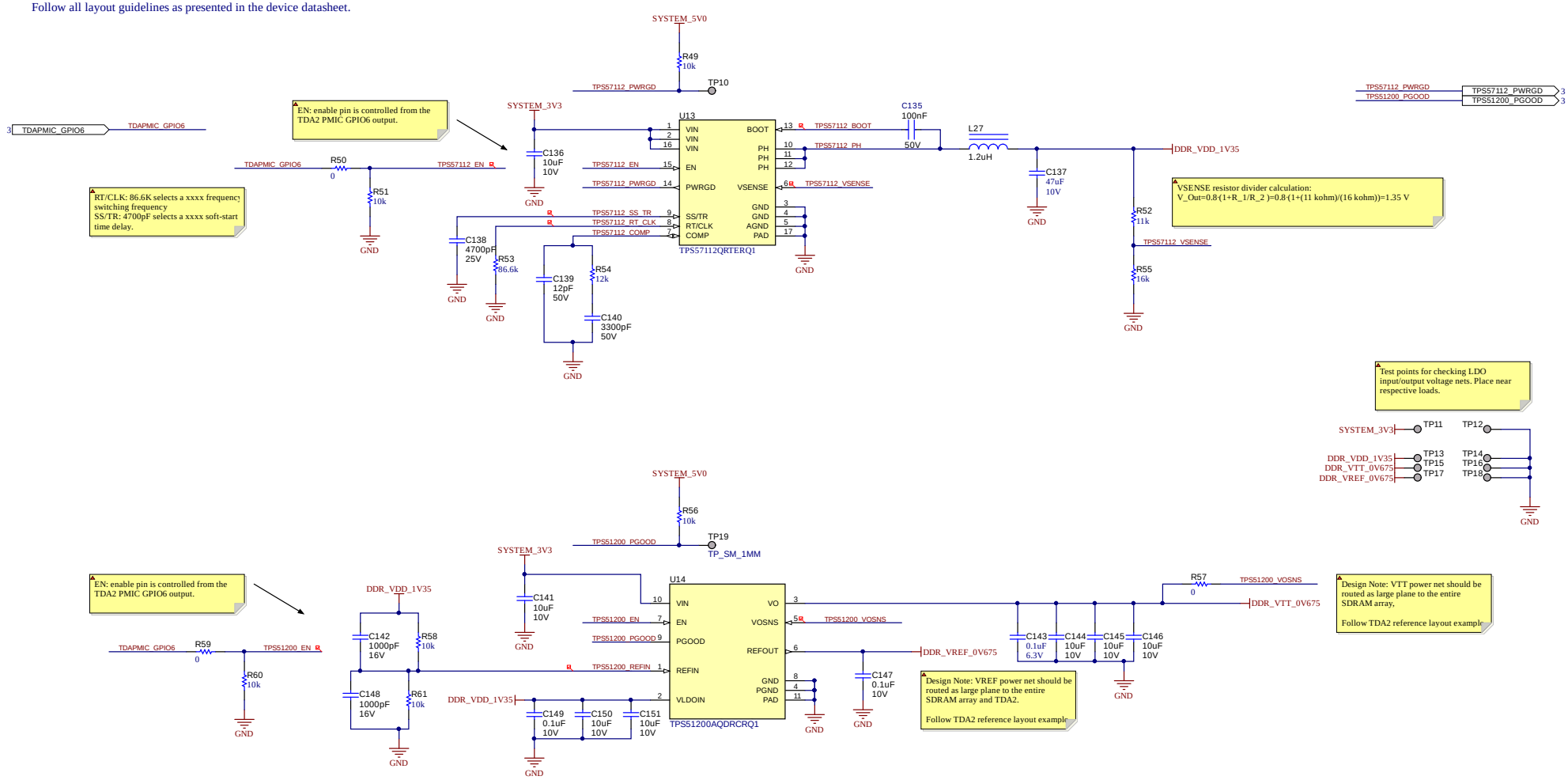
References

TPS57112-Q1 Datasheet

TPS51200-Q1 Datasheet

TPS57112-Q1 DDR3 1.35V Supply and TPS51200-Q1 VTT/VREF Supply

Follow all layout guidelines as presented in the device datasheet.



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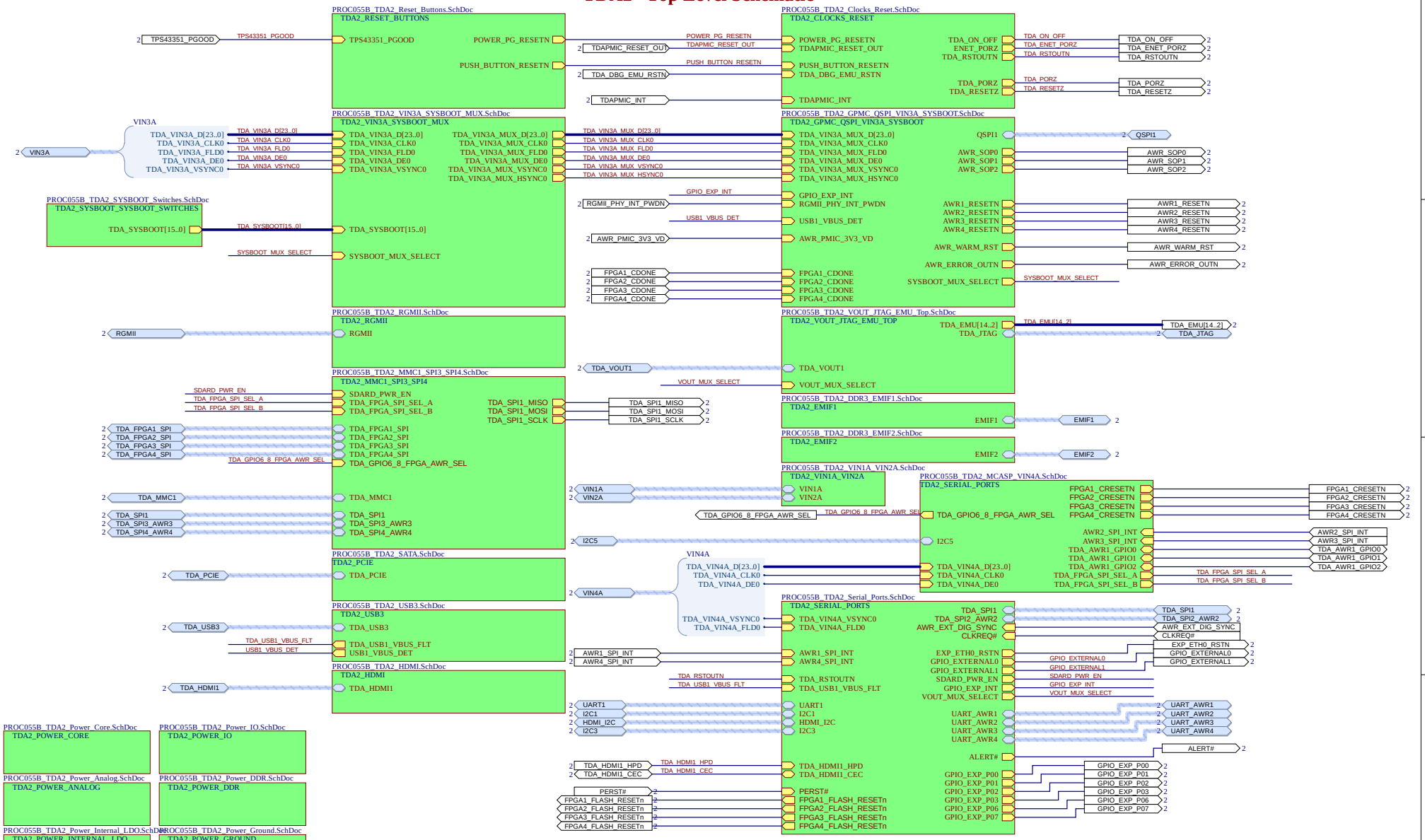
Number: PROC055	Rev: B	Sheet Title: DDR3L SDRAM 1.35V, VTT and VREF Supplies	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:12 of 66
Drawn By:Alec Schott		File: PROC055B_Power_DDR.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

TDA2 - Top Level Schematic



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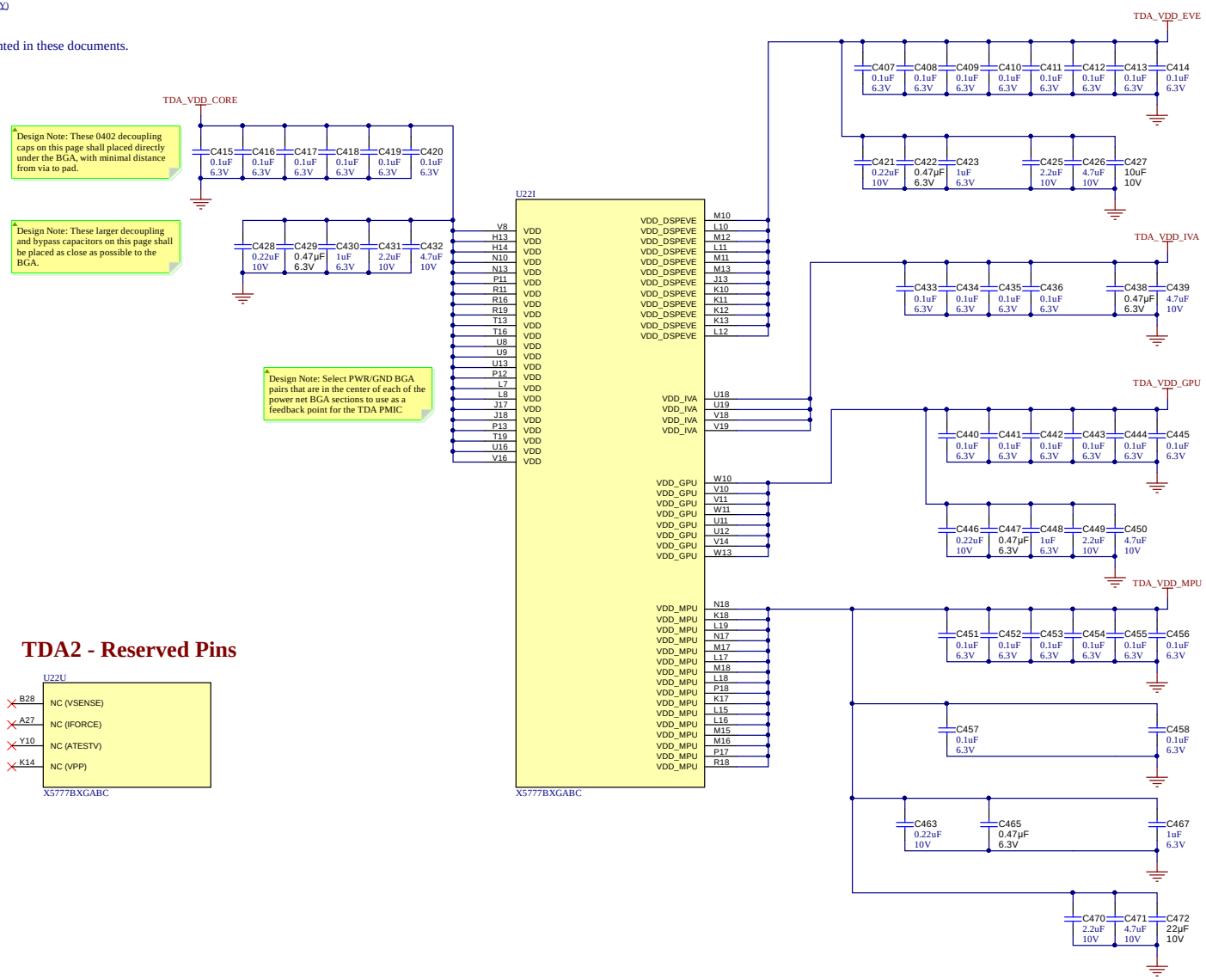
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TDA2 SoC - Top Level	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:13 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2x_Top.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

TDA2 - Core Power Nets and Decoupling

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.



TDA2 - Reserved Pins

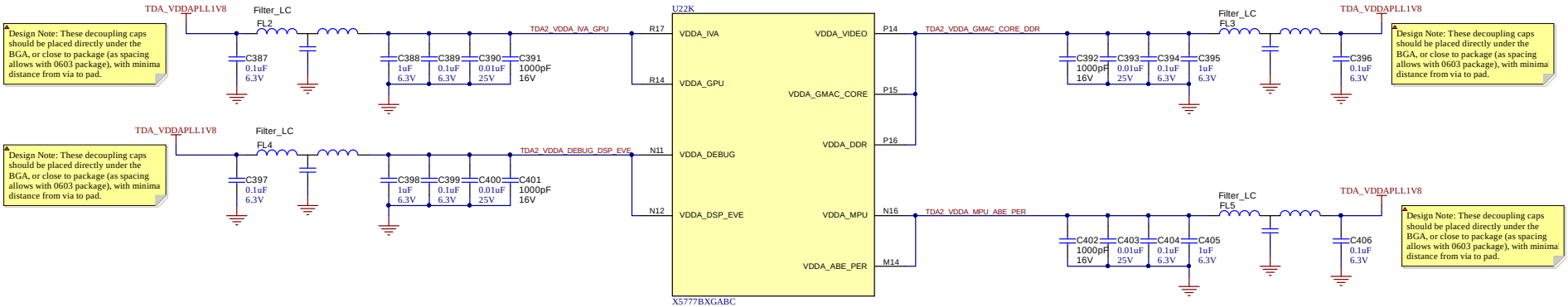
Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:14 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Power_Core.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

TDA2 - Analog Power Nets and Decoupling

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:15 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Power_Analog.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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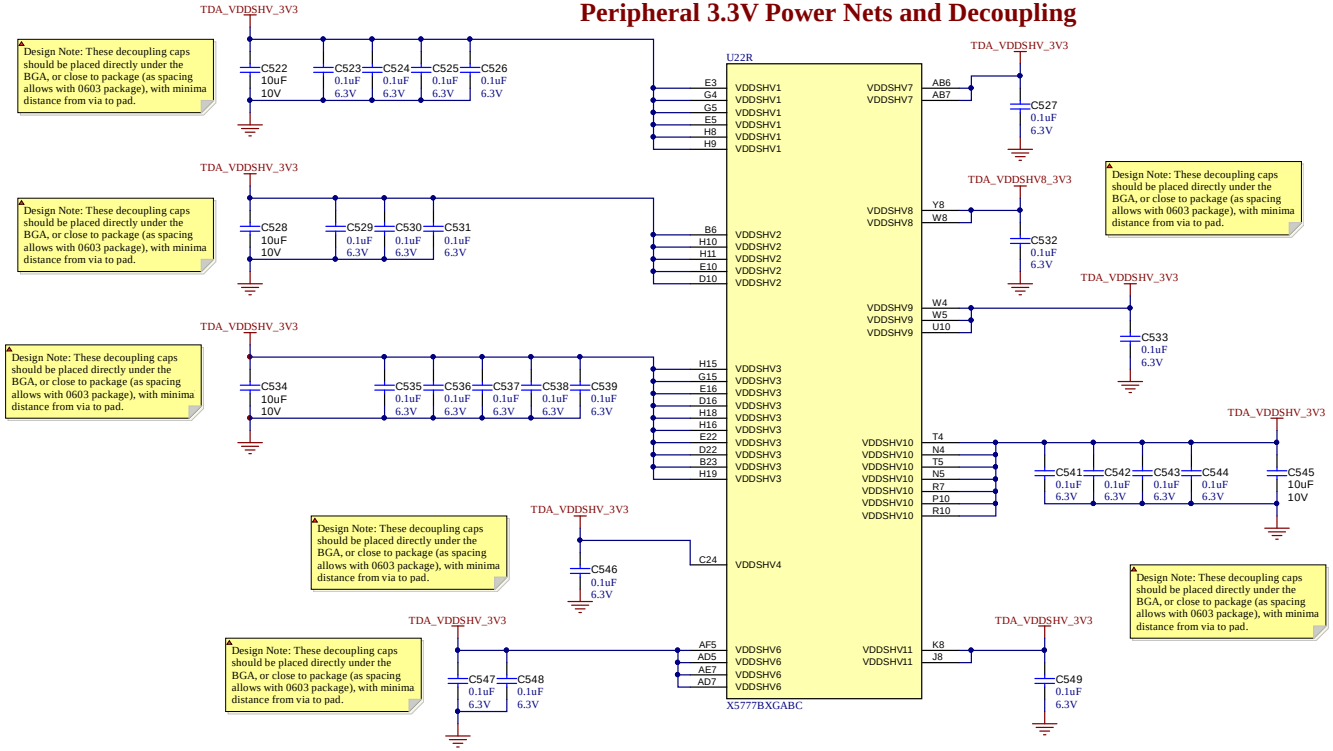
TDA2 - Peripheral 3.3V and 1.8V Power Nets and Decoupling

References

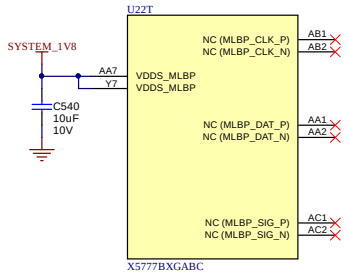
TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

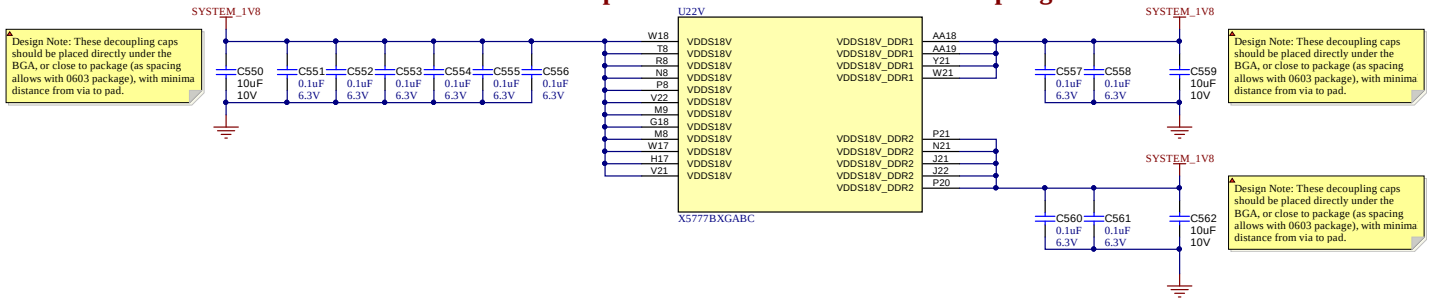
Peripheral 3.3V Power Nets and Decoupling



MLBP Power/Clocking



Peripheral 1.8V Power Nets and Decoupling



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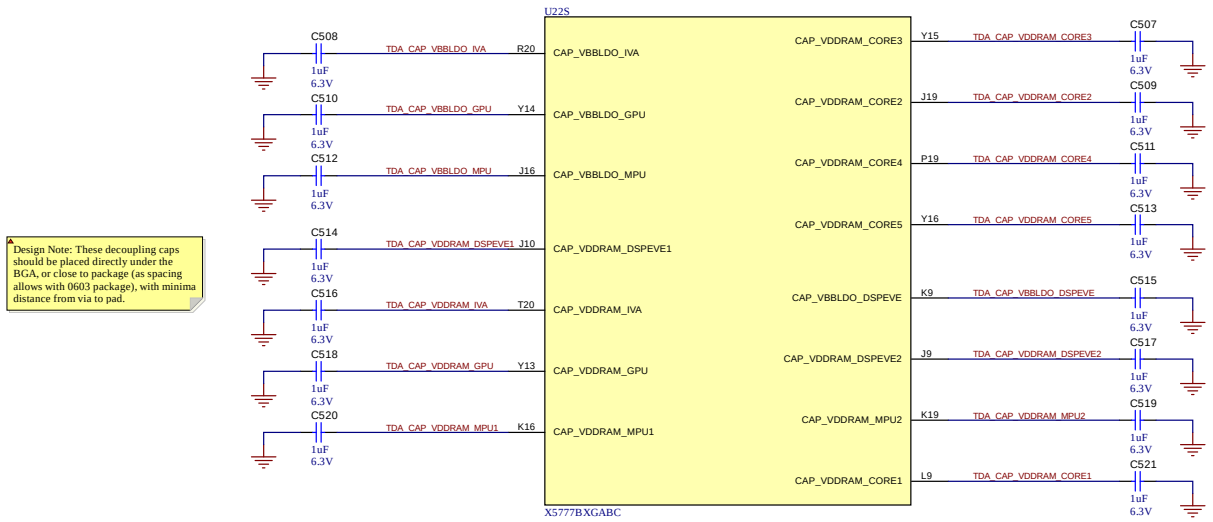
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:16 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Power_IO.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

TDA2 - Internal LDO External Output Capacitors

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.



Design Note: These decoupling caps should be placed directly under the BGA, or close to package (as spacing allows with 0603 package), with minima distance from via to pad.

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:17 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Power_Internal_LDO.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

References

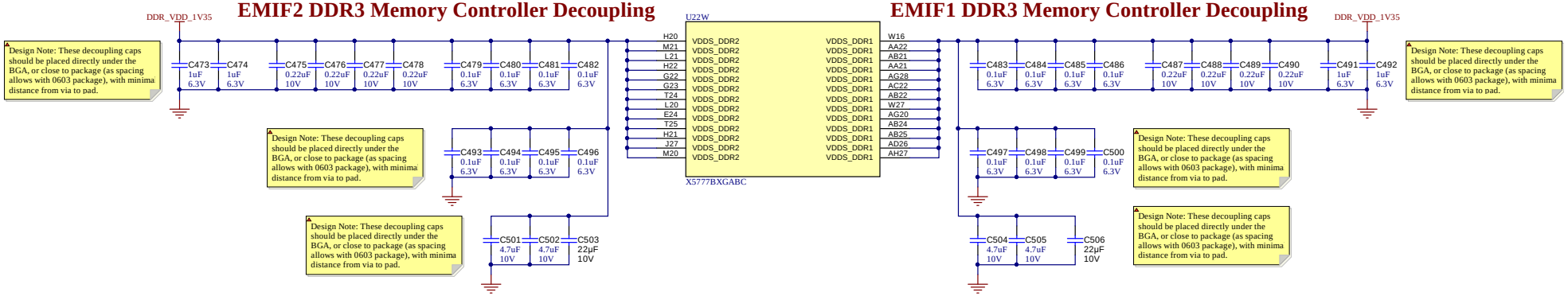
TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

TDA2 - DDR3 Memory Controller Power Nets and Decoupling

Follow all layout guidelines as presented in these documents.

Test points for checking SMPS output voltage nets. Place near respective loads.

EMIF2 DDR3 Memory Controller Decoupling



EMIF1 DDR3 Memory Controller Decoupling

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:18 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Power_DDR.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

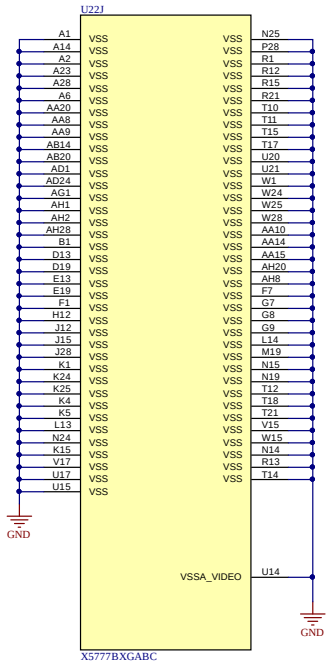
Texas Instruments
http://www.ti.com

TDA2 - Ground Return

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:19 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Power_Ground.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

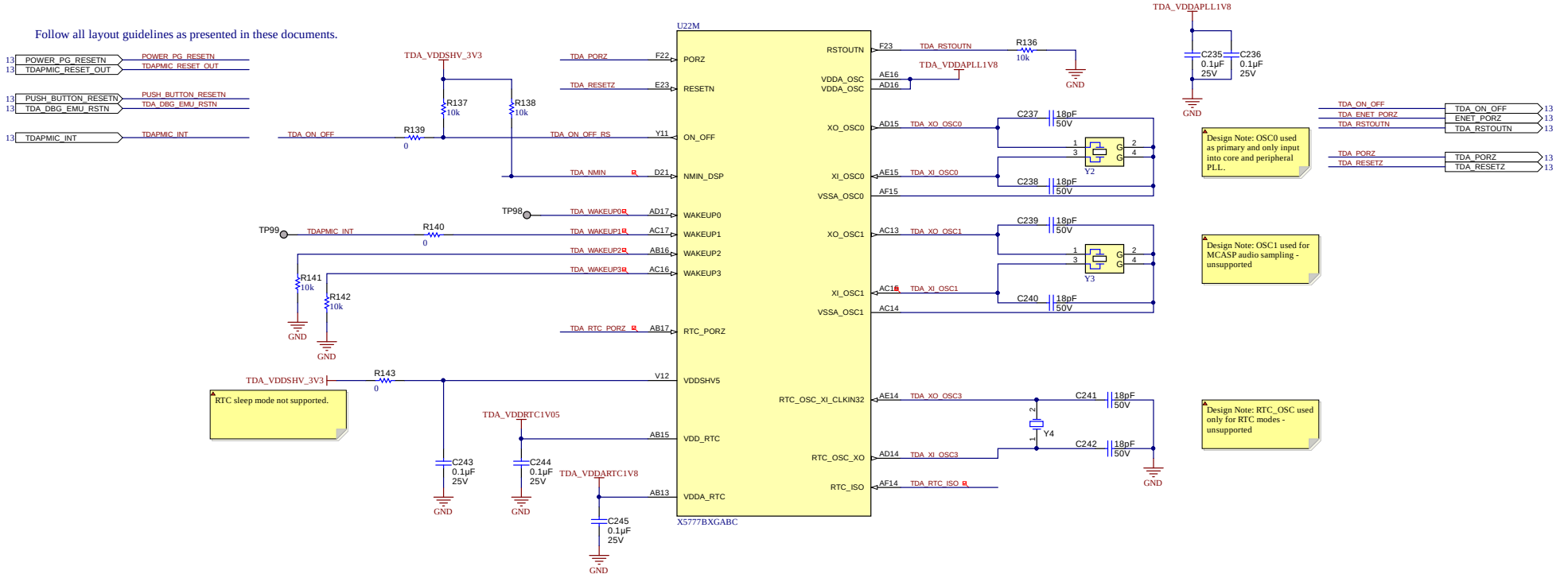
Texas Instruments
http://www.ti.com

TDA2 - Clock and Reset Signals

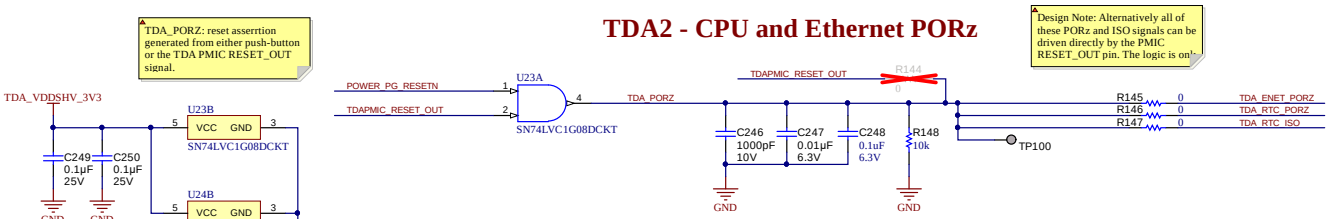
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

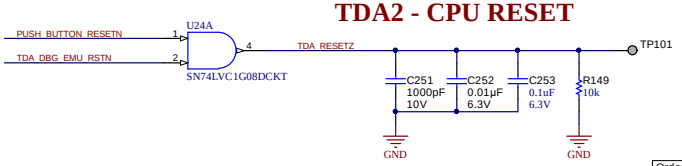
Follow all layout guidelines as presented in these documents.



TDA2 - CPU and Ethernet PORz



TDA2 - CPU RESET



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:20 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Clocks_Reset.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

TDA2 - Reset Generation and Reset Buttons

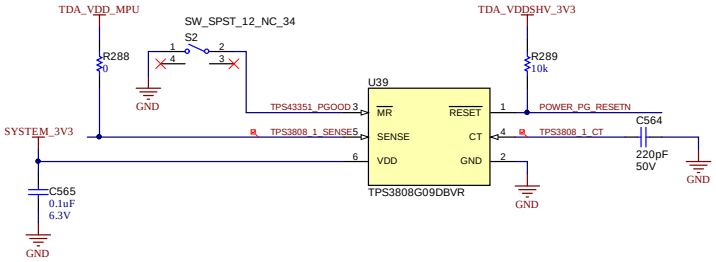
13 TPS43351_PGOOD — TPS43351_PGOOD

POWER_PG_RESETN — POWER_PG_RESETN 13
PUSH_BUTTON_RESETN — PUSH_BUTTON_RESETN 13

TPS3808 #1 - VDDMPU, System Supply and Pushbutton PORz

TPS3808 #1 - Generates a reset based on the status of the system level 5.0V and 3.3V supply power good signal TPS43351_PGOOD and the stat of the TDA_VDD_MPU SMPS rail.

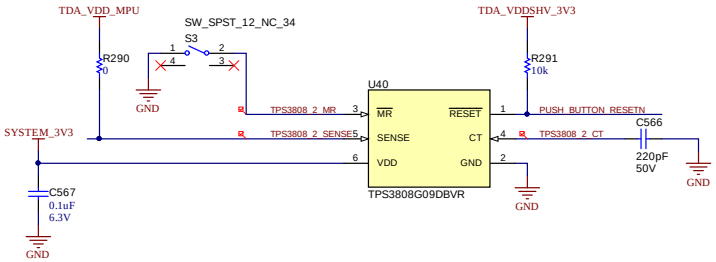
Pushbutton used to pull the MR pin low for PORz toggle.



TPS3808 #2 - VDDMPU and Pushbutton RESETz

TPS3808 #2 - Generates a reset based on the stat of the TDA_VDD_MPU SMPS rail.

Pushbutton used to pull the MR pin low for PORz toggle.



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:21 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Reset_Buttons.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

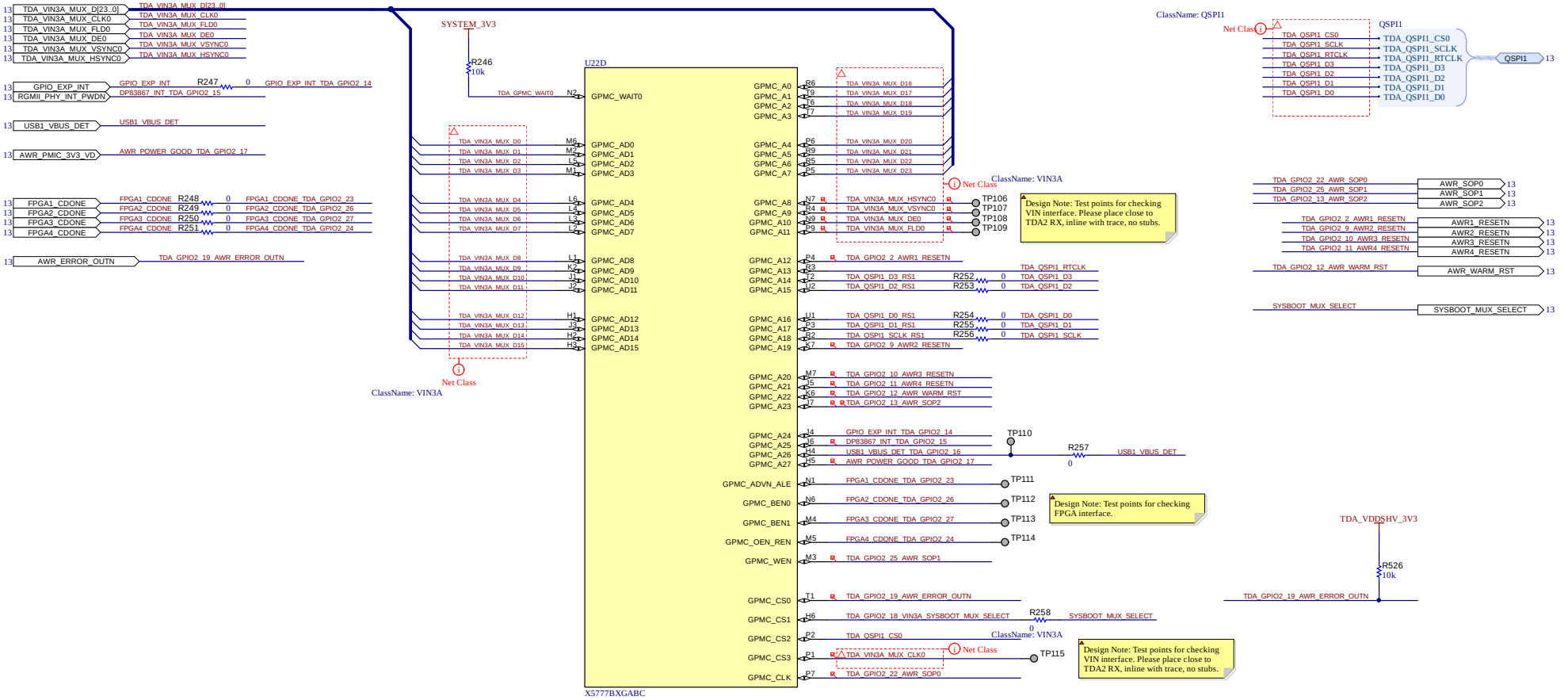
Texas Instruments
http://www.ti.com

TDA2 - GPMC, VIN3A, GPIO and SYSBOOT Interfaces

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

Follow all layout guidelines as presented in these documents.



Orderable: MMWCAS-DSP-EVM	Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A	Project Title: Cascade Radar Host Processor Board	
Number: PROC055 Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control	Assembly Variant:001	Sheet:22 of 66
Drawn By:Alec Schott	File: PROC055B_TDA2_GPMC_QSPI_VIN3A_SYSBOOT.SchDoc	
Engineer: Alec Schott	Contact: http://www.ti.com/mmwave	http://www.ti.com

TDA2 - VIN3A and SYSBOOT MUX

References

SN74CBTLV16212 Low-Voltage 24-Bit FET Buss-Exchange Switch
SN74CBTLV3257 Low-Voltage 4-Bit 1-of-2 FET
SN74LVC1G125 Single Bus Buffer Gate
SN74LVC1G04 Single Inverter Gate

Follow all layout guidelines as presented in these documents.

Design Note: MUX'ing and Delay Matching

The VIN3A data path is multiplexed with the SYSBOOT pins used for selecting the bootmode configuration of the TDA2 device.

This MUX set is used to select between the boot mode operation and functional mode operation.

Because some of the VIN3A signals are MUX'd ALL of the VIN3A signals must be run through a similar MUX architecture to ensure best delay matching across the bus. The extra channels on the 16212 are used for this purpose. The 3257 and the G125 a

SYSBOOT_MUX_SELECT
TDA_SYSBOOT[15..0]
TDA_VIN3A_D[23..0]
TDA_VIN3A_CLK0
TDA_VIN3A_FLD0
TDA_VIN3A_DE0
TDA_VIN3A_VSYNC0
Net Class
ClassName: VIN3A

SELECTN Generation

SYSTEM_3V3
R514 10k
U63A
SN74LVC1G04DCKR
U63B
C629 0.1uF 6.3V
GND

Delay Matching FET Switches

U65A
SN74LVC1G125DBVT
U65B
C631 0.1uF 6.3V
U66
SN74CBTLV3257DGVR
C632 0.1uF 6.3V
TP186
R519 10k
VIN3A signals from FPGA #3
VIN3A/SYSBOOT signals to TDA2

U62
SN74CBT16212CDGVR
C628 0.1uF 6.3V
VIN3A/SYSBOOT signals to TDA2
SYSBOOT state from boot selection switches.
VIN3A signals from FPGA #3
R515 R516 R517 0

U64
SN74CBT16212CDGVR
C630 0.1uF 6.3V
R520 R521 R522 0

Design Note: MUX Operations

SYSBOOT_MUX_SELECT = low: FPGA VIN3A -> TDA2x
SN74CBTLV16210 20-bit 2:1 MUX #1 - B2 -> A1
SN74CBTLV16210 20-bit 2:1 MUX #2 - B2 -> A1
SN74CBTLV3257 4-bit 2:1 MUX - B2->A

SYSBOOT_MUX_SELECT = high: Bootmode Switches -> TDA2x
SN74CBTLV16210 20-bit 2:1 MUX#1: B1 -> A1
SN74CBTLV16210 20-bit 2:1 MUX#2: B1 -> A1
SN74CBTLV3257 4-bit 2:1 MUX - B1->A

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:23 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_VIN3A_SYSBOOT_MUX.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

TDA2 - SYSBOOT Switches

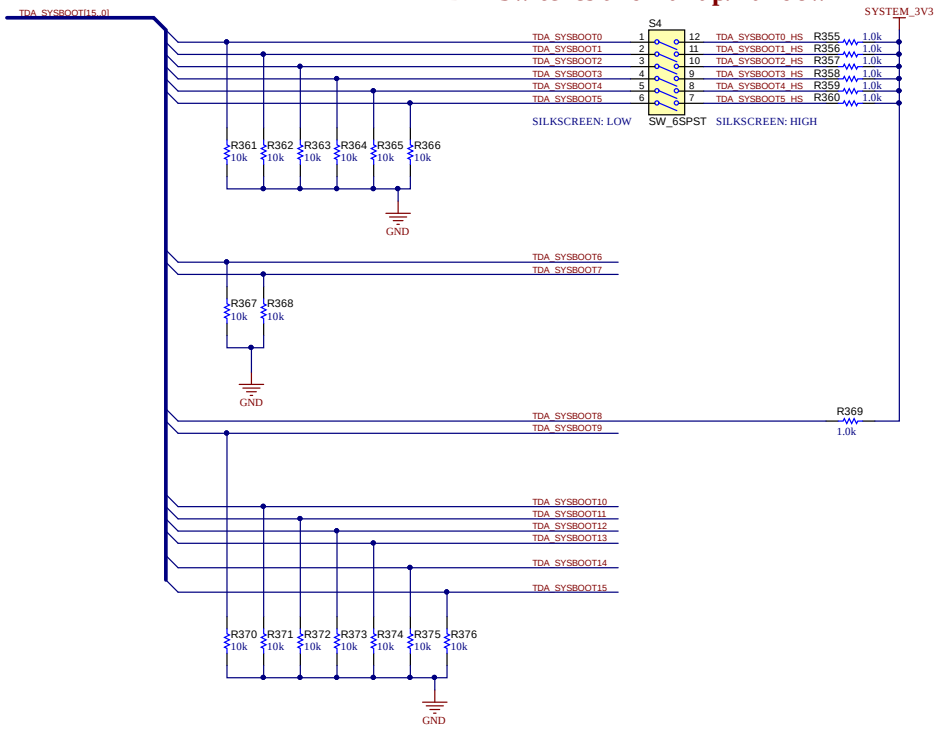
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
TDA2 Technical Reference Manual - Section 29.2.4 "Sysboot Configuration" (Internal Only)

Follow all layout guidelines as presented in these documents.

TDA_SYSBOOT[15..0] → TDA_SYSBOOT[15..0] 13

DIP Switches and Pullup/Pulldown



Design Note: SYSBOOT[5:0] Interfaces and devices boot list
-> See TRM Table 29-9 "Booting Devices Order"

SYSBOOT[5:0] - 0b110110 -> selects QSPI_1 bootmode.

Design Note: SYSBOOT[7:6]
SYSBOOT[7:6] - 0b00 -> Redundant SBL image offset set to 64KByte

Design Note: SYSBOOT[9:8] System Clock - SYS_CLK1 Speed Selection
SYSBOOT[9:8] - 0b01 -> 20 MHz XO frequency

Design Note:
SYSBOOT[13:10] - GPMC Unused - Tied Low

Design Note:
SYSBOOT[14] - Tied low per datasheet.

Design Note:
SYSBOOT[15] - 0b0 -> Software re-configuration of pull resistors is allowed.

Design Note: Bootmode selection with the SYSBOOT pins. SYSBOOT[15:0] pins latched on PORz de-assertion.

SYSBOOT[5:0] - Selects interfaces for the booting list

SYSBOOT[7:6] - Sector ofset for the location of the redundant SBL images in QSPI.

SYSBOOT[9:8] - Selects the SYS_CLK1 clock speed. Must be set correctly according to the speed of the connected crystal.

SYSBOOT[13:10] - Used to configure the GPMC interface when booting from XIP/NAND memory connected to GPMC.

SYSBOOT[14] - Must be pulled to vss for proper device operation.

SYSBOOT[15] - Must be pulled to vdd for proper device operation (SR1.x). Used to permanently disable the internal PU/PD resistors on pads gpmc_a[27:24, 22:19] (SR2.0).

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:24 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_SYSBOOT_Switches.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

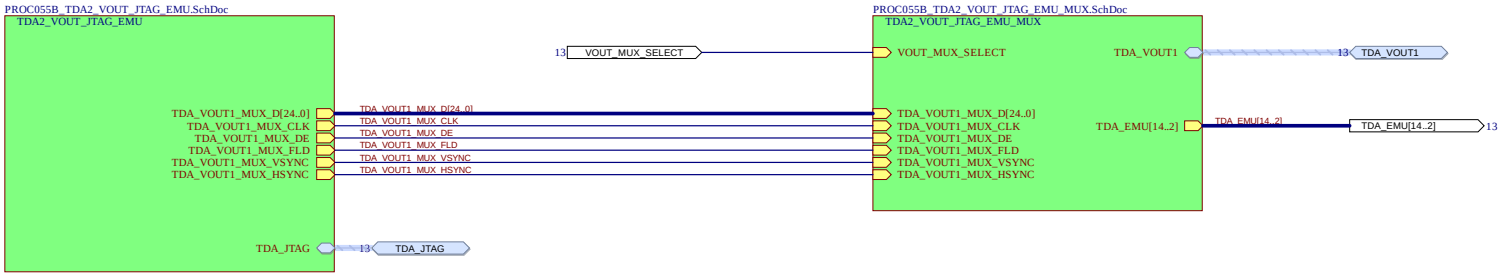
References

Follow all layout guidelines as presented in these documents.

Design Note: MUX'ing and Delay Matching

The VOUT1 bus is mux'd with the EMU port and many other GPIO signals used throughout the system.

TDA2 - VOUT1, EMU and JTAG Top



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 3/29/2021
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:25 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_VOUT_JTAG_EMU_Top.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

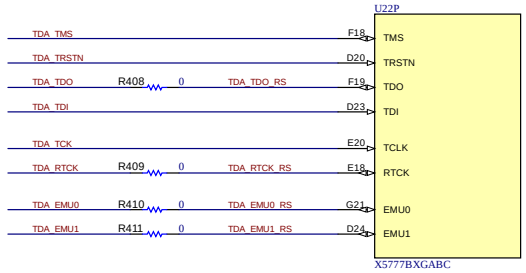
References

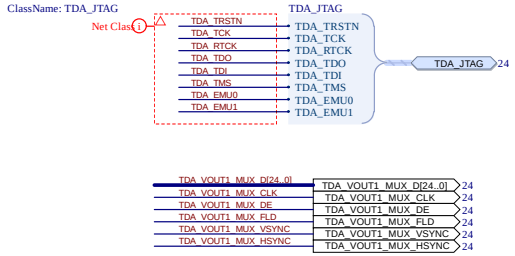
TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

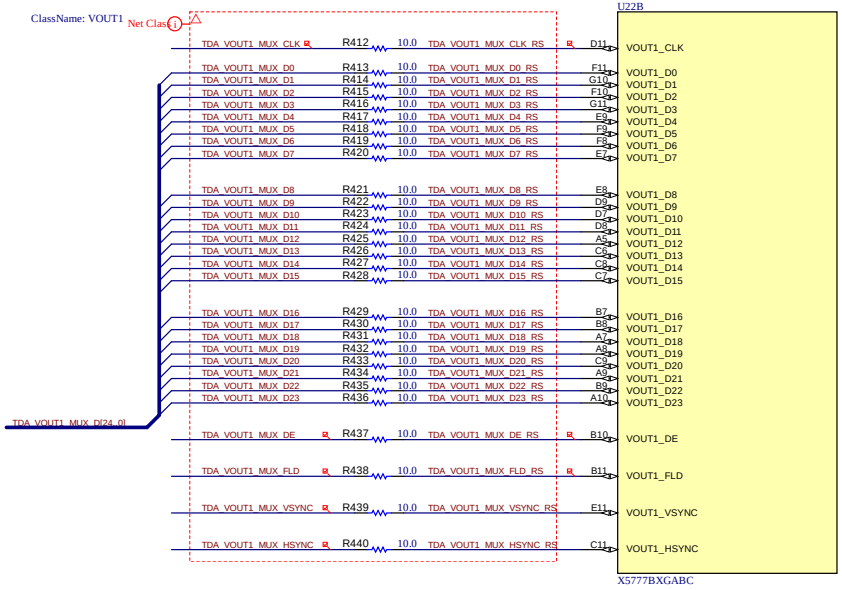
TDA2 - JTAG and Emulation/Trace Bus and Header

TDA2 - JTAG





TDA2 - VOUT1 and EMU Bus



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:26 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_VOUT_JTAG_EMU.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

TDA2 - VOUT1, EMU and GPIO MUX

References

SN74CBTLV16212 Low-Voltage 24-Bit FET Buss-Exchange Switch
SN74CBTLV3257 Low-Voltage 4-Bit 1-of-2 FET
SN74LVC1G125 Single Bus Buffer Gate
SN74LVC1G04 Single Inverter Gate

Follow all layout guidelines as presented in these documents.

Design Note: MUX'ing and Delay Matching

The VOUT1 bus is mux'd with the EMU port and many other GPIO signals used throughout the system.

24 VOUT_MUX_SELECT → VOUT_MUX_SELECT

24 TDA_VOUT1_MUX_D[24..0] → TDA_VOUT1_MUX_D[24..0]
24 TDA_VOUT1_MUX_CLK → TDA_VOUT1_MUX_CLK
24 TDA_VOUT1_MUX_DE → TDA_VOUT1_MUX_DE
24 TDA_VOUT1_MUX_FLD → TDA_VOUT1_MUX_FLD
24 TDA_VOUT1_MUX_VSYNC → TDA_VOUT1_MUX_VSYNC
24 TDA_VOUT1_MUX_HSYNC → TDA_VOUT1_MUX_HSYNC

TDA_VOUT1_D[23..0] → TDA_VOUT1_D[23..0]
TDA_VOUT1_CLK → TDA_VOUT1_CLK
TDA_VOUT1_DE → TDA_VOUT1_DE
TDA_VOUT1_FLD → TDA_VOUT1_FLD
TDA_VOUT1_VSYNC → TDA_VOUT1_VSYNC
TDA_VOUT1_HSYNC → TDA_VOUT1_HSYNC
TDA_VOUT1_D[23..0] + TDA_VOUT1_CLK + TDA_VOUT1_DE + TDA_VOUT1_FLD + TDA_VOUT1_VSYNC + TDA_VOUT1_HSYNC → 24 TDA_VOUT1

SELECTN Generation

SYSTEM_3V3
R400 10k
VOUT_MUX_SELECT → U56A (SN74LVC1G04DCKR) → VOUT_MUX_SELECTN
U56B (SN74LVC1G04DCKR): NC, VCC, GND
SYSTEM_3V3 → C620 0.1uF 6.3V → GND

EMU/VOUT/GPIO signals to/from TDA2

SYSTEM_3V3 → C619 0.1uF 6.3V → GND

U55 (SN74CBT16212CDGVR)
VCC
1A1 TDA_VOUT1_MUX_D0
2A1 TDA_VOUT1_MUX_D1
3A1 TDA_VOUT1_MUX_D2
4A1 TDA_VOUT1_MUX_D3
5A1 TDA_VOUT1_MUX_D4
6A1 TDA_VOUT1_MUX_D5
7A1 TDA_VOUT1_MUX_D6
8A1 TDA_VOUT1_MUX_D7
9A1 TDA_VOUT1_MUX_D8
10A1 TDA_VOUT1_MUX_D9
11A1 TDA_VOUT1_MUX_D10
12A1 TDA_VOUT1_MUX_D11
1B1 TDA_VOUT1_D0
2B1 TDA_VOUT1_D1
3B1 TDA_VOUT1_D2
4B1 TDA_VOUT1_D3
5B1 TDA_VOUT1_D4
6B1 TDA_VOUT1_D5
7B1 TDA_VOUT1_D6
8B1 TDA_VOUT1_D7
9B1 TDA_VOUT1_D8
10B1 TDA_VOUT1_D9
11B1 TDA_VOUT1_D10
12B1 TDA_VOUT1_D11
TDA_VOUT1_MUX_D[24..0] → TDA_VOUT1_D[23..0]
VOUT1 path to/from ECP5 FPGA prototyping header

1A1 TDA_EMU2
2A1 TDA_EMU5
3A1 TDA_EMU6
4A1 TDA_EMU7
5A1 TDA_EMU8
6A1 TDA_EMU9
7A1 TDA_EMU3
8A1 TDA_EMU10
1B2 TDA_EMU2
2B2 TDA_EMU5
3B2 TDA_EMU6
4B2 TDA_EMU7
5B2 TDA_EMU8
6B2 TDA_EMU9
7B2 TDA_EMU3
8B2 TDA_EMU10
TDA_EMU[14..2] → TDA_EMU[14..2] 24
EMU path to/from debug header

S0 VOUT_MUX_SELECT → R401 0 → TDA_VOUT_MUX_S0_RS
S1 VOUT_MUX_SELECTN → R402 0 → TDA_VOUT_MUX_S1_RS
S2 R403 0 → TDA_VOUT_MUX_S2_RS
GND, GND, GND, GND

Delay Matching FET Switches

GND
U58A (SN74LVC1G125DBVT): TDA_VOUT1_MUX_CLK → TDA_VOUT1_CLK_RS → R404 0 → TDA_VOUT1_CLK
SYSTEM_3V3
U58B (SN74LVC1G125DBVT): VCC, GND
C622 0.1uF 6.3V → GND

SYSTEM_3V3 → C623 0.1uF 6.3V → GND

U59 (SN74CBTLV3257DGVR)
VCC
1B1 TDA_VOUT1_MUX_DE
1B2 TDA_VOUT1_MUX_FLD
3B1 TDA_VOUT1_MUX_VSYNC
4B1 TDA_VOUT1_MUX_HSYNC
S VOUT_MUX_SELECTN
OE → GND
1A TDA_VOUT1_DE
2A TDA_VOUT1_FLD
3A TDA_VOUT1_VSYNC
4A TDA_VOUT1_HSYNC
GND

EMU/VOUT/GPIO signals to/from TDA2
VOUT1 path to/from ECP5 FPGA prototyping header

SYSTEM_3V3 → C621 0.1uF 6.3V → GND

U57 (SN74CBT16212CDGVR)
VCC
1A1 TDA_VOUT1_MUX_D12
2A1 TDA_VOUT1_MUX_D13
3A1 TDA_VOUT1_MUX_D14
4A1 TDA_VOUT1_MUX_D15
5A1 TDA_VOUT1_MUX_D16
6A1 TDA_VOUT1_MUX_D17
7A1 TDA_VOUT1_MUX_D18
8A1 TDA_VOUT1_MUX_D19
9A1 TDA_VOUT1_MUX_D20
10A1 TDA_VOUT1_MUX_D21
11A1 TDA_VOUT1_MUX_D22
12A1 TDA_VOUT1_MUX_D23
1B1 TDA_VOUT1_D12
2B1 TDA_VOUT1_D13
3B1 TDA_VOUT1_D14
4B1 TDA_VOUT1_D15
5B1 TDA_VOUT1_D16
6B1 TDA_VOUT1_D17
7B1 TDA_VOUT1_D18
8B1 TDA_VOUT1_D19
9B1 TDA_VOUT1_D20
10B1 TDA_VOUT1_D21
11B1 TDA_VOUT1_D22
12B1 TDA_VOUT1_D23
TDA_VOUT1_MUX_D[24..0] → TDA_VOUT1_D[23..0]
VOUT1 path to/from ECP5 FPGA prototyping header

1A1 TDA_EMU11
2A1 TDA_EMU12
3A1 TDA_EMU13
4A1 TDA_EMU14
5A1 TDA_EMU4
1B2 TDA_EMU11
2B2 TDA_EMU12
3B2 TDA_EMU13
4B2 TDA_EMU14
5B2 TDA_EMU4
TDA_EMU[14..2] → TDA_EMU[14..2] 24
EMU path to/from debug header

S0 VOUT_MUX_SELECT → R405 0 → TDA_VOUT_MUX_S0_RS
S1 VOUT_MUX_SELECTN → R406 0 → TDA_VOUT_MUX_S1_RS
S2 R407 0 → TDA_VOUT_MUX_S2_RS
GND, GND, GND, GND

Design Note: MUX Operations

SYSBOOT_MUX_SELECT = low: EMU Port and GPIO to TDA2x
SN74CBTLV16210 20-bit 2:1 MUX #1 - B2 -> A1
SN74CBTLV16210 20-bit 2:1 MUX #2 - B2 -> A1
SN74CBTLV3257 4-bit 2:1 MUX - B1->A

SYSBOOT_MUX_SELECT = high: VOUT1 Port to ECP5 FPGA Header
SN74CBTLV16210 20-bit 2:1 MUX#1: B1 -> A1
SN74CBTLV16210 20-bit 2:1 MUX#2: B1 -> A1
SN74CBTLV3257 4-bit 2:1 MUX - B2->A

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:27 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_VOUT_JTAG_EMU_MUX_Sch.DSN	Size:B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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http://www.ti.com

TDA2 - EMIF1 DDR3 Controller

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

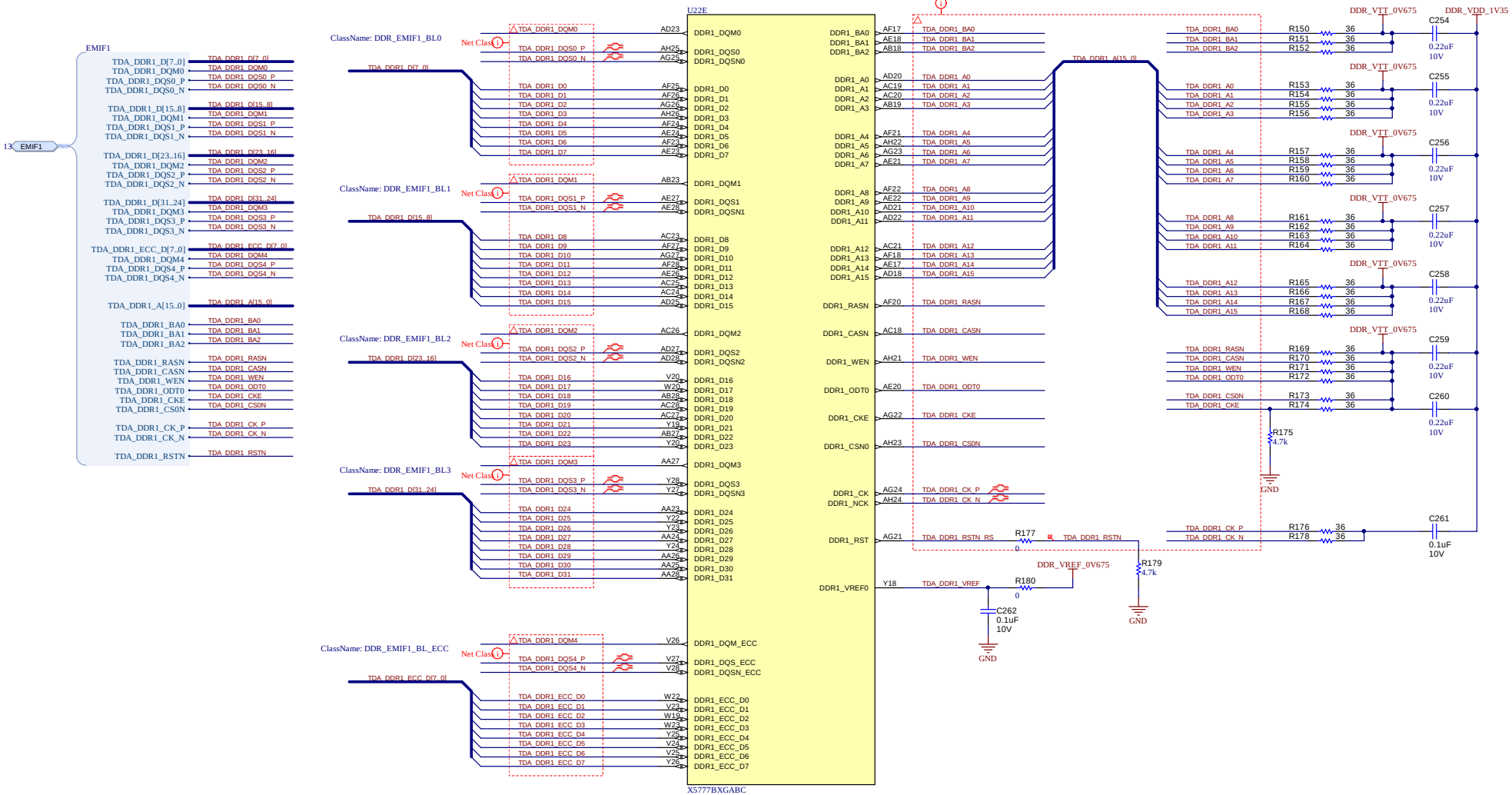
Micron Technical Note TN-41-13: DDR3 Point-to-Point Design Support
Micron Technical Note TDA2TN-41-01: Calculating Memory System Power For DDR3

Follow all layout guidelines as presented in these documents.

Design Note: All Data, Mask and Data-Strobe signals shall be routed point to point.

Design Note: All Clock, Address, Command and Control signals to be routed as DDR3L "Fly-By" signals. Series and Series-AC termination to be placed end of "Fly-By" routing.

EMIF1 Fly-By Terminations



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:28 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_DDR3_EMIF1.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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TDA2 - EMIF2 DDR3 Controller

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

Micron Technical Note TN-41-13: DDR3 Point-to-Point Design Support
Micron Technical Note TDA2TN-41-01: Calculating Memory System Power For DDR3

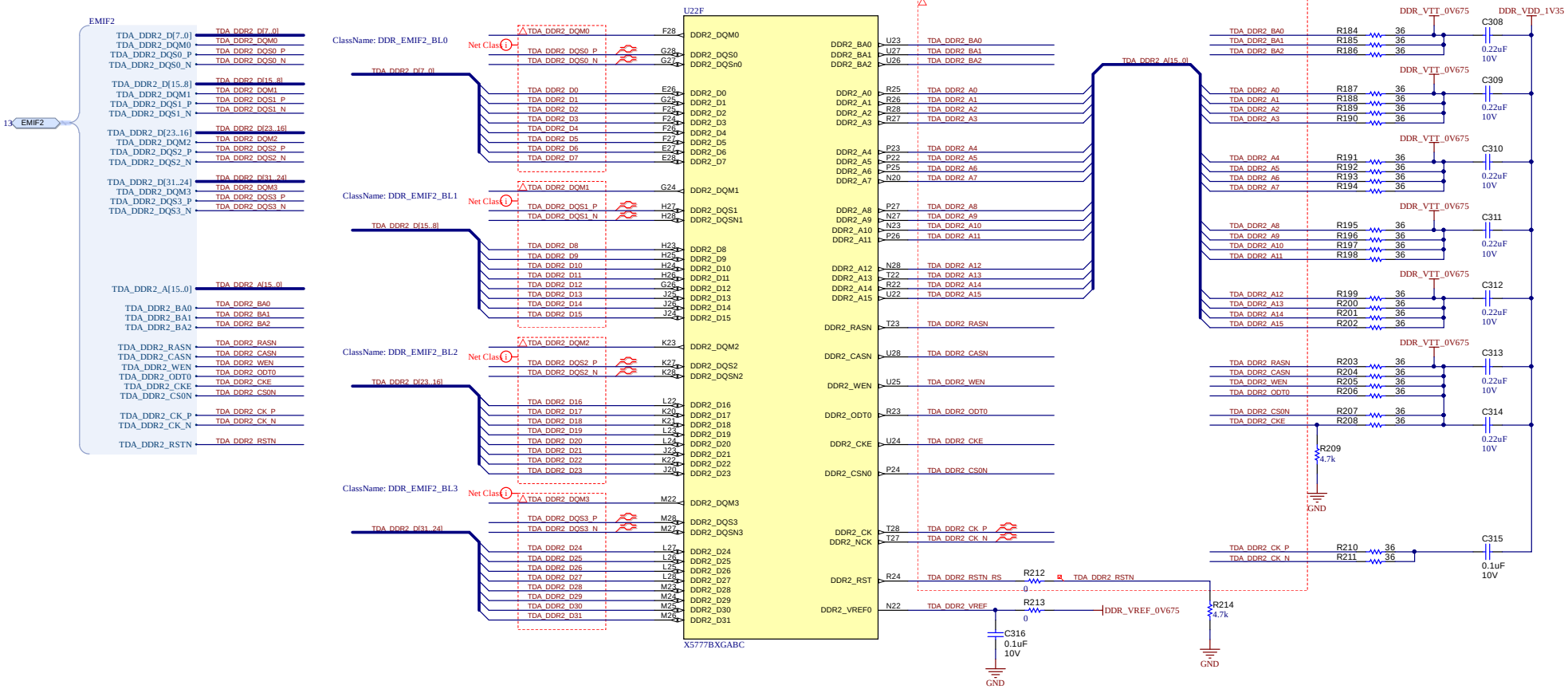
Follow all layout guidelines as presented in these documents.

Design Note: All Data, Mask and Data-Strobe signals shall be routed point to point.

Design Note: All Clock, Address, Command and Control signals to be routed as DDR3L "Fly-By" signals. Series and Series-AC termination to be placed end of "Fly-By" routing.

ClassName: DDR_EMIF2_ADDR_CMD_CTRL_CK
Net Class 1

EMIF2 Fly-By Terminations

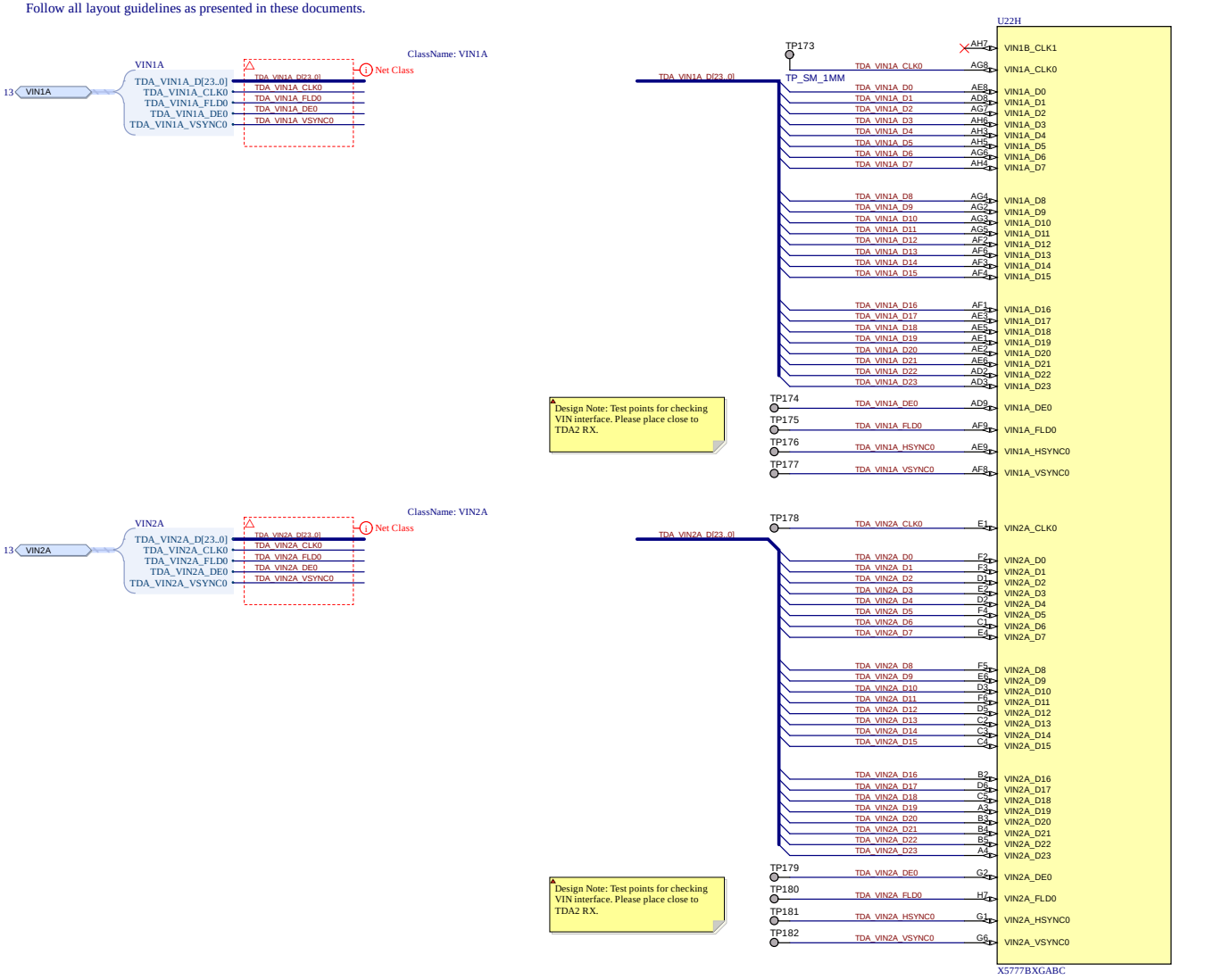


Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
BOM Rev: Not in version control		Assembly Variant:001	Sheet:29 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_DDR3_EMIF2.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

TDA2 - VIN1A and VIN2A Interfaces

References
TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

Follow all layout guidelines as presented in these documents.



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:30 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_VIN1A_VIN2A.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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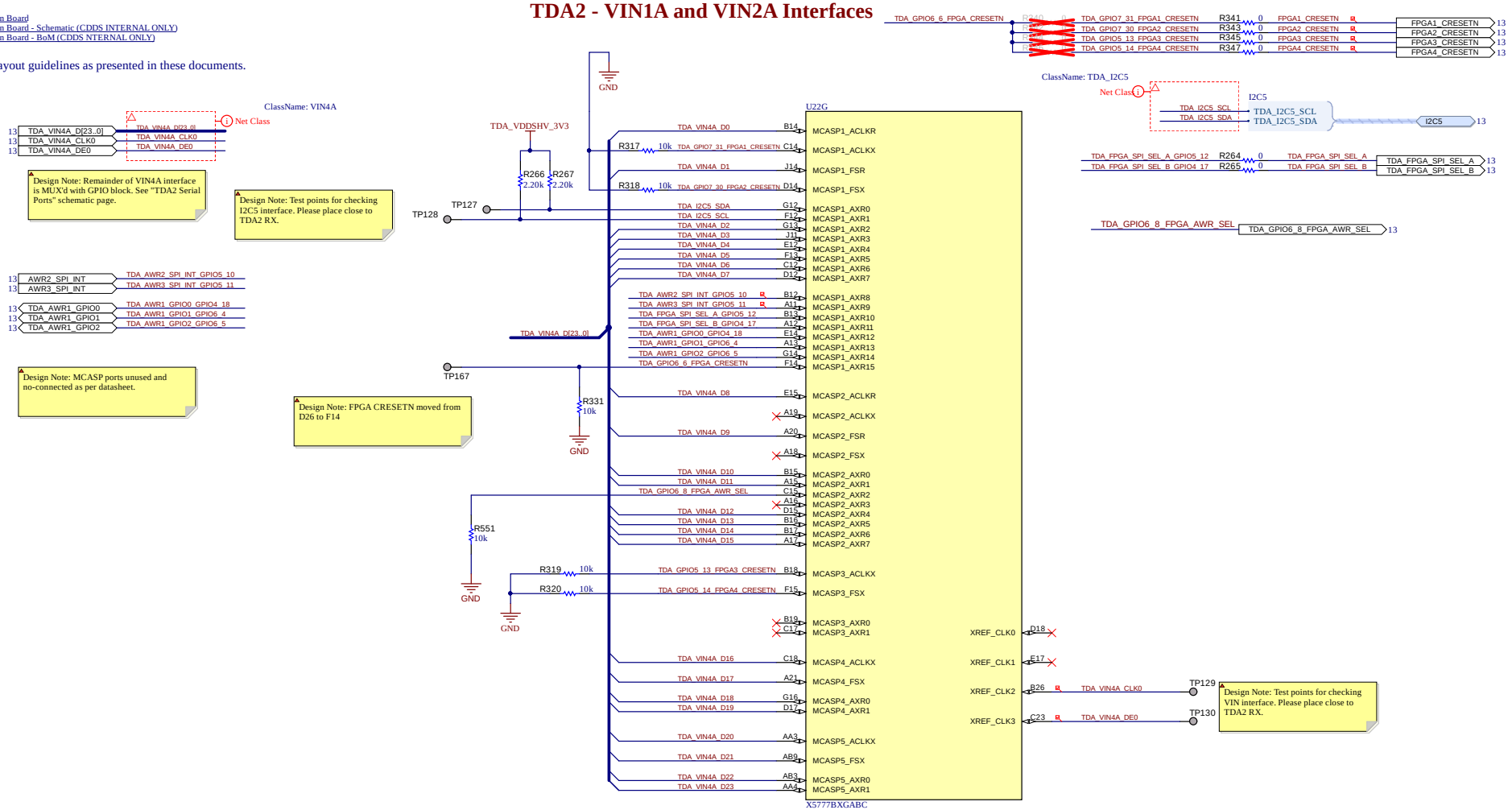
TDA2 - VIN1A and VIN2A Interfaces

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

Follow all layout guidelines as presented in these documents.



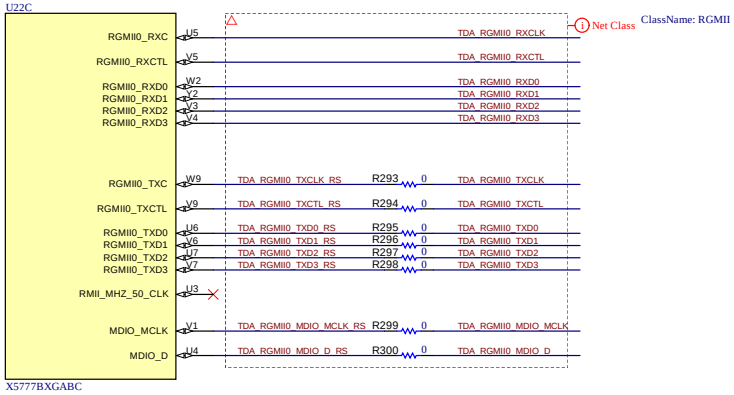
Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:31 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_MCASP_VIN4A.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

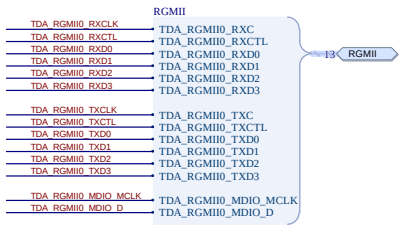
TDA2 - RGMII 1Gigabit Ethernet

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.





Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:32 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_RGMII.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

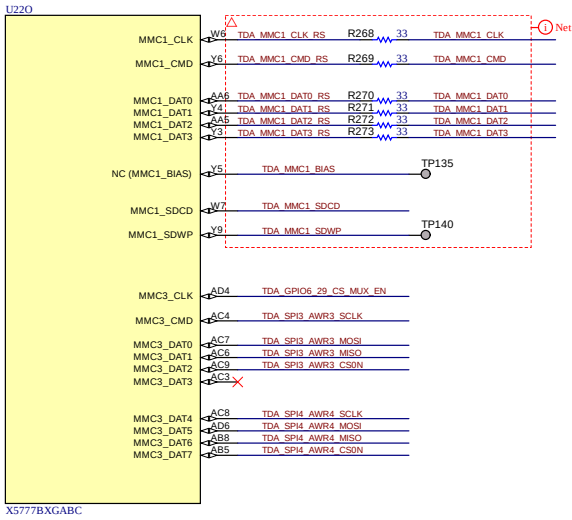
Texas Instruments
http://www.ti.com

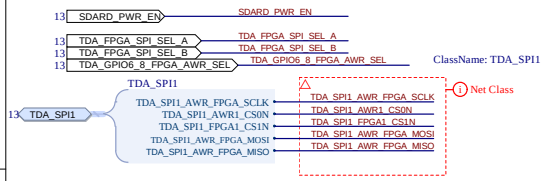
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

TDA2 - MMC1, SPI2 and SPI4 and SDCard Connector

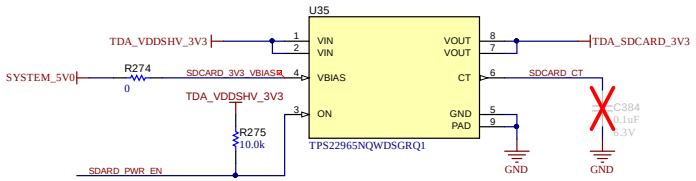




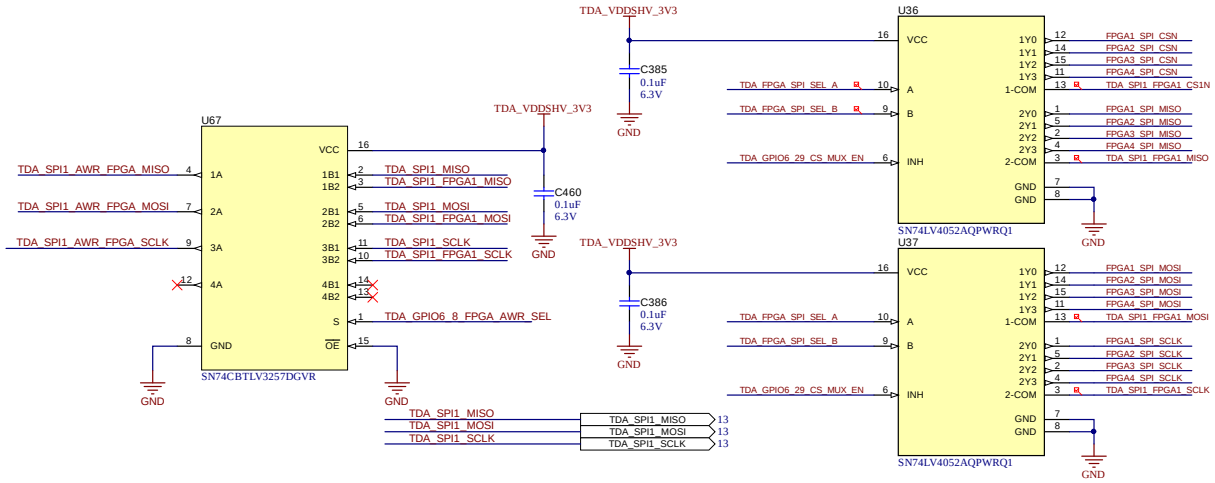
TDA2 - Fixed 3.3V SD Card Supply

A load switch is used to allow a TDA GPIO to control when the SD Card 3.3V I/O supply is sequenced.

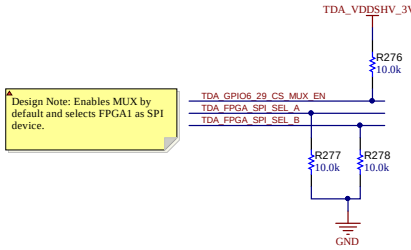
SDCARD 3.3V Power Switch

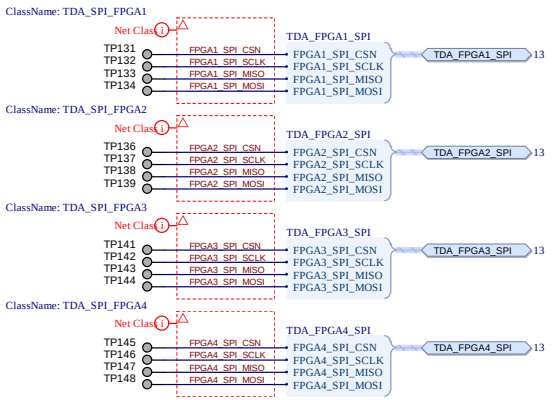


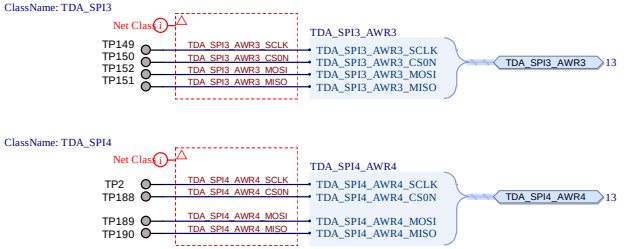
SPI4 - FPGA[4:1] MUX



SPI4 - FPGA[4:1] MUX - ENABLE and SELECT







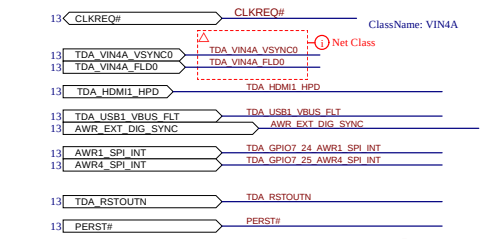
Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
BOM Rev: Not in version control		Assembly Variant:001	Sheet:33 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_MMC1_SPI3_SPI4.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

TDA2 - Serial Ports: UART1, UART2, I2C1, I2C2, SPI1, SPI2, DCAN1, UART1, UART2, UART3 and VIN4A

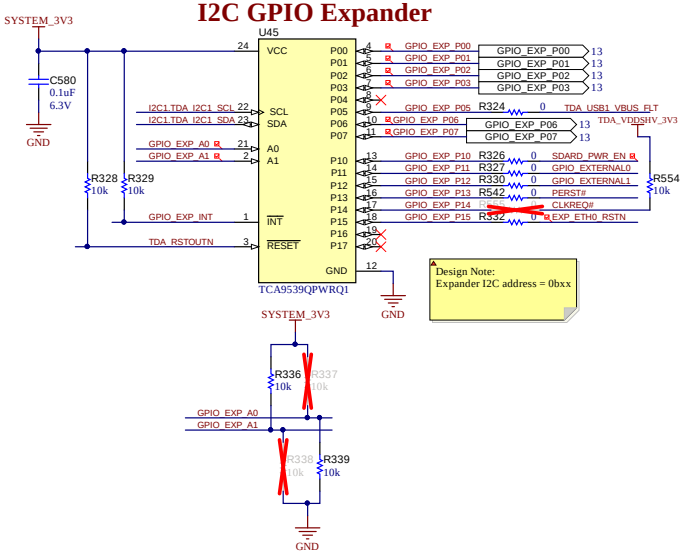
References

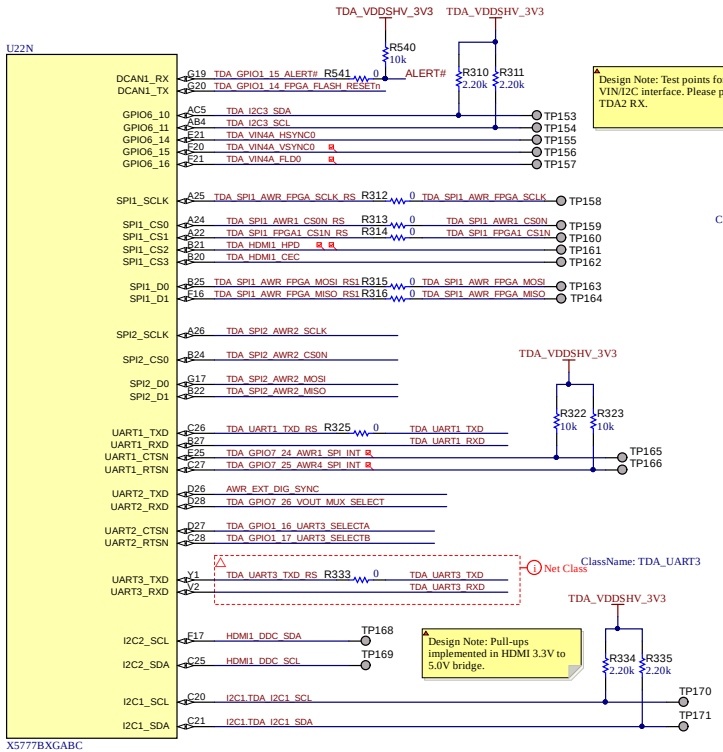
TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

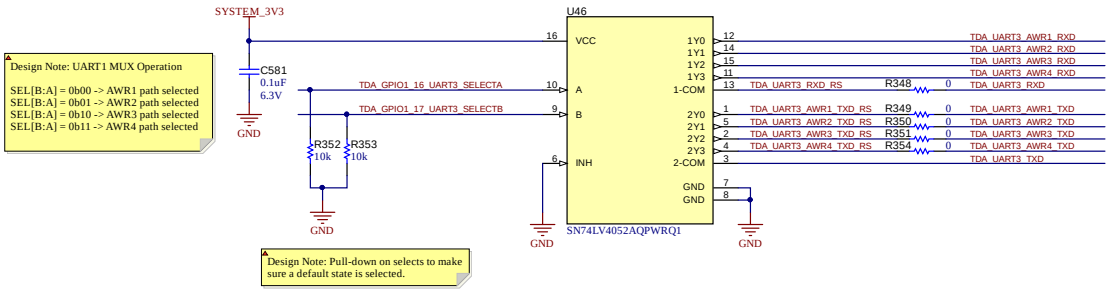


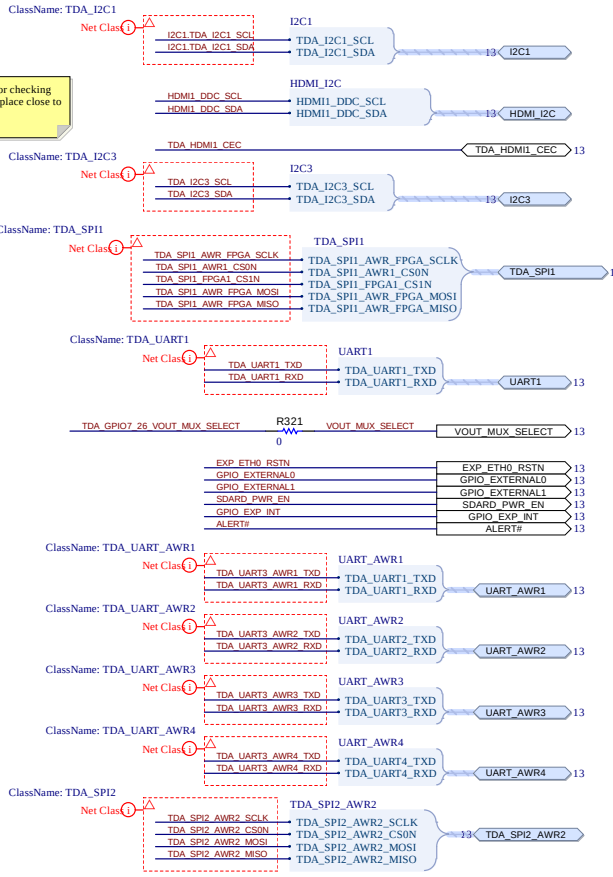
I2C GPIO Expander





UART1 - AWR[4:1] MUX





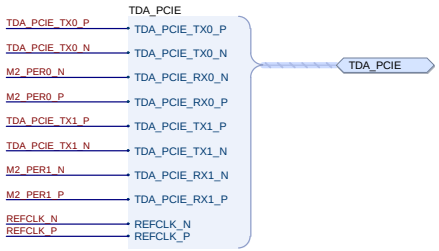
Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:34 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Serial_Ports.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

TDA2 - SATA and PCIe Interfaces

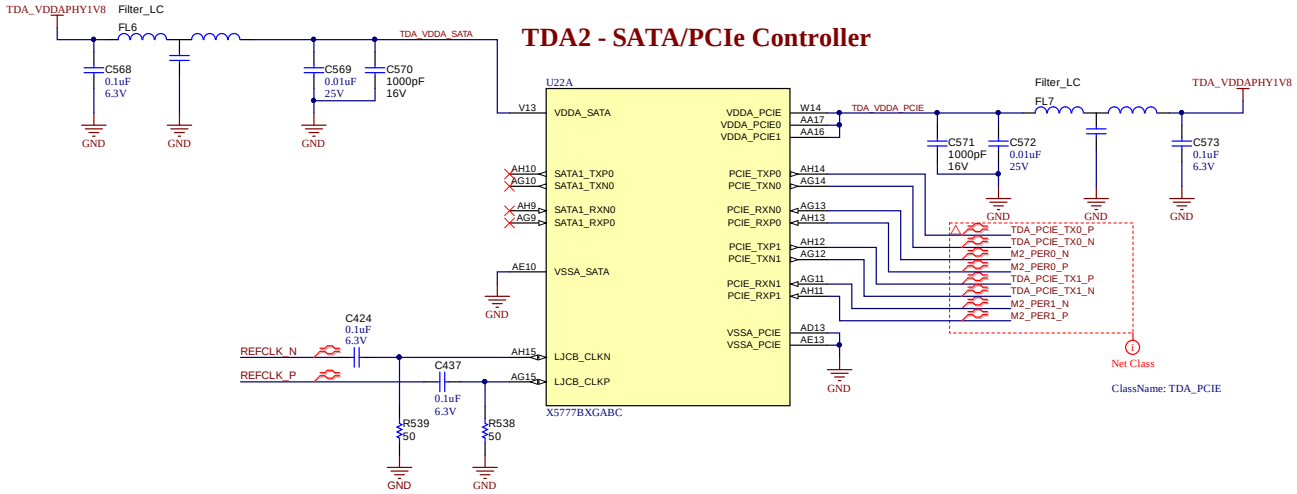
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.



TDA2 - SATA/PCIe Controller



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:35 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_SATA.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

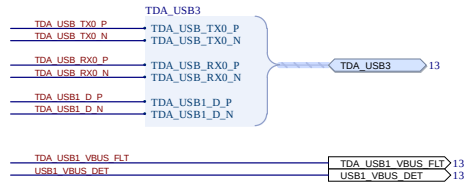
Texas Instruments
http://www.ti.com

References

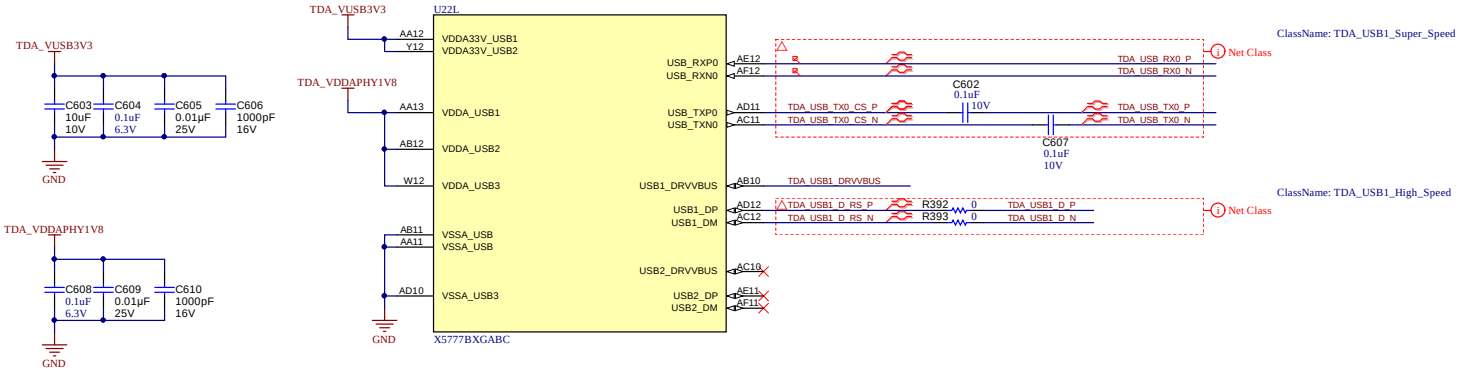
[TDA2 Evaluation Board]
[TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)]
[TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)]
[Vayu Power Integrity Analysis - (INTERNAL ONLY)]

Follow all layout guidelines as presented in these documents.

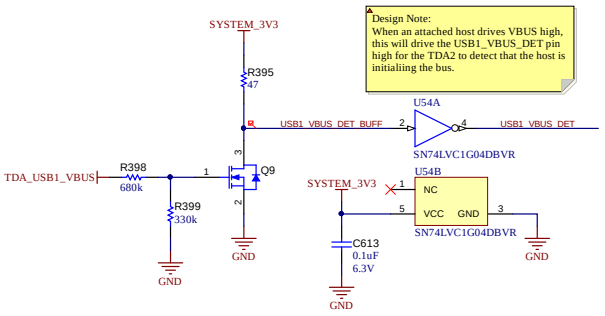
TDA2 - USB3 Interface



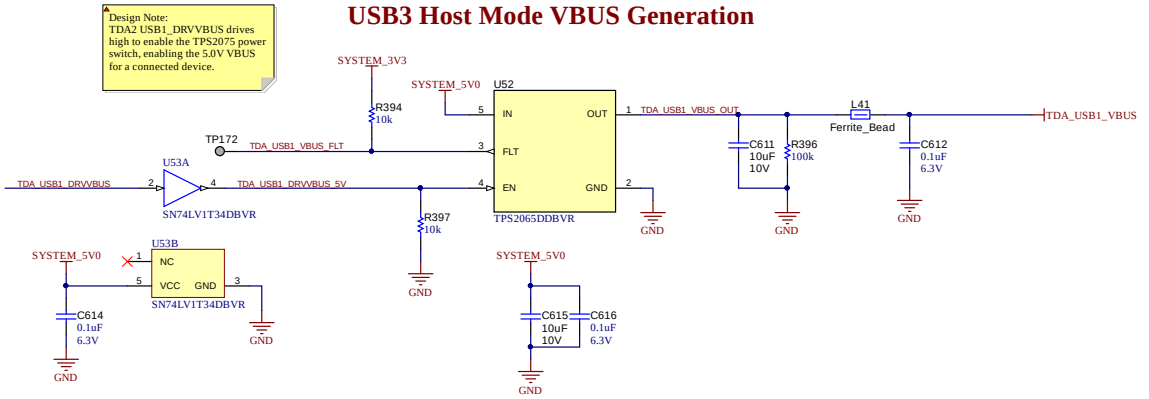
TDA2 - USB3.0 Super-Speed Interface



USB3 Device Mode VBUS Detect



USB3 Host Mode VBUS Generation



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
BOM Rev: Not in version control		Assembly Variant:001	Sheet:36 of 66
Drawn By:		File: PROC055B_TDA2_USB3.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

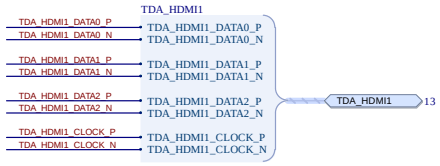
References

TDA2 Datamanual (CDDS INTERNALY ONLY!)

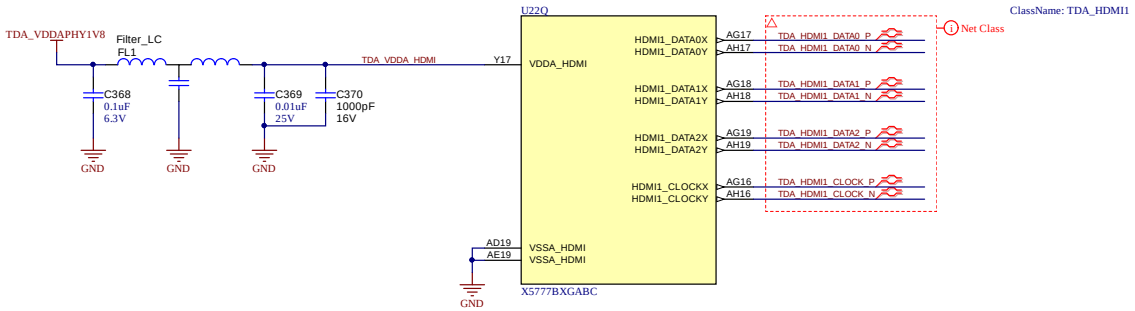
TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

TDA2 - HDMI Interface



TDA2 - HDMI 1.4b Interface



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:37 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_HDMI.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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TDA2 - EMIF1 DDR3 - SDRAM

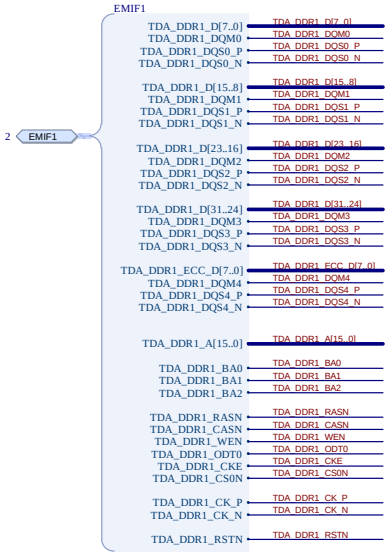
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

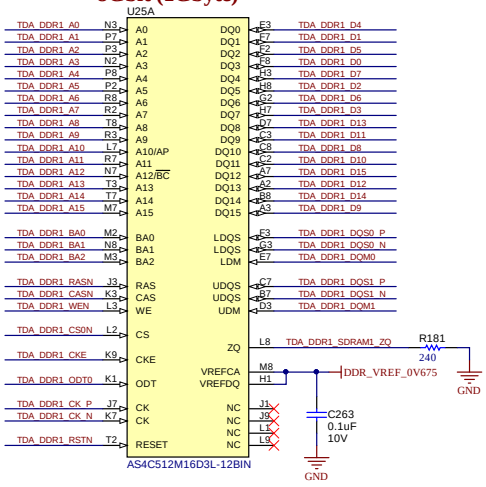
Micron Technical Note TN-41-13: DDR3 Point-to-Point Design Support
Micron Technical Note TDA2TN-41-01: Calculating Memory System Power For DDR3

Follow all layout guidelines as presented in these documents.

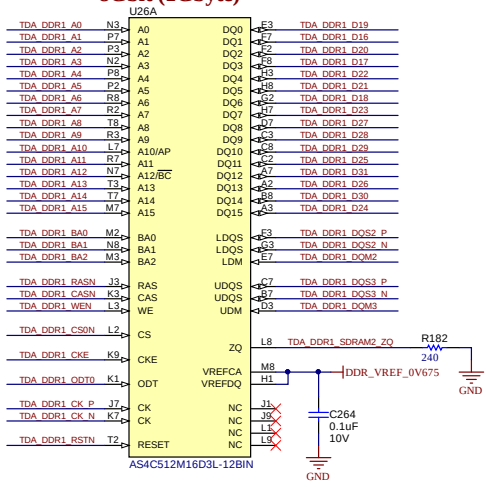
EMIF1



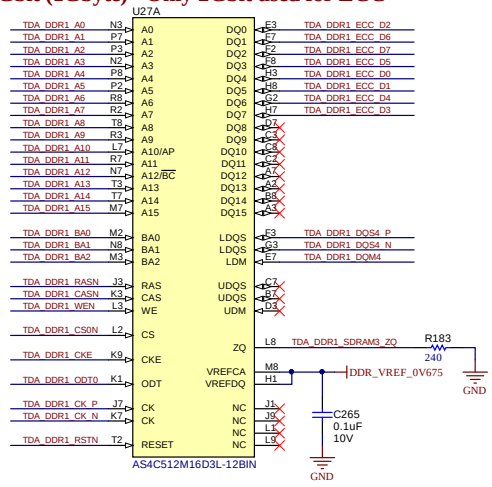
SDRAM1, 64 Meg x 16 x 8 banks 8Gbit (1Gbyte)

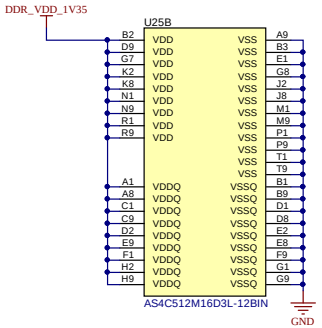


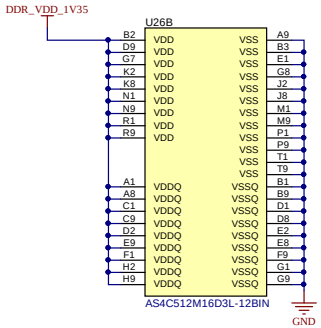
SDRAM2, 64 Meg x 16 x 8 banks 8Gbit (1Gbyte)

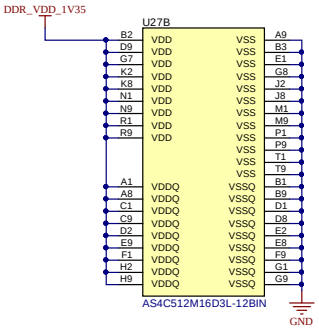


SDRAM2, 64 Meg x 16 x 8 banks 8Gbit (1Gbyte) - Only 2Gbit used for ECC

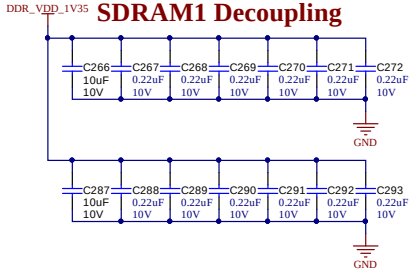




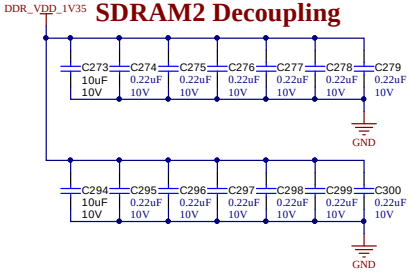




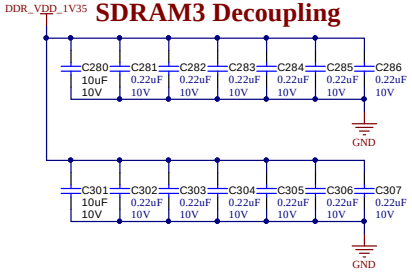
SDRAM1 Decoupling



SDRAM2 Decoupling



SDRAM3 Decoupling



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/18/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:38 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_DDR3_EMIF1_DDR3_SDRAM.SchDoc	Size:B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

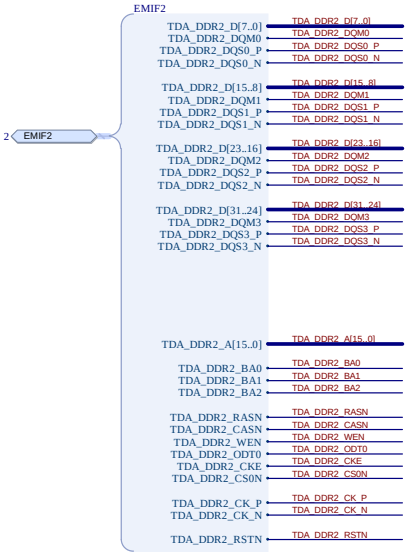
TDA2 - EMIF2 DDR3 - SDRAM

References

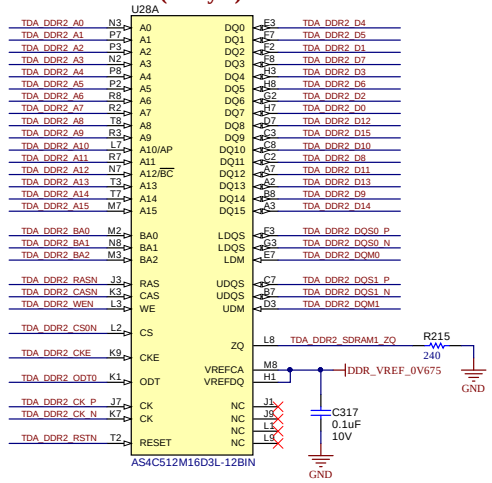
TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

Micron Technical Note TN-41-13: DDR3 Point-to-Point Design Support
Micron Technical Note TDA2TN-41-01: Calculating Memory System Power For DDR3

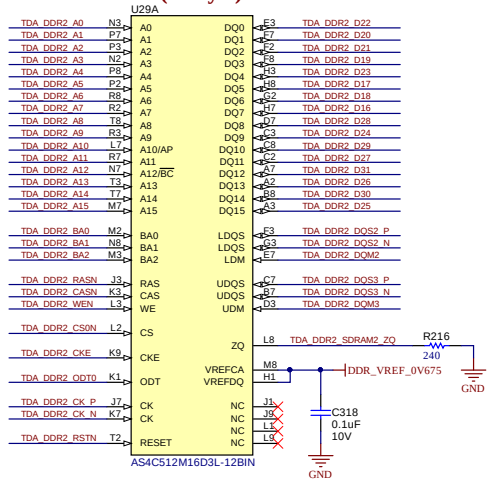
Follow all layout guidelines as presented in these documents.

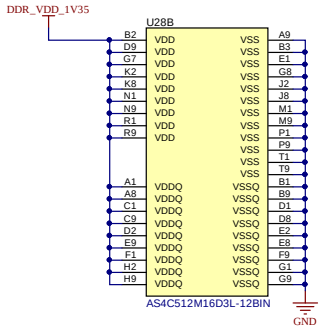


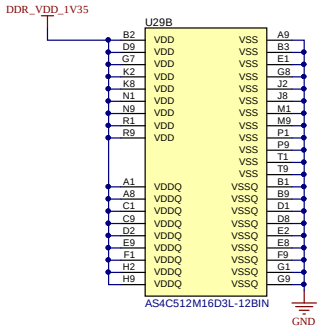
SDRAM1, 64 Meg x 16 x 8 banks 8Gbit (1Gbyte)



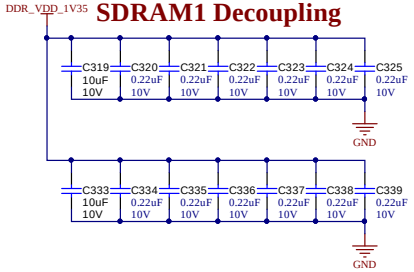
SDRAM2, 64 Meg x 16 x 8 banks 8Gbit (1Gbyte)



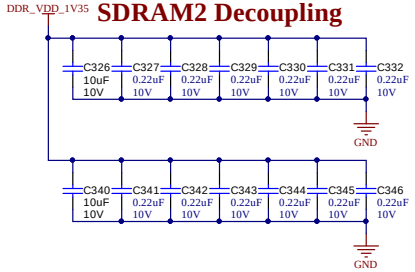




SDRAM1 Decoupling



SDRAM2 Decoupling



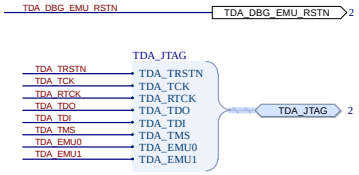
Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/18/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:39 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_DDR3_EMIF2_DDR3_SDRAM.SchDoc	
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	Rev:B

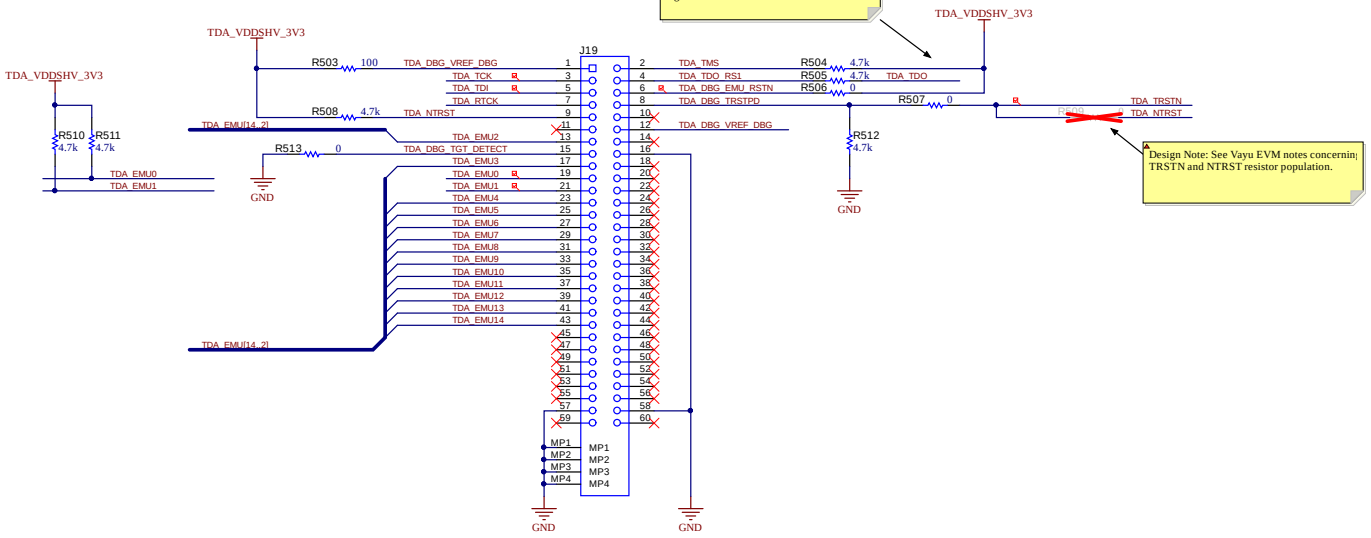
TDA2 - JTAG and EMU Debug Header

References

Emulation and Trace Headers TRM

Follow all layout guidelines as presented in these documents.





Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:40 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_JTAG_EMU_Connector.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

TDA2 - RGMII 1Gigabit Ethernet PHY and RJ45 Magnetics

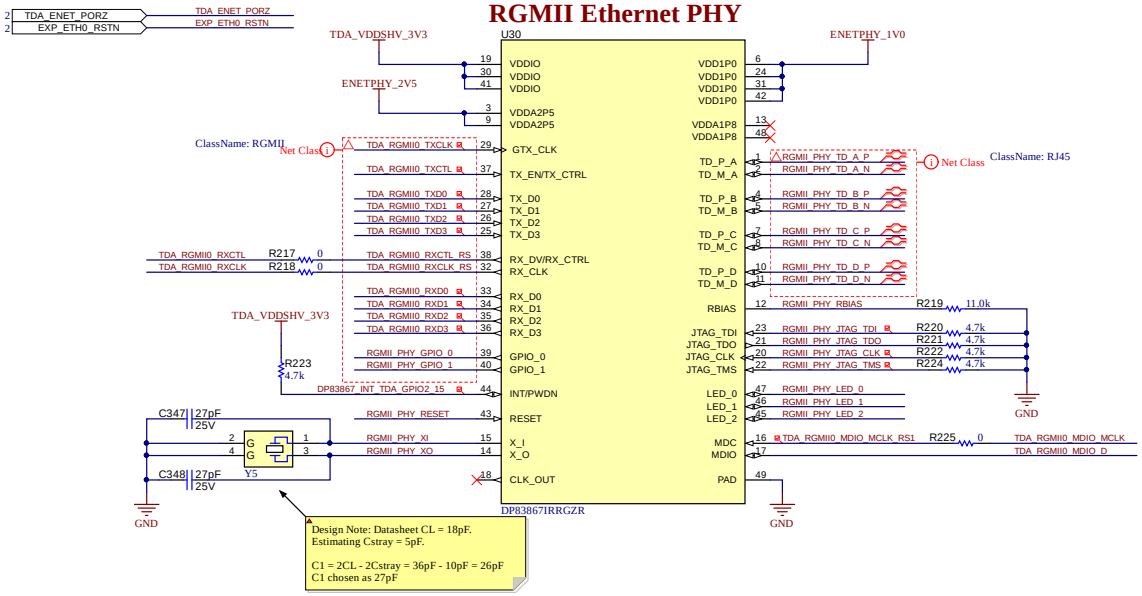
References

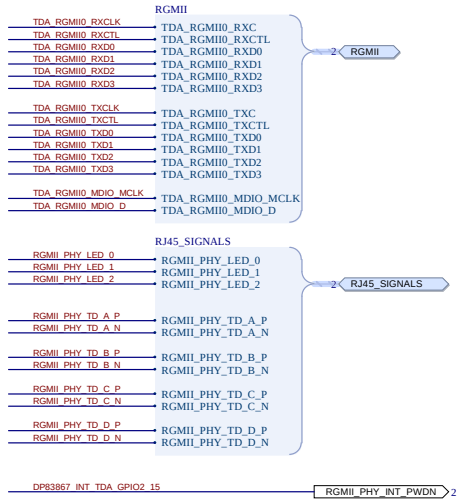
TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

TI Ethernet Physical Layer Controller 10/100/1000 Base-TX PHY Serial Interface 64-HTQFP (10x10)

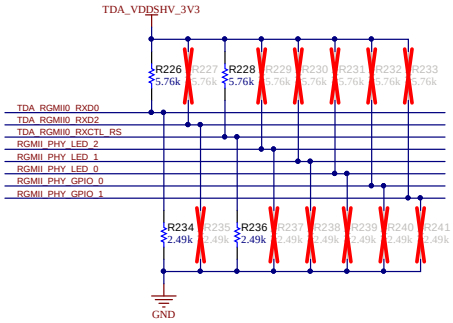
Follow all layout guidelines as presented in these documents.

RGMII Ethernet PHY



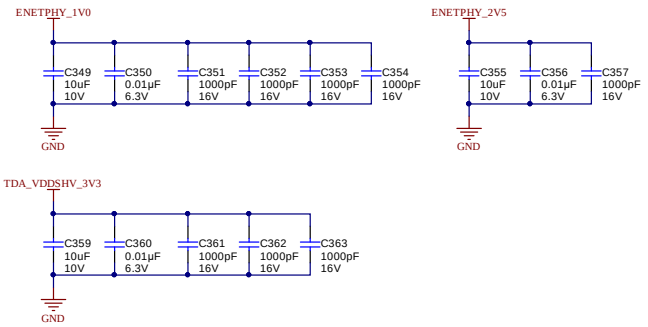


Ethernet PHY Bootstrap Pull-up/down

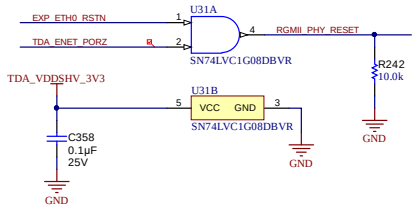


Design Note: See PHY datasheet Chapte 8.5 "Programming" for details on the 4-level mode boot-strap operation.

Ethernet PHY Decoupling



RGMII Ethernet PHY Reset



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:41 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Ethernet_PHY.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

TDA2 - RGMII 1Gigabit Ethernet RJ45 Magnetics

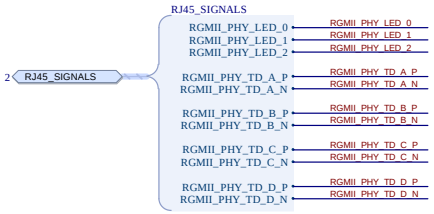
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

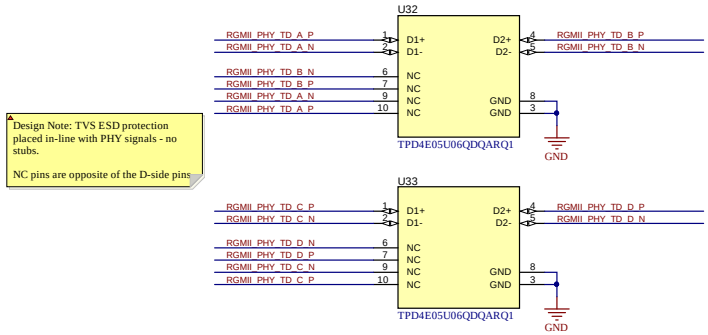
TI Ethernet Physical Layer Controller 10/100/1000 Base-TX PHY Serial Interface 64-HTQFP (10x10)
TPDxE05U06-Q1 1 and 4 Channel ESD Protection Diodes for SuperSpeed (Up to 6 Gbps) Interface

Follow all layout guidelines as presented in these documents.

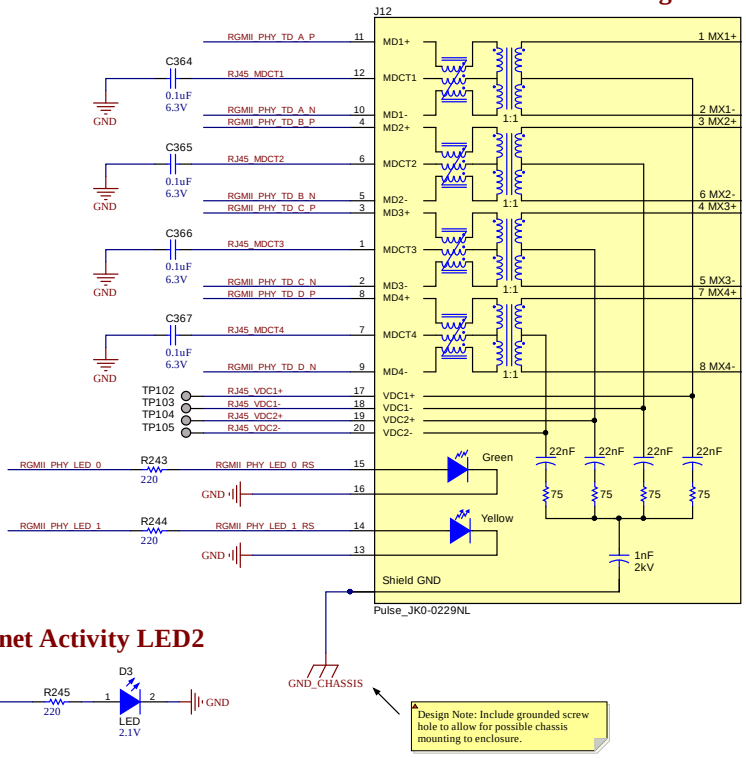
RGMII Ethernet PHY



Ethernet TVS ESD Protection



Ethernet RJ45 and Magnetics



Ethernet Activity LED2

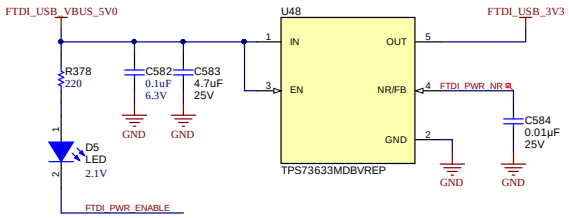
Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:42 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_Ethernet_RJ45.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

References

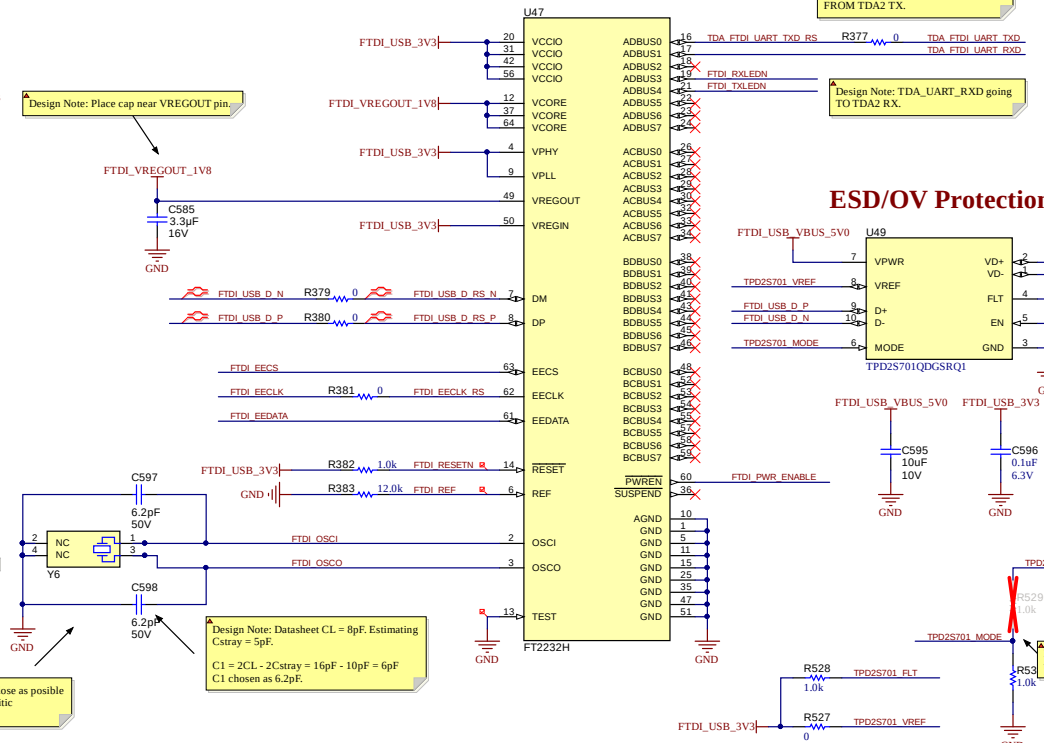
FTDI FT2232H Dual High-Speed USB to UART

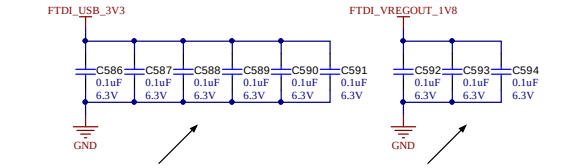
Follow all layout guidelines as presented in these documents.

5.0V to 3.3V Fixed LDO Regulator

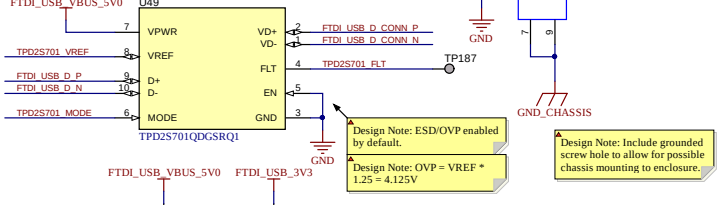


FTDI2232 UART to USB Bridge

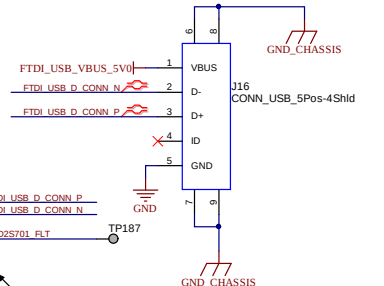




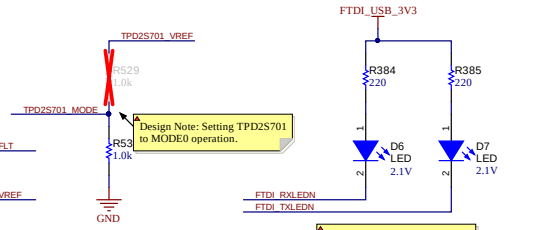
ESD/OV Protection



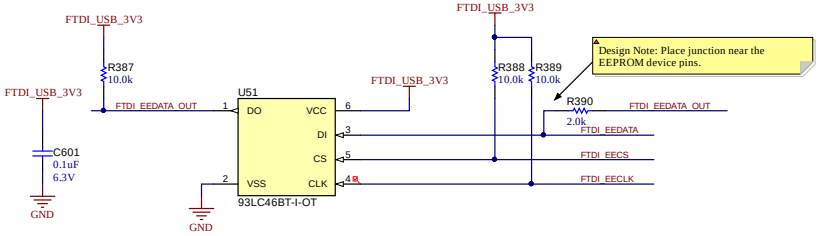
USB2.0 Mini-B Connector



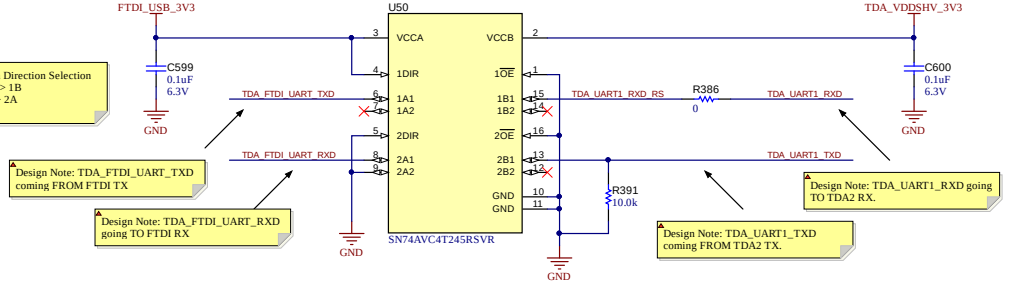
TX/RX Activity LEDs



FTDI 1Kb Configuration EEPROM



FTDI 3.3V to TDA2 3.3V Bus Isolation



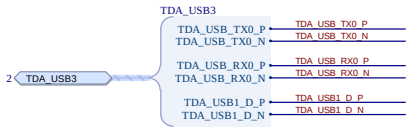
Orderable: MMWCAS-DSP-EVM	Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A	Project Title: Cascade Radar Host Processor Board	
Number: PROC055 Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control	Assembly Variant:001	Sheet:43 of 66
Drawn By:Alec Schott	File: PROC055B_TDA2_UART_USB_Bridge.SchDoc	Size: B
Engineer: Alec Schott	Contact: http://www.ti.com/mmwave	

TDA2 - USB3.0 Host Connector

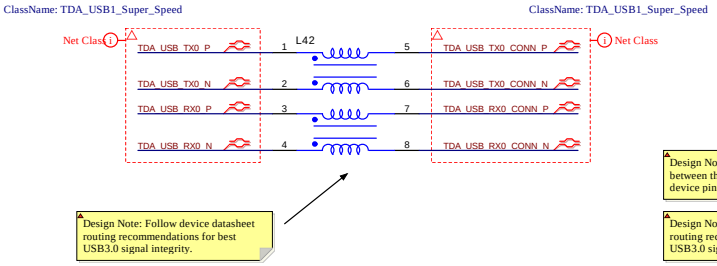
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

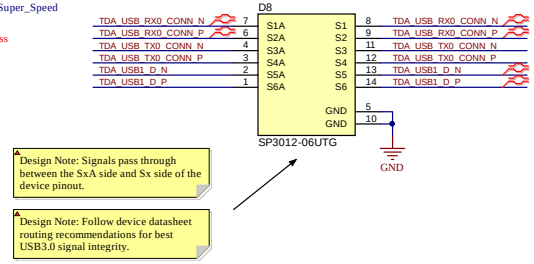
Follow all layout guidelines as presented in these documents.



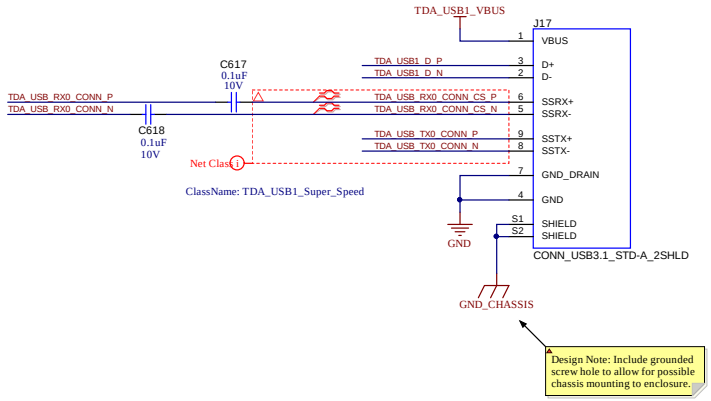
USB3.0 EMI Suppression



USB ESD Protection



USB3.0 Type-A Host Connector



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TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:44 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_USB3_Connector.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

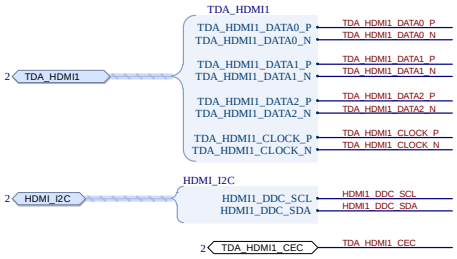
Texas Instruments
http://www.ti.com

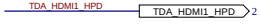
TDA2 - HDMI Connector

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

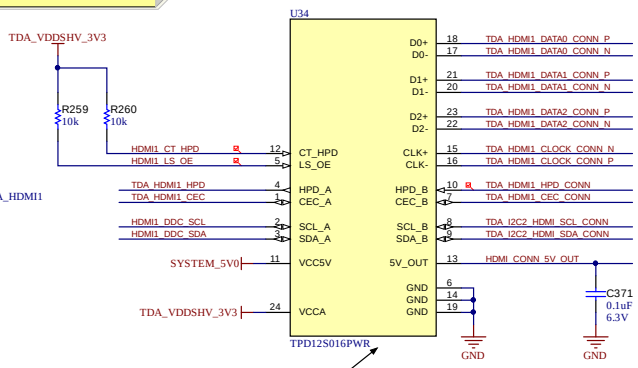
Follow all layout guidelines as presented in these documents.



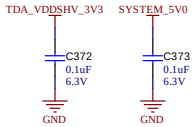


HDMI Control and ESD Protection

Design Note: TPDI2S01 integrates I2C pull-ups on both the 3.3V and 5.0V side.

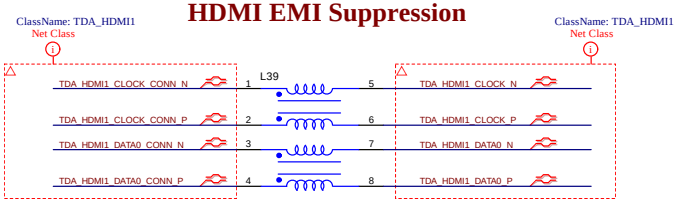


Design Note: Follow device datasheet routing recommendations for best HDMI signal integrity.



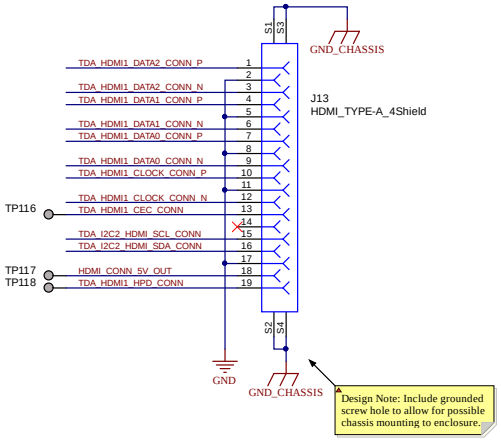
Design Note: Decoupling for the TPD12S016. Place near the device power pins.

HDMI EMI Suppression



Design Note: Follow device datasheet routing recommendations for best HDMI signal integrity.

HDMI Host Connector



Design Note: Include grounded screw hole to allow for possible chassis mounting to enclosure.

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:45 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_HDMI_Connector.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

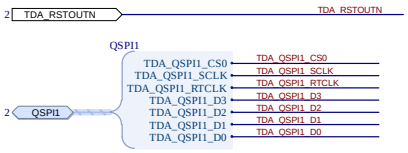
Texas Instruments
http://www.ti.com

References

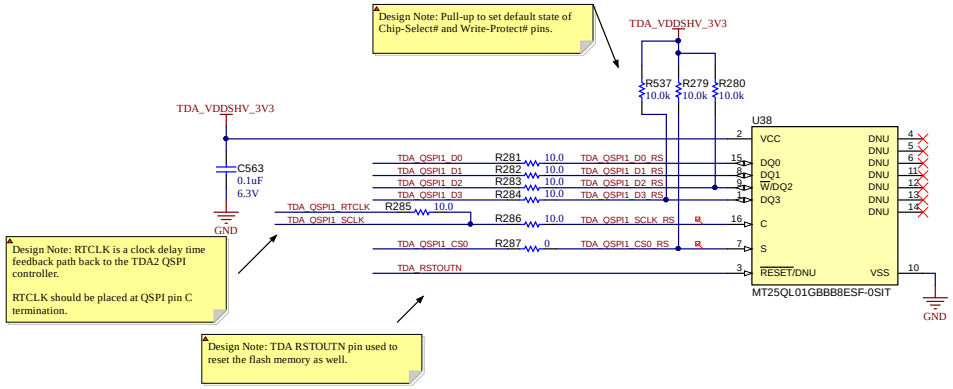
Micron Serial NOR Flash Memory MT25QL01GBBB (16-pin SOP2)

TDA2 QSPI Flash Memory

Follow all layout guidelines as presented in these documents.



1Gb (128M x 8) QSPI NOR Flash Memory



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TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:46 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_QSPI_Flash.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

TDA2 - m.2 PCIE/SATA Connector & EEPROM

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

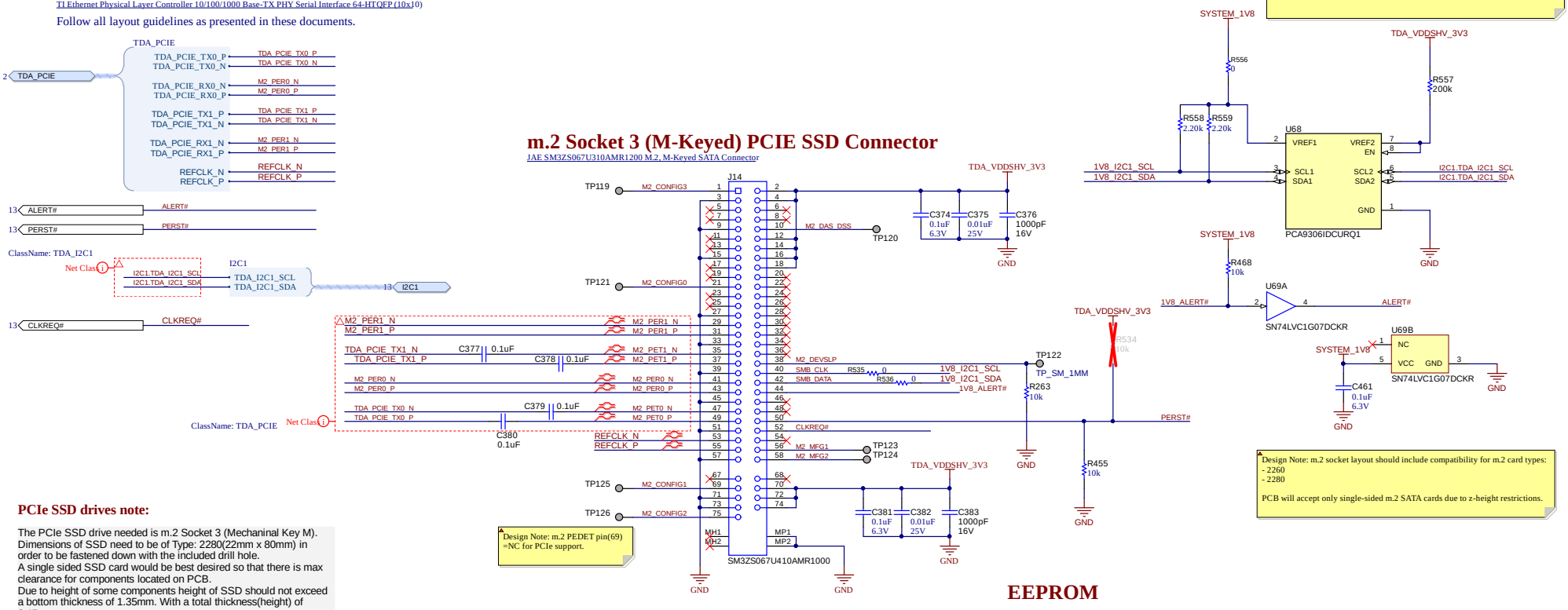
TI Ethernet Physical Layer Controller 10/100/1000 Base-TX PHY Serial Interface 64-HTQFP (10x10)

Follow all layout guidelines as presented in these documents.

Voltage translator needed for 1v8 I2C to 3V3 I2C transmission.
SCL1/SDA1 - Low voltage side
SCL2/SDA2 - High Voltage side

m.2 Socket 3 (M-Keyed) PCIE SSD Connector

JAE SM3ZS067U310AMR1200 M.2, M-Keyed SATA Connector

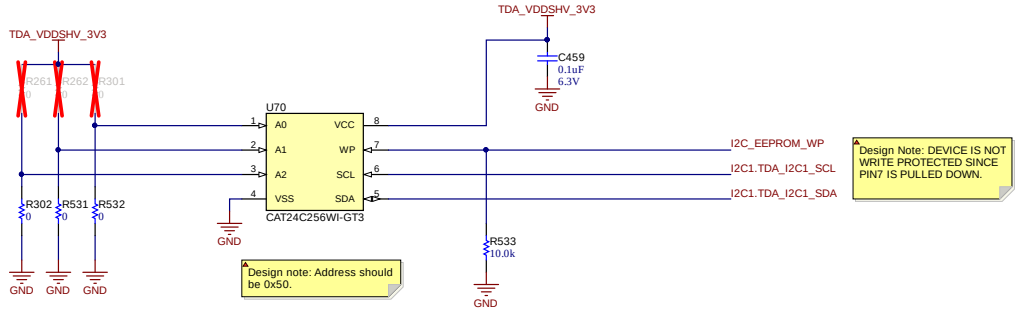


PCIe SSD drives note:

The PCIe SSD drive needed is m.2 Socket 3 (Mechaninal Key M). Dimensions of SSD need to be of Type: 2280(22mm x 80mm) in order to be fastened down with the included drill hole.
A single sided SSD card would be best desired so that there is max clearance for components located on PCB.
Due to height of some components height of SSD should not exceed a bottom thickness of 1.35mm. With a total thickness(height) of 2.45mm.

Reccommended device:
Name: NVMe SSD 960 Pro M.2 512GB
-P/N: MZVKP512HMHQ

EEPROM



Orderable: MMWCAS-DSP-EVM	Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A	Project Title: Cascade Radar Host Processor Board	
Number: PROC055 Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control	Assembly Variant:001	Sheet:47 of 66
Drawn By:Alec Schott	File: PROC055B_TDA2_m2_SATA_Connector.SchDoc	Size: B
Engineer: Alec Schott	Contact: http://www.ti.com/mmwave	

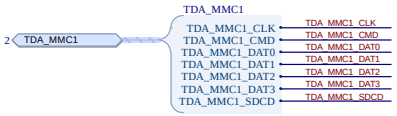
Texas Instruments
http://www.ti.com

TDA2 - MMC1, SPI2 and SPI4 and SDCard Connector

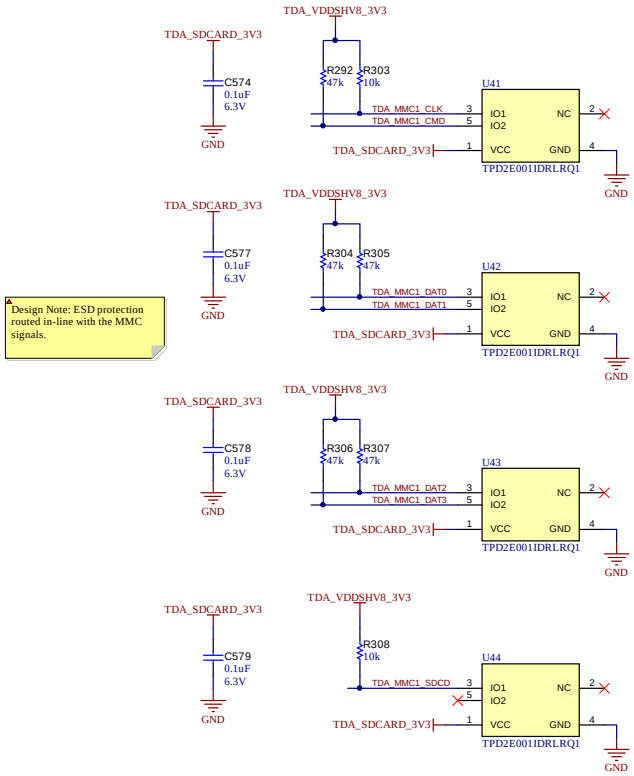
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

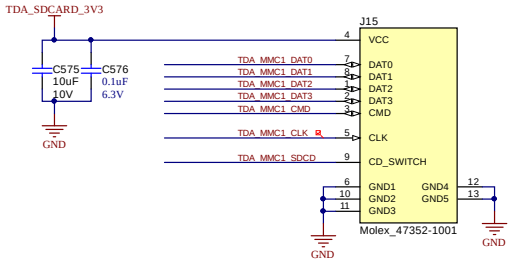


MicroSD ESD Protection



Design Note: ESD protection routed in-line with the MMC signals.

MicroSD Card Connector



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:48 of 66
Drawn By:Alec Schott		File: PROC055B_TDA2_SDcard_Connector.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

References
Lattice FPGA Embedded Vision Development Kit

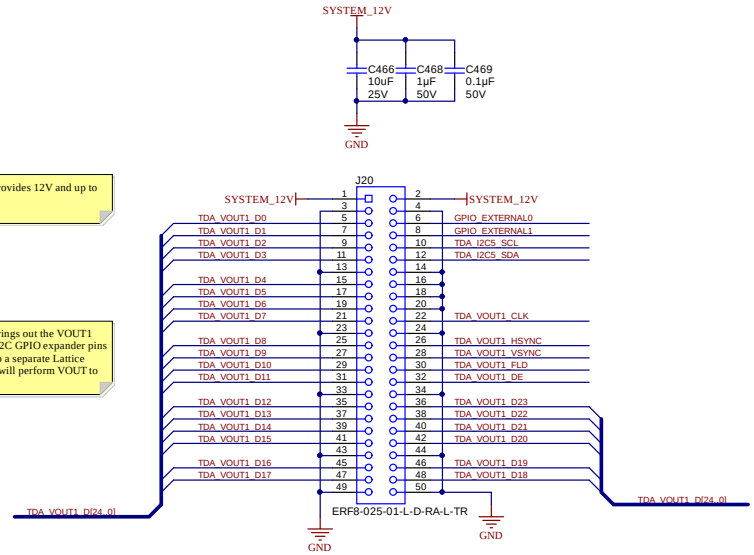
TDA2 - VOUT1 Lattice ECP5 FPGA Prototyping Connector

Follow all layout guidelines as presented in these documents.

2 GPIO_EXTERNAL0 — GPIO_EXTERNAL0
2 GPIO_EXTERNAL1 — GPIO_EXTERNAL1

TDA_VOUT1
TDA_VOUT1_D[23..0] — TDA_VOUT1_D[23..0]
TDA_VOUT1_CLK — TDA_VOUT1_CLK
TDA_VOUT1_DE — TDA_VOUT1_DE
TDA_VOUT1_FLD — TDA_VOUT1_FLD
TDA_VOUT1_VSYNC — TDA_VOUT1_VSYNC
TDA_VOUT1_HSYNC — TDA_VOUT1_HSYNC
2 TDA_VOUT1

I2C5
TDA_I2C5_SCL — TDA_I2C5_SCL
TDA_I2C5_SDA — TDA_I2C5_SDA
2 I2C5



Orderable: MMWCAS-DSP-EVM		Designed for: Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 49 of 66
Drawn By: Alec Schott		File: PROC055B_TDA2_VOUT1_Connector.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

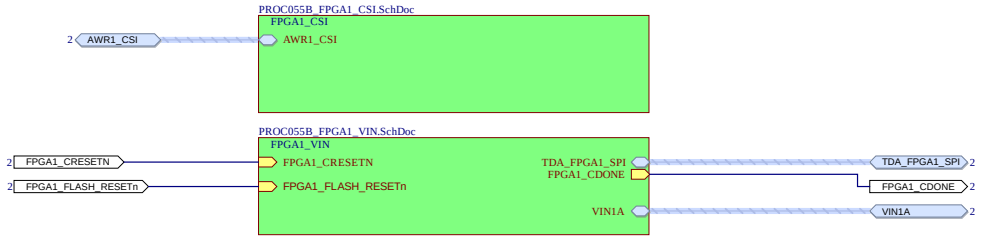
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #1



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 3/29/2021
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:50 of 66
Drawn By:Alec Schott		File: PROC055B_FPGA1_Top.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

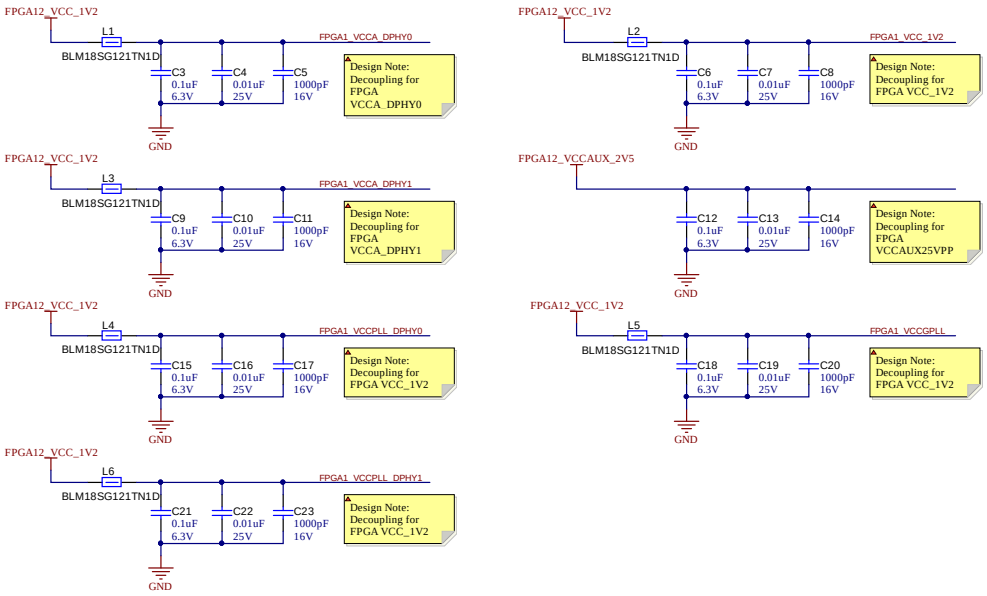
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

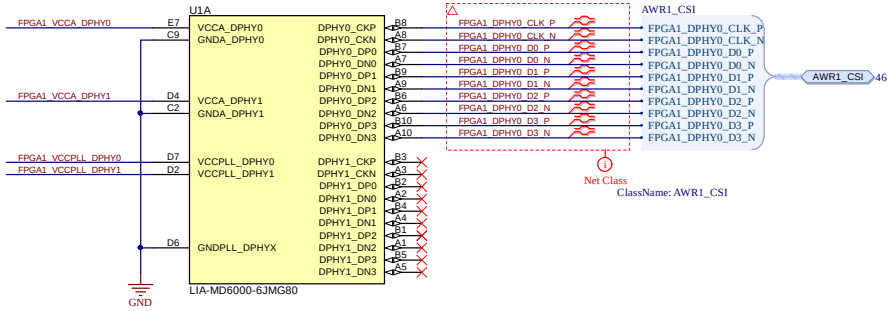
Follow all layout guidelines as presented in these documents.

Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #1 CSI2.0 Interface, FPGA1/4 Power Supplies

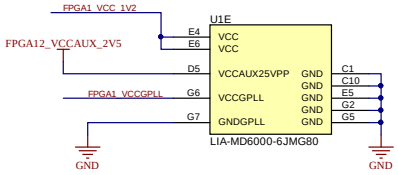
FPGA VCC, VCCAUX 2.5V and VCCGPLL Decoupling



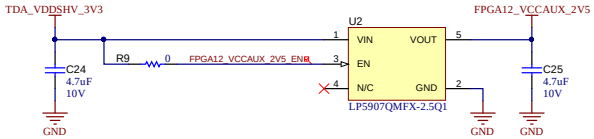
FPGA VCCA_PHY[1:0], VCCPLL_DPHY[1:0] and DPHY[1:0]



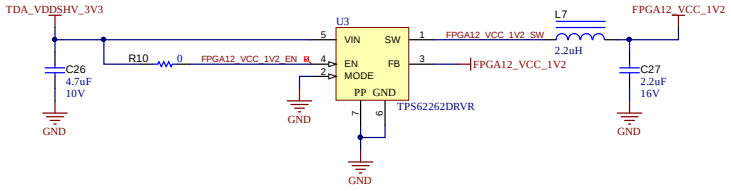
FPGA VCC, VCCAUX 2.5V and VCCGPLL



FPGA1/4 VCCAUX 2.5V Supply



FPGA1/4 VCC 1.2V Supply



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
BOM Rev: Not in version control		Assembly Variant:001	Sheet:51 of 66
Drawn By:Alec Schott		File: PROC055B_FPGA1_CSI.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #1
FPGA VIN, SPI and Configuration Interface

References
Lattice HW-USBN-2B Programming Cable
Lattice HW-USBN-2B Programming Cable User Guide
Lattice CrossFire FPGA Configuration Guide

Follow all layout guidelines as presented in these documents.

46 FPGA1_CRESETN — FPGA1_CRESETN
46 FPGA1_FLASH_RESETn — FPGA1_FLASH_RESETn

FPGA1_CDONE — FPGA1_CDONE 46

TDA_FPGA1_SPI
FPGA1_SPI_CSN — FPGA1_SPI_CSN
FPGA1_SPI_SCLK — FPGA1_SPI_SCLK
FPGA1_SPI_MISO — FPGA1_SPI_MISO
FPGA1_SPI_MOSI — FPGA1_SPI_MOSI
→ TDA_FPGA1_SPI 46

VIN1A
TDA_VIN1A_D[23..0] — TDA_VIN1A_D[23..0]
TDA_VIN1A_CLK0 — TDA_VIN1A_CLK0
TDA_VIN1A_FLD0 — TDA_VIN1A_FLD0
TDA_VIN1A_DE0 — TDA_VIN1A_DE0
TDA_VIN1A_VSYNC0 — TDA_VIN1A_VSYNC0
→ VIN1A 46

FPGA SPI/Config Interface

Design Note: Decoupling for FPGA VCCIO0

TDA_VDDSHV_3V3 — C28 0.1uF 6.3V — C29 0.01uF 25V — C30 1000pF 16V — GND

U11B
PB52/SPI_SS/CSN/SCL — H1 — FPGA1_FLASH_SPI_CSN
PB53/SPI_SCK/MCK/SDA — J1 — FPGA1_SPI_SCLK
PB50/MOSI — S1 — FPGA1_SPI_MOSI
PB51/MISO — K1 — FPGA1_SPI_MISO_RS
PB48/PCLKT0_1/USER_SCL — D1 — FPGA1_SPI_CSN
PB47/PCLKT0_0/USER_SDA — E2
PB49/PMU_WKUPN/CDONE — J2 — FPGA1_CDONE
CRESET_B — H2 — FPGA1_CRESETN
VCCIO0 — F4
LIA-MD6000-6JMG80

TDA_VDDSHV_3V3 — R11 10k — R12 10k
R13 0 (FPGA1_SPI_MISO_RS — FPGA1_SPI_MISO)
TDA_VDDSHV_3V3 — R14 10k
R15 10k — GND

Design Note: FPGA SPI interface run in SLAVE mode or MASTER mode. Pin-names indicate MASTER mode operation.

MISO and MOSI functionality swapped in SLAVE mode, allowing for SPI programming from Lattice HW-USBN-2B Programming Cable or TDA2 host processor.

Design Note: After internal POR circuit indicates good power a CRESETN low to high transition will start NVCM boot sequence.

TDA2/Programmer SPI CS Jumper

SH-J1 Shunt
FPGA1_SPI_CSN
FPGA1_FLASH_SPI_CSN
J2 Header_2x1
R543 0

FPGA and NOR Flash Programming Header

TDA_VDDSHV_3V3 — R19 0
J3 Header_5x2
1 FPGA1_VCCIO — 2
3 FPGA1_SPI_CSN — 4 FPGA1_SPI_MISO
5 FPGA1_FLASH_SPI_CSN — 6 FPGA1_CRESETN
7 FPGA1_SPI_SCLK — 8 FPGA1_CDONE
9 FPGA1_SPI_MOSI — 10
GND

Design Note: See notes from Lattice and TI programming reference documents fc HW-USBN-2B USB Programming Cable Flying-Lead Connections

TDA_VDDSHV_3V3 — C34 0.1uF 6.3V — GND

FPGA NOR Flash

TDA_VDDSHV_3V3 — R17 10k — R16 10k
ClassName: TDA_SPI_FPGA1
Net Class
FPGA1_SPI_MOSI — R18 0 — FPGA1_SPI_MISO_RS
FPGA1_FLASH_WPN
FPGA1_FLASH_RESETn

U4
VCC — 8 — SCLK — 6 — FPGA1_SPI_SCLK
SI/SIO0 — 5
SO/SIO1 — 2
WP/SIO2 — 3
RESET/SIO3 — 7
CS — 1 — FPGA1_FLASH_SPI_CSN
GND — 4
MX25L12835FM2I-10G
GND

Design Note: Running QSPI capable NOR flash in x1 SPI (XIO-SPI) mode.

FPGA VIN Interface

Design Note: Decoupling for FPGA VCCIO1

TDA_VDDSHV_3V3 — C31 0.1uF 6.3V — C32 0.01uF 25V — C33 1000pF 16V — GND

U11C
PB34A/GR_PCLK1_0 — E1 — TDA_VIN1A_VSYNC0
PB34B — E2 — TDA_VIN1A_DE0
PB38A — F1 — FPGA1_PB38A — TP6
PB38B — F2 — TDA_VIN1A_FLD0
PB38C — K4 — TDA_VIN1A_D0
PB38D — J4 — TDA_VIN1A_D1
PB29A/PCLKT1_0 — J7 — TDA_VIN1A_D2
PB29B/PCLKC1_0 — K7 — TDA_VIN1A_D3
PB29C/PCLKT1_1 — K6 — TDA_VIN1A_CLK0
PB29D/PCLKC1_1 — J6
PB34C/MIPI_CLKT1_0 — K5 — TDA_VIN1A_D4
PB34D/MIPI_CLKC1_0 — J5 — TDA_VIN1A_D5
PB43C — K3 — TDA_VIN1A_D6
PB43D — J3 — TDA_VIN1A_D7
VCCIO1 — F5
VCCIO1 — G4
LIA-MD6000-6JMG80
TDA_VDDSHV_3V3

TDA_VIN1A_D[23..0]

FPGA VIN Interface

Design Note: Decoupling for FPGA VCCIO2

TDA_VDDSHV_3V3 — C35 0.1uF 6.3V — C36 0.01uF 25V — C37 1000pF 16V — GND

U11D
PB16A/PCLKT2_0 — D9 — TDA_VIN1A_D8
PB16B/PCLKC2_0 — D10 — TDA_VIN1A_D9
PB12A/GPLLT2_0 — E9 — TDA_VIN1A_D10
PB12B/GPLLC2_0 — E10 — TDA_VIN1A_D11
PB6A/GR_PCLK2_0 — F9 — TDA_VIN1A_D12
PB6B — F10 — TDA_VIN1A_D13
PB2A — G9 — TDA_VIN1A_D14
PB2B — G10 — TDA_VIN1A_D15
PB6C — J10 — TDA_VIN1A_D16
PB6D — J9 — TDA_VIN1A_D17
PB2C/MIPI_CLKT2_0 — H10 — TDA_VIN1A_D18
PB2D/MIPI_CLKC2_0 — H9 — TDA_VIN1A_D19
PB16C/PCLKT2_1 — K8 — TDA_VIN1A_D20
PB16D/PCLKC2_1 — J8 — TDA_VIN1A_D21
PB12C — K10 — TDA_VIN1A_D22
PB12D — K9 — TDA_VIN1A_D23
VCCIO2 — F6
VCCIO2 — F7
LIA-MD6000-6JMG80
TDA_VDDSHV_3V3

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:52 of 66
Drawn By:Alec Schott		File: PROC055B_FPGA1_VIN.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

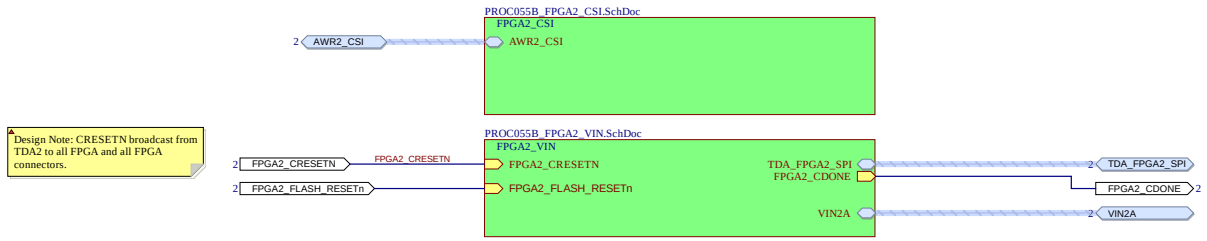
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #2



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 3/29/2021
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:53 of 66
Drawn By:Alec Schott		File: PROC055B_FPGA2_Top.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

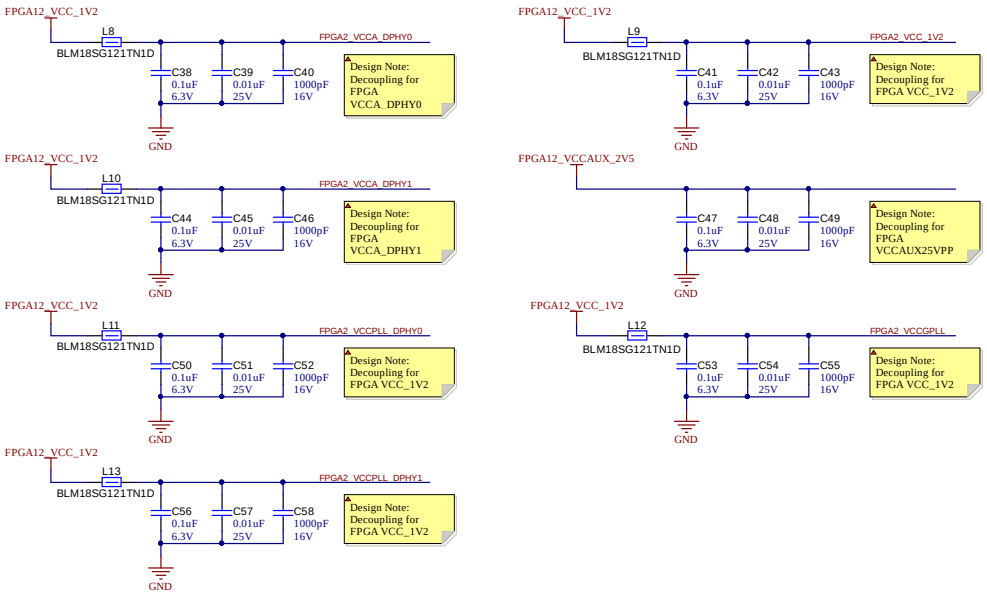
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

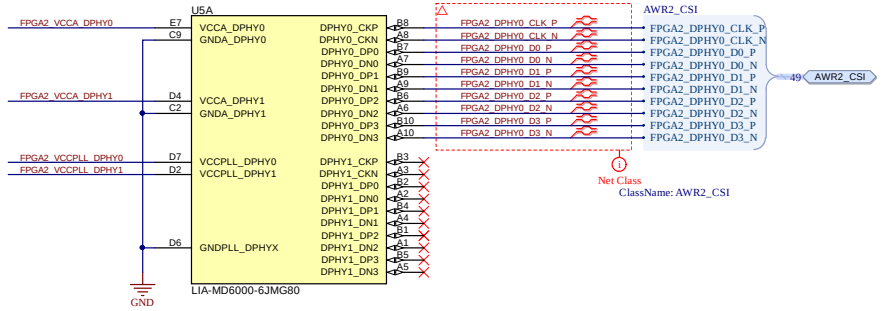
Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #2 CSI2.0 Interface, FPGA1/4 Power Supplies

Follow all layout guidelines as presented in these documents.

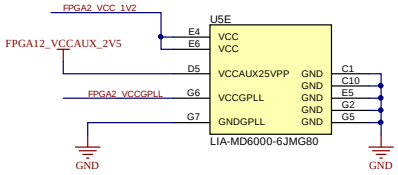
FPGA VCC, VCCAUX 2.5V and VCCGPLL Decoupling



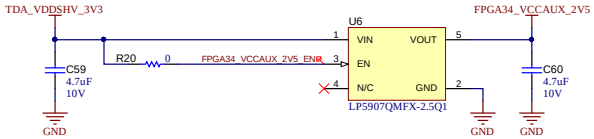
FPGA VCCA_PHY[1:0], VCCPLL_DPHY[1:0] and DPHY[1:0]



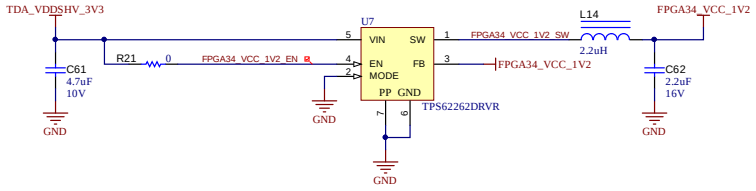
FPGA VCC, VCCAUX 2.5V and VCCGPLL



FPGA2/3 VCCAUX 2.5V Supply



FPGA2/3 VCC 1.2V Supply



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
BOM Rev: Not in version control		Assembly Variant:001	Sheet:54 of 66
Drawn By:		File: PROC055B_FPGA2_CSI.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #2
FPGA VIN, SPI and Configuration Interface

References
Lattice HW-USBN-2B Programming Cable
Lattice HW-USBN-2B Programming Cable User Guide
Lattice CrossFire FPGA Configuration Guide

Follow all layout guidelines as presented in these documents.

49 FPGA2_CRESETN — FPGA2_CRESETN
46 FPGA2_FLASH_RESETn — FPGA2_FLASH_RESETn

FPGA2_CDONE — FPGA2_CDONE 49

ClassName: TDA_SPI_FPGA2
Net Class 1
FPGA2_SPI_CSN, FPGA2_SPI_SCLK, FPGA2_SPI_MISO, FPGA2_SPI_MOSI
TDA_FPGA2_SPI
FPGA2_SPI_CSN, FPGA2_SPI_SCLK, FPGA2_SPI_MISO, FPGA2_SPI_MOSI
49 TDA_FPGA2_SPI

ClassName: VIN2A
Net Class 1
TDA_VIN2A_D[23..0], TDA_VIN2A_CLK0, TDA_VIN2A_FLD0, TDA_VIN2A_DE0, TDA_VIN2A_VSYNC0
VIN2A
TDA_VIN2A_D[23..0], TDA_VIN2A_CLK0, TDA_VIN2A_FLD0, TDA_VIN2A_DE0, TDA_VIN2A_VSYNC0
49 VIN2A

FPGA SPI/Config Interface

Design Note: Decoupling for FPGA VCCIO0
TDA_VDDSHV_3V3
C63 0.1uF 6.3V, C64 0.01uF 25V, C65 1000pF 16V
GND

U1B
LIA-MD6000-6JMG80
PB52/SPI_SS/CSN/SCL — H1 — FPGA2_FLASH_SPI_CSN
PB53/SPI_SCK/MCK/SDA — J1 — FPGA2_SPI_SCLK
PB50/MOSI — G1 — FPGA2_SPI_MOSI
PB51/MISO — K1 — FPGA2_SPI_MISO_RS — R24 0 — FPGA2_SPI_MISO
PB48/PCLKT0_1/USER_SCL — D1 — FPGA2_SPI_CSN
PB47/PCLKT0_0/USER_SDA — D2
PB49/PMU_WKUPN/CDONE — J2 — FPGA2_CDONE
CRESET_B — H2 — FPGA2_CRESETN
VCCIO0 — F4 — TDA_VDDSHV_3V3

TDA_VDDSHV_3V3
R22 10k, R23 10k
R25 10k
R26 10k
GND

Design Note: FPGA SPI interface run in SLAVE mode or MASTER mode. Pin-names indicate MASTER mode operation.

MISO and MOSI functionality swapped in SLAVE mode, allowing for SPI programming from Lattice HW-USBN-2B Programming Cable or TDA2 host processor.

Design Note: After internal POR circuit indicates good power a CRESETN low to high transition will start NVCM boot sequence.

Design Note: After internal POR circuit indicates good power a CRESETN low to high transition will start NVCM boot sequence.

FPGA VIN Interface

Design Note: Decoupling for FPGA VCCIO1
TDA_VDDSHV_3V3
C66 0.1uF 6.3V, C67 0.01uF 25V, C68 1000pF 16V
GND

U1C
LIA-MD6000-6JMG80
PB34A/GR_PCLK1_0 — E1 — TDA_VIN2A_VSYNC0
PB34B — E2 — TDA_VIN2A_DE0
PB38A — F1 — FPGA2_PB38A — TP7
PB38B — F2 — TDA_VIN2A_FLD0
PB38C — K4 — TDA_VIN2A_D0
PB38D — J4 — TDA_VIN2A_D1
PB29A/PCLKT1_0 — J7 — TDA_VIN2A_D2
PB29B/PCLKC1_0 — K7 — TDA_VIN2A_D3
PB29C/PCLKT1_1 — K6 — TDA_VIN2A_CLK0
PB29D/PCLKC1_1 — J6
PB34C/MIPI_CLKT1_0 — K5 — TDA_VIN2A_D4
PB34D/MIPI_CLKC1_0 — J5 — TDA_VIN2A_D5
PB43C — K3 — TDA_VIN2A_D6
PB43D — J3 — TDA_VIN2A_D7
VCCIO1 — F5, G4 — TDA_VDDSHV_3V3
TDA_VIN2A_D[23..0]

TDA2/Programmer SPI CS Jumper

SH-J2 Shunt
FPGA2_SPI_CSN
FPGA2_FLASH_SPI_CSN
J4 Header_2x1
R544 0

FPGA NOR Flash

TDA_VDDSHV_3V3
R28 10k, R27 10k
ClassName: TDA_SPI_FPGA2
Net Class 1
FPGA2_SPI_MOSI, FPGA2_SPI_MISO, R29 0 FPGA2_SPI_MISO_RS, FPGA2_FLASH_WPN, FPGA2_FLASH_RESETn

U8
MX25L12835FM2I-10G
VCC — 8 — TDA_VDDSHV_3V3
SCLK — 6 — FPGA2_SPI_SCLK
SI/SIO0 — 5
SO/SIO1 — 2
WP/SIO2 — 3
RESET/SIO3 — 7
CS — 1 — FPGA2_FLASH_SPI_CSN
GND — 4 — GND

Design Note: Running QSPI capable NOR flash in x1 SPI (XIO-SPI) mode.

Design Note: Flash WP and HOLD disabled

FPGA and NOR Flash Programming Header

TDA_VDDSHV_3V3
R30 0 — FPGA2_VCCIO
J5 Header_5x2
FPGA2_SPI_CSN 3, FPGA2_FLASH_SPI_CSN 5, FPGA2_SPI_SCLK 7, FPGA2_SPI_MOSI 9
FPGA2_SPI_MISO 4, FPGA2_CRESETN 6, FPGA2_CDONE 8
GND

TDA_VDDSHV_3V3
C69 0.1uF 6.3V
GND

FPGA VIN Interface

Design Note: Decoupling for FPGA VCCIO2
TDA_VDDSHV_3V3
C70 0.1uF 6.3V, C71 0.01uF 25V, C72 1000pF 16V
GND

U1D
LIA-MD6000-6JMG80
PB16A/PCLKT2_0 — D9 — TDA_VIN2A_D8
PB16B/PCLKC2_0 — D10 — TDA_VIN2A_D9
PB12A/GPLLT2_0 — E9 — TDA_VIN2A_D10
PB12B/GPLLC2_0 — E10 — TDA_VIN2A_D11
PB6A/GR_PCLK2_0 — F9 — TDA_VIN2A_D12
PB6B — F10 — TDA_VIN2A_D13
PB2A — G9 — TDA_VIN2A_D14
PB2B — G10 — TDA_VIN2A_D15
PB6C — J10 — TDA_VIN2A_D16
PB6D — J9 — TDA_VIN2A_D17
PB2C/MIPI_CLKT2_0 — H10 — TDA_VIN2A_D18
PB2D/MIPI_CLKC2_0 — H9 — TDA_VIN2A_D19
PB16C/PCLKT2_1 — K8 — TDA_VIN2A_D20
PB16D/PCLKC2_1 — J8 — TDA_VIN2A_D21
PB12C — K10 — TDA_VIN2A_D22
PB12D — K9 — TDA_VIN2A_D23
VCCIO2 — F6, F7 — TDA_VDDSHV_3V3

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:55 of 66
Drawn By:Alec Schott		File: PROC055B_FPGA2_VIN.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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http://www.ti.com

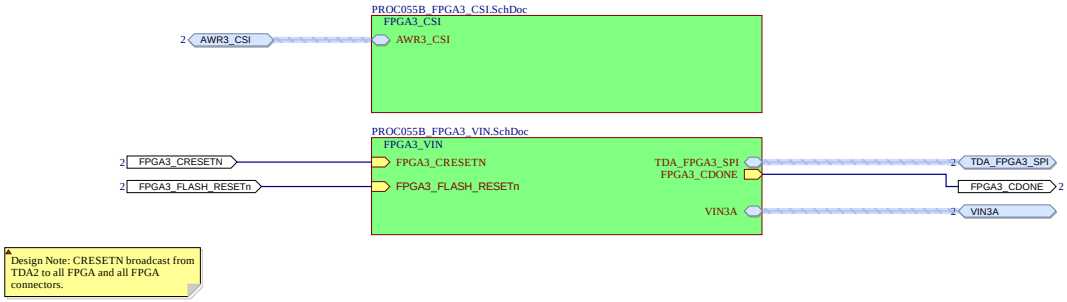
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #1



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 3/29/2021
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:56 of 66
Drawn By:Alec Schott		File: PROC055B_FPGA3_Top.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

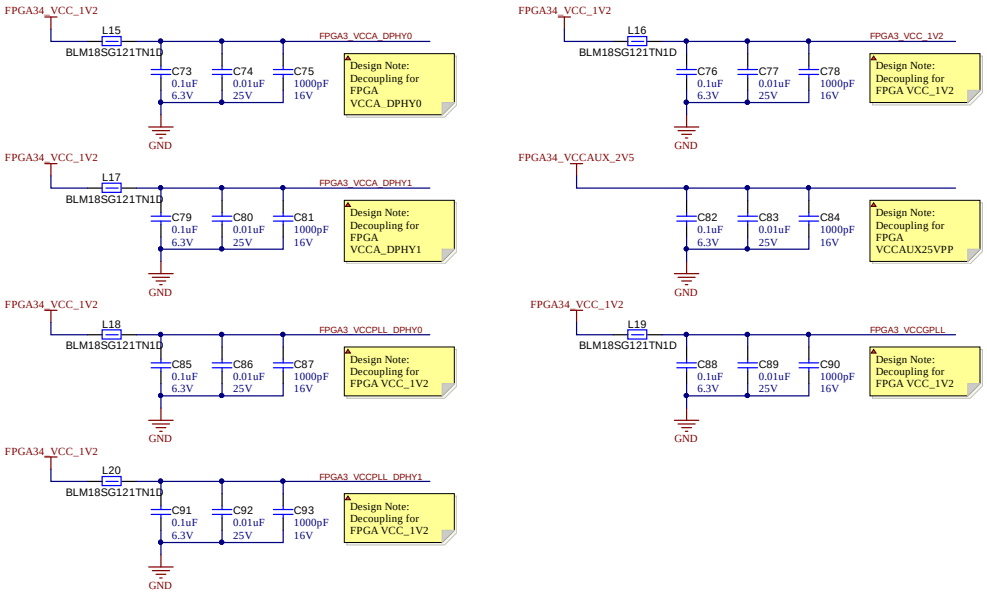
Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #1 CSI2.0 Interface, FPGA1/4 Power Supplies

References

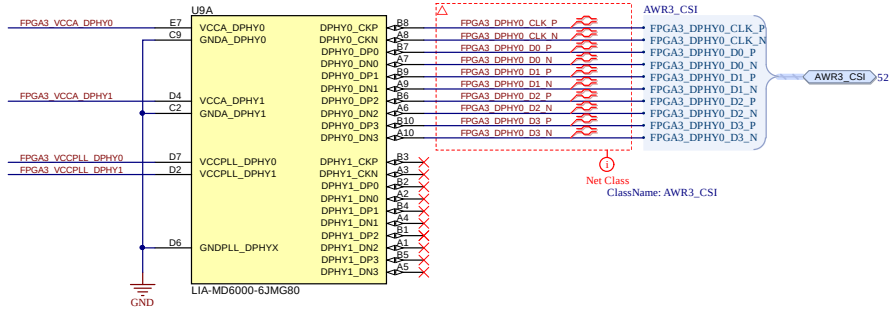
TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

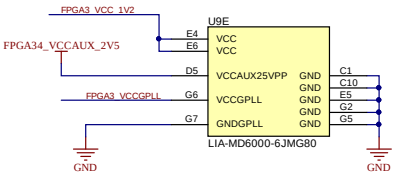
FPGA VCC, VCCAUX 2.5V and VCCGPLL Decoupling



FPGA VCCA_PHY[1:0], VCCPLL_DPHY[1:0] and DPHY[1:0]



FPGA VCC, VCCAUX 2.5V and VCCGPLL



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:57 of 66
Drawn By:Alec Schott		File: PROC055B_FPGA3_CSI.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #3
FPGA VIN, SPI and Configuration Interface

References
Lattice HW-USBN-2B Programming Cable
Lattice HW-USBN-2B Programming Cable User Guide
Lattice CrossFire FPGA Configuration Guide

Follow all layout guidelines as presented in these documents.

52 FPGA3_CRESETN — FPGA3_CRESETN
46 FPGA3_FLASH_RESETn — FPGA3_FLASH_RESETn

FPGA3_CDONE — FPGA3_CDONE 52

ClassName: TDA_SPI_FPGA3
Net Class 1
FPGA3_SPI_CSN, FPGA3_SPI_SCLK, FPGA3_SPI_MISO, FPGA3_SPI_MOSI
TDA_FPGA3_SPI: FPGA3_SPI_CSN, FPGA3_SPI_SCLK, FPGA3_SPI_MISO, FPGA3_SPI_MOSI — 52 TDA_FPGA3_SPI

ClassName: VIN3A
Net Class 1
TDA_VIN3A_D[23..0], TDA_VIN3A_CLK0, TDA_VIN3A_FLD0, TDA_VIN3A_DE0, TDA_VIN3A_VSYNC0
VIN3A: TDA_VIN3A_D[23..0], TDA_VIN3A_CLK0, TDA_VIN3A_FLD0, TDA_VIN3A_DE0, TDA_VIN3A_VSYNC0 — 52 VIN3A

FPGA SPI/Config Interface

Design Note: Decoupling for FPGA VCCIO0
TDA_VDDSHV_3V3
C94 0.1uF 6.3V
C95 0.01uF 25V
C96 1000pF 16V
GND

U5B
LIA-MD6000-6JMG80
PB52/SPI_SS/CSN/SCL — H1 — FPGA3_FLASH_SPI_CSN
PB53/SPI_SCK/MCK/SDA — J1 — FPGA3_SPI_SCLK
PB50/MOSI — G1 — FPGA3_SPI_MOSI
PB51/MISO — K1 — FPGA3_SPI_MISO_RS — R33 0 — FPGA3_SPI_MISO
PB48/PCLKT0_1/USER_SCL — D1 — FPGA3_SPI_CSN
PB47/PCLKT0_0/USER_SDA — D2
PB49/PMU_WKUPN/CDONE — J2 — FPGA3_CDONE
CRESET_B — H2 — FPGA3_CRESETN
VCCIO0 — F4 — TDA_VDDSHV_3V3

TDA_VDDSHV_3V3
R31 10k
R32 10k
R34 10k
R35 10k
GND

Design Note: FPGA SPI interface run in SLAVE mode or MASTER mode. Pin-names indicate MASTER mode operation.

MISO and MOSI functionality swapped in SLAVE mode, allowing for SPI programming from Lattice HW-USBN-2B Programming Cable or TDA2 host processor.

Design Note: After internal POR circuit indicates good power a CRESETN low to high transition will start NVCM boot sequence.

Design Note: After internal POR circuit indicates good power a CRESETN low to high transition will start NVCM boot sequence.

FPGA VIN Interface

Design Note: Decoupling for FPGA VCCIO1
TDA_VDDSHV_3V3
C97 0.1uF 6.3V
C98 0.01uF 25V
C99 1000pF 16V
GND

U5C
LIA-MD6000-6JMG80
PB34A/GR_PCLK1_0 — E1 — TDA_VIN3A_VSYNC0
PB34B — E2 — TDA_VIN3A_DE0
PB38A — F1 — FPGA3_PB38A — TP8
PB38B — F2 — TDA_VIN3A_FLD0
PB38C — K4 — TDA_VIN3A_D0
PB38D — J4 — TDA_VIN3A_D1
PB29A/PCLKT1_0 — J7 — TDA_VIN3A_D2
PB29B/PCLKC1_0 — K7 — TDA_VIN3A_D3
PB29C/PCLKT1_1 — K6 — TDA_VIN3A_CLK0
PB29D/PCLKC1_1 — J6
PB34C/MIPI_CLKT1_0 — K5 — TDA_VIN3A_D4
PB34D/MIPI_CLKC1_0 — J5 — TDA_VIN3A_D5
PB43C — K3 — TDA_VIN3A_D6
PB43D — J3 — TDA_VIN3A_D7
VCCIO1 — F5, G4 — TDA_VDDSHV_3V3

TDA_VIN3A_D[23..0]

TDA2/Programmer SPI CS Jumper

SH-J3 Shunt
FPGA3_SPI_CSN
FPGA3_FLASH_SPI_CSN
J6 Header_2x1
R545 0

FPGA NOR Flash

TDA_VDDSHV_3V3
R37 10k
R36 10k
ClassName: TDA_SPI_FPGA3
Net Class 1
FPGA3_SPI_MOSI
FPGA3_SPI_MISO
R38 0 FPGA3_SPI_MISO_RS
FPGA3_FLASH_WPN
FPGA3_FLASH_RESETn

U10
MX25L12835FM2I-10G
VCC — 8
SI/SIO0 — 5
SO/SIO1 — 2
WP/SIO2 — 3
RESET/SIO3 — 7
SCLK — 6 — FPGA3_SPI_SCLK
CS — 1 — FPGA3_FLASH_SPI_CSN
GND — 4
GND

Design Note: Running QSPI capable NOR flash in x1 SPI (XIO-SPI) mode.

Design Note: Flash WP and HOLD disabled

FPGA and NOR Flash Programming Header

TDA_VDDSHV_3V3
R39 0
C100 0.1uF 6.3V
GND

J7 Header_5x2
1 FPGA3_VCCIO
3 FPGA3_SPI_CSN
5 FPGA3_FLASH_SPI_CSN
7 FPGA3_SPI_SCLK
9 FPGA3_SPI_MOSI
2
4 FPGA3_SPI_MISO
6 FPGA3_CRESETN
8 FPGA3_CDONE
10
GND

FPGA VIN Interface

Design Note: Decoupling for FPGA VCCIO2
TDA_VDDSHV_3V3
C101 0.1uF 6.3V
C102 0.01uF 25V
C103 1000pF 16V
GND

U5D
LIA-MD6000-6JMG80
PB16A/PCLKT2_0 — D9 — TDA_VIN3A_D8
PB16B/PCLKC2_0 — D10 — TDA_VIN3A_D9
PB12A/GPLLT2_0 — E9 — TDA_VIN3A_D10
PB12B/GPLLC2_0 — E10 — TDA_VIN3A_D11
PB6A/GR_PCLK2_0 — F9 — TDA_VIN3A_D12
PB6B — F10 — TDA_VIN3A_D13
PB2A — G9 — TDA_VIN3A_D14
PB2B — G10 — TDA_VIN3A_D15
PB6C — J10 — TDA_VIN3A_D16
PB6D — J9 — TDA_VIN3A_D17
PB2C/MIPI_CLKT2_0 — H10 — TDA_VIN3A_D18
PB2D/MIPI_CLKC2_0 — H9 — TDA_VIN3A_D19
PB16C/PCLKT2_1 — K8 — TDA_VIN3A_D20
PB16D/PCLKC2_1 — J8 — TDA_VIN3A_D21
PB12C — K10 — TDA_VIN3A_D22
PB12D — K9 — TDA_VIN3A_D23
VCCIO2 — F6, F7 — TDA_VDDSHV_3V3

Orderable: MMWCAS-DSP-EVM	Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A	Project Title: Cascade Radar Host Processor Board	
Number: PROC055 Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
BOM Rev: Not in version control	Assembly Variant:001	Sheet:58 of 66
Drawn By:Alec Schott	File: PROC055B_FPGA3_VIN.SchDoc	Size: B
Engineer: Alec Schott	Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

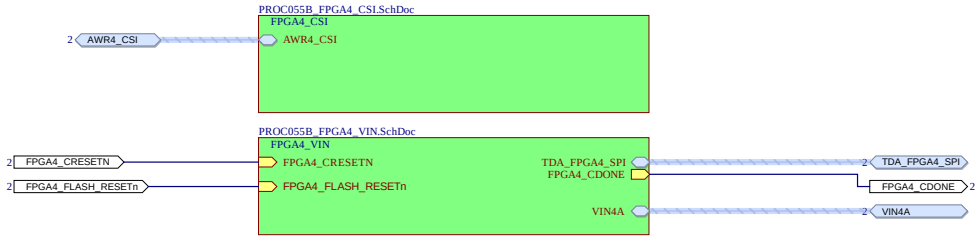
Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #4

References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.



Design Note: CRESETN broadcast from TDA2 to all FPGA and all FPGA connectors.

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 3/29/2021
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:59 of 66
Drawn By:Alec Schott		File: PROC055B_FPGA4_Top.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

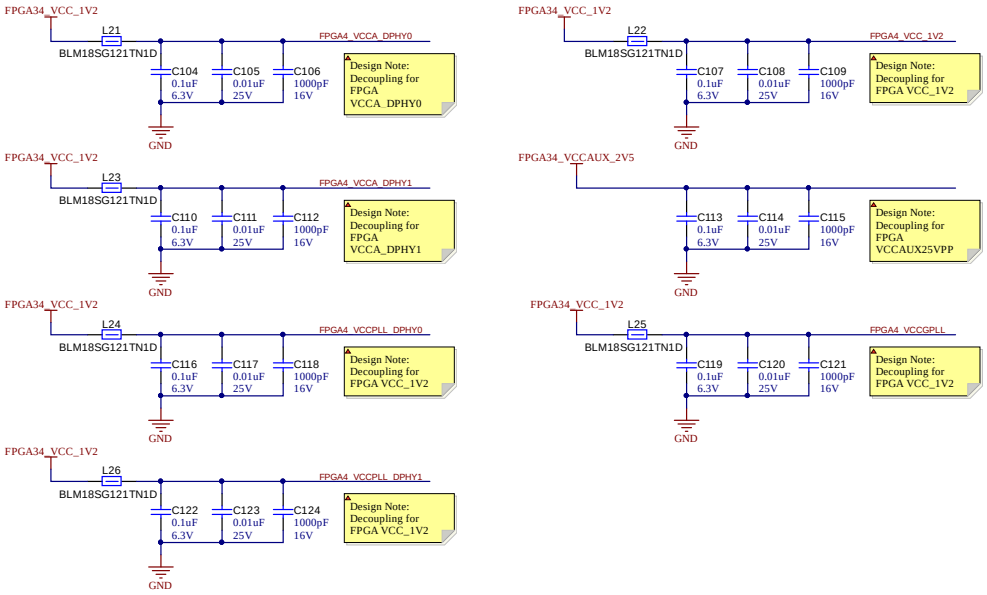
References

TDA2 Evaluation Board
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)
TDA2 Technical Reference Manual - Section 15.3 "EMIF Controller" (CDDS INTERNAL ONLY)

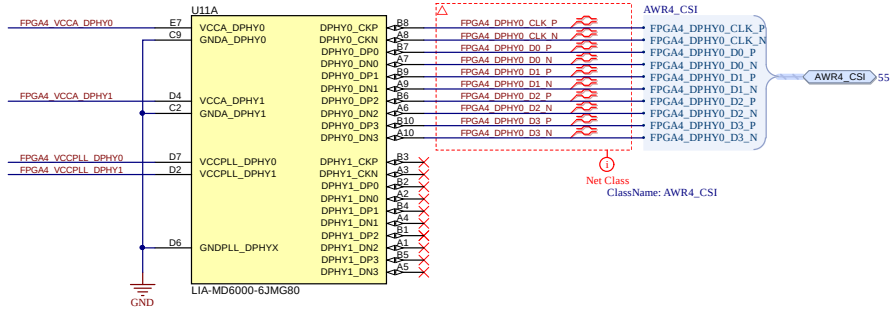
Follow all layout guidelines as presented in these documents.

Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #1 CSI2.0 Interface, FPGA1/4 Power Supplies

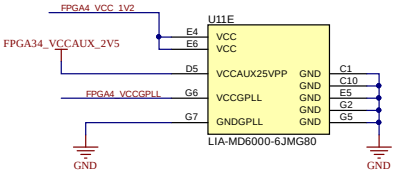
FPGA VCC, VCCAUX 2.5V and VCCGPLL Decoupling



FPGA VCCA_PHY[1:0], VCCPLL_DPHY[1:0] and DPHY[1:0]



FPGA VCC, VCCAUX 2.5V and VCCGPLL



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:60 of 66
Drawn By:Alec Schott		File: PROC055B_FPGA4_CSI.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments
http://www.ti.com

Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #4
FPGA VIN, SPI and Configuration Interface

References
Lattice HW-USBN-2B Programming Cable
Lattice HW-USBN-2B Programming Cable User Guide
Lattice CrossFire FPGA Configuration Guide

Follow all layout guidelines as presented in these documents.

55 FPGA4_CRESETN — FPGA4_CRESETN
46 FPGA4_FLASH_RESETn — FPGA4_FLASH_RESETn

FPGA4_CDONE → FPGA4_CDONE 55

ClassName: TDA_SPI_FPGA4
Net Class 1
FPGA4_SPI_CSN, FPGA4_SPI_SCLK, FPGA4_SPI_MISO, FPGA4_SPI_MOSI → TDA_FPGA4_SPI → 55 TDA_FPGA4_SPI

ClassName: VIN4A
Net Class 1
TDA_VIN4A_D[23..0], TDA_VIN4A_CLK0, TDA_VIN4A_FLD0, TDA_VIN4A_DE0, TDA_VIN4A_VSYNC0 → VIN4A → 55 VIN4A

FPGA SPI/Config Interface

Design Note: Decoupling for FPGA VCCIO0

TDA_VDDSHV_3V3 — C125 0.1uF 6.3V, C126 0.01uF 25V, C127 1000pF 16V — GND

Design Note: FPGA SPI interface run in SLAVE mode or MASTER mode. Pin-names indicate MASTER mode operation.

MISO and MOSI functionality swapped in SLAVE mode, allowing for SPI programming from Lattice HW-USBN-2B Programming Cable or TDA2 host processor.

TDA_VDDSHV_3V3 — R40 10k, R41 10k

U9B
PB52/SPI_SS/CSN/SCL — H1 — FPGA4_FLASH_SPI_CSN
PB53/SPI_SCK/MCK/SDA — J1 — FPGA4_SPI_SCLK
PB50/MOSI — G1 — FPGA4_SPI_MOSI
PB51/MISO — K1 — FPGA4_SPI_MISO_RS — R42 0 — FPGA4_SPI_MISO
PB48/PCLKT0_1/USER_SCL — D1 — FPGA4_SPI_CSN
PB47/PCLKT0_0/USER_SDA — D2
PB49/PMU_WKUPN/CDONE — J2 — FPGA4_CDONE
CRESET_B — H2 — FPGA4_CRESETN
VCCIO0 — F4 — TDA_VDDSHV_3V3
LIA-MD6000-6JMG80

TDA_VDDSHV_3V3 — R43 10k

Design Note: After internal POR circuit indicates good power a CRESETN low to high transition will start NVCM boot sequence.

Design Note: After internal POR circuit indicates good power a CRESETN low to high transition will start NVCM boot sequence.

R44 10k — GND

TDA2/Programmer SPI CS Jumper

SH-J4 Shunt
FPGA4_SPI_CSN
FPGA4_FLASH_SPI_CSN
J8 Header_2x1
R546 0

FPGA and NOR Flash Programming Header

TDA_VDDSHV_3V3 — R48 0
J9 Header_5x2
FPGA4_VCCIO 1, FPGA4_SPI_CSN 3, FPGA4_FLASH_SPI_CSN 5, FPGA4_SPI_SCLK 7, FPGA4_SPI_MOSI 9
2, 4 FPGA4_SPI_MISO, 6 FPGA4_CRESETN, 8 FPGA4_CDONE, 10
GND

Design Note: See notes from Lattice and TI programming reference documents fo HW-USBN-2B USB Programming Cable Flying-Lead Connections

FPGA NOR Flash

TDA_VDDSHV_3V3 — C131 0.1uF 6.3V — GND

TDA_VDDSHV_3V3 — R46 10k, R45 10k
ClassName: TDA_SPI_FPGA4
Net Class 1
FPGA4_SPI_MOSI, FPGA4_SPI_MISO — R47 0 — FPGA4_SPI_MISO_RS
FPGA4_FLASH_WPN
FPGA4_FLASH_RESETn

U12
VCC — 8 — TDA_VDDSHV_3V3
SCLK — 6 — FPGA4_SPI_SCLK
SI/SIO0 — 5
SO/SIO1 — 2
WP/SIO2 — 3
RESET/SIO3 — 7 — TDA_VDDSHV_3V3
CS — 1 — FPGA4_FLASH_SPI_CSN
GND — 4 — GND
MX25L12835FM2I-10G

Design Note: Flash WP and HOLD disabled

Design Note: Running QSPI capable NOR flash in x1 SPI (XIO-SPI) mode.

FPGA VIN Interface

Design Note: Decoupling for FPGA VCCIO1

TDA_VDDSHV_3V3 — C128 0.1uF 6.3V, C129 0.01uF 25V, C130 1000pF 16V — GND

U9C
PB34A/GR_PCLK1_0 — E1 — TDA_VIN4A_VSYNC0
PB34B — E2 — TDA_VIN4A_DE0
PB38A — F1 — FPGA4_PB38A — TP9
PB38B — F2 — TDA_VIN4A_FLD0
PB38C — K4 — TDA_VIN4A_D0
PB38D — J4 — TDA_VIN4A_D1
PB29A/PCLKT1_0 — J7 — TDA_VIN4A_D2
PB29B/PCLKC1_0 — K7 — TDA_VIN4A_D3
PB29C/PCLKT1_1 — K6 — TDA_VIN4A_CLK0
PB29D/PCLKC1_1 — J6
PB34C/MIPI_CLKT1_0 — K5 — TDA_VIN4A_D4
PB34D/MIPI_CLKC1_0 — J5 — TDA_VIN4A_D5
VCCIO1 — F5 — TDA_VDDSHV_3V3
VCCIO1 — G4
PB43C — K3 — TDA_VIN4A_D6
PB43D — J3 — TDA_VIN4A_D7
LIA-MD6000-6JMG80

TDA_VIN4A_D[23..0]

FPGA VIN Interface

Design Note: Decoupling for FPGA VCCIO2

TDA_VDDSHV_3V3 — C132 0.1uF 6.3V, C133 0.01uF 25V, C134 1000pF 16V — GND

U9D
PB16A/PCLKT2_0 — D9 — TDA_VIN4A_D8
PB16B/PCLKC2_0 — D10 — TDA_VIN4A_D9
PB12A/GPLLT2_0 — E9 — TDA_VIN4A_D10
PB12B/GPLLC2_0 — E10 — TDA_VIN4A_D11
PB6A/GR_PCLK2_0 — F9 — TDA_VIN4A_D12
PB6B — F10 — TDA_VIN4A_D13
PB2A — G9 — TDA_VIN4A_D14
PB2B — G10 — TDA_VIN4A_D15
PB6C — J10 — TDA_VIN4A_D16
PB6D — J9 — TDA_VIN4A_D17
PB2C/MIPI_CLKT2_0 — H10 — TDA_VIN4A_D18
PB2D/MIPI_CLKC2_0 — H9 — TDA_VIN4A_D19
PB16C/PCLKT2_1 — K8 — TDA_VIN4A_D20
PB16D/PCLKC2_1 — J8 — TDA_VIN4A_D21
VCCIO2 — F6 — TDA_VDDSHV_3V3
VCCIO2 — F7
PB12C — K10 — TDA_VIN4A_D22
PB12D — K9 — TDA_VIN4A_D23
LIA-MD6000-6JMG80

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title: TPS659039-Q1 TDA2 PMIC - SMPS6/7/8/9	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:61 of 66
Drawn By:Alec Schott		File: PROC055B_FPGA4_VIN.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments http://www.ti.com

TDA2 AWR RF Board Connectors - Top

References

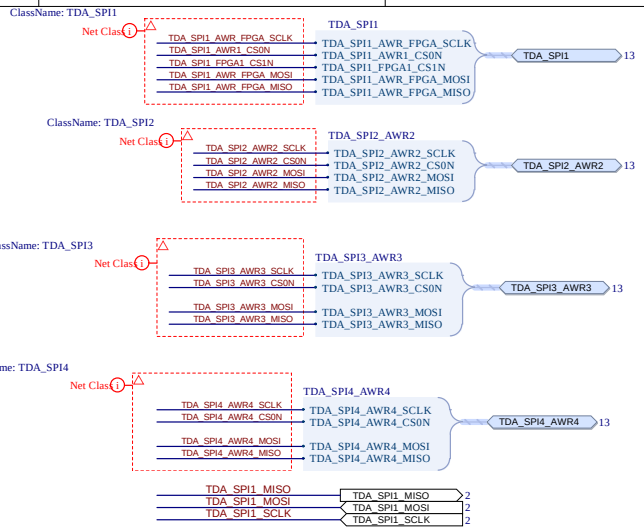
TDA2 Evaluation Board

TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)

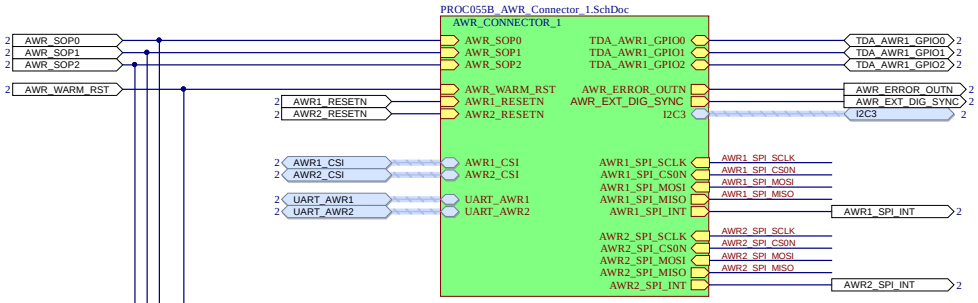
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

TI Ethernet Physical Layer Controller 10/100/1000 Base-TX PHY Serial Interface 64-HTQFP (10x10)

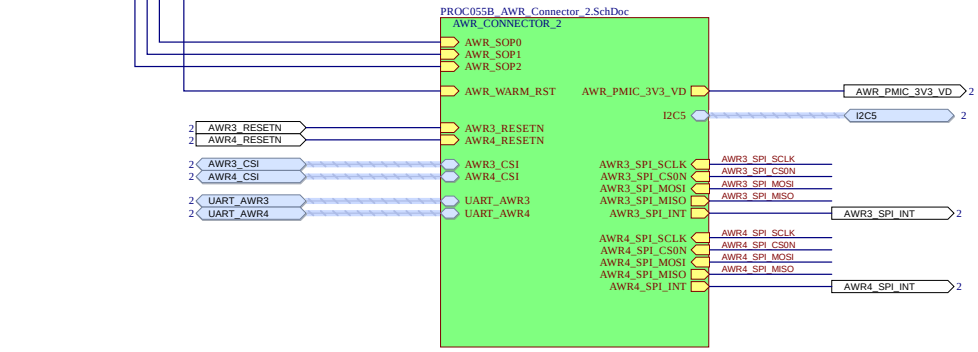
Follow all layout guidelines as presented in these documents.



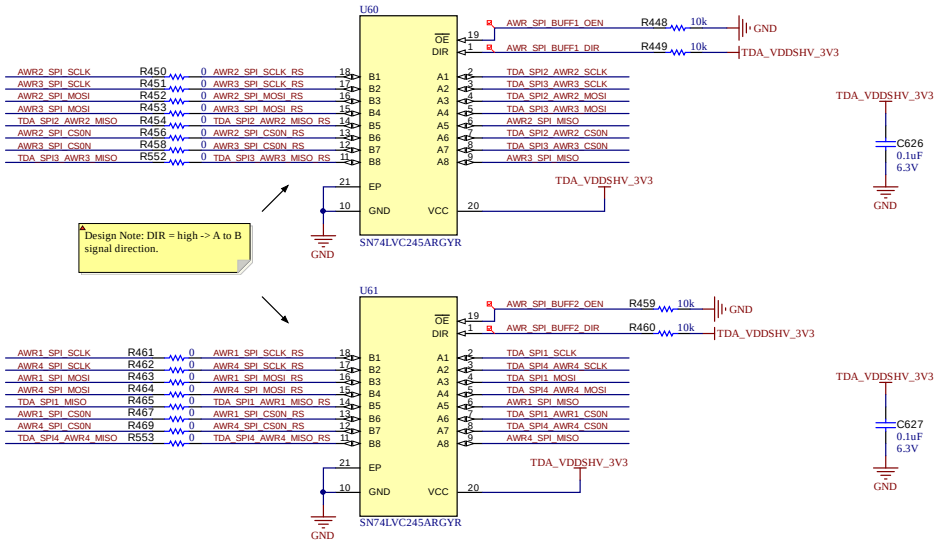
AWR RF Board Connector 1 - AWR1 and AWR2



AWR RF Board Connector 2 - AWR3 and AWR4



TDA2/AWR SPI Port Fanout and Buffer



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 3/29/2021
TID #: N/A		Project Title:Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title:	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:62 of 66
Drawn By:Alec Schott		File: PROC055B_AWR_Connector_Top.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

Texas Instruments http://www.ti.com

TDA2 AWR RF Board Connector 1 - Power, Control and Data Interfaces

References

TDA2 Evaluation Board

TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)

TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

TI Ethernet Physical Layer Controller 10/100/1000 Base-TX PHY Serial Interface 64-HTQFP (10x10)

Follow all layout guidelines as presented in these documents.

58 AWR_SOP0 — TDA_GPIO2_22_AWR_SOP0
58 AWR_SOP1 — TDA_GPIO2_25_AWR_SOP1
58 AWR_SOP2 — TDA_GPIO2_13_AWR_SOP2
58 AWR_WARM_RST — TDA_GPIO2_12_AWR_WARM_RST
58 AWR1_RESETN — TDA_GPIO2_2_AWR1_RESETN
58 AWR2_RESETN — TDA_GPIO2_9_AWR2_RESETN

Mates to AWR RF Board P1

J1
Hirose_FX23-120S-0_5SV10

AWR_CONN1_MON	1	61	TDA_AWR1_GPIO2_GPIO6_5	TDA_AWR1_GPIO2	58
AWR_CONN_TP1	2	62	TDA_AWR1_GPIO1_GPIO6_4	TDA_AWR1_GPIO1	58
	3	63	TDA_AWR1_GPIO0_GPIO4_18	TDA_AWR1_GPIO0	58
	4	64	AWR_EXT_DIG_SYNC		
	5	65			
	6	66	AWR1_SPI_MISO		
	7	67	TDA_GPIO7_24_AWR1_SPI_INT		
	8	68	AWR1_SPI_CS0N		
	9	69	AWR1_SPI_MOSI		
	10	70	AWR1_SPI_SCLK		
	11	71			
FPGA1_DPHY0_D3_P	12	72	TDA_I2C3_SCL		
FPGA1_DPHY0_D3_N	13	73	TDA_I2C3_SDA		
	14	74	AWR_CONN_TP5	TP3	
	15	75	TDA_GPIO2_19_AWR_ERROR_OUTN		
FPGA1_DPHY0_D2_P	16	76			
FPGA1_DPHY0_D2_N	17	77	TDA_UART3_AWR1_TXD		
	18	78	TDA_UART3_AWR1_RXD		
FPGA1_DPHY0_CLK_P	19	79	AWR1_MSS_LOGGER	TP191	
FPGA1_DPHY0_CLK_N	20	80	AWR1_BSS_LOGGER	TP192	
	21	81			
AWR_CONN_TP2	22	82	AWR1_SOP2 — R1 0	TDA_GPIO2_13_AWR_SOP2	
	23	83	AWR1_SOP1 — R2 0	TDA_GPIO2_25_AWR_SOP1	
	24	84	AWR1_SOP0 — R3 0	TDA_GPIO2_22_AWR_SOP0	
FPGA1_DPHY0_D1_P	25	85	TDA_GPIO2_2_AWR1_RESETN		
FPGA1_DPHY0_D1_N	26	86	AWR1_WARM_RST — R4 0	TDA_GPIO2_12_AWR_WARM_RST	
	27	87			
FPGA1_DPHY0_D0_P	28	88			
FPGA1_DPHY0_D0_N	29	89			
	30	90			
	31	91			
	32	92			
	33	93	AWR2_SPI_MISO		
	34	94	TDA_AWR2_SPI_INT_GPIO5_10		
	35	95			
	36	96	AWR2_SPI_CS0N		
	37	97	AWR2_SPI_MOSI		
	38	98	AWR2_SPI_SCLK		
	39	99			
	40	100	TDA_UART3_AWR2_TXD		
FPGA2_DPHY0_D3_P	41	101	TDA_UART3_AWR2_RXD		
FPGA2_DPHY0_D3_N	42	102	AWR2_MSS_LOGGER	TP193	
	43	103	AWR2_BSS_LOGGER	TP194	
	44	104			
FPGA2_DPHY0_D2_P	45	105			
FPGA2_DPHY0_D2_N	46	106			
	47	107			
	48	108			
FPGA2_DPHY0_CLK_P	49	109	TDA_GPIO2_9_AWR2_RESETN		
FPGA2_DPHY0_CLK_N	50	110	AWR2_WARM_RST — R5 0	TDA_GPIO2_12_AWR_WARM_RST	
	51	111			
AWR_CONN_TP3	52	112	AWR2_SOP2 — R6 0	TDA_GPIO2_13_AWR_SOP2	
	53	113	AWR2_SOP1 — R7 0	TDA_GPIO2_25_AWR_SOP1	
	54	114	AWR2_SOP0 — R8 0	TDA_GPIO2_22_AWR_SOP0	
FPGA2_DPHY0_D1_P	55	115			
FPGA2_DPHY0_D1_N	56	116			
	57	117			
FPGA2_DPHY0_D0_P	58	118			
FPGA2_DPHY0_D0_N	59	119			
	60	120	AWR_CONN1_MON		
	P1	P3		SYSTEM_5V0	
	P2	P4			
	MH1	MH3			
	MH2	MH4			

TP1, TP4, TP5

C1 47uF 10V, C2 47uF 10V

GND GND GND GND

Design Note: TDA I2C3 interfaces to primary AWR PMIC I2C port.

Design Note: TO AWR devices

Design Note: FROM AWR devices

Design Note: TO AWR devices

Design Note: FROM AWR devices

Net Class: ClassName: AWR1_SPI

AWR1_SPI_SCLK	AWR1_SPI_SCLK	58
AWR1_SPI_CS0N	AWR1_SPI_CS0N	58
AWR1_SPI_MOSI	AWR1_SPI_MOSI	58
AWR1_SPI_MISO	AWR1_SPI_MISO	58
TDA_GPIO7_24_AWR1_SPI_INT	AWR1_SPI_INT	58

Net Class: ClassName: AWR2_SPI

AWR2_SPI_SCLK	AWR2_SPI_SCLK	58
AWR2_SPI_CS0N	AWR2_SPI_CS0N	58
AWR2_SPI_MOSI	AWR2_SPI_MOSI	58
AWR2_SPI_MISO	AWR2_SPI_MISO	58
TDA_AWR2_SPI_INT_GPIO5_10	AWR2_SPI_INT	58

AWR1_CSI

FPGA1_DPHY0_CLK_P	FPGA1_DPHY0_CLK_P	
FPGA1_DPHY0_CLK_N	FPGA1_DPHY0_CLK_N	
FPGA1_DPHY0_D0_P	FPGA1_DPHY0_D0_P	
FPGA1_DPHY0_D0_N	FPGA1_DPHY0_D0_N	
FPGA1_DPHY0_D1_P	FPGA1_DPHY0_D1_P	
FPGA1_DPHY0_D1_N	FPGA1_DPHY0_D1_N	
FPGA1_DPHY0_D2_P	FPGA1_DPHY0_D2_P	
FPGA1_DPHY0_D2_N	FPGA1_DPHY0_D2_N	
FPGA1_DPHY0_D3_P	FPGA1_DPHY0_D3_P	
FPGA1_DPHY0_D3_N	FPGA1_DPHY0_D3_N	
	AWR1_CSI	58

AWR2_CSI

FPGA2_DPHY0_CLK_P	FPGA2_DPHY0_CLK_P	
FPGA2_DPHY0_CLK_N	FPGA2_DPHY0_CLK_N	
FPGA2_DPHY0_D0_P	FPGA2_DPHY0_D0_P	
FPGA2_DPHY0_D0_N	FPGA2_DPHY0_D0_N	
FPGA2_DPHY0_D1_P	FPGA2_DPHY0_D1_P	
FPGA2_DPHY0_D1_N	FPGA2_DPHY0_D1_N	
FPGA2_DPHY0_D2_P	FPGA2_DPHY0_D2_P	
FPGA2_DPHY0_D2_N	FPGA2_DPHY0_D2_N	
FPGA2_DPHY0_D3_P	FPGA2_DPHY0_D3_P	
FPGA2_DPHY0_D3_N	FPGA2_DPHY0_D3_N	
	AWR2_CSI	58

UART_AWR1

TDA_UART3_AWR1_TXD	TDA_UART1_TXD	
TDA_UART3_AWR1_RXD	TDA_UART1_RXD	
	UART_AWR1	58

UART_AWR2

TDA_UART3_AWR2_TXD	TDA_UART2_TXD	
TDA_UART3_AWR2_RXD	TDA_UART2_RXD	
	UART_AWR2	58

I2C3

TDA_I2C3_SCL	TDA_I2C3_SCL	
TDA_I2C3_SDA	TDA_I2C3_SDA	
	I2C3	58

TDA_GPIO2_19_AWR_ERROR_OUTN	AWR_ERROR_OUTN	58
AWR_EXT_DIG_SYNC	AWR_EXT_DIG_SYNC	58

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title:	
BOM Rev: Not in version control		Assembly Variant:001	Sheet:63 of 66
Drawn By:Alec Schott		File: PROC055B_AWR_Connector_1.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

http://www.ti.com

TDA2 AWR RF Board Connector 2 - Power, Control and Data Interfaces

References

TDA2 Evaluation Board

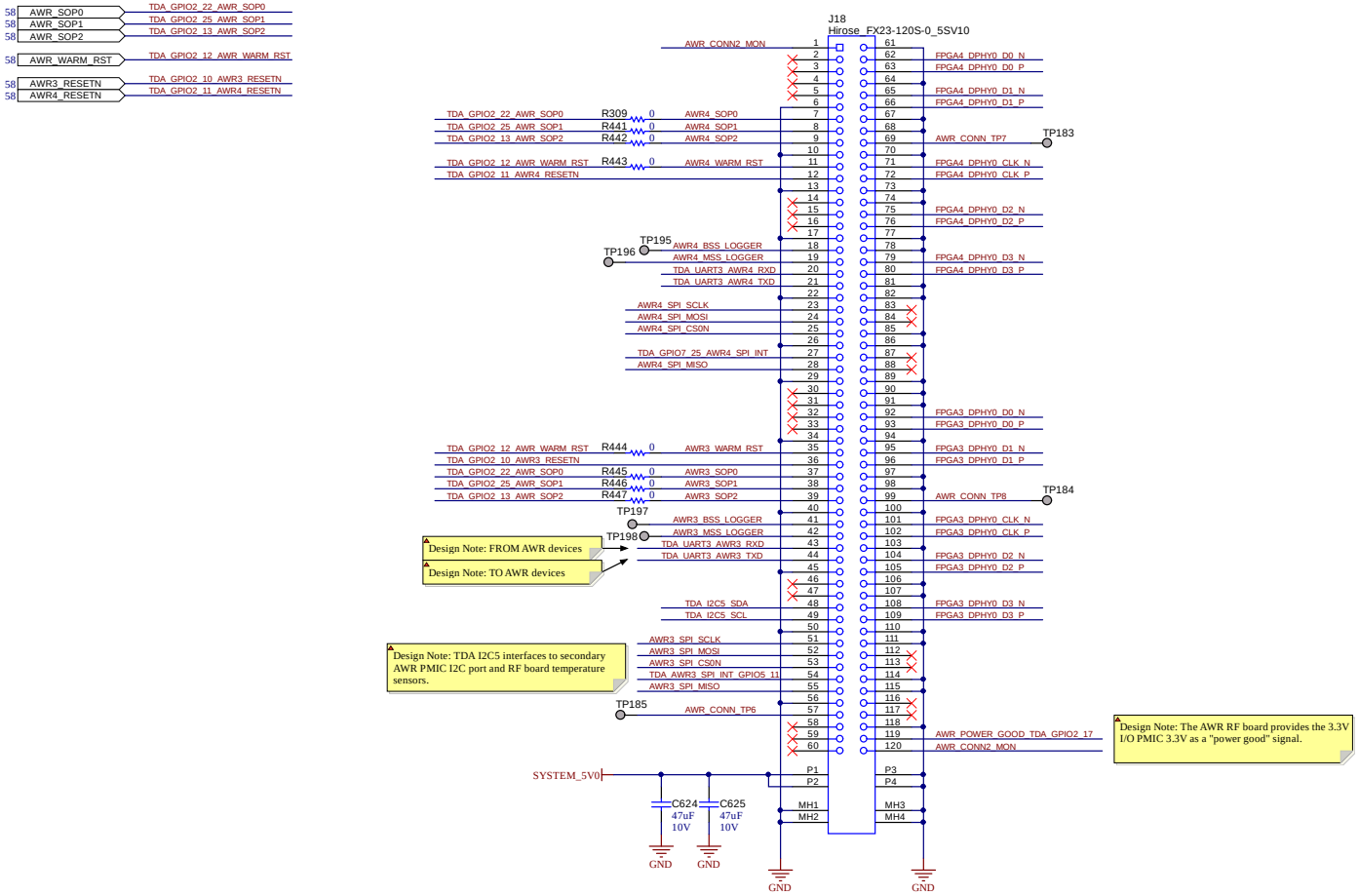
TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)

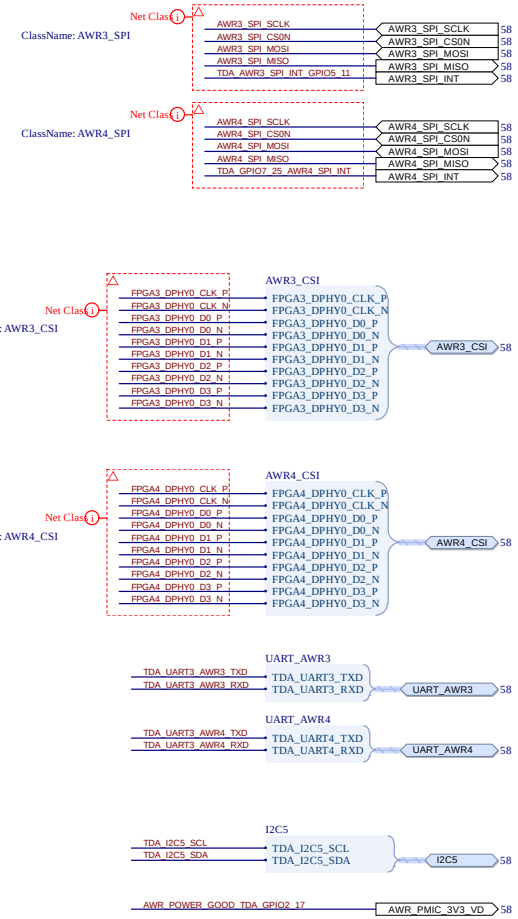
TDA2 Evaluation Board - BoM (CDDS NTERNAL ONLY)

TI Ethernet Physical Layer Controller 10/100/1000 Base-TX PHY Serial Interface 64-HTQFP (10x10)

Follow all layout guidelines as presented in these documents.

Mates to AWR RF Board P2



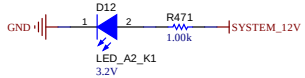


Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant:001	Sheet:64 of 66
Drawn By:Alec Schott		File: PROC055B_AWR_Connector_2.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

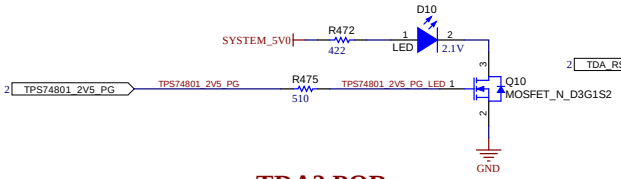
Cascade Radar Host Board - LED Indicators

I2C GPIO Expander LEDs

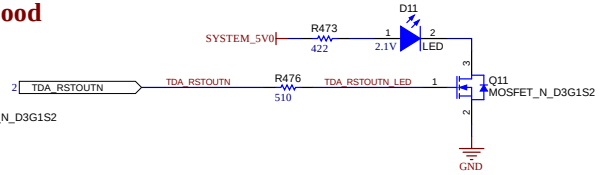
Input 12V Power Indicator



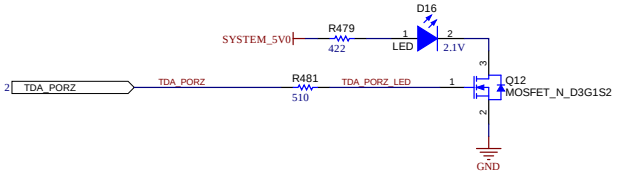
TPS74801 Ethernet 2.5V Power Good



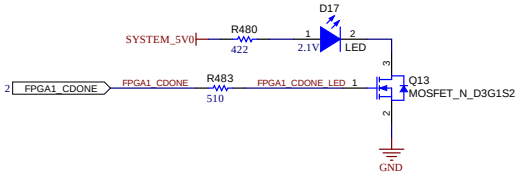
TDA2 RESTOUTz



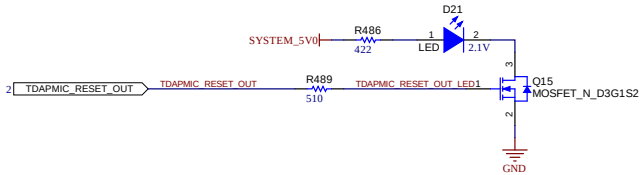
TDA2 PORz



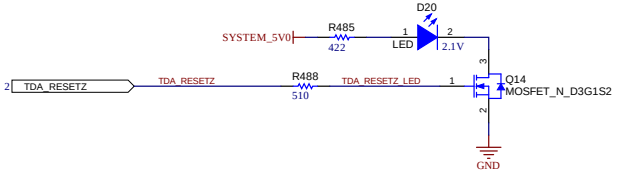
FPGA1 CDONE LED



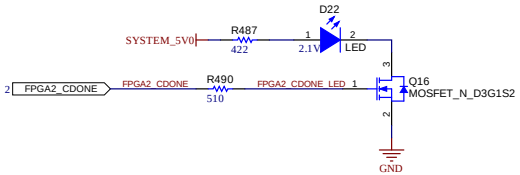
TDA2 PMIC Reset Out



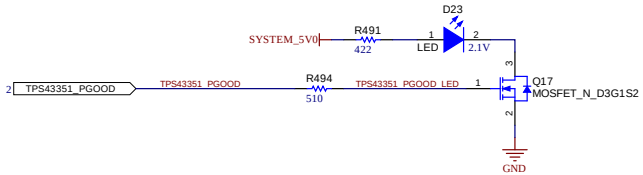
TDA2 RESETz



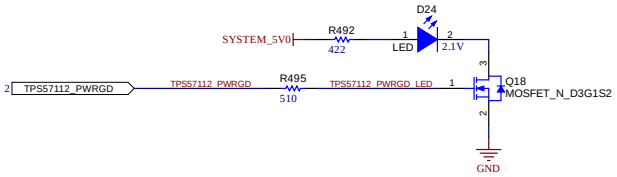
FPGA2 CDONE LED



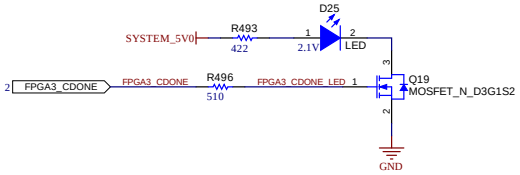
TPS43351 3.3V and 5.0V Power Good



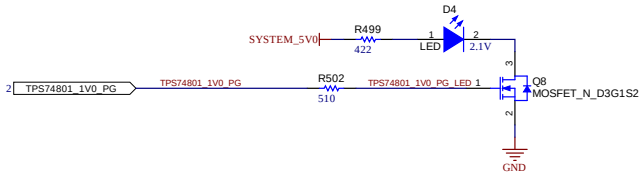
TPS57112 DDR3 1.35V Power Good



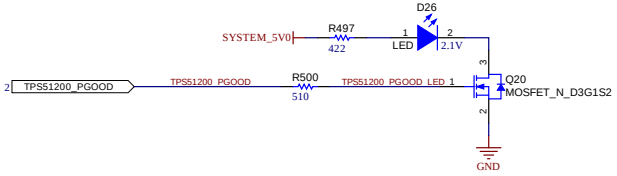
FPGA3 CDONE LED



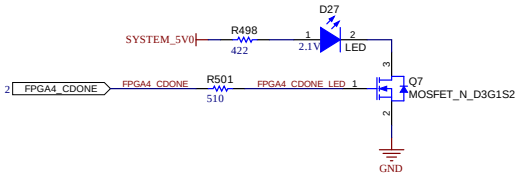
TPS74801 Ethernet 1.0V Power Good



TPS51200 DDR3 VTT and VREF Power Good



FPGA4 CDONE LED



Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 9/17/2019
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title:	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:65 of 66
Drawn By:Alec Schott		File: PROC055B_LED_Indicators.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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Cascade Radar Host Board - Hardware Tracking

H1
8418

H2
8418

H3
8418

H4
8418

H5
PMSSS 632 0038 PH

H6
PMSSS 632 0038 PH

H7
PMSSS 632 0038 PH

H8
PMSSS 632 0038 PH

Design Note: All screw-holes should be connected to PCB GND to allow for possible chassis mounting to enclosure.

FID1
Fiducial

FID2
Fiducial

FID3
Fiducial

FID4
Fiducial

FID5
Fiducial

FID6
Fiducial

PCB Number: PROC055
PCB Rev: B
Printed Circuit Board

Logo1
PCB LOGO
Texas Instruments

Logo2
PCB LOGO
WEEE logo

Logo3
PCB LOGO
FCC disclaimer

Logo5
CE Mark

H9
MPMS 002 0005 PH

LOGO4
CAUTION HOT SURFACE

MP1
1
1
9774025243R
GND

MP2
BDN10-3CB/A01
BDN10-3CB/A01

MD1
MB-MP16DA/AM

MD2
MZ-V7P512BW

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5
Assembly Note
INDICATION FOR COMPONENTS D* (WITH 2 PINS) ARE GIVEN AT THEIR CATHODE SIDE.

ZZ6
Assembly Note
MP1 must be soldered down to the "Top Layer" of PCB.

ZZ7
Assembly Note
Refer to Test Procedure Document for installing uSD, H9, and SSD Drive

Orderable: MMWCAS-DSP-EVM		Designed for:Public Release	Mod. Date: 3/29/2021
TID #: N/A		Project Title: Cascade Radar Host Processor Board	
Number: PROC055	Rev: B	Sheet Title:	
EVM Rev: Not in version control		Assembly Variant:001	Sheet:66 of 66
Drawn By:Alec Schott		File: PROC055B_EVM_Hardware.SchDoc	Size: B
Engineer: Alec Schott		Contact: http://www.ti.com/mmwave	

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http://www.ti.com

Bill of Materials

Bill of Materials For Variant [001] of Project [PROC055B_Cascade_Radar_Host.PrjPcb

Source Data From: PROC055B_Cascade_Radar_Host.PrjPcb
Project: PROC055B_Cascade_Radar_Host.PrjPcb
Variant: 001

Creation Date: 4/7/2021 9:55:13 AM
Print Date: 07-Apr-21 9:56:11 AM

Footprint	Comment	LibRef	Designator	Description	Quantity
	Printed Circuit Board	CMP-0003618-2	PCB1	Printed Circuit Board	1
1210_270	Capacitor	CMP-0009220-2, CMP-0009224-2	C1, C2, C137, C168, C170, C184, C624, C625	CAP, CERM, 47 uF, 10 V, +/- 10%, X7R, 1210, CAP, CERM, 22 uF, 25 V, +/- 10%, X7R, 1210	8
0402S	Capacitor	CMP-0006623-2, CMP-0006594-2, CMP-0006305-2, CMP-0006218-2, CMP-0006630-2, CMP-0064947-2	C3, C6, C9, C12, C15, C18, C21, C27, C28, C31, C34, C35, C38, C41, C44, C47, C50, C53, C56, C62, C63, C66, C69, C70, C73, C76, C79, C82, C85, C88, C91, C94, C97, C100, C101, C104, C107, C110, C113, C116, C119, C122, C125, C128, C131, C132, C143, C152, C154, C156, C158, C178, C193, C198, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C234, C248, C253, C254, C255, C256, C257, C258, C259, C260, C267, C268, C269, C270, C271, C272, C274, C275, C276, C277, C278, C279, C281, C282, C283, C284, C285, C286, C288, C289, C290, C291, C292, C293, C295, C296, C297, C298, C299, C300, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C320, C321, C322, C323, C324, C325, C327, C328, C329, C330, C331, C332, C334, C335, C336, C337, C338, C339, C341, C342, C343, C344, C345, C346, C364, C365, C366, C367, C368, C371, C372, C373, C374, C381, C385, C386, C387, C388, C389, C394, C395, C396, C397, C398, C399, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C423, C424, C428, C430, C433, C434, C435, C436, C437, C440, C441, C442, C443, C444, C445, C446,	CAP, CERM, 0.1 uF, 6.3 V, +/- 10%, X7R, 0402, CAP, CERM, 2.2 uF, 16 V, +/- 10%, X5R, 0402, CAP, CERM, 100 pF, 50 V, +/- 10%, X7R, 0402, CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0402, CAP, CERM, 0.22 uF, 10 V, +/- 10%, X7R, 0402, CAP, CERM, 1 uF, 6.3 V,+/- 10%, X7R, 0402	334
0402S	GCM155R71E103KA37D	CMP-0006352-2	C4, C7, C10, C13, C16, C19, C22, C29, C32, C36, C39, C42, C45, C48, C51, C54, C57, C64, C67, C71, C74, C77, C80, C83, C86, C89, C92, C95, C98, C102, C105, C108, C111, C114, C117, C120, C123, C126, C129, C133, C369, C375, C382, C390, C393, C400, C403, C569, C572	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0402	49
0201L	GRM033R71C102KA01D	CMP-0009745-1	C5, C8, C11, C14, C17, C20, C23, C40, C43, C46, C49, C52, C55, C58, C75, C78, C81, C84, C87, C90, C93, C106, C109, C112, C115, C118, C121, C124	CAP, CERM, 1000 pF, 16 V, +/- 10%, X7R, 0201	28
0603S	GRM188Z71A475ME15D	CMP-0007498-4	C24, C25, C26, C59, C60, C61, C426, C432, C439, C450, C471, C501, C502, C504, C505	CAP, CERM, 4.7 uF, 10 V, +/- 20%, X7R, 0603	15
0402S	AC0402KRX7R7BB102	CMP-0086247-1	C30, C33, C37, C65, C68, C72, C96, C99, C103, C127, C130, C134, C142, C148, C351, C352, C353, C354, C357, C361, C362, C363, C370, C376, C383, C391, C392, C401, C402, C570, C571, C606, C610	CAP, CERM, 1000 pF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0402	33
FP-GCM188L81H104KA57D_0603-MFG	GCM188L81H104KA57D	CMP-0086535-1	C135	0.1µF ±10% 50V Ceramic Capacitor X8L 0603 (1608 Metric)	1
0603S	GRM188D71A106MA73D	CMP-0007298-4	C136, C141, C144, C145, C146, C150, C151, C153, C157, C266, C273, C280, C287, C294, C301, C319, C326, C333, C340, C349, C355, C359, C427, C522, C528, C534, C540, C545, C550, C559, C562, C575, C595, C603, C611, C615	CAP, CERM, 10 uF, 10 V, +/- 20%, X7T, 0603	36
0402S	CC0402KRX7R8BB472	CMP-0860557-1	C138	CAP, CERM, 4700 pF, 25 V,+/- 10%, X7R, 0402	1
0402S	CL05C120JB5NNNC	CMP-0006345-2	C139	CAP, CERM, 12 pF, 50 V, +/- 5%, C0G/NP0, 0402	1
0402S	CC0402KRX7R9BB332	CMP-0860559-1	C140	CAP, CERM, 3300 pF, 50 V,+/- 10%, X7R, 0402	1
0402S	CL05B104KP5NNNC	CMP-0006343-2	C147, C149, C261, C262, C263, C264, C265, C315, C316, C317, C318	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0402	11
0402S	CL05B561KB5NNNC	CMP-0860565-1	C155, C159	CAP, CERM, 560 pF, 50 V,+/- 10%, X7R, 0402	2
0402S	UMK105B7104MV-FR	CMP-0860570-1	C160, C161, C469	CAP, CERM, 0.1 µF, 50 V,+/- 20%, X7R, 0402	3
0805L	GCM21BR71H105KA03K	CMP-0086249-1	C162, C163, C468	CAP, CERM, 1 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	3
0805L	GRM21BC71E106KE11L	CMP-0008262-2	C164, C165, C466	CAP, CERM, 10 uF, 25 V, +/- 10%, X7S, 0805	3
0805L	Capacitor	CMP-0007671-2	C166	CAP, CERM, 0.22 uF, 16 V, +/- 10%, X7R, 0805	1
1206_180L	GCM31CR71H225KA55L	CMP-0008814-2	C167	CAP, CERM, 2.2 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	1
0402S	CL05B224KO5NNNC	CMP-0860563-1	C169, C177	CAP, CERM, 0.22 µF, 16 V,+/- 10%, X7R, 0402	2
7343-31	Cap_Polarized	CMP-0011752-2, CMP-0011755-2	C171, C172, C173, C185, C186, C187, C188, C189	CAP, TA, 220 uF, 6.3 V, +/- 10%, 0.7 ohm, SMD, CAP, TA, 100 uF, 16 V, +/- 20%, 0.1 ohm, SMD	8
0603S	GRM188R61E475KE11D	CMP-0007347-5	C174, C200, C216, C217, C220, C222, C224, C226, C228, C230, C232, C583	CAP, CERM, 4.7 uF, 25 V, +/- 10%, X5R, 0603	12
0402S	CC0402KRX7R7BB103	CMP-0860554-1	C175, C180	CAP, CERM, 0.01 µF, 16 V,+/- 10%, X7R, 0402	2
0402S	CL05B103KB5NNNC	CMP-0860562-1	C176, C182	CAP, CERM, 0.01 µF, 50 V,+/- 10%, X7R, 0402	2
FP-CL05C560JB5NNNC_0402(1005 Metric)-IPC_C	CL05C560JB5NNNC	CMP-0086455-1	C179	Cap Ceramic 56pF 50V C0G 5% SMD 0402 125C Paper T/R	1
0402S	CL05B272KB5NNNC	CMP-0860564-1	C181	CAP, CERM, 2700 pF, 50 V,+/- 10%, X7R, 0402	1
0201L	Capacitor	CMP-0009752-1, CMP-0064969-1	C183, C602, C607, C617, C618	CAP, CERM, 2200 pF, 16 V, +/- 10%, X7R, 0201, CAP, CERM, 0.1 uF, 10 V,+/- 10%, X7S, 0201	5
0402S	0402B103K6R3CT	CMP-0860544-1	C190, C247, C252, C350, C356, C360	CAP, CERM, 0.01 µF, 6.3 V,+/- 10%, X7R, 0402	6
0402S	CC0402KRX7R8BB333	CMP-0860556-1	C191, C192	CAP, CERM, 0.033 µF, 25 V,+/- 10%, X7R, 0402	2
0402S	CC0402JRNPO9BN220	CMP-0860553-1	C194	CAP, CERM, 22 pF, 50 V,+/- 5%, C0G/NP0, 0402	1
0402S	CL05B102KB5NNNC	CMP-0860560-1	C195	CAP, CERM, 1000 pF, 50 V,+/- 10%, X7R, 0402	1
0402S	CC0402JRNPO9BN180	CMP-0860552-1	C196, C197, C237, C238, C239, C240, C241, C242	CAP, CERM, 18 pF, 50 V,+/- 5%, C0G/NP0, 0402	8
0402S	CC0402KRX7R8BB104	CMP-0860555-1	C199, C201, C235, C236, C243, C244, C245, C249, C250, C358	CAP, CERM, 0.1 µF, 25 V,+/- 10%, X7R, 0402	10
1210	C1210C476K9RAC7800	CMP-0860548-1	C218, C219, C221, C223, C225, C227, C229, C231, C233	CAP, CERM, 47 µF, 6.3 V,+/- 10%, X7R, 1210	9
0402S	0402ZC102KAT2A	CMP-0860545-1	C246, C251	CAP, CERM, 1000 pF, 10 V,+/- 10%, X7R, 0402	2
0402S	C0402C270J3GAC7867	CMP-0860547-1	C347, C348	CAP, CERM, 27 pF, 25 V,+/- 5%, C0G/NP0, 0402	2
0201_033	GRM033C71C104KE14D	CMP-0009670-3	C377, C378, C379, C380	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X5R, 0201	4
0603S	0603B474K6R3CT	CMP-0860546-1	C422, C429, C438, C447, C465	CAP, CERM, 0.47 µF, 6.3 V,+/- 10%, X7R, 0603	5
0603S	GRM188R71A225KE15D	CMP-0007370-4	C425, C431, C449, C470	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, 0603	4
0603_HV	C0603C331K5RACTU	CMP-0006921-4	C462, C464	CAP, CERM, 330 pF, 50 V, +/- 10%, X7R, 0603	2
0805L	C2012X6S1A226M125AC	CMP-0860550-1	C472, C503, C506	CAP, CERM, 22 µF, 10 V,+/- 20%, X6S, 0805	3
0402S	CC0402KRX7R9BB221	CMP-0860558-1	C564, C566	CAP, CERM, 220 pF, 50 V,+/- 10%, X7R, 0402	2
0402S	CL05B103KA5NNNC	CMP-0860561-1	C584, C605, C609	CAP, CERM, 0.01 µF, 25 V,+/- 10%, X7R, 0402	3
0805L	C2012X7R1C335K125AB	CMP-0860551-1	C585	CAP, CERM, 3.3 µF, 16 V,+/- 10%, X7R, 0805	1
0402S	GJM1555C1H6R2CB01D	CMP-0860567-1	C597, C598	CAP, CERM, 6.2 pF, 50 V,+4.032/-4.032%, C0G/NP0, 0402	2
SMC	Diode_TVS_Uni	CMP-0005687-2	D1, D2	Diode, TVS, Uni, 28 V, SMC	2
LED_LTST-C190	LED	CMP-0002827-2	D3, D4, D5, D6, D7, D9, D10, D11, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27	LED, Green, SMD	23
uDFN-14	SP3012-06UTG	CMP-0077876-1	D8	0.5pF Diode Array for USB3.0, uDFN-14	1
WL-SMCW_GREEN	LED_A2_K1	CMP-0002905-1	D12	LED, Green, SMD	1
1206M	Fuse	CMP-0003460-1	F1	Fuse, 8 A, 32VAC/VDC, SMD	1
Murata_NFM21PC	Filter_LC	CMP-0065400-1	FL1, FL2, FL3, FL4, FL5, FL6, FL7	Chip EMIFIL Chip 3-Terminal Capacitor for Large Current for General	7
Keystone_8418	8418	CMP-0003898-1	H1, H2, H3, H4		4
B-F_PMSSS_632_0038_PH	PMSSS 632 0038 PH	CMP-0003820-1	H5, H6, H7, H8	MACHINE SCREW PAN PHILLIPS 6-32	4
	MPMS 002 0005 PH	CMP-0003812-1	H9	MACHINE SCREW PAN PHILLIPS M2	1
Hirose_FX23-120S-0_5SV10	Hirose_FX23-120S-0_5SV10	CMP-0077866-1	J1, J18	Receptacle, 120 Pos Signal, 4 Pos Power, SMT	2
CONN_2510-6002	Header_5x2	CMP-0055448-1	J3, J5, J7, J9	Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH	4
CUI_PJ-082BH	PJ-082BH	CMP-0078272-1	J10	DC POWER JACK, R/A, TH	1
PhoenixContact_1727010	Receptacle_2x1	CMP-0055472-1	J11	Conn Term Block, 2POS, 3.81mm, TH	1
JK0-0177NL	Pulse_JK0-0229NL	CMP-0001610-2	J12	Connector, RJ45 with integrated magnetics, R/A, TH	1
Molex_47151-0001	HDMI_TYPE-A_4Shield	CMP-0055278-1	J13	Receptacle, HDMI, 0.5mm, 19 Pos, R/A, Gold, SMT	1
JAE_SM3ZS067U410AMR1000	SM3ZS067U410AMR1000	CMP-0078205-2	J14	PCI Express M.2 connector, 0.5mm, M Key, Gold, R/A, SMD	1
Molex_47352-1001	Molex_47352-1001	CMP-0055286-1	J15	MicroSD Card Connector, 1.1mm Pitch, R/A, Tin, SMT	1
Wurth_65100516121	CONN_USB_5Pos-4Shld	CMP-0054809-1	J16	Connector, Receptacle, USB Mini B 2.0, SMT	1
Amphenol_GSB4111312HR	CONN_USB3.1_STD-A_2SHLD	CMP-0075155-1	J17	Connector, Receptacle, USB 3.1 Type A, R/A, TH	1
Samtec_QSH-030-01-X-D-A	Receptacle_30x2_4MP_LeftRight	CMP-0075524-1	J19	Receptacle, 0.5 mm, 30x2, Gold, TH	1
CONN_ERF8-025-01-L-D-RA-L	ERF8-025-01-L-D-RA-L-TR	CMP-0055965-1	J20	Connector, Micro High Speed Socket Strip, 0.8mm, 25x2, R/A, SMT	1
0603S	BLM18SG121TN1D	CMP-0003352-2	L1, L2, L3, L4, L5, L6, L8, L9, L10, L11, L12, L13, L15, L16, L17, L18, L19, L20, L21, L22, L23, L24, L25, L26	Ferrite Bead, 120 ohm @ 100 MHz, 3 A, 0603	24
IND_TAIYO-4x4	Inductor_Iron	CMP-0059802-1	L7, L14	Inductor, Shielded, Powdered Iron, 2.2 uH, 2.2 A, 0.042 ohm, SMD	2
SRP4012TA	SRP4012TA-1R2M	CMP-0056933-1	L27	Inductor, Shielded, 1.2 uH, 3.5 A, 0.056 ohm, AEC-Q200 Grade 0, SMD	1
SRP1238A	Inductor_Iron	CMP-0056865-1	L28	Inductor, Shielded, Powdered Iron, 2.2 uH, 16 A, 0.008 ohm, SMD	1
FP-SRP1238A-3R3M_SMT_IND_13MMS_12MMS-MFG	SRP1238A-3R3M	CMP-0092086-1	L29	Inductor Power Shielded Wirewound 3.3uH 20% 100KHz 20Q-Factor Carbonyl Powder 12A 13.5mOhm DCR Automotive T/R	1
SRP4012TA	Inductor_Iron	CMP-0056932-1	L30, L31, L32, L33, L34, L35, L36, L37, L38	Inductor, Wirewound, 1 uH, 4 A, 0.047 ohm, SMD	9
MuRata_DLP2AD	DLP2ADA900HL4L	CMP-0077850-2	L39, L40, L42	Coupled inductor, 1.4 ohm, SMD	3
0805L	Ferrite_Bead	CMP-0003363-1	L41	Ferrite Bead, 220 ohm @ 100 MHz, 2 A, 0805	1
FP-MB-MP16DA/AM_CARD_MICRO_SD-MFG	MB-MP16DA/AM	CMP-0086926-1	MD1	MicroSDHC EVO Memory Card 16GB	1
FP-MZ-V7P512BW_NVMe_SSD_CARD-MFG	MZ-V7P512BW	CMP-0086927-1	MD2	970 PRO NVMe M.2 SSD	1
FP-9774025243R_SPACER_SMT_M2-MFG	9774025243R	CMP-0087027-2	MP1	WURTH ELEKTRONIK Spacer, SMT, Swage Round, Steel, 4.35x2.5mm	1
FP-BDN10-3CBA01_HEAT_SINK-MFG	BDN10-3CB/A01	CMP-0087594-1	MP2	Heat Sink Passive Pin Array Adhesive 26.4C/W Black Anodized	1
DQJ0008A	MOSFET_N_D56789G4S123	CMP-0000714-1	Q1, Q2, Q3, Q4, Q5	MOSFET, N-CH, 40 V, 100 A, DQJ0008A (VSONP-8)	5
SOT-363	NX3008CBKS,115	CMP-0082233-1	Q6	MOSFET, 2-CH, N/P-CH, -30 V, -0.2 A, AEC-Q101, SOT-363	1
SOT-23	MOSFET_N_D3G1S2	CMP-0000947-2, CMP-0000755-1	Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q20	MOSFET, N-CH, 100 V, 0.17 A, SOT-23, MOSFET, N-CH, 50 V, 0.22 A, SOT-23	14
0402S	Resistor	CMP-0026822-2, CMP-0026825-4, CMP-0026800-2, CMP-0026582-1, CMP-0026834-2, CMP-0026846-2, CMP-0026414-1, CMP-0026336-1, CMP-0026093-2, CMP-0026088-2, CMP-0026404-1, CMP-0026403-1, CMP-0026027-2, CMP-0026071-2, CMP-0026823-2, CMP-0026578-1, CMP-0026915-2, CMP-0026857-4, CMP-0026227-1, CMP-0026938-4, CMP-0026882-2, CMP-	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R66, R67, R68, R69, R70, R71, R72, R73, R74, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R100, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R145, R146, R147, R148, R149, R175, R177, R179, R180, R181, R182, R183, R209, R212, R213, R214, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R242, R243, R244, R245, R246, R247, R248, R249, R250, R251, R252, R253, R254, R255, R256, R257, R258, R259, R260, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R278, R279, R280, R281, R282, R283, R284, R285, R286, R287, R288, R289, R290, R291, R292, R293, R294, R295,	RES, 0, 5%, 0.063 W, 0402, RES, 10 k, 5%, 0.063 W, 0402, RES, 11 k, 5%, 0.063 W, 0402, RES, 86.6 k, 1%, 0.063 W, 0402, RES, 12 k, 5%, 0.063 W, 0402, RES, 16 k, 5%, 0.063 W, 0402, RES, 4.99 k, 1%, 0.063 W, 0402, RES, 3.57 k, 1%, 0.063 W, 0402, RES, 1.69 k, 1%, 0.063 W, 0402, RES, 1.50 k, 1%, 0.063 W, 0402, RES, 49.9, 1%, 0.063 W, 0402, RES, 49.9 k, 1%, 0.063 W, 0402, RES, 15.0 k, 1%, 0.063 W, 0402, RES, 1.00 k, 1%, 0.063 W, 0402, RES, 100 k, 5%, 0.063 W, 0402, RES, 84.5 k, 1%, 0.063 W, 0402, RES, 39 k, 5%, 0.063 W, 0402, RES, 1.6 k, 5%, 0.063 W, 0402, RES, 2.00 k, 1%, 0.063 W, 0402, RES, 4.7 k, 5%, 0.063 W, 0402, RES, 240, 5%, 0.063 W, 0402, RES, 11.0 k, 1%, 0.063 W, 0402, RES, 10.0 k, 0.5%, 0.063 W, 0402, RES, 220, 5%, 0.063 W, 0402, RES, 2.20 k, 1%, 0.063 W, 0402, RES, 33, 5%, 0.063 W, 0402, RES, 10.0, 1%, 0.063 W, 0402, RES, 47 k, 5%, 0.063 W, 0402, RES, 1.0 k, 5%, 0.063 W, 0402, RES, 12.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402, RES, 2.0 k, 5%, 0.063 W, 0402, RES, 47, 5%, 0.063 W, 0402, RES, 680 k, 5%, 0.063 W, 0402, RES, 330 k, 5%, 0.063 W, 0402, RES, 422, 1%, 0.063 W, 0402, RES, 510, 5%, 0.063 W, 0402, RES, 100, 1%, 0.063 W, 0402	462
0402	CRCW04021K27FKED	CMP-0026081-2	R65	RES, 1.27 k, 1%, 0.063 W, 0402	1
2728	CSSH2728FT5L00	CMP-0077959-1	R75, R523	RES, 0.005, 1%, 4 W, AEC-Q200 Grade 0, 2728	2
0402S	CRCW0402100KDHEDP	CMP-0026768-1	R101	RES, 100 k, 0.5%, 0.063 W, 0402	1
0402S	CRCW040236R0JNED	CMP-0026912-3	R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R176, R178, R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R197, R198, R199, R200, R201, R202, R203, R204, R205, R206, R207, R208, R210, R211	RES, 36, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	54
0402S	CRCW04025K76FKED	CMP-0026468-1	R226, R228	RES, 5.76 k, 1%, 0.063 W, 0402	2
0402S	CRCW04022K49FKED	CMP-0026237-1	R234, R236	RES, 2.49 k, 1%, 0.063 W, 0402	2
0201L	Resistor	CMP-0027008-3	R392, R393	RES, 0, 5%, 0.05 W, 0201	2
0603_HV	RT0603BRD0710RL	CMP-0023651-3	R457, R466	RES, 10.0, 0.1%, 0.1 W, 0603	2
0402	S04L50R0FTNCFT	CMP-0025948-2	R538, R539	RES, 50, 1%, 0.125 W, AEC-Q200 Grade 1, 0402	2
0402S	CRCW0402200KJNED	CMP-0026873-2	R557	RES, 200 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	1
SW_TL1105RF	SW_SPST_12_NC_34	CMP-0002300-2	S1, S2, S3	Switch, SPST-NO, Off-Mom, 0.05 A, 12 VDC, TH	3
SW_TDA06H0SB1	SW_6SPST	CMP-0002278-1	S4	DIP Switch, SPST, 6Pos, Slide, SMT	1
Keystone5001	5001	CMP-0055138-1	TP32, TP43, TP71, TP75	Test Point, Miniature, Black, TH	4
CTFBGA-80	LIA-MD6000-6JMG80	CMP-0077872-1	U1, U5, U9, U11	CrossLink Automotive Family, FBGA-80	4
DBV0005A_N	LP5907	CMP-0077858-1	U2, U6	Automotive 250mA Ultralow-Noise Low-IQ LDO, DBV0005A (SOT-23-5)	2
DRV0006A	TI-TPS62262DRV6-1600X1000TP	CMP-0037845-4	U3, U7	Buck Step Down Regulator with 2 to 6 V Input and 1.2 V Output, -40 to 85 degC, 6-Pin SON (DRV), Green (RoHS & no Sb/Br)	2
SOP-8_200MIL	MX25L12835FM2I-10G	CMP-0082306-1	U4, U8, U10, U12	3V 128M-BIT [x 1/x 2/x 4] CMOS MXSMIO (SERIAL MULTI I/O) FLASH MEMORY, SOP-8	4
RTE0016F	TPS57112QRTERQ1	CMP-0067076-2	U13	Automotive 2.95V to 6V Input, 2A, 2MHz Synchronous Step-Down SWIFT(TM) DCDC Converter, RTE0016F (WQFN-16)	1
DRC0010J	TPS51200AQDRCRQ1	CMP-0860895-1	U14	Sink and Source DDR Termination Regulator, DRC0010J (VSON-10)	1
RGW0020A	TPS74801RGW	CMP-0066853-3	U15, U16	Automotive Catalog Single Output LDO, 1.5A, Adj. (0.8 to 3.6V), Programmable Soft-Start, RGW0020A (VQFN-20)	2
DGK0008A_N	LM74610	CMP-0076397-1	U17	Zero Iq Reverse Polarity Protection Smart Diode Controller, DGK0008A (VSSOP-8)	1
DAP0038B_N	TPS43350-1	CMP-0067265-1	U18	Automotive Low Iq Dual Synchronous Buck Controller with Frequency Spread Spectrum, DAP0038B (TSSOP-38)	1
SOT-23-8	LTC2950ITS8-1#TRMPBF	CMP-0077901-1	U19	Pushbutton On/Off Controller, SOT-23-8	1
ZWS0169A	O9039A387IZWSRQ1	CMP-0077865-3	U20	Automotive 3.15V to 5.5V, 7 Buck & 6 LDO Power Management IC (PMIC) for ARM Cortex A15 Processors, ZWS0169A (NFBGA-169)	1
DSG0008B	TPS22965TDSGRQ1	CMP-0073678-3	U21	5.5V, 4A, 16mΩ Automotive Load Switch With Adjustable Rise Time and Optional Quick Output Discharge, DSG0008B (WSON-8)	1
ABC0760A	XS777BXGABC	CMP-0077950-1	U22	ADAS Applications Processor, ABC0760A (FCBGA-760)	1
DCK0005A_N	SN74LVC1G08DCKT	CMP-0051559-3	U23, U24	Single 2-Input Positive-AND Gate, DCK0005A, SMALL T&R	2
FP-AS4C512M16D3L-12BIN_FBGA96-IPC_A	AS4C512M16D3L-12BIN	CMP-0087696-2	U25, U26, U27, U28, U29	SDRAM - DDR3L Memory IC 8Gb (512M x 16) Parallel 800MHz 13.75ns 96-FBGA (14x9)	5
RGZ0048B	DP83867IRRGZR	CMP-0076014-2	U30	Gigabit Ethernet PHY Customized for Harsh Industrial Environments, RGZ0048B (VQFN-48)	1
DBV0005A_N	SN74LVC1G08DBVR	CMP-0051588-2	U31	Single 2-Input Positive-AND Gate, DBV0005A, LARGE T&R	1
DQA0010A	TPD4E05U06	CMP-0073599-2	U32, U33	Automotive 4-Channel ESD Protection Solution for SuperSpeed (up to 5 Gbps) Interface, DQA0010A (USON-10)	2
PW0024A_N	TI-TPD12S016-TSSOP_PW-24	CMP-0043129-1	U34	Value-Line HDMI Companion Chip for Portable Applications, 12 Channels, -40 to +85 degC, 24-pin TSSOP (PW), Green (RoHS & no Sb/Br)	1
DSG0008B	TPS22965DSG	CMP-0073676-2	U35	5.5V, 4A, 16mΩ Automotive Load Switch With Adjustable Rise Time and Optional Quick Output Discharge, DSG0008B (WSON-8)	1
PW0016A_N	SN74LV4052A-Q1	CMP-0066257-1	U36, U37, U46	Automotive Catalog Dual 4-Channel Analog Multiplexer/Demultiplexer, PW0016A (TSSOP-16)	3
SOIC-16	MT25QL01GBBB8ESF-0SIT	CMP-0077939-2	U38	3V, Multiple I/O, 4KB, 32KB, 64KB Sector Erase, SOIC-16	1
DBV0006A_N	TPS3808G09DBVR	CMP-0032362-1	U39, U40	Low Quiescent Current, Programmable-Delay Supervisory Circuit, 1 Supply Monitored, -40 to 125 degC, 6-pin SOT-23 (DBV), Green (RoHS & no Sb/Br)	2
DRL0005A	TI-TPD2E001-SOT_DRL-5	CMP-0043127-2	U41, U42, U43, U44	Automotive Catalog Low-Capacitance + / - 15 kV ESD-Protection Array for High-Speed Data Inter, 2 Channels, -40 to +85 degC, 5-pin SOT (DRL), Green (RoHS & no Sb/Br)	4
PW0024A_N	TCA9539PW	CMP-0065792-1	U45	Automotive Low-Voltage 16-Bit I2C and SMBus Low-Power I/O Expander, PW0024A (TSSOP-24)	1
LQFP64_N	FT2232H	CMP-0004796-1	U47	Dual High Speed USB To Multipurpose UART/FIFO IC, LQFP-64	1
DBV0005A_N	TPS73633MDBVREP	CMP-0036868-2	U48	Enhanced Product Cap-Free, Nmos, 400-Ma Low-Dropout Regulator W/ Reverse Current Protection, DBV0005A (SOT-23-5)	1
DGS0010A_N	TPD2S701QDGSRQ1	CMP-0013329-2	U49	Automotive USB 2-Ch Data Line Short-to-Battery, Short-to-VBUS, and IEC ESD protection, DGS0010A (VSSOP-10)	1
RSV0016A	SN74AVC4T245RSV	CMP-0066450-1	U50	4-Bit Dual-Supply Bus Transceiver with Configurable Voltage-Level Shifting and 3-State Outputs, RSV0016A (UQFN-16)	1
SOT-23-6	93LC46BT-I-OT	CMP-0005246-2	U51	1K Microwire Compatible Serial EEPROM, SOT-23-6	1
DBV0005A_N	TPS2065D	CMP-0074278-2	U52	Current-Limited, Power-Distribution Switches, DBV0005A (SOT-23-5)	1
DBV0005A_N	SN74LV1T34DBVR	CMP-0051712-2	U53	Single Power Supply BUFFER Logic Level Shifter (no enable), DBV0005A, LARGE T&R	1
DBV0005A_N	SN74LVC1G04DBVR	CMP-0051683-2	U54	Single Inverter, DBV0005A, LARGE T&R	1
DGV0056A_N	SN74CBT16212CDGVR	CMP-0077854-1	U55, U57, U62, U64	24-Bit Bus-Exchange Switch with -2V Undershoot Protection, TVSOP-56, DGV0056A (TVSOP-56)	4
DCK0005A_N	SN74LVC1G04DCKR	CMP-0051684-2	U56, U63	Single Inverter, DCK0005A, LARGE T&R	2
DBV0005A_N	SN74LVC1G125DBVT	CMP-0051316-2	U58, U65	Single Bus Buffer Gate With 3-State Outputs, DBV0005A, SMALL T&R	2
DGV0016A_N	SN74CBTLV3257DGV	CMP-0076547-1	U59, U66, U67	Low-Voltage 4-Bit 1-Of-2 FET Multiplexer/Demultiplexer, DGV0016A (TVSOP-16)	3
RGY0020A	TI-SN74XXXXXQ245XKRGY0020A-20	CMP-0048585-2	U60, U61	Octal Bus Transceiver With 3-State Outputs, RGY0020A, LARGE T&R	2
DCU0008A_N	PCA9306IDCURQ1	CMP-0043322-2	U68	Automotive Dual Bidirectional I2C Bus and SMBus Voltage-Level Translator, DCU0008A (VSSOP-8)	1
DCK0005A_N	SN74LVC1G07DCKR	CMP-0051390-2	U69	Single Buffer/Driver With Open-Drain Output, DCK0005A, LARGE T&R	1
SOIC-8	CAT24C256WI-GT3	CMP-0005313-2	U70	256 kb I2C CMOS Serial EEPROM, SOIC-8	1
Abracon_ABM8AIG	ABM8AIG-16.384MHZ-12-22-T3	CMP-0077944-3	Y1	Crystal, 16.384 MHz, 12 pF, AEC-Q200 Grade 1, SMD	1
ABRACON_ABM3B	ABM3B-20.000MHZ-B2-T	CMP-0004591-3	Y2, Y3	Crystal, 20 MHz, 18pF, SMD	2
XTAL_ABS07	ABS07-32.768KHZ-T	CMP-0004628-3	Y4	CRYSTAL, 32.768KHz, 12.5PF, SMD	1
Abracon_ABM8AIG	ABM8AIG-25.000MHZ-12-22-T3	CMP-0004682-5	Y5	Crystal, 25 MHz, 12pF, AEC-Q200 Grade 1, SMD	1
Kyocera_CX3225CA	CX3225CA12000D0HSSCC	CMP-0082230-1	Y6	Crystal, 12 MHz, 8 pF, AEC-Q200 Grade 1, SMD	1
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Approved | **Notes**