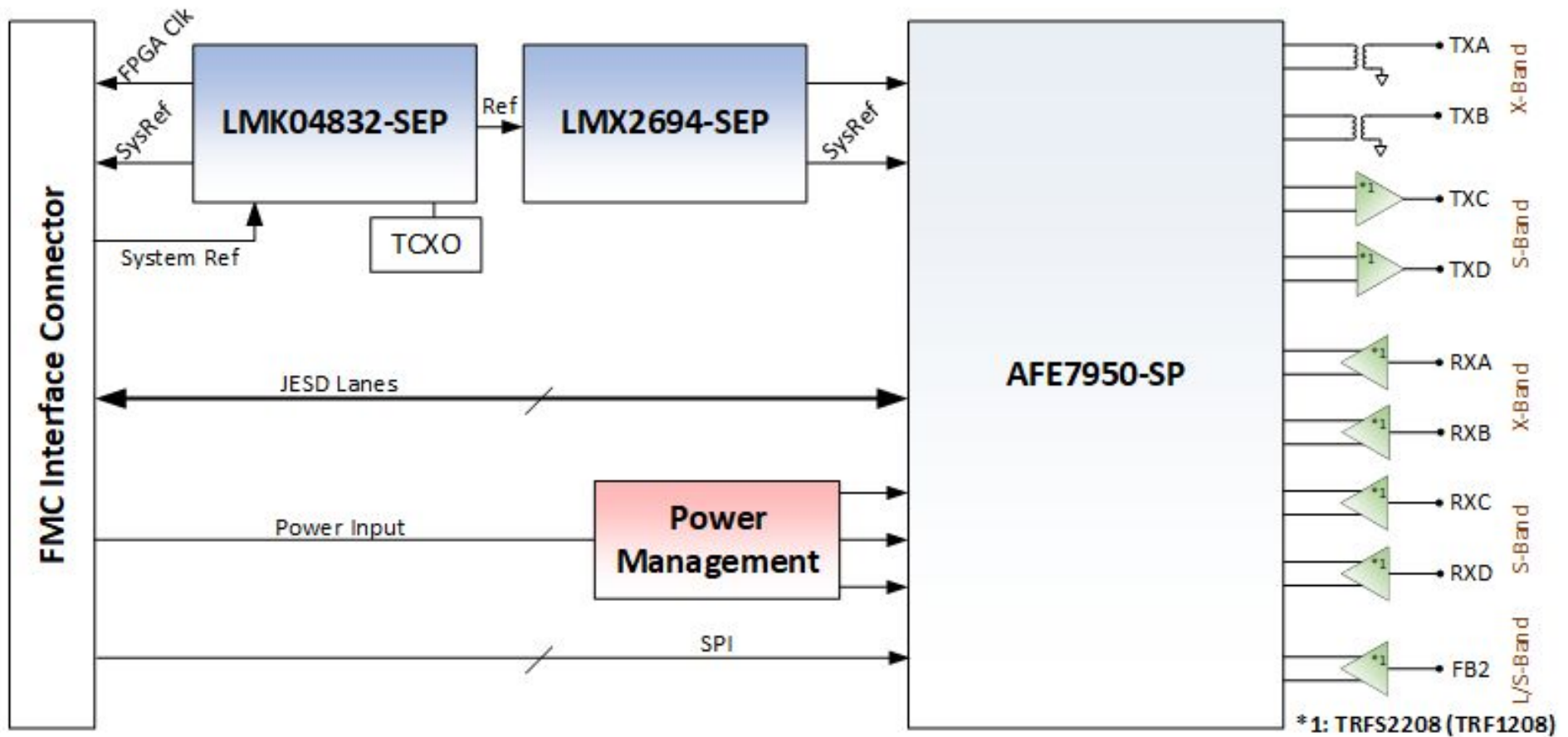
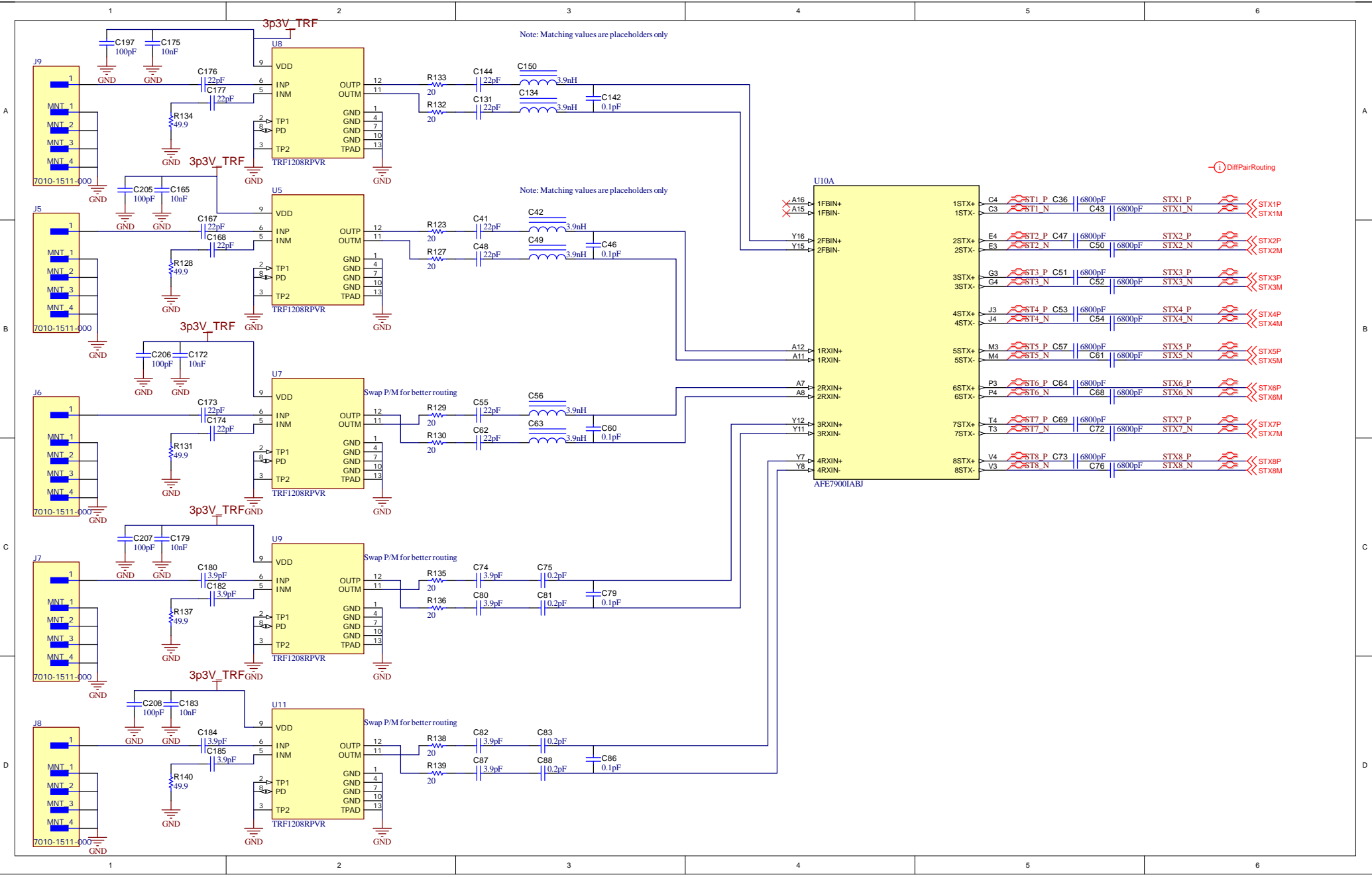
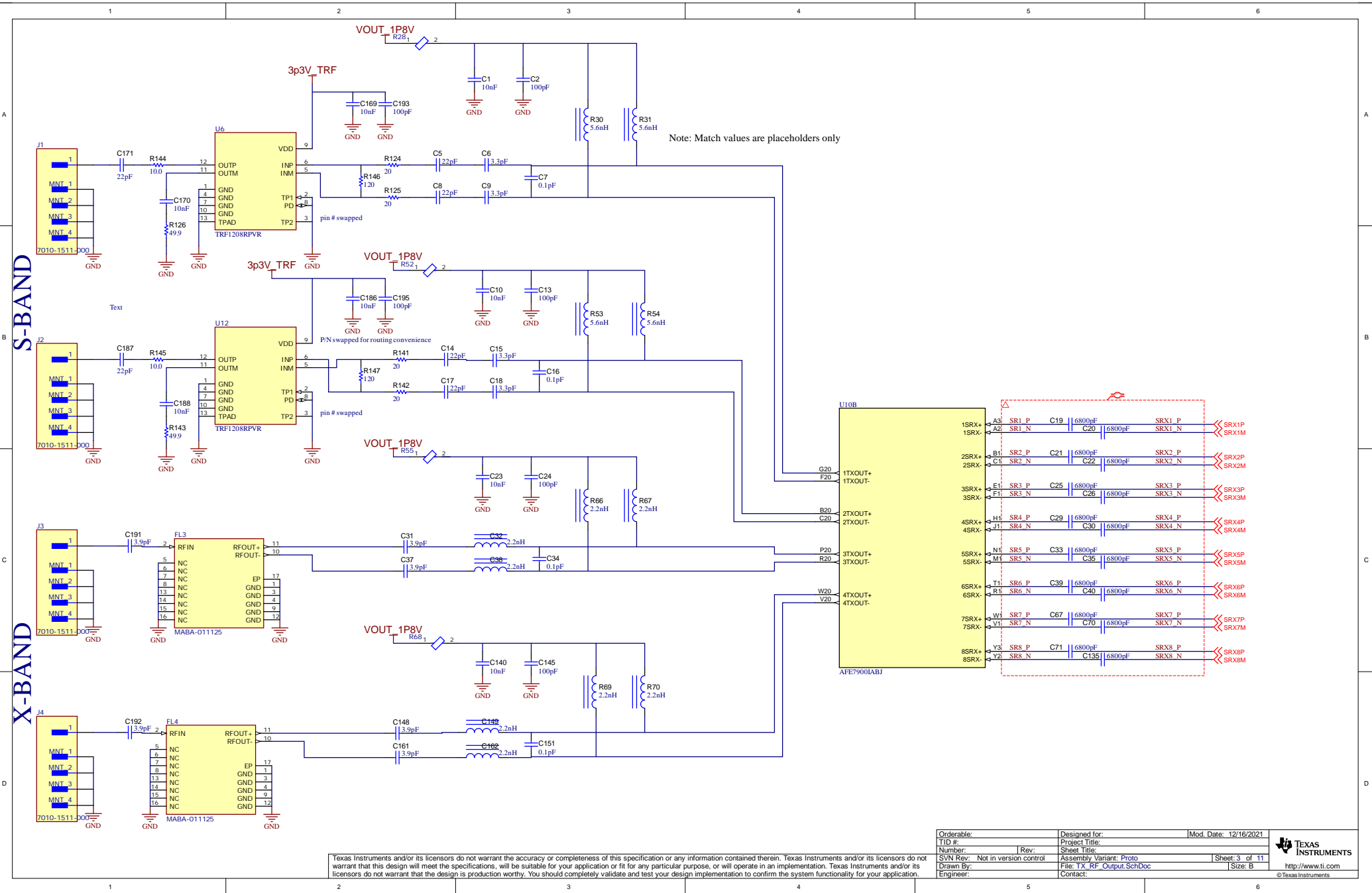


AFE7950-SP

4T4R1F Reference Design



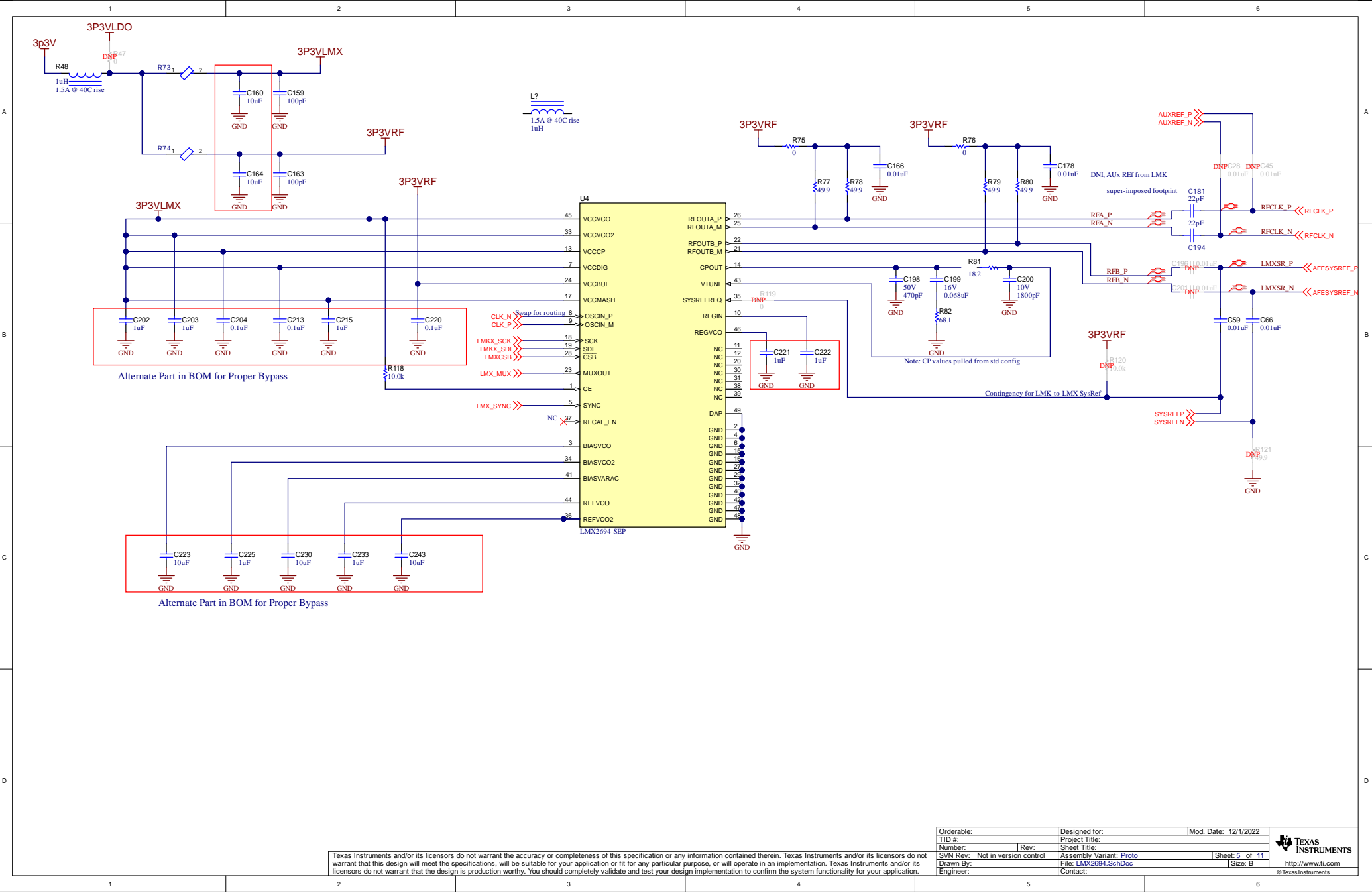




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Drawn By:	File: TX_RF_Output_SchDoc	Size: B
Engineer:	Contact:	

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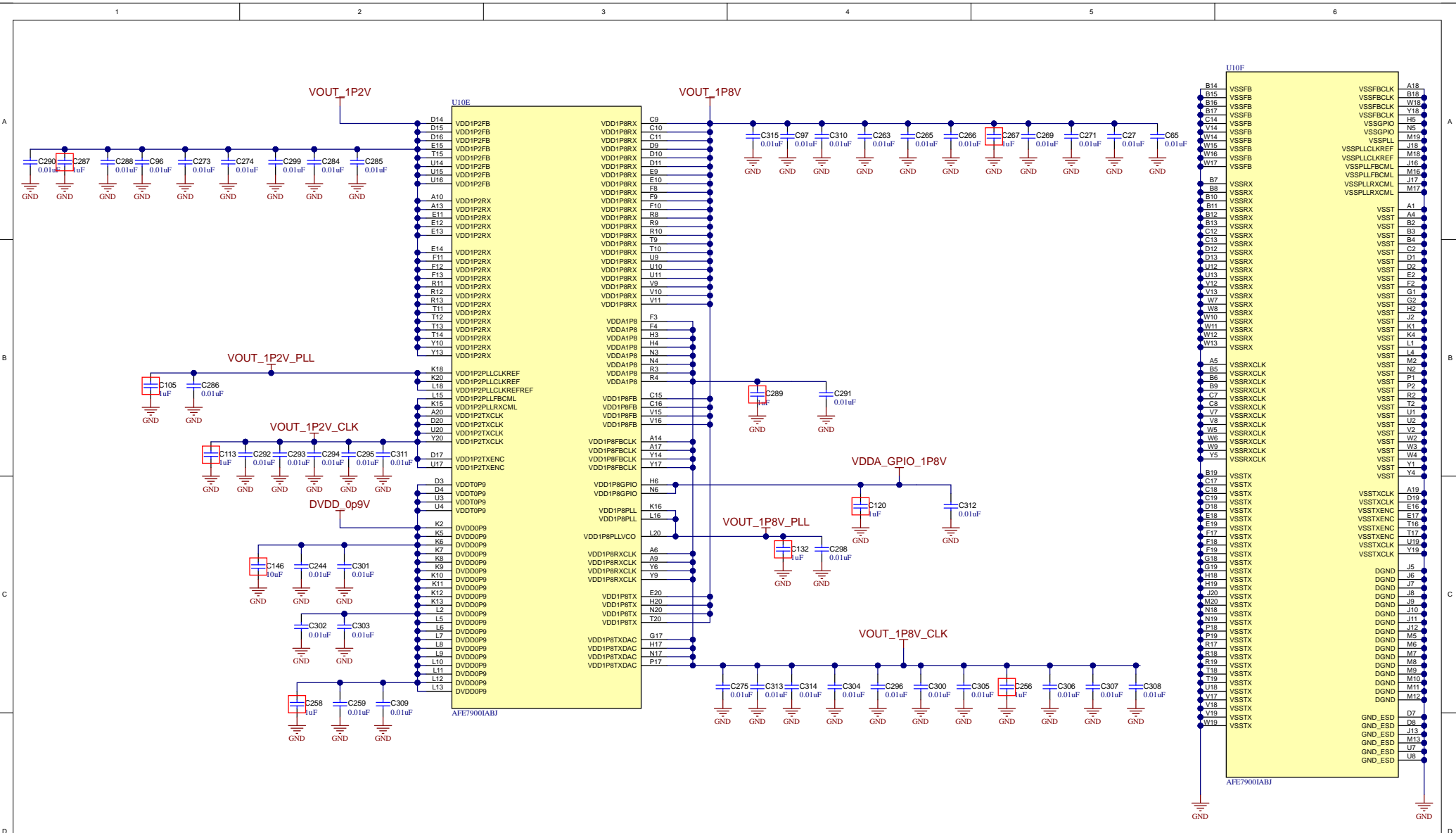


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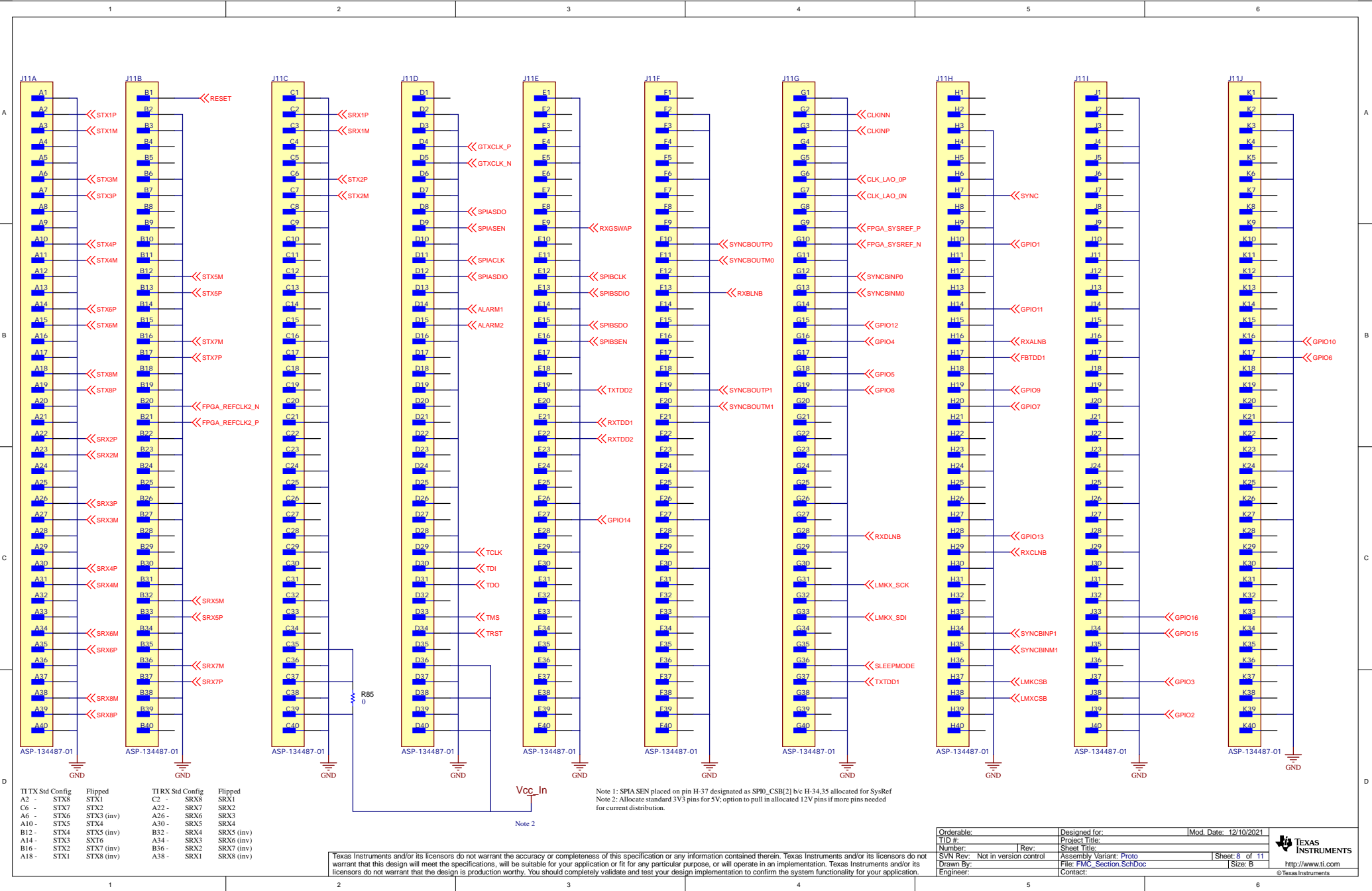


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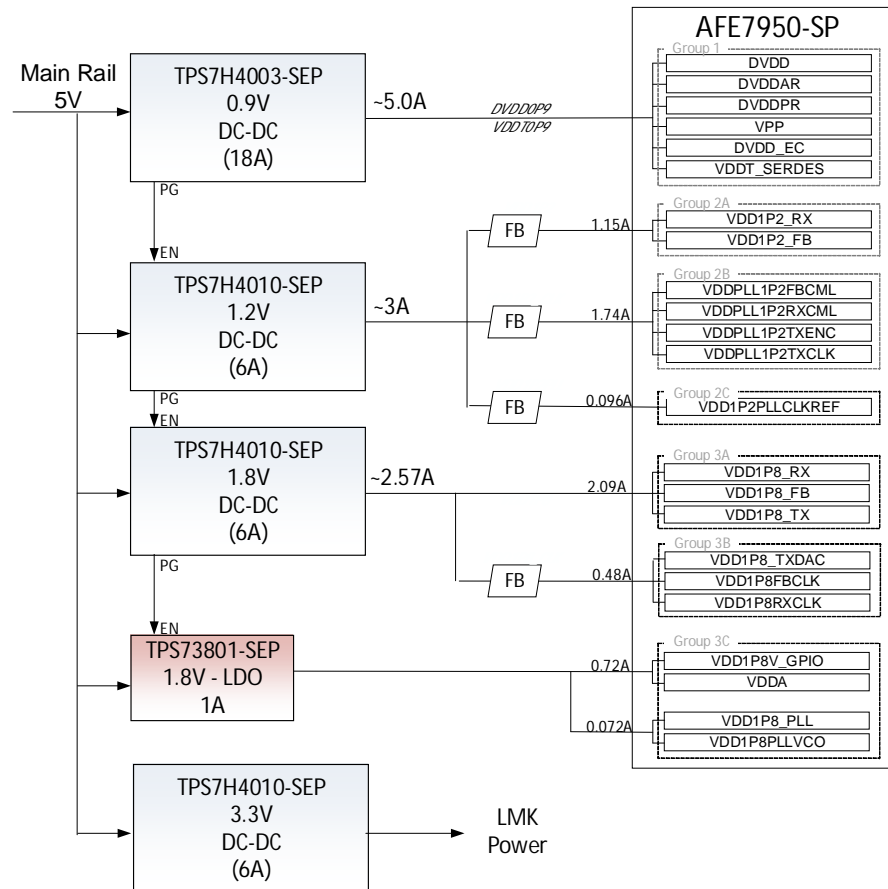
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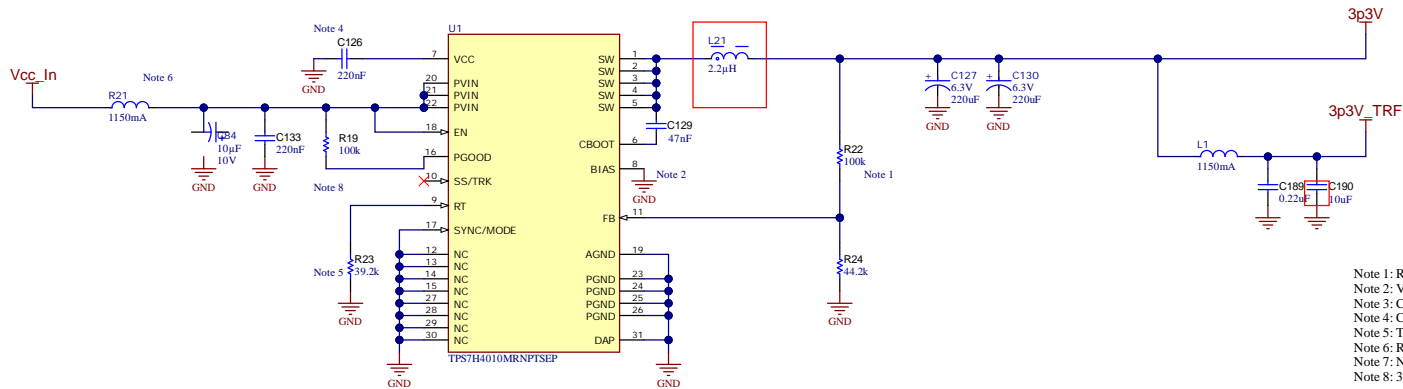

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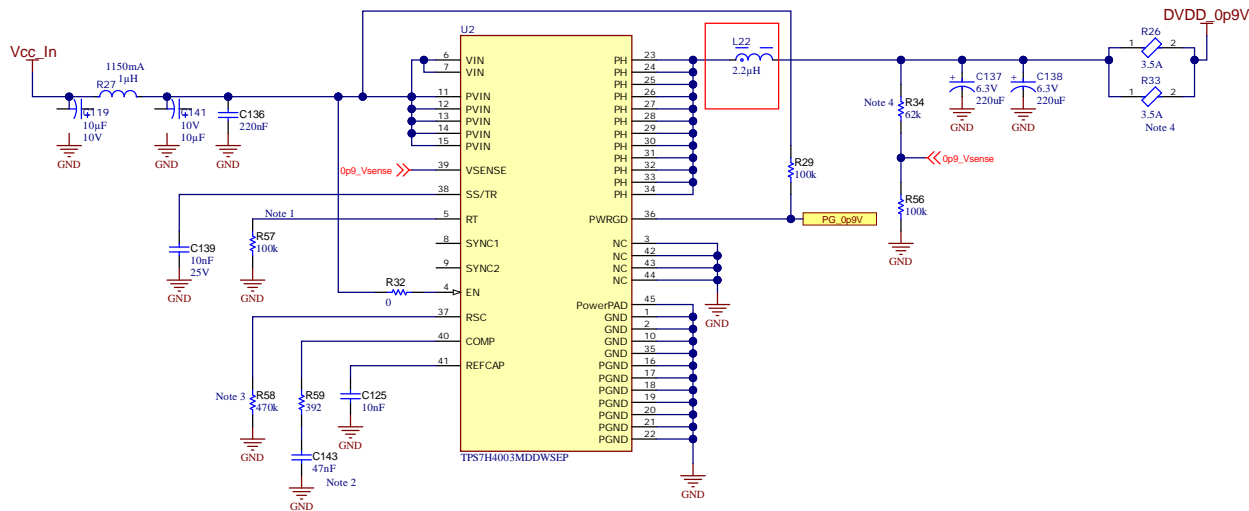
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SVN Rev: Not in version control	Assembly Variant: Proto	File: PowerBlockDiagram.SchDoc
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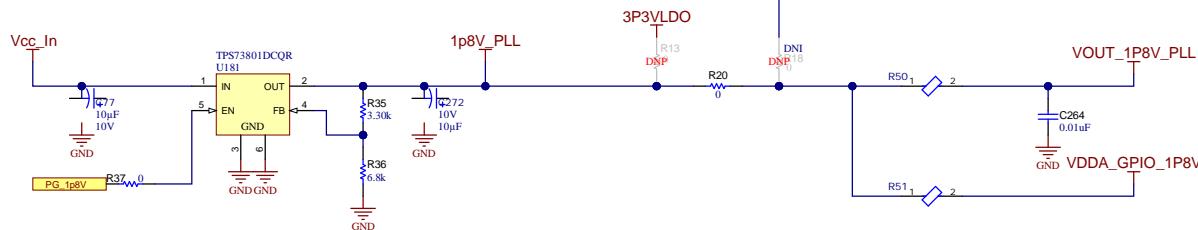
- Note 1: RFBT low enough that no CFF needed
 Note 2: Vout < 3.3V; Vbias not used; tied to ground
 Note 3: CBoot recommended 47 nF
 Note 4: CVcc recommended 2.2 uF; use 220 nF based on MIL availability
 Note 5: Target Fsw = 1 MHz
 Note 6: R/L/FB + C provides RC/LC filtering of any noise/spurs to infecting Vcc supply from DC-DC
 Note 7: Null
 Note 8: 3.3V PGOOD not used for anything but placeholder applied



- Note 1: 100 kohm FSW 765 kHz; max for low Vout
 Note 2: Comp Filter ideal given FSW: 370 ohm, 45 nF
 Note 3: Rough value for RSC resistor
 Note 4: Increase from 51k to 62k corresponding to 0.912V to 0.978V to account for FB voltage drop

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