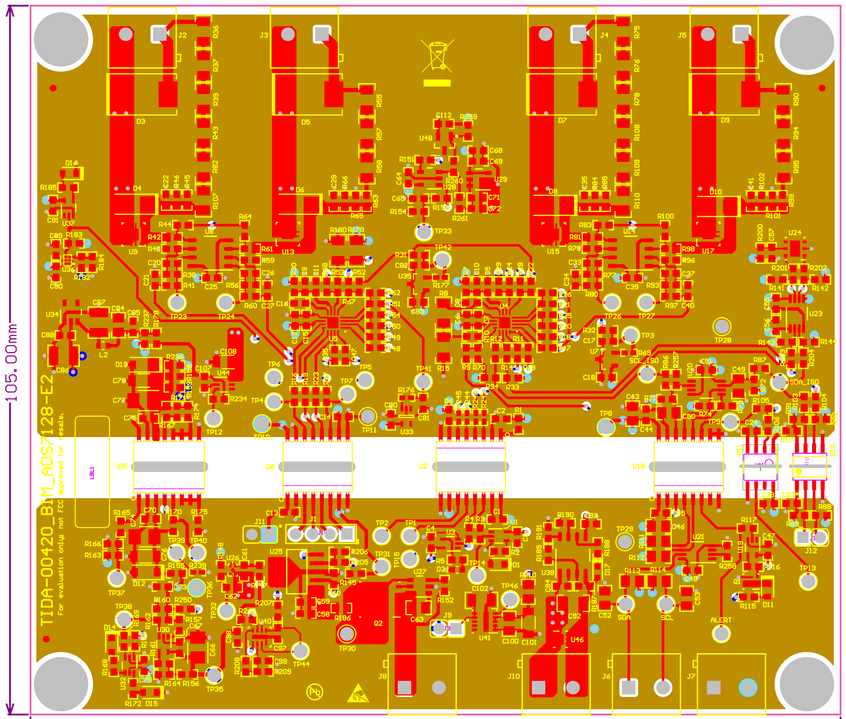
ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4 High Tg	20.00mil	4.2	
5	GND	Copper	1.40mil		
6	Dielectric2	FR-4 High Tg	17.00mil	4.8	
7	PWR	Copper	1.40mil		
8	Dielectric 3	FR-4 High Tg	20.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANTS [No Variations]

ALL VIAS ARE TENTED EXCEPT THERMAL VIAS
THIS IS NOT AN IMPEDENCE CONTROLLED BOARD

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 5.90 MIL EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 63 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[ ] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: TIDA-00420_BIM_ADS7128

DESIGNED FOR: PUBLIC RELEASE

FILE NAME: TIDA-00420_BIM_ADS7128.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE | BOARD #: TIDA-00420_BIM_ADS7128 | REV: E2 | SUN REV: Not In VersionControl

LAYER NAME = Top Overlay,Top Solder,Top Layer,Dielectric 1,GND,Dielectric2,PWR,Dielectric 3,Bottom Layer,Bottom

TID #: 00420

PLOT NAME = Multilayer Composite Print

GENERATED : 3/8/2021 4:05:32 PM

TEXAS INSTRUMENTS

ENGINEER: SREENIVASA KALLIKUPPA

LAYOUT BY: Avinash N

SCALE: 1.00

ALTIUM DESIGNER VERSION: 18.1.9.240