PSM Power Entry Terminal

600V, 60A Screw Terminal Block

TERMINAL_L

TERMINAL_VCC

J1
2A
2
1A
1
0399100102

D3
CDSOD323-T15SC
15V

C9
0.1µF
X7R
100V

R9
DNP
0

T1
SRF0905-472Y

R10
DNP
0

C10
1µF
X7R
25V

R11
1.0k

D4
Green
2.1V

J5
1
2

GND
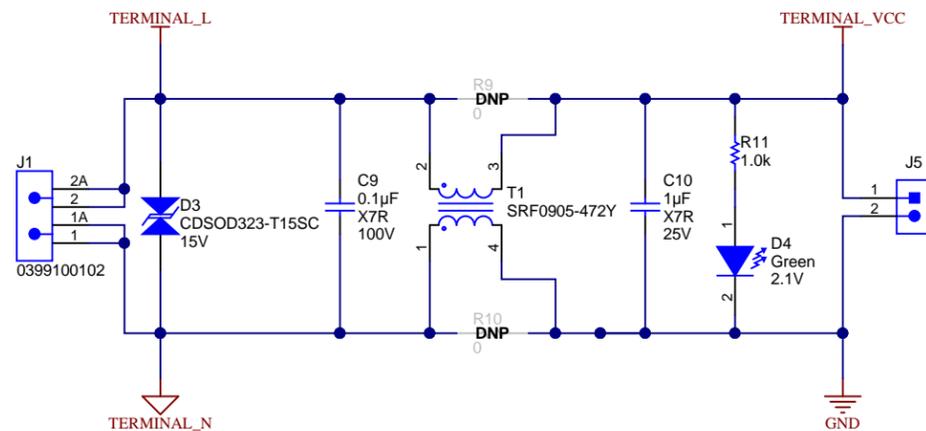
TERMINAL_N

NOTE: T1 is a provision for a common mode choke. If populating T1, do not populate R9 and R10.
If not populating T1, populate R9 and R10 to bypass T1.

NOTE: TERMINAL_N connects to a dedicated EMC ground plane to provide a capacitive coupling plane to reference ground.
TVS diode D3 clamps TERMINAL_L to the EMC ground plane and, ultimately, the TERMINAL_N return pin.

NOTE: Common mode choke T1 is placed after the TVS diode D3 to protect it from high voltage transients due to ESD or EFT events.

NOTE: Capacitor C9 works with the TVS diode clamp to prevent high-frequency transients on the input rail.

NOTE: Capacitor C10 provides smoothing of the input rail after the TVS clamp and common mode choke.

PSM Isolated IO Terminal

This terminal provides access to a UART port to communicate with the CSM.
The UART interface is isolated, and a 2.8V to 5V rail must be provided.

NOTE: TVS protection diodes U3, U4, and U6 make up the primary ESD clamp in the IO domain.

NOTE: Resistors R3/R4 form a low pass filter with capacitors C2/C3, with a cutoff frequency of approximately 3 MHz.

NOTE: LED D2 indicates that the isolated (terminal) side of the IO domain is powered.

J2

IO_VCC

IO_TXD
IO_RXD

U3 TPD1E10B06DPYR
U4 TPD1E10B06DPYR
U6 TPD1E10B06DPYR

R3 51
R4 51

C2 1000pF
C3 1000pF
C4 0.1µF

R5
120
5%

D2
Green
2.1V

IO_GND

U2
2 OUTA   INA 7
3 INB   OUTB 6
1 VCC1   VCC2 8
4 GND1   GND2 5
ISO7221CD

Isolation

CSM_TXD
CSM_RXD

CSM_VCC

C1
0.1µF

GND

CSM Interface Headers

2x2 0.1 Pitch Header Interface to the Capacitive Sensing Module (CSM)

CSM_VCC
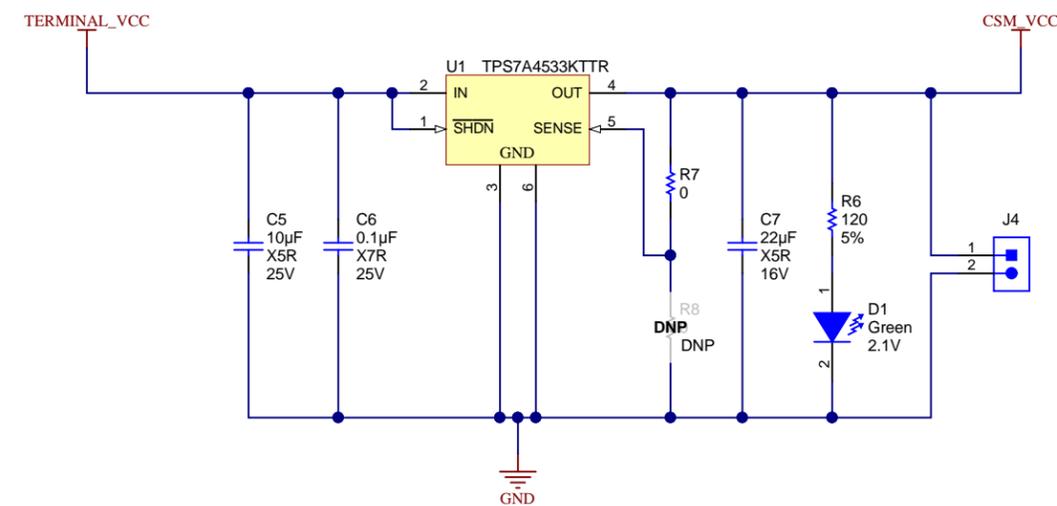
J3
1   2
3   4
CSM_TXD
CSM_RXD

GND
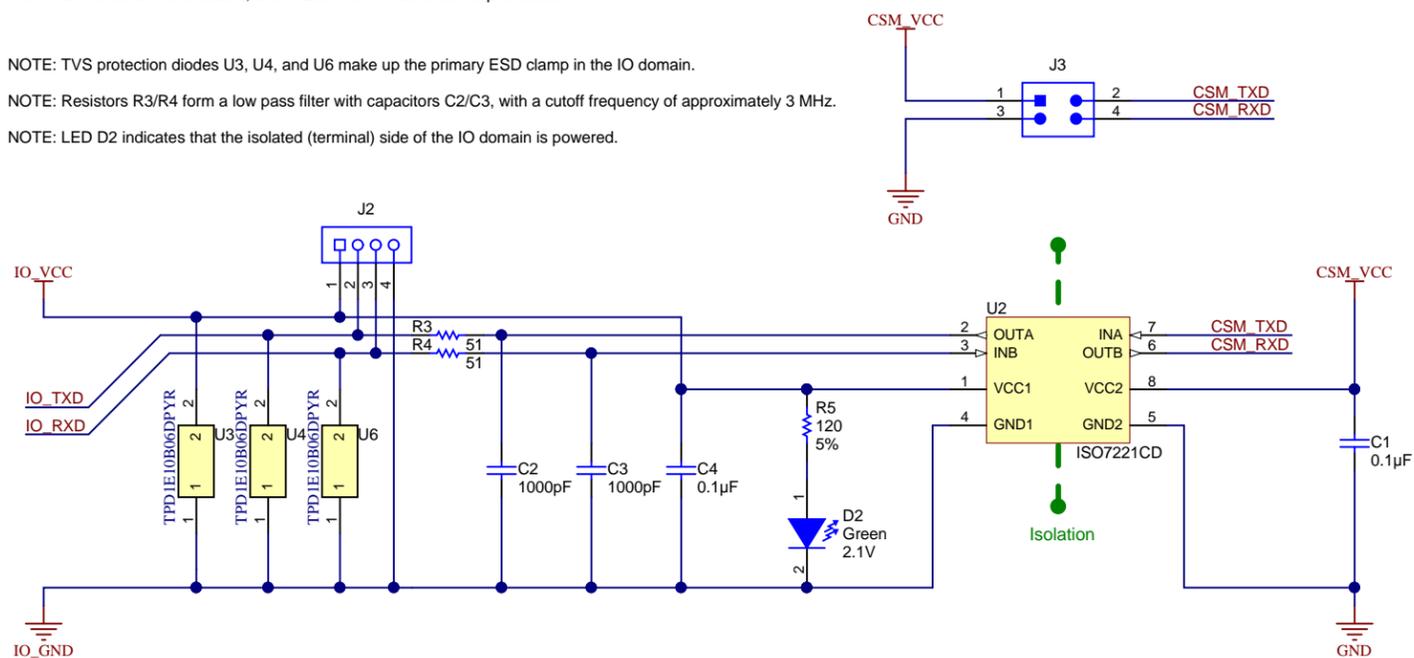
CSM Low Voltage DC Supply

100mA Maximum Drive

Allows for fixed-output or adjustable-output versions of the linear regulator

Supplies CSM and Isolated Communications Block (Internal Side)

NOTE: LED D1 indicates that the CSM is powered.

NOTE: Resistors R7 and R8 form the feedback circuit for the linear regulator U1. For a fixed-ouput regulator, R7 must be a 0-ohm, and R8 must be a DNP.
For an adjustable-output regulator, R7 and R8 may be set as required to achieve the desired output voltage.

TERMINAL_VCC

CSM_VCC

U1 TPS7A4533KTTR
2 IN   OUT 4
1 SHDN   SENSE 5
       GND
3   6

C5
10µF
X5R
25V

C6
0.1µF
X7R
25V

R7
0

R8
DNP
DNP

C7
22µF
X5R
16V

R6
120
5%

D1
Green
2.1V

J4
1
2

GND

PCB
LOGO
Texas Instruments

HS_LABEL1
CAUTION HOT SURFACE

Orderable: No
TID #: TIDM-CAPTOUCHEMCREF
Number: PSM-12VDCTO3P3VDC   Rev: B
SVN Rev: Version control disabled
Drawn By: W. Schnoor
Engineer: Walter Schnoor

Designed for: Public Release
Project Title: Noise Tolerant Capacitive Touch HMIs
Sheet Title: Schematic
Assembly Variant: With Choke
File: PSM-12VDCTO3P3VDC.SchDoc

Mod. Date: 5/26/2016

Sheet: 1 of 1
Size: B