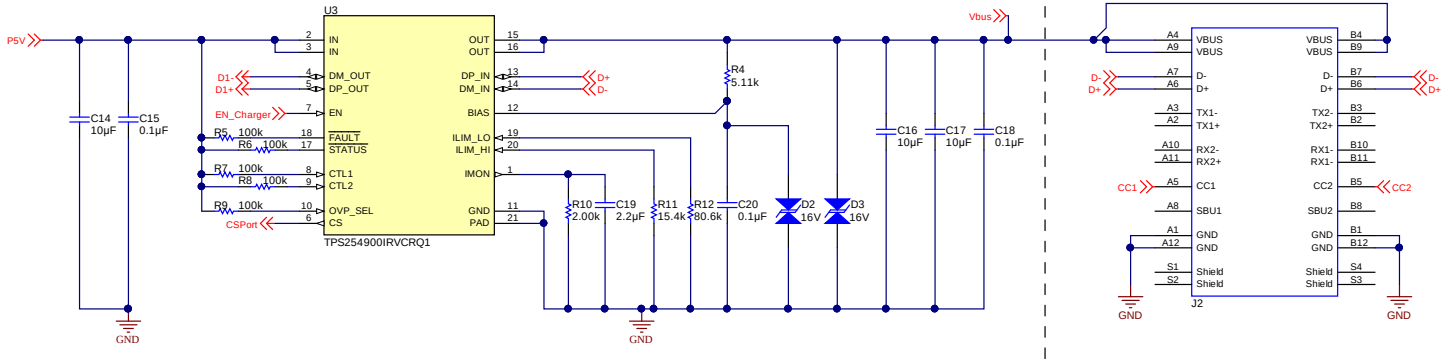
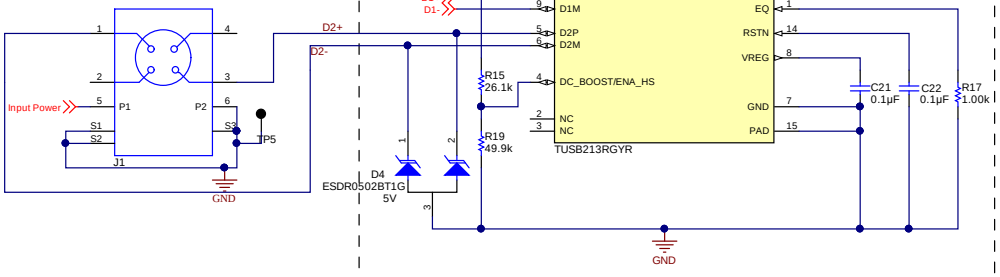
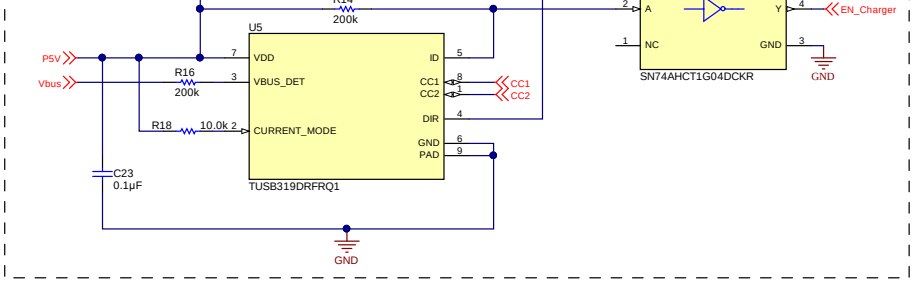
## TPS254900 - Legacy BC1.2 Controller




## TUSB213 - USB 2.0 Redriver with DC Boost



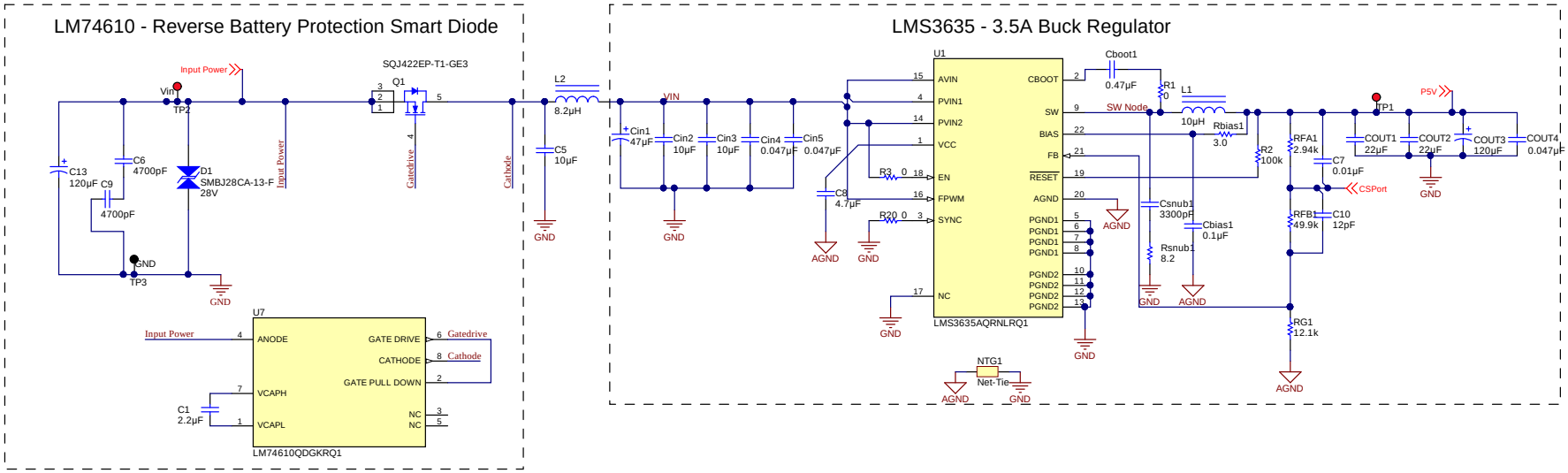

## TUSB319 - USB Type-C Negotiator






| | | | |
|---|---|---|---|
| Orderable: EVM_orderable | | Designed for:Not for Public Release | Mod. Date: 7/10/2017 |
| TID #: N/A | | Project Title:TIDA-01432 | |
| Number: TIDA-01432 | Rev: E1 | Sheet Title: | |
| EVM Rev: Version control disabled | | Assembly Variant:[No Variations] | Sheet:1 of 3 |
| Drawn By: | | File: TIDA-01432 E1 Schematic.SchDoc | Size: B |
| Engineer: H.Bovenzi | | Contact: http://www.ti.com/support | |

Texas Instruments
http://www.ti.com




| | | | |
|---|---|---|---|
| Orderable: EVM_orderable | | Designed for:Not for Public Release | Mod. Date: 6/7/2017 |
| TID #: N/A | | Project Title:TIDA-01432 | |
| Number: TIDA-01432 | Rev: E1 | Sheet Title: | |
| SVN Rev: Version control disabled | | Assembly Variant:[No Variations] | Sheet:2 of 3 |
| Drawn By: | | File: TIDA-01432 E1 Power Schematic.SchDoc | Size: B |
| Engineer: H.Bovenzi | | Contact: http://www.ti.com/support | |

FID1 FID2 FID3 FID4

PCB Number: TIDA-01432
PCB Rev: E1

PCB LOGO
Texas Instruments

PCB LOGO
Pb-Free Symbol

PCB LOGO
FCC disclaimer


HOTSURFACE

| Variant/Label Table | |
|---|---|
| Variant | Label Text |
| 001 | TIDA-01432 |
| | |
| | |
| | |
| | |
| | |
| | |

LBL1
PCB Label
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



| | | | |
|---|---|---|---|
| Orderable: EVM_orderable | | Designed for:Not for Public Release | Mod. Date: 7/24/2017 |
| TID #: N/A | | Project Title:TIDA-01432 | |
| Number: TIDA-01432 | Rev: E1 | Sheet Title: | |
| EVM Rev: Version control disabled | | Assembly Variant:[No Variations] | Sheet:3 of 3 |
| Drawn By: | | File: TIDA-01432 E1_Hardware.SchDoc | Size: B |
| Engineer: H.Bovenzi | | Contact: http://www.ti.com/support | |

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http://www.ti.com

| Layer | Name | Material | Thickness | Constant | Board Layer Stack |
|---|---|---|---|---|---|
| 1 | Top Overlay | | | | |
| 2 | Top Solder | Solder Resist | 0.40mil | 3.5 | |
| 3 | Top Layer | Copper | 1.40mil | | |
| 4 | Dielectric1 | FR-4 | 6.00mil | 4.8 | |
| 5 | Signal Layer 1 | Copper | 1.40mil | | |
| 6 | Dielectric2 | | 44.00mil | 4.2 | |
| 7 | Signal Layer 2 | Copper | 1.40mil | | |
| 8 | Dielectric 3 | | 6.00mil | 4.2 | |
| 9 | Bottom Layer | Copper | 1.40mil | | |
| 10 | Bottom Solder | Solder Resist | 0.40mil | 3.5 | |
| 11 | Bottom Overlay | | | | |

ZZ1
ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2
ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

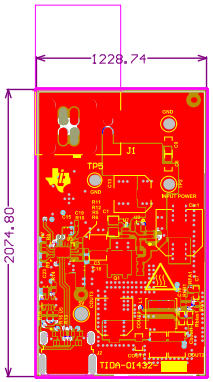
DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 8 MIL
MIN. VIA PAD SIZE: 16 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[X] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER




1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

TEXAS INSTRUMENTS

PROJECT TITLE: TIDA-01432
DESIGNED FOR: Not for Public Release
FILE NAME: TIDA-01432_E1.PcbDoc
ENGINEER: H. Bovenzi
LAYOUT BY: Bovenzi/Clanin
SCALE: 1.00
ALTIUM DESIGNER VERSION: 17.1.5.472