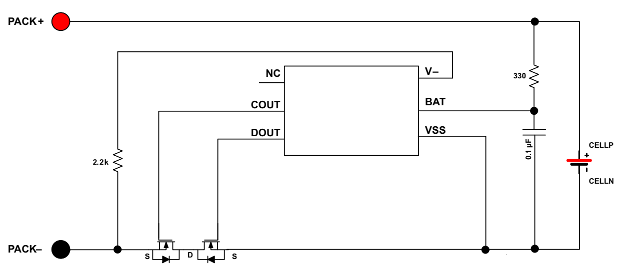
BQ297xx Cost-Effective Voltage and Current Protection Integrated Circuit for Single-Cell Li-Ion and Li-Polymer Batteries

1 Features

- Input voltage range pack+: VSS – 0.3V to 12V
- FET drive:
  – CHG and DSG FET drive output
- Voltage sensing across external FETs for overcurrent protection (OCP) is within ±5mV (typical)
- Fault detection
  – Overcharge detection (OVP)
  – Over-discharge detection (UVP)
  – Charge overcurrent detection (OCC)
  – Discharge overcurrent detection (OCD)
  – Load short-circuit detection (SCP)
- Zero voltage charging for depleted battery
- Factory programmed fault protection thresholds
  – Fault detection voltage thresholds
  – Fault trigger timers
  – Fault recovery timers
- Modes of operation without battery charger enabled
  – NORMAL mode I_{CC} = 4μA
  – Shutdown Iq = 100nA
- Operating temperature range T_A = –40°C to +85°C
- Package:
  – 6-pin DSE (1.50mm × 1.50mm × 0.75mm)



Simplified Schematic

2 Applications

- Tablet PCs
- Mobile handsets
- Handheld data terminals

3 Description

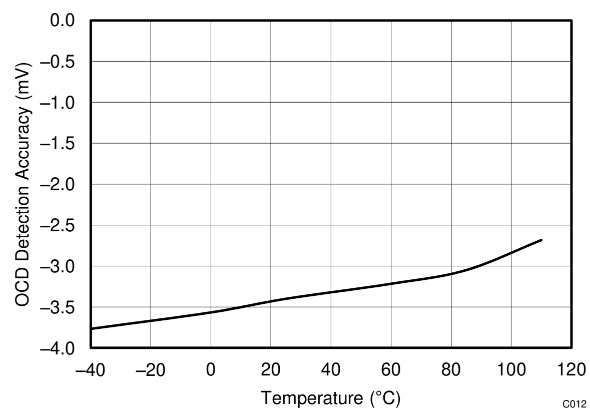
The BQ2970 battery cell protection device provides an accurate monitor and trigger threshold for overcurrent protection during high discharge/charge current operation or battery overcharge conditions.

The BQ2970 device provides the protection functions for Li-ion/Li-polymer cells, and monitors across the external power FETs for protection due to high charge or discharge currents. In addition, there is overcharge and depleted battery monitoring and protection. These features are implemented with low current consumption in NORMAL mode operation.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
BQ2970, BQ2971, BQ2972, BQ2973	WSON (6)	1.50mm × 1.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



OCD Detection Accuracy Versus Temperature

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4 Device Comparison Table

PART NUMBER[(1)]	OVP (V)	OVP DELAY (sec)	UVP (V)	UVP DELAY (ms)	OCC (V)	OCC DELAY (ms)	OCD (V)	OCD DELAY (ms)	SCD (V)	SCD DELAY (µs)
BQ29700	4.275	1.25	2.800	144	–0.100	8	0.100	20	0.5	250
BQ29701	4.280	1.25	2.300	144	–0.100	8	0.125	8	0.5	250
BQ29702	4.350	1	2.800	96	–0.155	8	0.160	16	0.3	250
BQ29703	4.425	1.25	2.300	20	–0.100	8	0.160	8	0.5	250
BQ29704	4.425	1.25	2.500	20	–0.100	8	0.125	8	0.5	250
BQ29705	4.425	1.25	2.500	20	–0.100	8	0.150	8	0.5	250
BQ29706	3.850	1.25	2.500	144	–0.150	8	0.200	8	0.6	250
BQ29707	4.280	1	2.800	96	–0.090	6	0.090	16	0.3	250
BQ29716	4.425	1.25	2.300	20	–0.100	8	0.165	8	0.5	250
BQ29717	4.425	1.25	2.500	20	–0.100	8	0.130	8	0.5	250
BQ29718	4.425	1.25	2.500	20	–0.100	8	0.100	8	0.5	250
BQ29723	4.425	1	2.500	96	–0.060	4	0.100	8	0.3	250
BQ29728	4.280	1.25	2.800	144	–0.100	8	0.150	8	0.5	250
BQ29729	4.275	1.25	2.300	20	–0.100	8	0.130	8	0.5	250
BQ29732	4.280	1.25	2.500	144	–0.100	8	0.190	8	0.5	250
BQ29733	4.400	1.25	2.800	20	–0.100	8	0.120	8	0.3	250
BQ29737	4.250	1	2.800	96	–0.050	16	0.100	16	0.3	250
BQ29740	4.450	1	2.500	96	–0.100	8	0.100	8	0.3	250
BQ297xy	3.85–4.6	0.25, 1, 1.25, 4.5	2.0–2.8	20, 96, 125, 144	–0.045 to –0.155	4, 6, 8, 16	0.090–0.200	8, 16, 20, 48	0.3, 0.4, 0.5, 0.6	250

(1) All of the protections have a recovery delay time. The recovery timer starts as soon as the fault is triggered. The device starts to check for a recovery condition only when the recovery timer expires. This is NOT a delay time between recovery condition to FETs recovery. OVP recovery delay = 12ms; UVP/OCC/OCD recovery delay = 8ms.

5 Pin Configuration and Functions

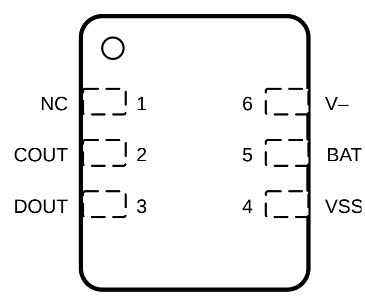


Figure 5-1. DSE Package 6-PIN WSON Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BAT	5	P	VDD pin
COUT	2	O	Gate Drive Output for Charge FET
DOUT	3	O	Gate Drive Output for Discharge FET
NC	1	NC	No Connection (electrically open)
VSS	4	P	Ground pin
V–	6	I/O	Input pin for charger negative voltage

5.1 Pin Descriptions

5.1.1 Supply Input: BAT

This pin is the input supply for the device and is connected to the positive terminal of the battery pack. A 0.1µF input capacitor is connected to ground for filtering noise.

5.1.2 Cell Negative Connection: VSS

This pin is an input to the device for cell negative ground reference. Internal circuits associated with cell voltage measurements and overcurrent protection input to differential amplifier for either Vds sensing or external sense resistor sensing will be referenced to this node.

5.1.3 Voltage Sense Node: V–

This is a sense node used for measuring several fault detection conditions, such as overcurrent charging or overcurrent discharging configured as Vds sensing for protection. This input, in conjunction with VSS, forms the differential measurement for the stated fault detection conditions. A 2.2kΩ resistor is connected between this input pin and Pack– terminal of the system in the application.

5.1.4 Discharge FET Gate Drive Output: DOUT

This pin is an output to control the discharge FET. The output is driven from an internal circuitry connected to the BAT supply. This output transitions from high to low when a fault is detected, and requires the DSG FET to turn OFF. A 5MΩ high impedance resistor is connected from DOUT to VSS for gate capacitance discharge when the FET is turned OFF.

5.1.5 Charge FET Gate Drive Output: COUT

This pin is an output to control the charge FET. The output is driven from an internal circuitry connected to the BAT supply. This output transitions from high to low when a fault is detected, and requires the CHG FET to turn OFF. A 5MΩ high impedance resistor is connected from COUT to Pack– for gate capacitance discharge when FET is turned OFF.

6 Specifications

6.1 Absolute Maximum Ratings

		MIN [1]	MAX	UNIT
Supply control and input	Input voltage: BAT	–0.3	12	V
	V– pin(pack–)	BAT – 28	BAT + 0.3	V
FET drive and protection	DOUT (Discharge FET Output), GDSG (Discharge FET Gate Drive)	VSS – 0.3	BAT + 0.3	V
	COUT (Charge FET Output), GCHG (Charge FET Gate Drive)	BAT – 28	BAT + 0.3	V
	Operating temperature: T_{FUNC}	–40	85	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD} [1]	Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS–001, all pins [2]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [3]	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 1000V can have higher performance.

(3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250V can have higher performance.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Supply control and input	Positive input voltage: BAT	–0.3	8	V
	Negative input voltage: V–	BAT – 25	BAT	V
FET drive and protection	Discharge FET control: DOUT	VSS	BAT	V
	Charge FET control: COUT	BAT – 25	BAT	V
Temperature Ratings	Operating temperature: T_{Amb}	–40	85	°C
	Storage temperature: T_S	–55	150	°C
	Lead temperature (soldering 10s)		300	°C
	Thermal resistance junction to ambient, θ_{JA}		250	°C/W

6.4 Thermal Information

THERMAL METRIC (1)		BQ297xx DSE (WSON) 12 PINS	UNIT
$R_{\theta JA,\ High\ K}$	Junction-to-ambient thermal resistance	190.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	94.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	149.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	152.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 DC Characteristics

Typical Values stated where T_A = 25°C and BAT = 3.6V. Min/Max values stated where T_A = –40°C to 85°C, and BAT = 3V to 4.2V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current consumption						
V_{BAT}	Device operating range	BAT – VSS	1.5		8	V
		BAT – V–	1.5		28	
I_{NORMAL}	Current consumption in NORMAL mode	BAT = 3.8V, V– = 0V		4	5.5	μA
I_{Power_down}	Current consumption in power down mode	BAT = V– = 1.5V			0.1	μA
FET Output, DOUT and COUT						
V_{OL}	Charge FET low output	I_{OL} = 30μA, BAT = 3.8V		0.4	0.5	V
V_{OH}	Charge FET high output	I_{OH} = –30μA, BAT = 3.8V	3.4	3.7		V
V_{OL}	Discharge FET low output	I_{OL} = 30μA, BAT = 2V		0.2	0.5	V
V_{OH}	Discharge FET high output	I_{OH} = –30μA, BAT = 3.8V	3.4	3.7		V
Pullup Internal Resistance on V–						
$R_{V–D}$	Resistance between V– and VBAT	V_{BAT} = 1.8V, V– = 0V	100	300	550	kΩ
Current sink on V–						
$I_{V–S}$	Current sink on V– to VSS	V_{BAT} = 3.8V	8		24	μA
Load short detection on V–						
V_{short}	Short detection voltage	V_{BAT} = 3.8V and R_{PackN} = 2.2kΩ		V_{BAT} – 1V		V

6.5 DC Characteristics (continued)

Typical Values stated where T_A = 25°C and BAT = 3.6V. Min/Max values stated where T_A = –40°C to 85°C, and BAT = 3V to 4.2V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
0V battery charge function						
V_{0CHG}	0V battery charging start voltage	0V battery charging function allowed	1.7			V
0V battery charge inhibit function						
V_{0INH}	0V battery charging inhibit voltage threshold	0V battery charging function disallowed			0.75	V

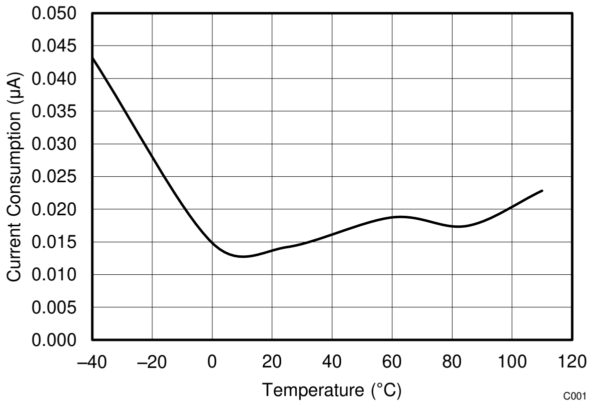
6.6 Programmable Fault Detection Thresholds

PARAMETER		CONDITION		MIN	TYP	MAX	UNIT
V_{OVP}	Overcharge detection voltage	Factory Device Configuration: 3.85V to 4.60V in 50mV steps	T_A = 25°C	–10		10	mV
			T_A = 0°C to 60°C	–20		20	mV
$V_{OVP–Hys}$	Overcharge release hysteresis voltage	100mV and (VSS – V–) > OCC (min) for release, T_A = 25°C		–20		20	mV
V_{UVP}	Over-discharge detection voltage	Factory Device Configuration: 2.00V to 2.80V in 50mV steps, T_A = 25°C		–50		50	mV
$V_{UVP+Hys}$	Over-discharge release hysteresis voltage	100mV and (BAT – V–) > 1V for release, T_A = 25°C		–50		50	mV
V_{OCD}	Discharging overcurrent detection voltage	Factory Device Configuration: 90mV to 200mV in 5mV steps	T_A = 25°C	–10		10	mV
			T_A = –40°C to 85°C	–15		15	mV
Release of V_{OCD}	Release of discharging overcurrent detection voltage	Release when BAT – V– > 1V			1		V
V_{OCC}	Charging overcurrent detection voltage	Factory Device Configuration: –45mV to –155mV in 5mV steps	T_A = 25°C	–10		10	mV
			T_A = –40°C to 85°C	–15		15	mV
Release of V_{OCC}	Release of overcurrent detection voltage	Release when VSS – V– ≥ OCC (min)			40		mV
V_{SCC}	Short Circuit detection voltage	Factory Device Configuration: 300mV, 400mV, 500mV, 600mV	T_A = 25°C	–100		100	mV
V_{SCCR}	Release of Short Circuit detection voltage	Release when BAT – V– ≥ 1V			1		V

6.7 Programmable Fault Detection Timer Ranges

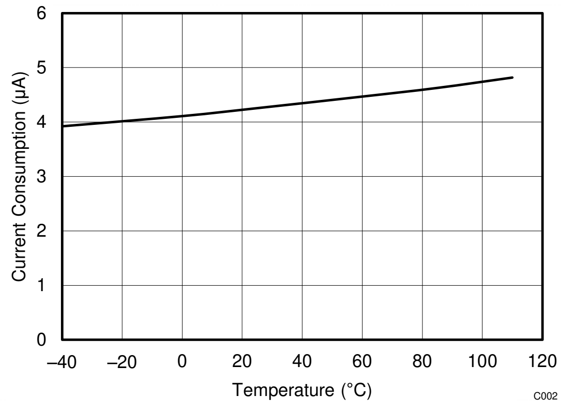
PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
t_{OVPD}	Overcharge detection delay time	Factory Device Configuration: 0.25s, 1s, 1.25s, 4.5s	–20%		20%	s
t_{UVPD}	Over-discharge detection delay time	Factory Device Configuration: 20ms, 96ms, 125ms, 144ms	–20%		20%	ms
t_{OCDD}	Discharging overcurrent detection delay time	Factory Device Configuration: 8ms, 16ms, 20ms, 48ms	–20%		20%	ms
t_{OCCD}	Charging overcurrent detection delay time	Factory Device Configuration: 4ms, 6ms, 8ms, 16ms	–20%		20%	ms
t_{SCCD}	Short Circuit detection delay time	250µs (fixed)	–50%		50%	µs

6.8 Typical Characteristics



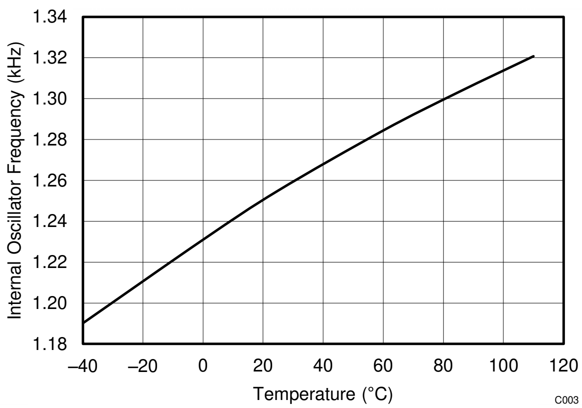
V_{BAT} = 1.5V

Figure 6-1. 1.5V I_{BAT} Versus Temperature



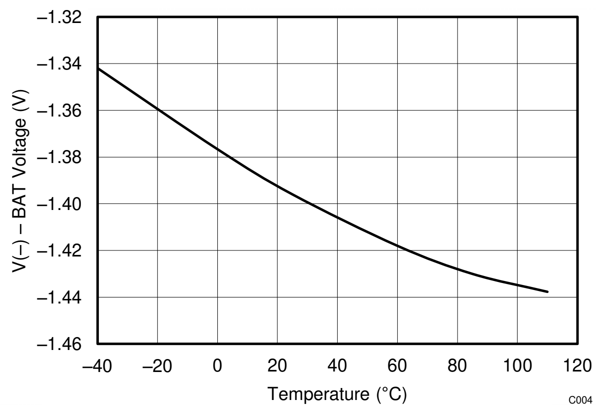
V_{BAT} = 3.9V

Figure 6-2. 3.9V I_{BAT} Versus Temperature



F_{OSC}, Setting = 1.255kHz

Figure 6-3. Internal Oscillator Frequency Versus Temperature



V_{BAT}, Setting = 0V

Figure 6-4. 0V Charging Allowed Versus Temperature

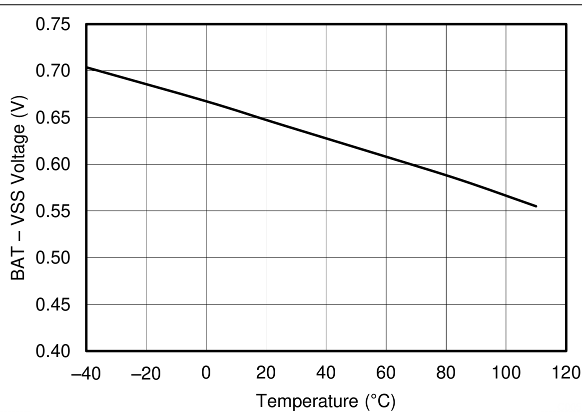
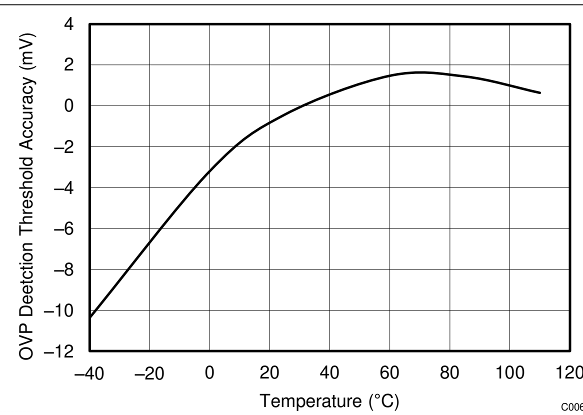
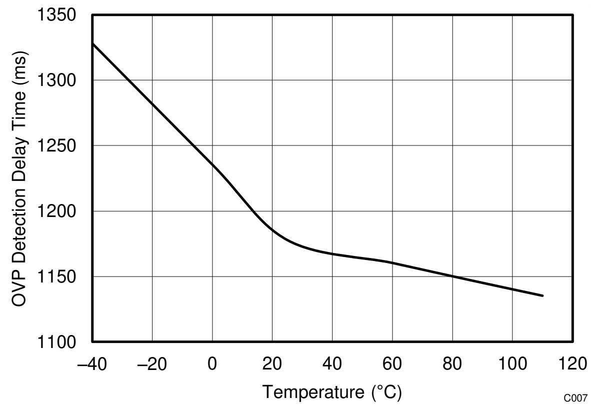


Figure 6-5. 0V Charging Disallowed Versus Temperature



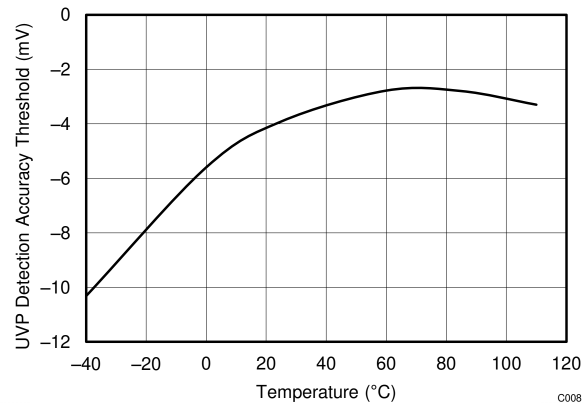
OVP, Setting = 4.275V

Figure 6-6. OVP Detection Accuracy Versus Temperature



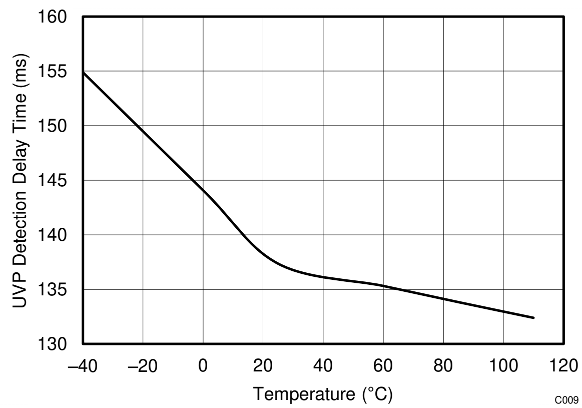
t_{OVPD}, Setting = 1.25s

Figure 6-7. OVP Detection Dely Time Versus Temperature



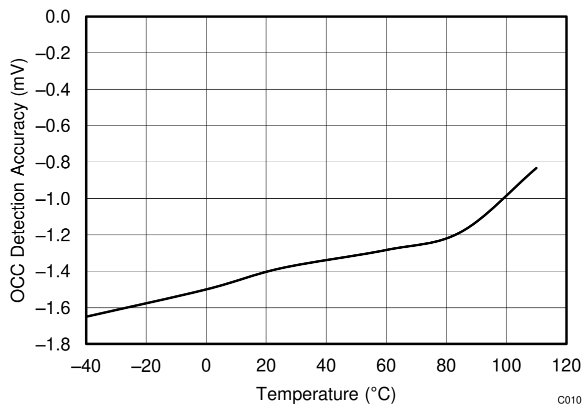
UVP, Setting = 2.800V

Figure 6-8. UVP Detection Accuracy Versus Temperature



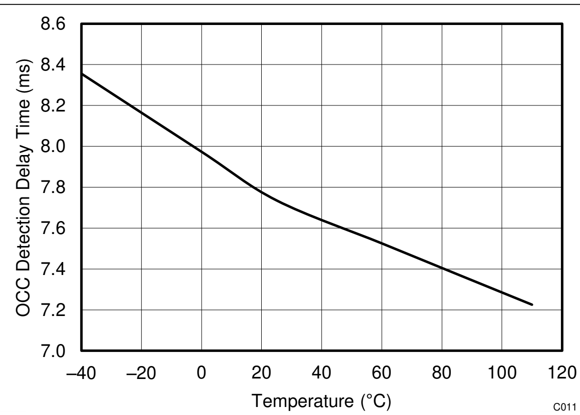
t_{UVPD}, Setting = 144ms

Figure 6-9. UVP Detection Delay Time Versus Temperature



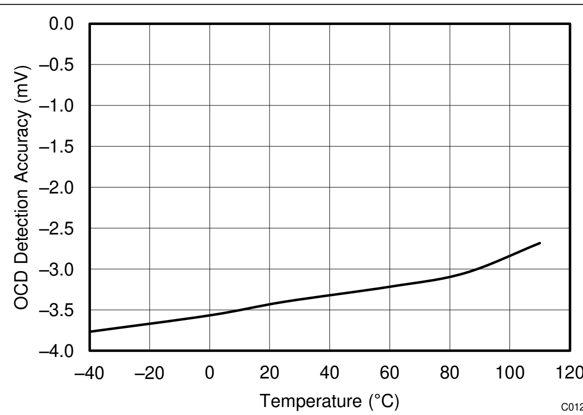
V_{OCC}, Setting = –100mV

Figure 6-10. OCC Detection Accuracy Versus Temperature



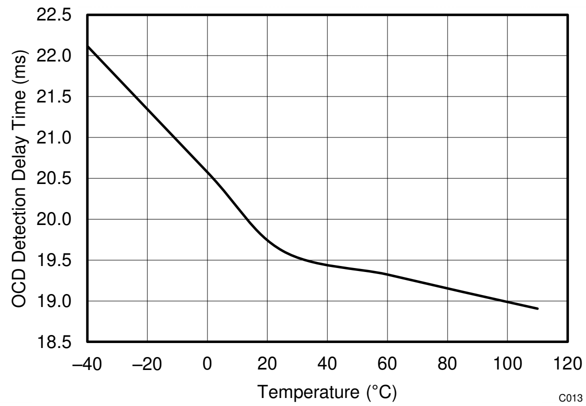
t_{OCCD}, Setting = 8ms

Figure 6-11. OCC Detection Delay Time Versus Temperature



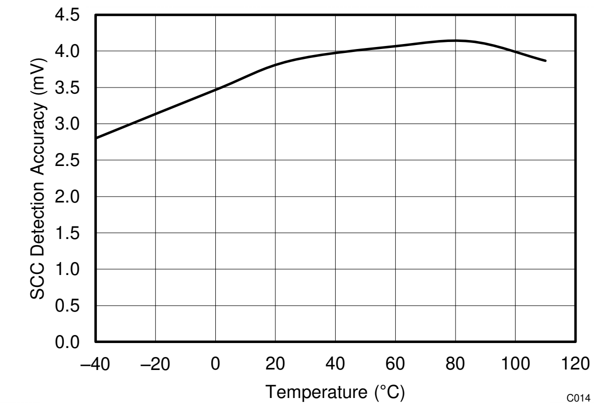
V_{OCD}, Setting = 100mV

Figure 6-12. OCD Detection Accuracy Versus Temperature



t_{UVPD}, Setting = 20ms

Figure 6-13. OCD Detection Delay Time Versus Temperature



V_{SCC}, Setting = 500mV

Figure 6-14. SCC Detection Accuracy Versus Temperature

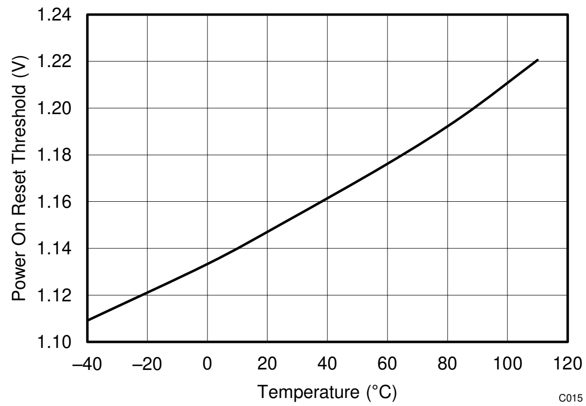
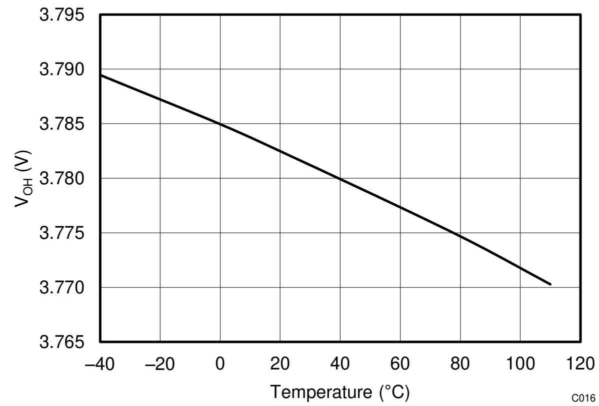
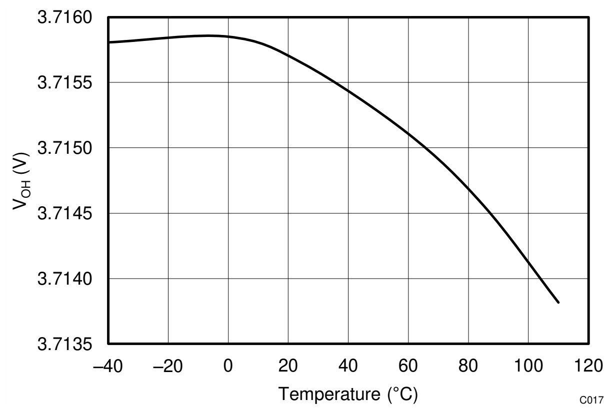


Figure 6-15. Power On Reset Versus Temperature



V_{BAT}, Setting = 3.9V

Figure 6-16. COUT Versus Temperature with I_{oh} = –30µA



V_{BAT}, Setting = 3.9V

Figure 6-17. DOUT Versus Temperature with I_{oh} = –30µA

7 Parameter Measurement Information

7.1 Timing Charts

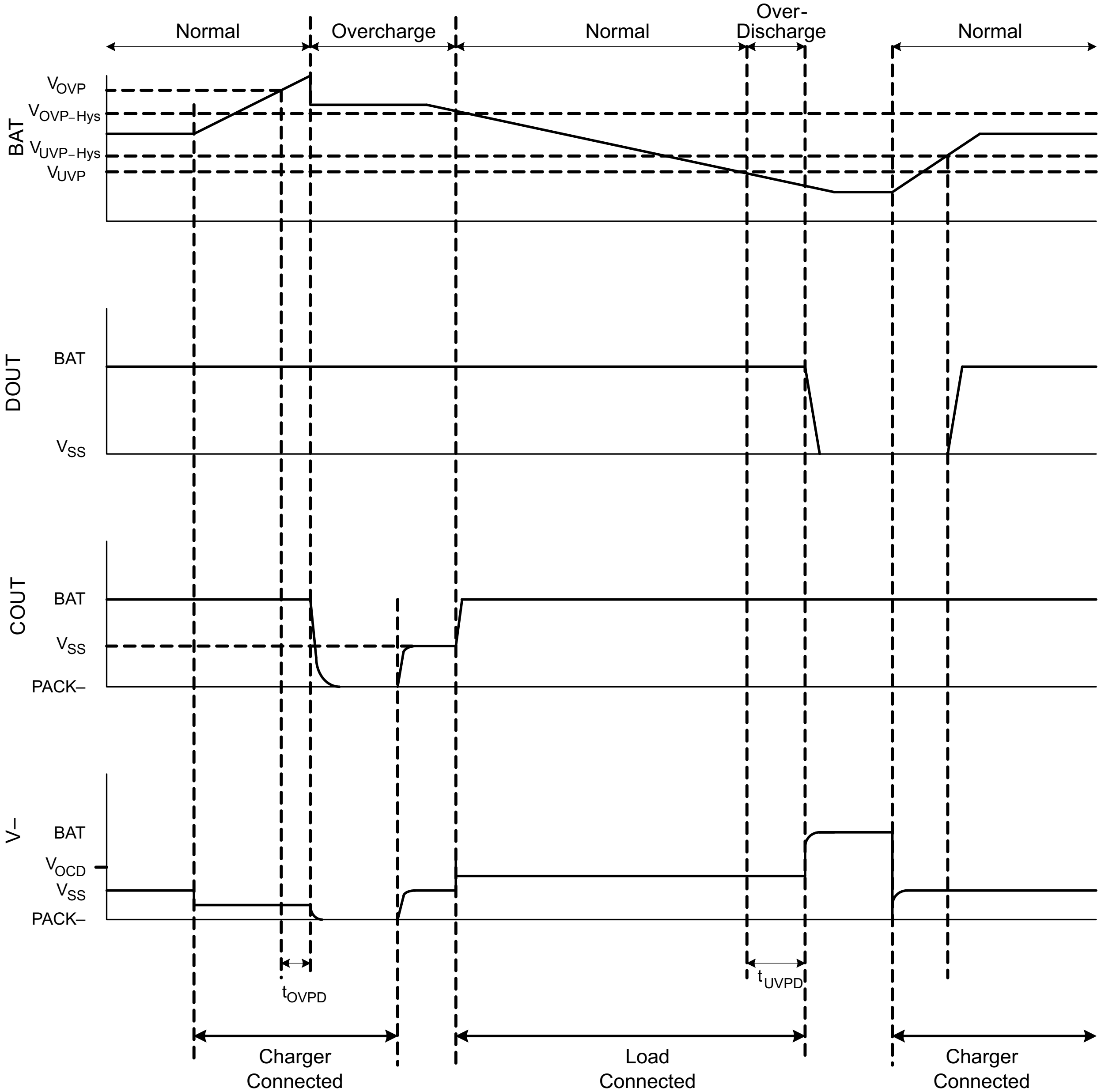


Figure 7-1. Overcharge Detection, Over-Discharge Detection

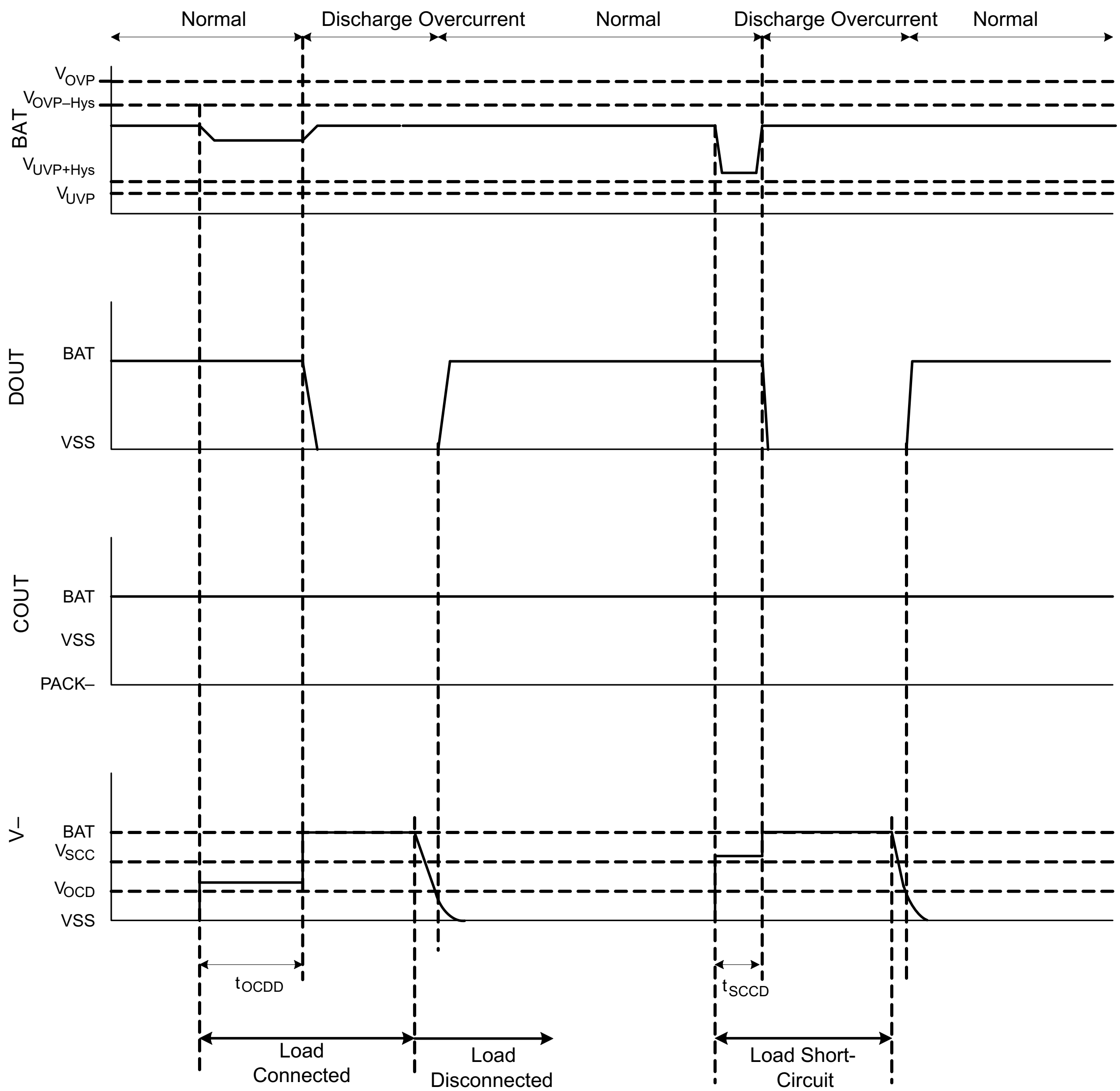


Figure 7-2. Discharge Overcurrent Detection

7.2 Test Circuits

The following tests are referenced as follows: The COUT and DOUT outputs are "H," which are higher than the threshold voltage of the external logic level FETs and regarded as ON state. "L" is less than the turn ON threshold for external NMOS FETs and regarded as OFF state. The COUT pin is with respect to V–, and the DOUT pin is with respect to VSS.

1. ***Overcharge detection voltage and overcharge release voltage (Test Circuit 1):***

   The overcharge detection voltage (V_{OVP}) is measured between the BAT and VSS pins, respectively. Once V1 is increased, the over-detection is triggered, and the delay timer expires. Then, COUT transitions from a high to low state and reduces the V1 voltage to check for the overcharge hysteresis parameter ($V_{OVP\text{-}Hys}$). The delta voltage between overcharge detection voltages (V_{OVP}) and the overcharge release occurs when the CHG FET drive output goes from low to high.
2. ***Over-discharge detection voltage and over-discharge release voltage (Test Circuit 2):***

   Over-discharge detection (V_{UVP}) is defined as the voltage between BAT and VSS at which the DSG drive output goes from high to low by reducing the V1 voltage. V1 is set to 3.5V and gradually reduced while V2 is set to 0V. The over-discharge release voltage is defined as the voltage between BAT and VSS at which the DOUT drive output transition from low to high when V1 voltage is gradually increased from a V_{UVP} condition. The overcharge hysteresis voltage is defined as the delta voltage between V_{UVP} and the instance at which the DOUT output drive goes from low to high.
3. ***Discharge overcurrent detection voltage (Test Circuit 2):***

   The discharge overcurrent detection voltage (V_{OCD}) is measured between V– and VSS pins and triggered when the V2 voltage is increased above V_{OCD} threshold with respect to VSS. This delta voltage once satisfied will trigger an internal timer t_{OCDD} before the DOUT output drive transitions from high to low.
4. ***Load short circuit detection voltage (Test Circuit 2):***

   Load short-circuit detection voltage (V_{SCC}) is measured between V– and VSS pins and triggered when the V2 voltage is increased above V_{SCC} threshold with respect to VSS within 10µs. This delta voltage, once satisfied, triggers an internal timer t_{SCCD} before the DOUT output drive transitions from high to low.
5. ***Charge overcurrent detection voltage (Test Circuit 2):***

   The charge overcurrent detection voltage (V_{OCC}) is measured between VSS and V– pins and triggered when the V2 voltage is increased above V_{OCC} threshold with respect to V–. This delta voltage, once satisfied, triggers an internal timer t_{OCCD} before the COUT output drive transitions from high to low.
6. ***Operating current consumption (Test Circuit 2):***

   The operating current consumption $I_{BNORMAL}$ is the current measured going into the BAT pin under the following conditions: V1 = 3.9V and V2 = 0V.
7. ***Power down current consumption (Test Circuit 2):***

   The operating current consumption I_{Power_down} is the current measured going into the BAT pin under the following conditions: V1 = 1.5V and V2 = 1.5V.
8. ***Resistance between V– and BAT pin (Test Circuit 3):***

   Measure the resistance (R_{V_D}) between V– and BAT pins by setting the following conditions: V1 = 1.8V and V2 = 0V.
9. ***Current sink between V– and VSS (Test Circuit 3):***

   Measure the current sink $I_{V\text{–}S}$ between V– and VSS pins by setting the following condition: V1 = 4V.
10. ***COUT current source when activated High (Test Circuit 4):***

    Measure I_{COUT} current source on the COUT pin by setting the following conditions: V1 = 3.9V, V2 = 0V, and V3 = 3.4V.
11. ***COUT current sink when activated Low (Test Circuit 4):***

    Measure I_{COUT} current sink on COUT pin by setting the following conditions: V1 = 4.5V, V2 = 0V, and V3 = 0.5V.
12. ***DOUT current source when activated High (Test Circuit 4):***

Measure I_{DOUT} current source on DOUT pin by setting the following conditions: V1 = 3.9V, V2 = 0V, and V3 = 3.4V.

13. ***DOUT current sink when activated Low (Test Circuit 4):***

    Measure I_{DOUT} current sink on DOUT pin by setting the following conditions: V1 = 2.0V, V2 = 0V, and V3 = 0.4V.

14. ***Overcharge detection delay (Test Circuit 5):***

    The overcharge detection delay time t_{OVPD} is the time delay before the COUT drive output transitions from high to low once the voltage on V1 exceeds the V_{OVP} threshold. Set V2 = 0V and then increase V1 until BAT input exceeds the V_{OVP} threshold, then check the time for when COUT goes from high to low.

15. ***Over-discharge detection delay (Test Circuit 5):***

    The over-discharge detection delay time t_{UVPD} is the time delay before the DOUT drive output transitions from high to low once the voltage on V1 decreases to V_{UVP} threshold. Set V2 = 0V and then decrease V1 until BAT input reduces to the V_{UVP}threshold, then check the time of when DOUT goes from high to low.

16. ***Discharge overcurrent detection delay (Test Circuit 5):***

    The discharge overcurrent detection delay time t_{OCDD} is the time for DOUT drive output to transition from high to low after the voltage on V2 is increased from 0V to 0.35V. V1 = 3.5V and V2 starts from 0V and increases to trigger threshold.

17. ***Load short circuit detection delay (Test Circuit 5):***

    The load short-circuit detection delay time t_{SCCD} is the time for DOUT drive output to transition from high to low after the voltage on V2 is increased from 0V to V1 – 1V. V1 = 3.5V and V2 starts from 0V and increases to trigger threshold.

18. ***Charge overcurrent detection delay (Test Circuit 5):***

    The charge overcurrent detection delay time t_{OCCD} is the time for COUT drive output to transition from high to low after the voltage on V2 is decreased from 0V to –0.3V. V1 = 3.5V and V2 starts from 0V and decreases to trigger threshold.

19. ***0V battery charge starting charger voltage (Test Circuit 2):***

    The 0V charge for start charging voltage V_{0CHA} is defined as the voltage between BAT and V– pins at which COUT goes high when voltage on V2 is gradually decreased from a condition of V1 = V2 = 0V.

20. ***0V battery charge inhibition battery voltage (Test Circuit 2):***

    The 0V charge inhibit for charger voltage V_{0INH} is defined as the voltage between BAT and VSS pins at which COUT should go low as V1 is gradually decreased from V1 = 2V and V2 = –4V.

7.3 Test Circuit Diagrams

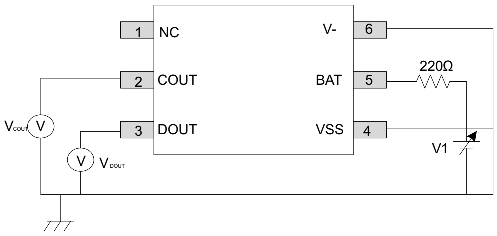


Figure 7-3. Test Circuit 1

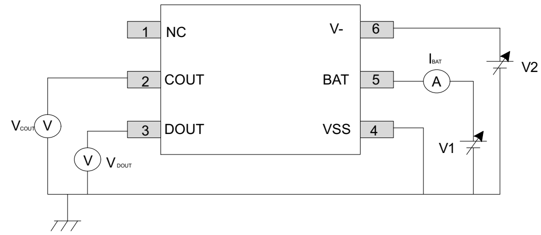


Figure 7-4. Test Circuit 2

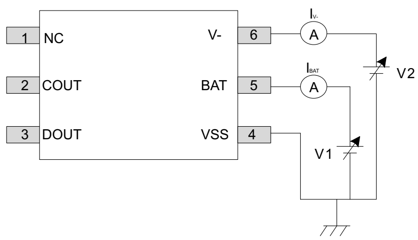


Figure 7-5. Test Circuit 3

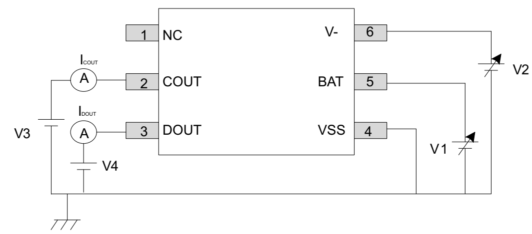


Figure 7-6. Test Circuit 4

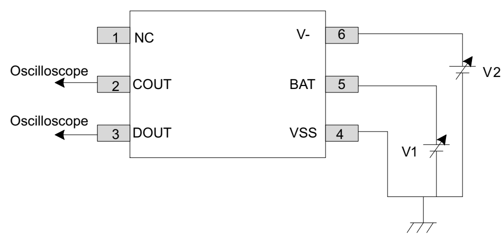


Figure 7-7. Test Circuit 5

8 Detailed Description

8.1 Overview

This BQ2970 device is a primary protector for a single-cell Li-ion/Li-polymer battery pack. The device uses a minimum number of external components to protect for overcurrent conditions due to high discharge/charge currents in the application. In addition, it monitors and helps to protect against battery pack overcharging or depletion of energy in the pack. The BQ2970 device is capable of having an input voltage of 8V from a charging adapter and can tolerate a voltage of BAT – 25V across the two input pins. In the condition when a fault is triggered, there are timer delays before the appropriate action is taken to turn OFF either the CHG or DSG FETs. The recovery period also has a timer delay once the threshold for recovery condition is satisfied. These parameters are fixed once they are programmed. There is also a feature called zero voltage charging that enables depleted cells to be charged to an acceptable level before the battery pack can be used for normal operation. Zero voltage charging is allowed if the charger voltage is above 1.7V. For Factory Programmable Options, see Table 8-1.

Table 8-1. Factory Programmable Options

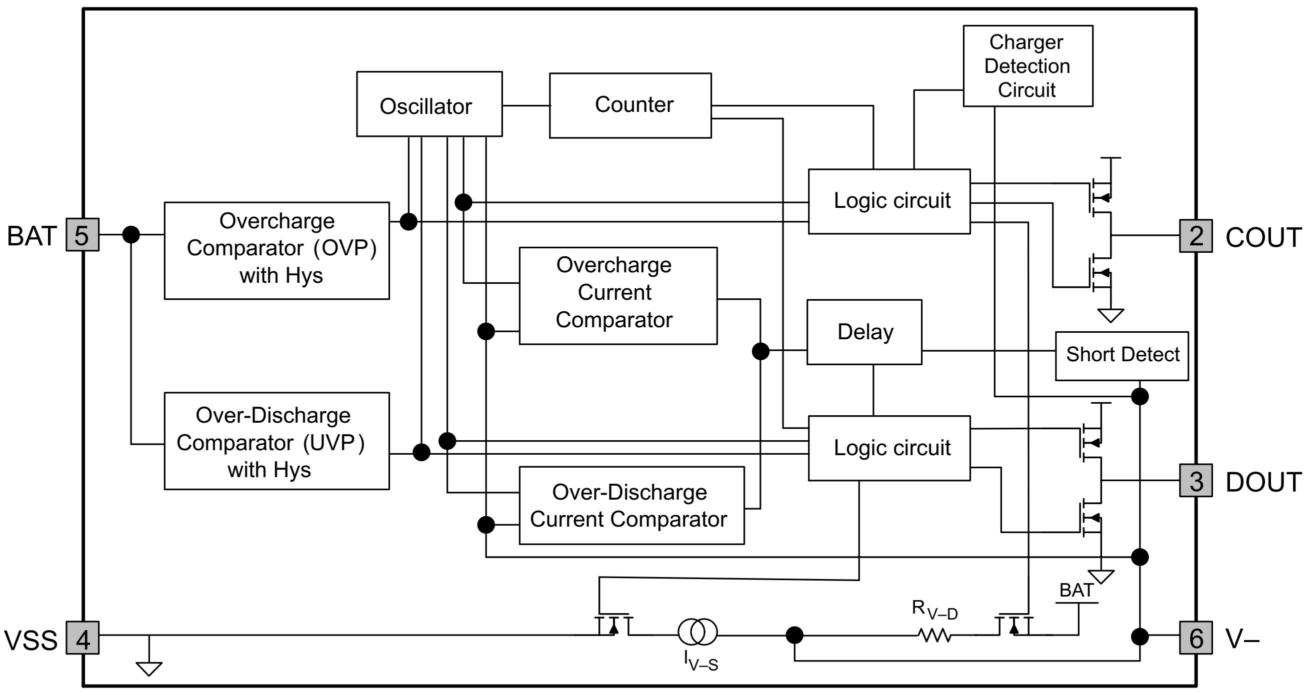
PARAMETER		FACTORY DEVICE CONFIGURATION
V_{OVP}	Overcharge detection voltage	3.85V to 4.60V in 50mV steps
V_{UVP}	Over-discharge detection voltage	2.00V to 2.80V in 50mV steps
V_{OCD}	Discharging overcurrent detection voltage	90mV to 200mV in 5mV steps
V_{OCC}	Charging overcurrent detection voltage	–45mV to –155mV in 5mV steps
V_{SCC}	Short Circuit detection voltage	300mV, 400mV, 500mV, 600mV
t_{OVPD}	Overcharge detection delay time	0.25s, 1.00s, 1.25s, 4.50s
t_{UVPD}	Over-discharge detection delay time	20ms, 96ms, 125ms, 144ms

Table 8-1. Factory Programmable Options (continued)

PARAMETER		FACTORY DEVICE CONFIGURATION
t_{OCDD}	Discharging overcurrent detection delay time	8ms, 16ms, 20ms, 48ms
t_{OCCD}	Charging overcurrent detection delay time	4ms, 6ms, 8ms, 16ms
t_{SCCD}	Short Circuit detection delay time	250µs (fixed)

For available released devices, see the *Released Device Configurations* table.

8.2 Functional Block Diagram



8.3 Feature Description

The BQ2970 family of devices measures voltage drops across several input pins for monitoring and detection of the following faults: OCC, OCD, OVP, and UVP. An internal oscillator initiates a timer to the fixed delays associated with each parameter once the fault is triggered. Once the timer expires due to a fault condition, the appropriate FET drive output (COUT or DOUT) is activated to turn OFF the external FET. The same method is applicable for the recovery feature once the system fault is removed and the recovery parameter is satisfied, then the recovery timer is initiated. If there are no reoccurrences of this fault during this period, the appropriate gate drive is activated to turn ON the appropriate external FET.

8.4 Device Functional Modes

8.4.1 Normal Operation

This device monitors the voltage of the battery connected between BAT pin and VSS pin and the differential voltage between V– pin and VSS pin to control charging and discharging. The system is operating in NORMAL mode when the battery voltage range is between the over-discharge detection threshold (V_{UVP}) and the overcharge detection threshold (V_{OVP}), and the V– pin voltage is within the range for charge overcurrent threshold (V_{OCC}) to over-discharge current threshold (V_{OCD}) when measured with respect to VSS. If these conditions are satisfied, the device turns ON the drive for COUT and DOUT FET control.

CAUTION

When the battery is connected for the first time, the discharging circuit might not be enabled. In this case, short the V– pin to the VSS pin.

Alternatively, connect the charger between the Pack+ and Pack– terminals in the system.

8.4.2 Overcharge Status

This mode is detected when the battery voltage measured is higher than the overcharge detection threshold (V_{OVP}) during charging. If this condition exists for a period greater than the overcharge detection delay (t_{OVPD}) or longer, the COUT output signal is driven low to turn OFF the charging FET to prevent any further charging of the battery.

The overcharge condition is released if one of the following conditions occurs:

- If the V– pin is higher than the overcharge detection voltage (V_{OCC_Min}), the device releases the overcharge status when the battery voltage drops below the overcharge release voltage ($V_{OVP\text{-}Hys}$).
- If the V– pin is higher than or equal to the over-discharge detection voltage (V_{OCD}), the device releases the overcharge status when the battery voltage drops below the overcharge detection voltage (V_{OVP}).

The discharge is initiated by connecting a load after the overcharge detection. The V– pin rises to a voltage greater than VSS due to the parasitic diode of the charge FET conducting to support the load. If the V– pin voltage is higher than or equal to the discharge overcurrent detection threshold (V_{OCD}), the overcurrent condition status is released only if the battery voltage drops lower than or equal to the overcharge detection voltage (V_{OVP}).

CAUTION

1. If the battery is overcharged to a level greater than overcharge detection (V_{OVP}) and the battery voltage does *not* drop below the overcharge detection voltage (V_{OVP}) with a heavy load connected, the discharge overcurrent and load short-circuit detection features do *not* function until the battery voltage drops below the overcharge detection voltage (V_{OVP}). The internal impedance of a battery is in the order of tens of mΩ, so application of a heavy load on the output should allow the battery voltage to drop immediately, enabling discharge overcurrent detection and load short-circuit detection features after an overcharge release delay.
2. When a charger is connected after an overcharge detection, the overcharge status does *not* release even if the battery voltage drops below the overcharge release threshold. The overcharge status is released when the V– pin voltage exceeds the overcurrent detection voltage (V_{OCD}) by removing the charger.

8.4.3 Over-Discharge Status

If the battery voltage drops below the over-discharge detection voltage (V_{UVP}) for a time greater than (t_{UVPD}) the discharge control output, DOUT is switched to a low state and the discharge FET is turned OFF to prevent further discharging of the battery. This is referred to as an over-discharge detection status. In this condition, the V– pin is internally pulled up to BAT by the resistor $R_{V–D}$. When this occurs, the voltage difference between V– and BAT pins is 1.3V or lower, and the current consumption of the device is reduced to power-down level $I_{STANDBY}$. The current sink $I_{V–S}$ is not active in power-down state or over-discharge state. The power-down state is released when a charger is connected and the voltage delta between V– and BAT pins is greater than 1.3V.

If a charger is connected to a battery in over-discharge state and the voltage detected at the V– is lower than –0.7V, the device releases the over-discharge state and allows the DOUT pin to go high and turn ON the discharge FET once the battery voltage exceeds over-discharge detection voltage (V_{UVP}).

If a charger is connected to a battery in over-discharge state and the voltage detected at the V– is higher than –0.7V, the device releases the over-discharge state and allows the DOUT pin to go high and turn

ON the discharge FET once the battery voltage exceeds over-discharge detection release hysteresis voltage ($V_{UVP\ +Hys}$).

8.4.4 Discharge Overcurrent Status (Discharge Overcurrent, Load Short-Circuit)

When a battery is in normal operation and the V– pin is equal to or higher than the discharge overcurrent threshold for a time greater than the discharge overcurrent detection delay, the DOUT pin is pulled low to turn OFF the discharge FET and prevent further discharge of the battery. This is known as the discharge overcurrent status. In the discharge overcurrent status, the V– and VSS pins are connected by a constant current sink $I_{V–S}$. When this occurs and a load is connected, the V– pin is at BAT potential. If the load is disconnected, the V– pin goes to VSS (BAT/2) potential.

This device detects the status when the impedance between Pack+ and Pack– (see Figure 26) increases and is equal to the impedance that enables the voltage at the V– pin to return to BAT – 1V or lower. The discharge overcurrent status is restored to the normal status.

Alternatively, by connecting the charger to the system, the device returns to normal status from discharge overcurrent detection status, because the voltage at the V– pin drops to BAT – 1V or lower.

The resistance $R_{V–D}$ between V– and BAT is not connected in the discharge overcurrent detection status.

8.4.5 Charge Overcurrent Status

When a battery is in normal operation status and the voltage at V– pin is lower than the charge overcurrent detection due to high charge current for a time greater than charge overcurrent detection delay, the COUT pin is pulled low to turn OFF the charge FET and prevent further charging to continue. This is known as charge overcurrent status.

The device is restored to normal status from charge overcurrent status when the voltage at the V– pin returns to charge overcurrent detection voltage or higher by removing the charger from the system.

The charge overcurrent detection feature does *not* work in the over-discharge status.

The resistance $R_{V–D}$ between V– and BAT and the current sink $I_{V–S}$ is not connected in the charge overcurrent status.

8.4.6 0V Charging Function Enabled

This feature enables recharging a connected battery that has very low voltage due to self-discharge. When the charger applies a voltage greater than or equal to V_{0CHG} to Pack+ and Pack– connections, the COUT pin gate drive is fixed by the BAT pin voltage.

Once the voltage between the gate and the source of the charging FET becomes equal to or greater than the turn ON voltage due to the charger voltage, the charging FET is ON and the battery is charged with current flow through the charging FET and the internal parasitic diode of the discharging FET. Once the battery voltage is equal to or higher than the over-discharge release voltage, the device enters normal status.

CAUTION

1. Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to have the 0V battery charger function.
2. The 0V battery charge feature has a higher priority than the charge overcurrent detection function. In this case, the 0V charging will be allowed and the battery charges forcibly, which results in charge overcurrent detection being disabled if the battery voltage is lower than the over-discharge detection voltage.

8.4.7 0V Charging Inhibit Function

This feature inhibits recharging a battery that has an internal short circuit of a 0V battery. If the battery voltage is below the charge inhibit voltage V_{0INH} or lower, the charge FET control gate is fixed to the Pack– voltage to inhibit charging. When the battery is equal to V_{0INH} or higher, charging can be performed. The 0V charge inhibit function is available in all configurations of the BQ297xx device.

CAUTION

Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to enable or inhibit the 0V battery charger function.

8.4.8 Delay Circuit

The detection delay timers are based from an internal clock with a frequency of 10kHz.

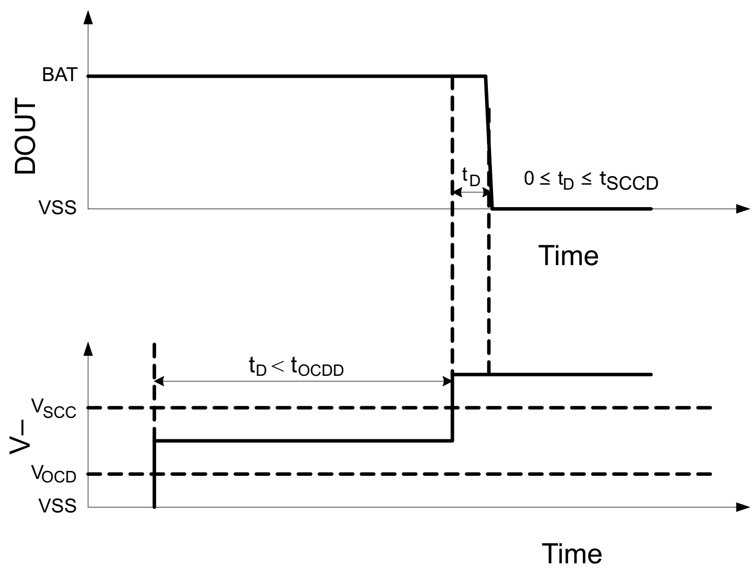


Figure 8-1. Delay Circuit

If the over-discharge current is detected, but remains below the over-discharge short circuit detection threshold, the over-discharge detection conditions must be valid for a time greater than or equal to over-discharge current delay t_{OCCD} time before the DOUT goes low to turn OFF the discharge FET. However, during any time the discharge overcurrent detection exceeds the short circuit detection threshold for a time greater than or equal to load circuit detection delay t_{SCCD}, the DOUT pin goes low in a faster delay for protection.

9 Application and Implementation

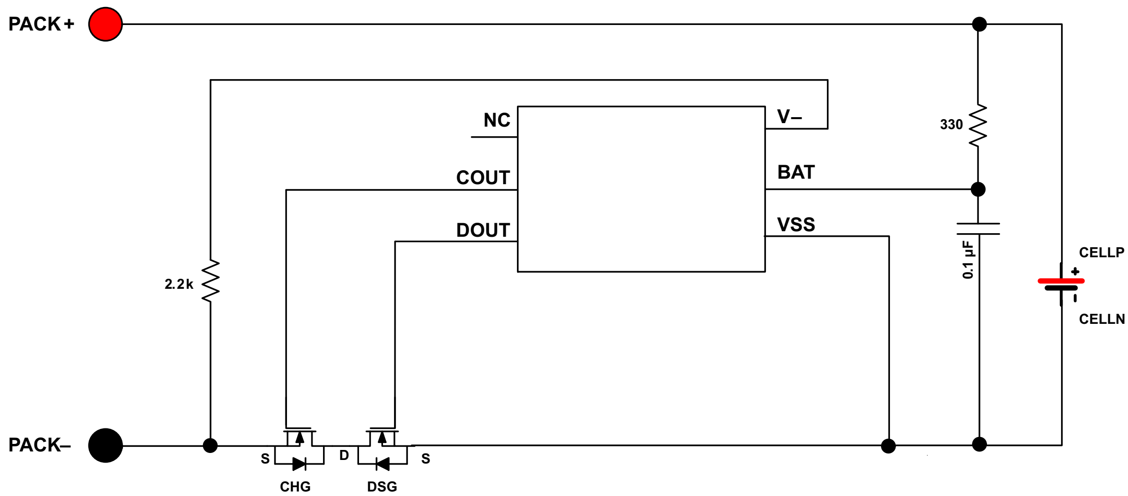
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The BQ2970 devices are a family of primary protectors used for protection of the battery pack in the application. The application drives two low-side NMOS FETs that are controlled to provide energy to the system loads or interrupt the power in the event of a fault condition.

9.2 Typical Application



The 5-M resistor for an external gate-source is optional.

Figure 9-1. Typical Application Schematic, BQ2970

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE at T_A = 25°C
Input voltage range	4.5V to 7V
Maximum operating discharge current	7A
Maximum Charge Current for battery pack	4.5A
Overvoltage Protection (OVP)	4.275V
Overvoltage detection delay timer	1.2s
Overvoltage Protection (OVP) release voltage	4.175V
Undervoltage Protection (UVP)	2.8V
Undervoltage detection delay timer	150ms
Undervoltage Protection (UVP) release voltage	2.9V
Charge Overcurrent detection (OCC) voltage	–70mV
Charge Overcurrent Detection (OCC) delay timer	9ms
Discharge Overcurrent Detection (OCD) voltage	100mV
Discharge Overcurrent Detection (OCD) delay timer	18ms
Load Short Circuit Detection SCC) voltage, BAT to –V ≤ threshold	500mV
Load Short Circuit Detection (SCC) delay timer	250µs
Load Short Circuit release voltage, BAT to –V ≥ Threshold	1V

9.2.2 Detailed Design Procedure

Note

The external FET selection is important to ensure the battery pack protection is sufficient and complies to the requirements of the system.

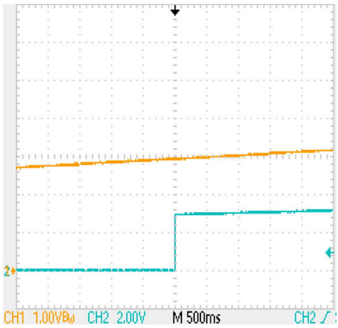
- FET Selection: Because the maximum desired discharge current is 7A, ensure that the Discharge Overcurrent circuit does *not* trigger until the discharge current is above this value.
- The total resistance tolerated across the two external FETs (CHG + DSG) should be 100mV/7A = 14.3mΩ.

- Based on the information of the total ON resistance of the two switches, determine what would be the Charge Overcurrent Detection threshold, 14.3mΩ × 4.5A = 65mV. Selecting a device with a 70mV trigger threshold for Charge Overcurrent trigger is acceptable.
- The total Rds ON should factor in any worst-case parameter based on the FET ON resistance, derating due to temperature effects and minimum required operation, and the associated gate drive (Vgs). Therefore, the FET choice should meet the following criteria:

  Vdss = 25V

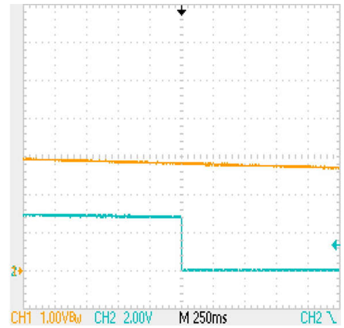
  Each FET Rds ON = 7.5mΩ at Tj = 25°C and Vgs = 3.5V
- Imax > 50A to allow for short Circuit Current condition for 350µs (max delay timer). The only limiting factor during this condition is Pack Voltage/(Cell Resistance + (2 × FET_RdsON) + Trace Resistance).
- Use the CSD16406Q3 FET for the application.
- An RC filter is required on the BAT for noise, and enables the device to operate during sharp negative transients. The 330Ω resistor also limits the current during a reverse connection on the system.
- TI recommends placing a high impedance 5MΩ across the gate source of each external FET to deplete any charge on the gate-source capacitance.

9.2.3 Application Performance Plots



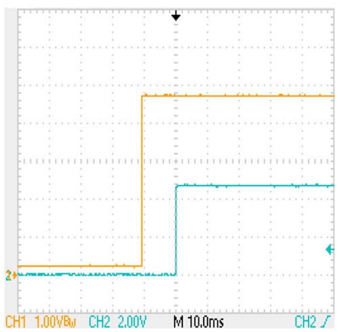
Orange Line (Channel 1) = Power Up Ramp on BAT Pin
Turquoise Line (Channel 2) = DOUT Gate Drive Output
DOUT goes from low to high when UVP Recovery = UVP Set Threshold +100mV

Figure 9-2. UVP Recovery



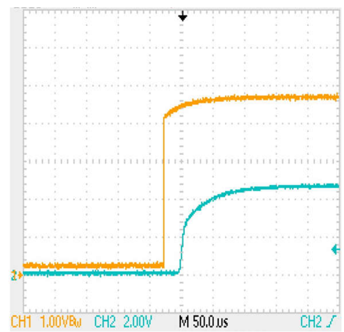
Orange Line (Channel 1) = Power Down Ramp on BAT Pin
Turquoise Line (Channel 2) = DOUT Date Drive Output
DOUT goes from high to low when UVP threshold = UVP set Threshold + set delay time

Figure 9-3. UVP Set Condition



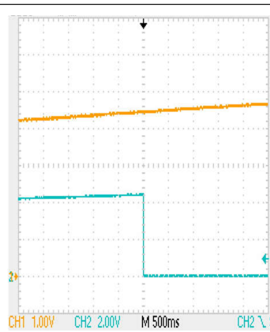
Orange Line (Channel 1) = Power Up Ramp on BAT pin
Turquoise Line (Channel 2) = DOUT Gate Drive Output

Figure 9-4. Initial Power Up, DOUT



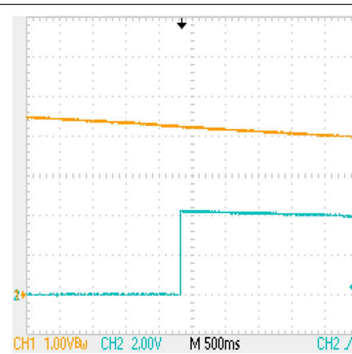
Orange Line (Channel 1) = Power Up Ramp on BAT Pin
Turquoise Line (Channel 2) = COUT Gate Drive Output

Figure 9-5. Initial Power Up, COUT



Orange Line (Channel 1) = Power Up Ramp on BAT Pin
Turquoise Line (Channel 2) = COUT Gate Drive Output
COUT goes from high to low when OVP threshold = OVP set Threshold + set delay time

Figure 9-6. OVP Set Condition



Orange Line (Channel 1) = Decrease Voltage on BAT Pin
Turquoise Line (Channel 2) = COUT Gate Drive Output
COUT goes from low to high when OVP Recovery = OVP Set Threshold –100mV

Figure 9-7. OVP Recovery Condition

9.3 Power Supply Recommendations

The recommended power supply for this device is a maximum 8V operation on the BAT input pin.

9.4 Layout

9.4.1 Layout Guidelines

The following are the recommended layout guidelines:

1. Ensure the external power FETs are adequately compensated for heat dissipation with sufficient thermal heat spreader based on worst-case power delivery.
2. The connection between the two external power FETs should be very close to ensure there is not an additional drop for fault sensing.
3. The input RC filter on the BAT pin should be close to the terminal of the IC.

9.4.2 Layout Example

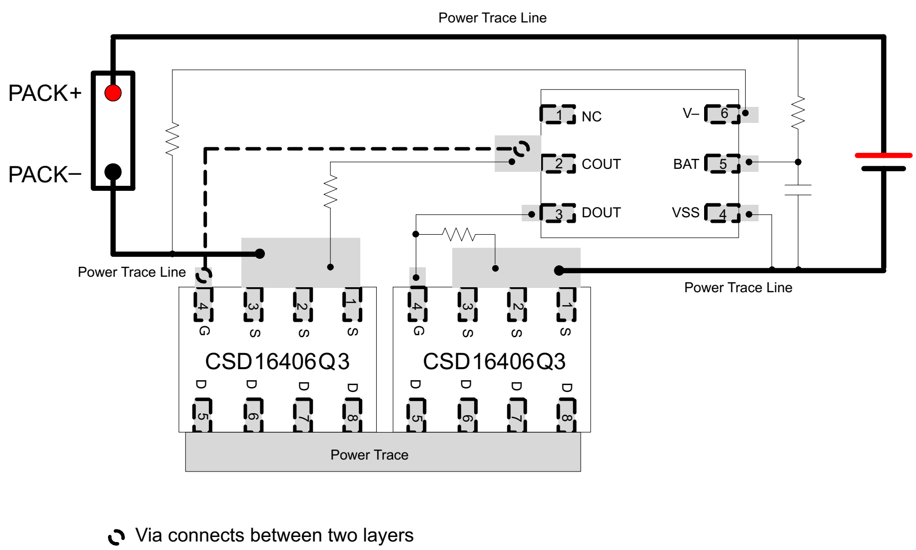


Figure 9-8. BQ2970 Board Layout

10 Device and Documentation Support

10.1 Related Documentation

BQ29700 Single-Cell Li-Ion Protector EVM User's Guide (SLUUAZ3)

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

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All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (June 2021) to Revision I (August 2024)	Page
• Added BQ29740 to the *Device Comparison Table*.	3

Changes from Revision G (December 2018) to Revision H (June 2021)	Page
• Changed the BQ29728 and BQ29737 devices to Production Data	3

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ29700DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA	Samples
BQ29700DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA	Samples
BQ29701DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FY	Samples
BQ29701DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FY	Samples
BQ29702DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FZ	Samples
BQ29702DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FZ	Samples
BQ29703DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F1	Samples
BQ29703DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F1	Samples
BQ29704DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F2	Samples
BQ29704DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F2	Samples
BQ29705DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F3	Samples
BQ29705DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F3	Samples
BQ29706DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F4	Samples
BQ29706DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F4	Samples
BQ29707DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F5	Samples
BQ29707DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F5	Samples
BQ29716DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3P	Samples
BQ29716DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3P	Samples
BQ29717DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3Q	Samples
BQ29717DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ29718DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3R	Samples
BQ29718DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3R	Samples
BQ29723DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3S	Samples
BQ29723DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3S	Samples
BQ29728DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EJ	Samples
BQ29728DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EJ	Samples
BQ29729DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3T	Samples
BQ29729DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3T	Samples
BQ29732DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3U	Samples
BQ29732DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3U	Samples
BQ29733DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4Q	Samples
BQ29733DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4Q	Samples
BQ29737DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EI	Samples
BQ29737DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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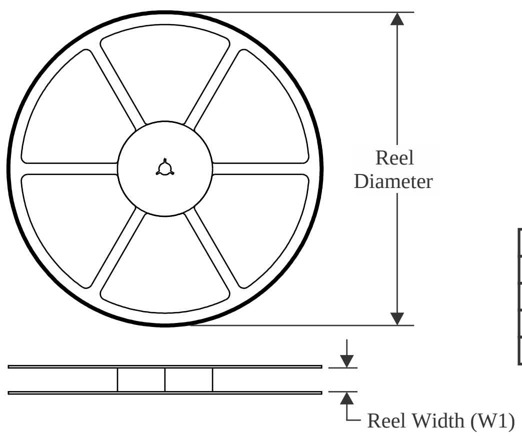
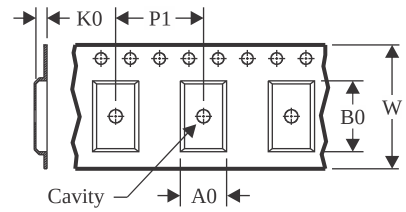
TAPE AND REEL INFORMATION

REEL DIMENSIONS

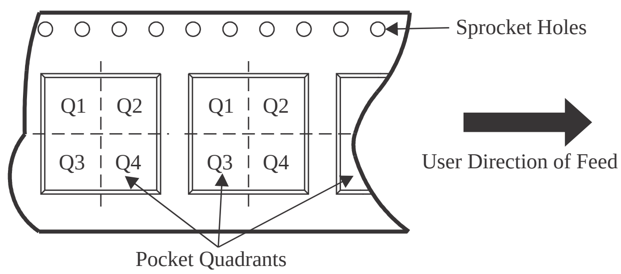


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

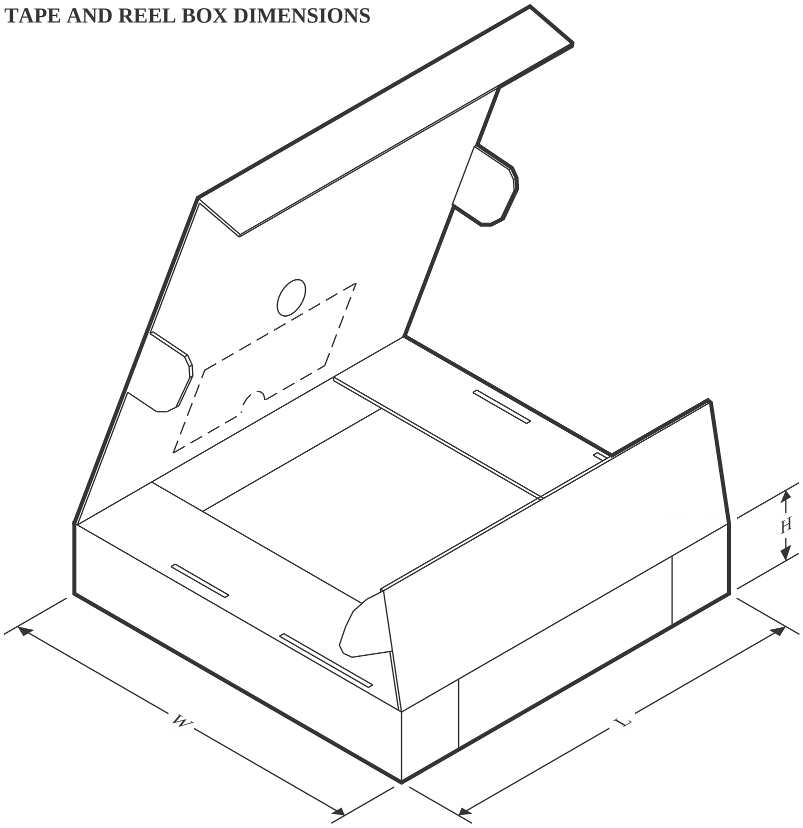


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29700DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29700DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29701DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29701DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29702DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29702DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29703DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29703DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29704DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29704DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29705DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29705DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29706DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29706DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29707DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29707DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29716DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29716DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29717DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29717DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29718DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29718DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29723DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29723DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29728DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29728DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29729DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29729DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29732DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29732DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29733DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29733DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29737DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29737DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

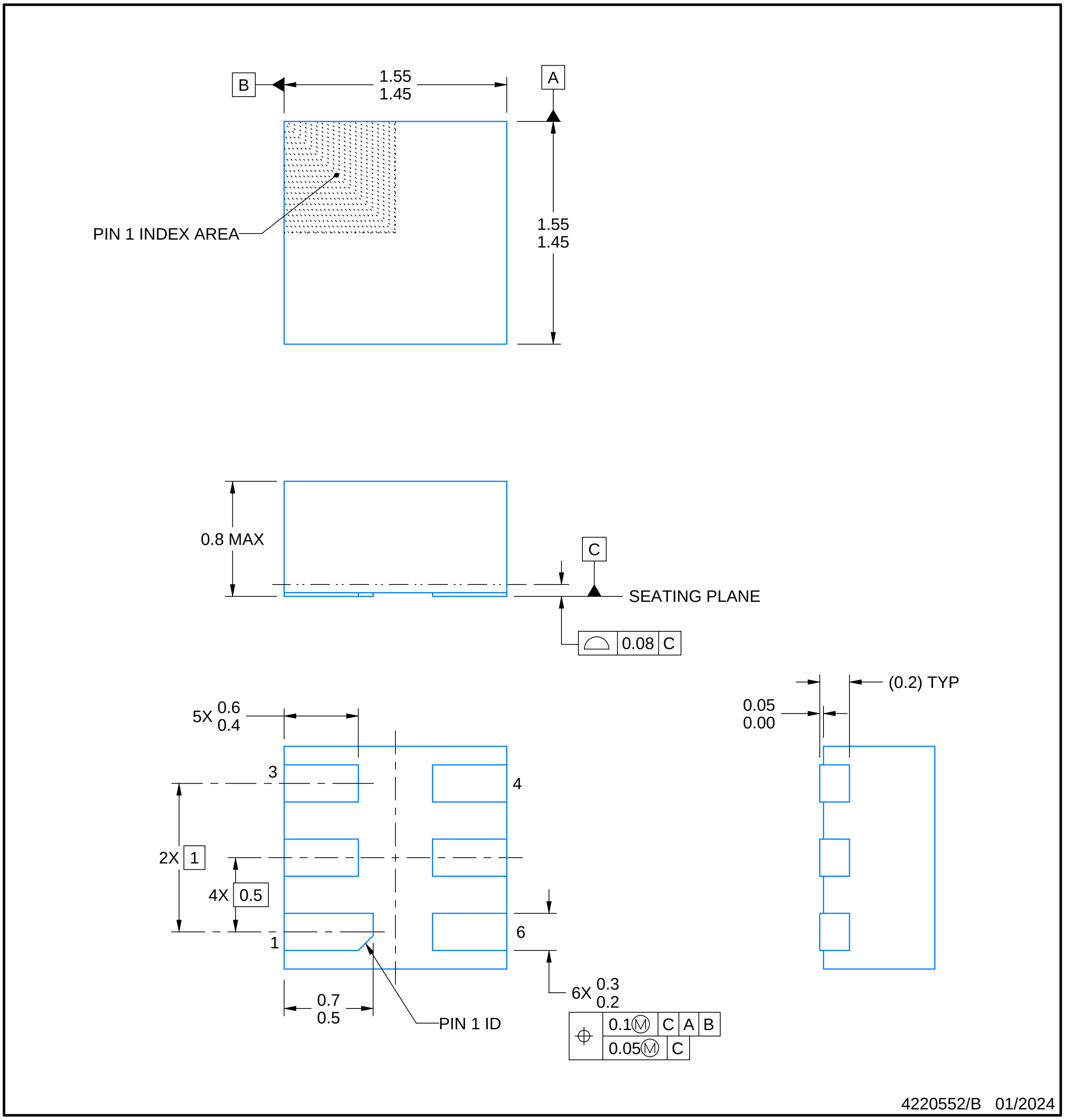
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

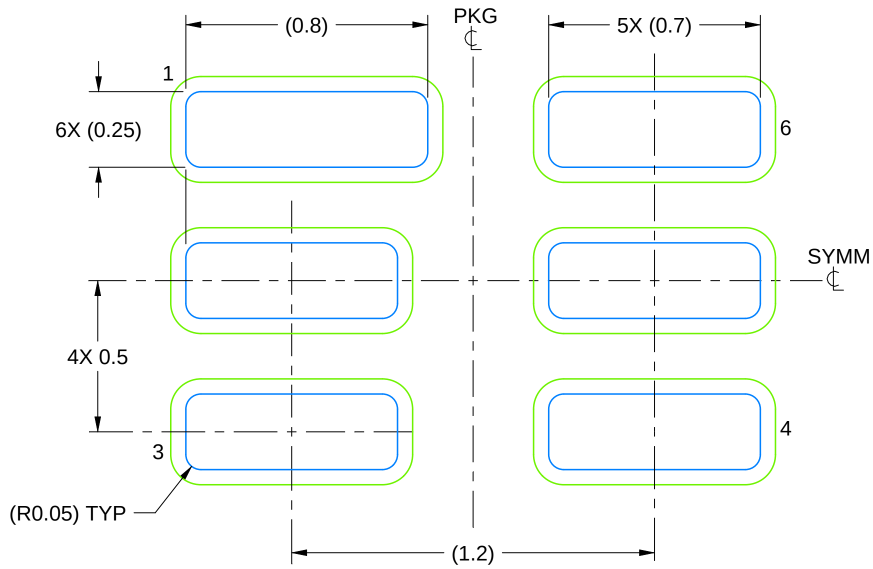
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29700DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29700DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29701DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29701DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29702DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29702DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29703DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29703DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29704DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29704DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29705DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29705DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29706DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29706DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29707DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29707DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29716DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29716DSET	WSON	DSE	6	250	182.0	182.0	20.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29717DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29717DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29718DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29718DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29723DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29723DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29728DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29728DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29729DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29729DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29732DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29732DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29733DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29733DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29737DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29737DSET	WSON	DSE	6	250	182.0	182.0	20.0

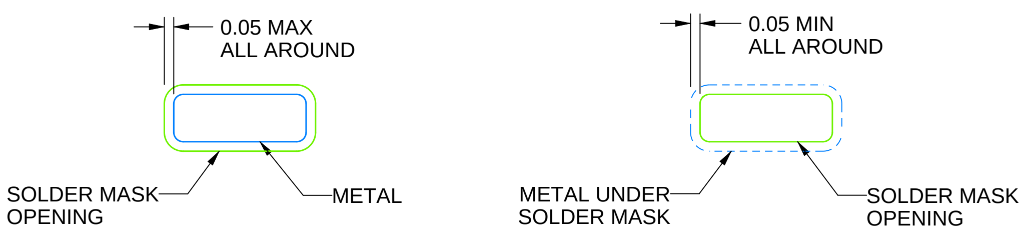


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



PADS 4-6
NON SOLDER MASK
DEFINED

PADS 1-3
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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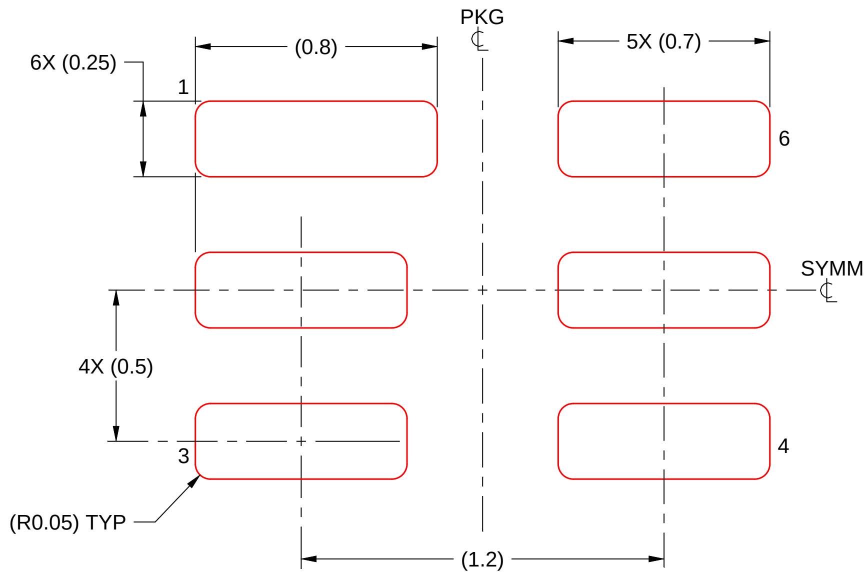
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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