CC274xR-Q1, CC274xP-Q1 AutomotiveSimpleLink™ Bluetooth® 6.0 Low Energy Wireless MCU

1 Features

Wireless MCU Processing Elements

- Arm® Cortex®-M33 processor (96MHz) with FPU (floating point unit), TrustZone®-M support and CDE (custom datapath extension) for machine learning acceleration
- Algorithm Processing Unit (APU) (96MHz)
  - Mathematical accelerator for efficient vector and matrix operations
  - Bluetooth® 6.0 Channel Sounding post-processing support for IFFT and advanced super-resolution algorithms like MUSIC (MUltiple SIgnal Classification)

Wireless MCU Memory

- Up to 1MB of in-system programmable flash
- Up to 162KB of SRAM
- 32KB of System ROM with secure boot root of trust (RoT) and a serial (SPI/UART) bootloader
- Serial wire debug (SWD)

Qualified for automotive application

- AEC-Q100 Grade 2 qualified:
  - Device temperature: –40°C to +125°C junction temperature
- HBM ESD Classification Level 2
- CDM ESD Classification Level C3

MCU Peripherals

- 23 GPIOs, digital peripherals can be routed to multiple GPIOs
  - Two IO pads SWD, multiplexed with GPIOs
  - Two IO pads LFXT, multiplexed with GPIOs
  - 19 DIOs (analog or digital IOs)
- All GPIOs with wakeup and interrupt capabilities
- 3 × 16-bit and 1 × 32-bit general-purpose timers, quadrature decode mode support
- Real-time clock (RTC)
- Watchdog timer
- System timer for radio, RTOS, and application operations for Bluetooth channel sounding postprocessing
- 12-bit ADC, up to 1.2Msps, 8 external inputs
- Temperature sensor and battery monitor
- 1× low power comparator
- 2× UART with LIN capability
- 2× SPI
- 1× I2C
- 1× I2S
- 1× CAN-FD controller

Security enablers

- ISO21434 Automotive Cybersecurity Compliant
- Hardware Security Module (HSM) with proprietary controller and dedicated memories supporting accelerated cryptographic operations and secure key storage:
  - AES (up to 256 bits) crypto accelerator
  - ECC (up to 521 bits), RSA (up to 3072 bits) public key accelerator
  - SHA-2 (up to 512 bits) accelerator
  - True random number generator
  - HSM firmware update support
- Separate AES 128bit crypto accelerator (LAES) for latency-critical link-layer crypto operations
- Secure boot and secure firmware updates
- Cortex®-M33 TrustZone-M, MPU, memory firewalls for software isolation
- Voltage glitch monitor (VGM)

Low power consumption (at 3.3V)

- On-chip buck DC/DC converter
- RX current: 6.1mA
- TX current at 0dBm: 7.7mA
- TX current at +10dBm: 24mA
- TX current at +20dBm: 128mA (P version)
- Active mode MCU 96MHz (CoreMark®): 6.8mA
- Standby: 0.9µA (low power mode, RTC on, full RAM retention)
- Reset or Shutdown: 160nA

Wireless protocol support High-performance radio

- 2.4GHz RF transceiver compatible with Bluetooth® Low Energy specification
- Output power up to +10dBm (R version)
- Output power up to +20dBm (P version)
- Integrated BALUN
- Integrated RF switch
- Receiver sensitivity:
  - -103.5dBm for Bluetooth® LE 125kbps
  - -97dBm for Bluetooth® LE 1Mbps

Regulatory compliance

- Designed for systems targeting compliance with worldwide radio frequency regulations
  - EN 300 328 (Europe)
  - FCC CFR47 Part 15 (US)
  - ARIB STD-T66 (Japan)

Development Tools and Software

- LP-EM-CC2745R10-Q1 LaunchPad™ Development Kit

- BP-EM-CS Multiple antenna board for Bluetooth 6.0 Channel Sounding
- SimpleLink™ Low Power F3 Software Development Kit (SDK)
  - Fully qualified Bluetooth® software protocol stack in SDK
    - Up to 32 concurrent multirole connections
    - Bluetooth 6.0 Channel Sounding Support
    - CCC Digital Key 3 / ICCE Bluetooth APIs support for secure car access systems
- SysConfig system configuration tool
- SmartRF™ Studio for simple radio configuration

Operating range:

- Junction temperature T_J: –40ºC to 125ºC
- Wide supply voltage range 1.71V to 3.8V

Package

- 6mm × 6mm QFN40 with wettable flanks
- RoHS-compliant package

2 Applications

- Automotive
  - Car access and security systems
    - Digital key
    - Phone as a key (PaaK)
    - Passive entry passive start (PEPS)
    - Remote keyless entry (RKE)

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3 Description

The SimpleLink™ CC274xR-Q1 and CC274xP-Q1 devices are AEC-Q100 complaint wireless microcontrollers (MCUs) supporting Bluetooth® Low Energy 6.0 for automotive applications. These devices are optimized for low-power wireless communication in applications such as car access including passive entry passive start (PEPS), phone as a key (PaaK), and remote keyless entry (RKE). The key features of this device include:

- Support for Bluetooth® 6.0 and earlier version features:
  - LE Coded PHYs (Long Range), LE 2Mbit PHY (high speed), advertising extensions, multiple advertisement Sets, CSA#2, as well as backward compatibility with earlier Low Energy specifications.
  - Bluetooth® Channel Sounding technology and Algorithm Processing Unit (APU) to enable high accuracy, low cost, and secure phase-based ranging mechanism for distance estimation.
    - APU enables latency and power-efficient execution of distance-ranging signal processing algorithms including FFT and super-resolution complex algorithms like MUSIC (MUltiple SIgnal Classification) at the lowest energy consumption.
- Arm (Custom Data Extension) CDE instruction support for machine learning acceleration
- Fully qualified Bluetooth software protocol stack included with the SimpleLink™ Low Power F3 Software Development Kit (SDK)
- Advanced security features for connected wireless MCUs:
  - Isolated HSM environment with a dedicated controller handling accelerated cryptographic and random number generation operations
  - Secure boot and firmware updates with the root of trust enabled by immutable system ROM
  - ARM Cortex M33 TrustZone-M based trusted execution environment support
  - Secure key storage support with HSM and TrustZone-M
  - Hardware fault sensors to mitigate low-cost, low-effort, non-invasive physical attack threats like voltage glitch injection.
  - Dedicated AES-128 HW accelerator for handling timing critical link layer encryption/decryption operations
- Ultra-low standby current with full 162KB SRAM retention and RTC operation that enables significant battery life extension, especially for applications with longer sleep intervals.
- Extended temperature support with the lowest standby current
- Integrated BALUN and integrated RF switch to support both transmit and receive operations on the same RF pin even for the P version; thereby, enabling reduced a bill-of-material (BOM) board layout
- Excellent radio sensitivity and robustness (selectivity and blocking) performance for Bluetooth Low Energy

The CC274xR/P-Q1 devices are part of the SimpleLink™ MCU platform, which consists of Wi-Fi®, Bluetooth Low Energy, Thread, Zigbee, Sub1GHz MCUs, and host MCUs that all share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink™ platform enables you to add any combination of the portfolio's devices into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit SimpleLink™ MCU platform.

Table 3-1. Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
CC2745P10-Q1	QFN40	6.0mm × 6.0mm
CC2745R10-Q1	QFN40	6.0mm × 6.0mm
CC2745R7-Q1	QFN40	6.0mm × 6.0mm
CC2744R7-Q1	QFN40	6.0mm × 6.0mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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4 Functional Block Diagram

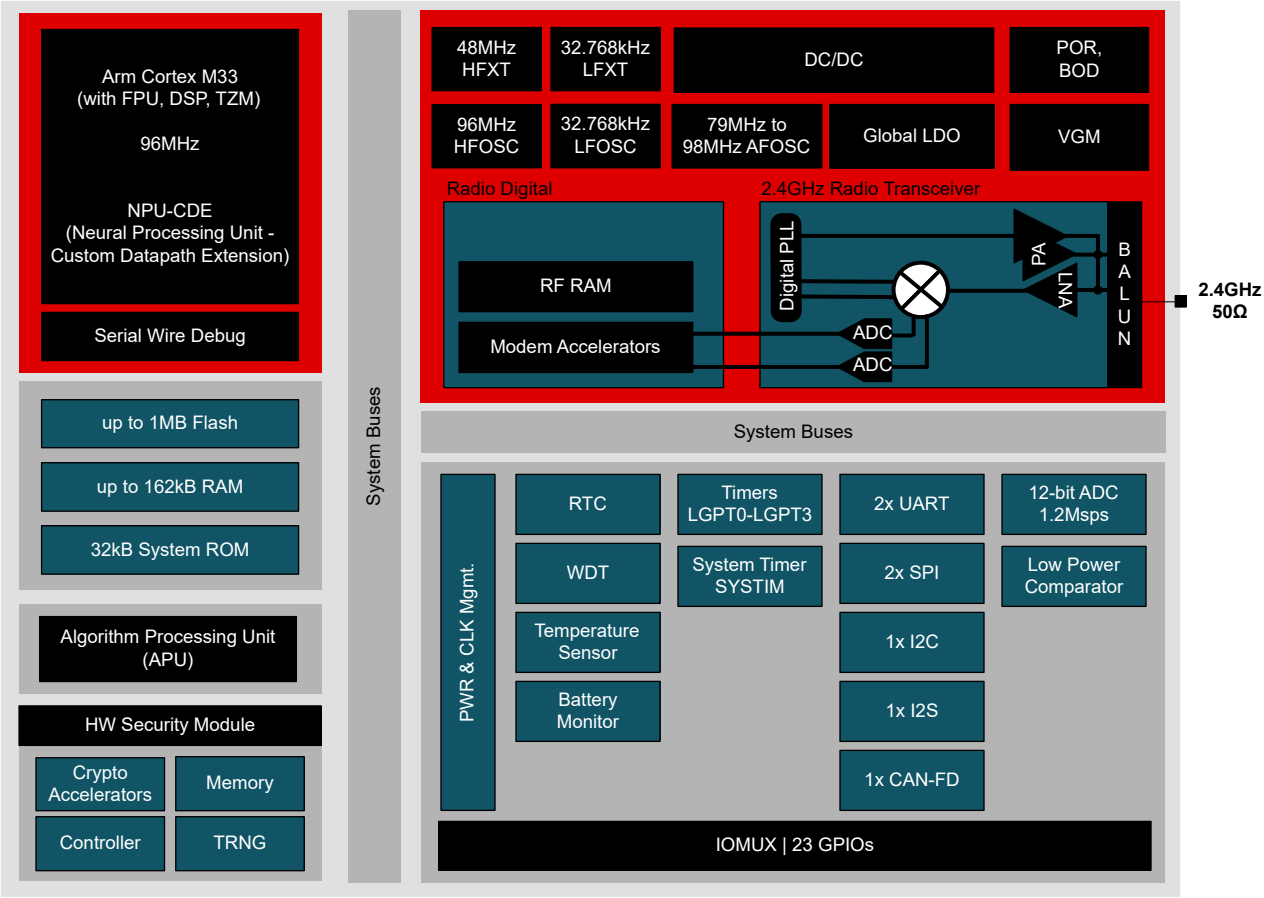

Figure 4-1. Functional Block Diagram

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5 Device Comparison

IP	CC2745P10-Q1	CC2745R10-Q1	CC2745R7-Q1	CC2744R7-Q1
CM33 (MCU)	✓	✓	✓	✓
APU (Algorithm Processing Unit) (Bluetooth Channel Sounding Post-processing)	✓	✓	✓	✓
CAN-FD Controller	✓	✓	✓	
HSM	✓	✓	✓	✓
VGM	✓	✓	✓	✓
2x UART, 2x SPI, 1x I2C, 1x I2S	✓	✓	✓	✓
+10dBm PA	✓	✓	✓	✓
+20dBm PA	✓			
ADC12	✓	✓	✓	✓
Flash (KB)	1024(1)	1024(1)	768(1)	768(1)
SRAM (KB) (parity disabled)	162	162	128	128
SRAM (KB) (parity enabled)	144	144	128	128
GPIO	23	23	23	23
QFN PKG Size (mm x mm)	6 x 6	6 x 6	6 x 6	6 x 6

(1) 96KB of the device flash memory is reserved for the HSM firmware.

6 Pin Configuration and Functions

6.1 Pin Diagram—RHA package

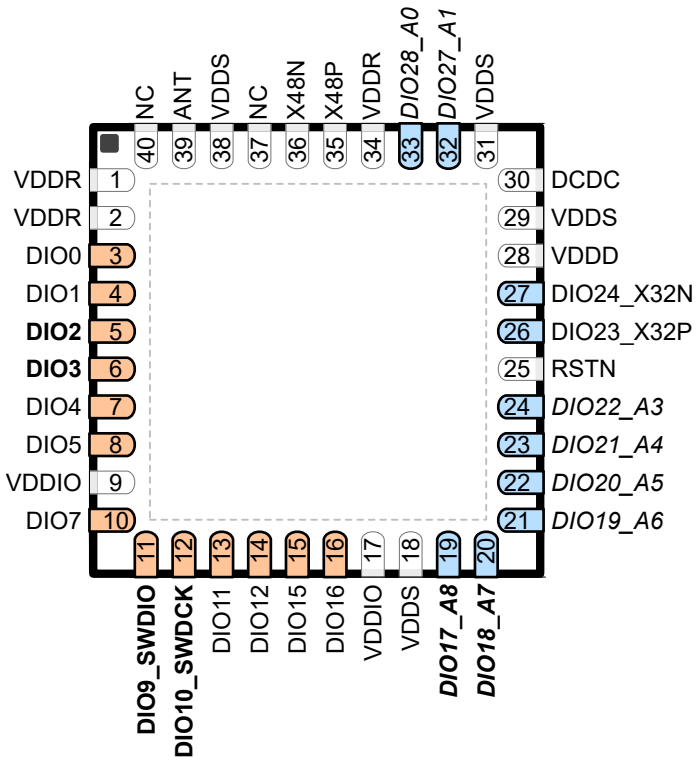

Figure 6-1. RHA (6mm × 6mm) Pinout, 0.5mm Pitch (Top View)

The following I/O pins marked in Figure 6-1 in **bold** have high-drive capabilities:

- Pin 5, DIO2
- Pin 6, DIO3
- Pin 11, DIO9_SWDIO
- Pin 12, DIO10_SWDCK
- Pin 19, DIO17_A8
- Pin 20, DIO18_A7

The following I/O pins marked in Figure 6-1 in *italics* have analog capabilities:

- Pin 19, DIO17_A8
- Pin 20, DIO18_A7
- Pin 21, DIO19_A6
- Pin 22, DIO20_A5
- Pin 23, DIO21_A4
- Pin 24, DIO22_A3
- Pin 32, DIO27_A1
- Pin 33, DIO28_A0

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The following I/O pins marked in Figure 6-1 in *orange color* are supplied by VDDIO:

- Pin 3, DIO0
- Pin 4, DIO1
- Pin 5, DIO2
- Pin 6, DIO3
- Pin 7, DIO4
- Pin 8, DIO5
- Pin 10, DIO7
- Pin 11, DIO9_SWDIO
- Pin 12, DIO10_SWDCK
- Pin 13, DIO11
- Pin 14, DIO12
- Pin 15, DIO15
- Pin 16, DIO16

The following I/O pins marked in Figure 6-1 in *blue color* are supplied by VDDS:

- Pin 19, DIO17_A8
- Pin 20, DIO18_A7
- Pin 21, DIO19_A6
- Pin 22, DIO20_A5
- Pin 23, DIO21_A4
- Pin 24, DIO22_A3
- Pin 26, DIO23_X32P
- Pin 27, DIO24_X32N
- Pin 32, DIO27_A1
- Pin 33, DIO28_A0

6.2 Signal Descriptions – RHA Package

Table 6-1. Signal Descriptions—RHA Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDR	1	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(1) (2) (3)
VDDR	2	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(1) (2) (3)
DIO0	3	I/O	Digital	GPIO
DIO1	4	I/O	Digital	GPIO
DIO2	5	I/O	Digital	GPIO, high-drive capability
DIO3	6	I/O	Digital	GPIO, high-drive capability
DIO4	7	I/O	Digital	GPIO
DIO5	8	I/O	Digital	GPIO
VDDIO	9	—	Power	1.71V to 3.8V split rail I/O supply(4)
DIO7	10	I/O	Digital	GPIO
DIO9_SWDIO	11	I/O	Digital	GPIO, SWD interface: mode select or SWDIO, high-drive capability
DIO10_SWDCK	12	I/O	Digital	GPIO, SWD interface: clock, high-drive capability
DIO11	13	I/O	Digital	GPIO
DIO12	14	I/O	Digital	GPIO
DIO15	15	I/O	Digital	GPIO
DIO16	16	I/O	Digital	GPIO
VDDIO	17	—	Power	1.71V to 3.8V split rail I/O supply(4)
VDDS	18	—	Power	1.71V to 3.8V supply(4)
DIO17_A8	19	I/O	Digital or Analog	GPIO, analog capability, high-drive capability
DIO18_A7	20	I/O	Digital or Analog	GPIO, analog capability, high-drive capability
DIO19_A6	21	I/O	Digital or Analog	GPIO, analog capability
DIO20_A5	22	I/O	Digital or Analog	GPIO, analog capability
DIO21_A4	23	I/O	Digital or Analog	GPIO, analog capability
DIO22_A3	24	I/O	Digital or Analog	GPIO, analog capability
RSTN	25	I	Digital	Reset, active low. No internal pullup resistor
DIO23_X32P	26	I/O	Digital or Analog	GPIO, 32kHz crystal oscillator pin 1, Optional TCXO input
DIO24_X32N	27	I/O	Digital or Analog	GPIO, 32kHz crystal oscillator pin 2
VDDD	28	—	Power	For decoupling of internal 1.32V regulated core-supply. Connect an external 1µF decoupling capacitor.(1)
VDDS	29	—	Power	1.71V to 3.8V supply. Connect an external 10 µF decoupling capacitor.(4)
DCDC	30	—	Power	Switching node of internal DC/DC converter(4)
VDDS	31	—	Power	1.71V to 3.8V supply(4)
DIO27_A1	32	I/O	Digital or Analog	GPIO, analog capability
DIO28_A0	33	I/O	Digital or Analog	GPIO, analog capability
VDDR	34	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO. Connect an external 10 µF decoupling capacitor.(1) (2) (3)
X48P	35	—	Analog	48MHz crystal oscillator pin 1
X48N	36	—	Analog	48MHz crystal oscillator pin 2
NC	37	—	—	No Connect
VDDS	38	—	Power	1.71V to 3.8V supply(4)

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Table 6-1. Signal Descriptions—RHA Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
ANT	39	—	RF	2.4GHz TX, RX
NC	40	—	—	No Connect (6)
EGP	—	—	GND	Ground – exposed ground pad(5)

(1) Do not supply external circuitry from this pin.
(2) VDDR pins 1, 2, and 34 must be tied together on the PCB.
(3) Output from internal DC/DC and LDO is trimmed to 1.5V.
(4) For more details, see the technical reference manual listed in Documentation Support.
(5) EPG is the only ground connection for the device. A good electrical connection to the device ground on a printed circuit board (PCB) is imperative for proper device operation.
(6) This pin is not connected to the die. In LP-EM-CC2745R10-Q1, LP-EM-CC2755P10 reference design, this pin is connected to the ground to give better shielding on the antenna path.

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6.3 Connections for Unused Pins and Modules—RHA Package

Table 6-2. Connections for Unused Pins—RHA Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO (digital)	DIOn	3–8 10 13–16	NC, GND, or VDDS	NC
SWD	DIO9_SWDIO	11	NC, GND, or VDDS	GND or VDDS
	DIO10_SWDCK	12	NC, GND, or VDDS	GND or VDDS
GPIO (digital or analog)	DIOn_Am	19–24 32–33	NC, GND, or VDDS	NC
32.768kHz crystal	DIO23_X32P	26	NC or GND	NC
	DIO24_X32N	27		
DC/DC converter(2)	DCDC	30	NC	NC
	VDDS	18, 29, 31, 38	VDDS	VDDS
Split Rail I/O supply	VDDIO	9, 17	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC and VDDR can be removed. VDDR must still be connected and the 10 µF capacitor must be kept on the VDDR net.

6.4 RHA Peripheral Pin Mapping

Table 6-3. RHA (QFN40) Peripheral Pin Mapping

PIN NO. QFN40	PIN NAME	SIGNAL NAME	SIGNAL TYPE[1]	PIN MUX ENCODING	SIGNAL DIRECTION
1	VDDR	VDDR	—	N/A	N/A
2	VDDR	VDDR	—	N/A	N/A
3	DIO0	GPIO0	I/O	0	I/O
		T0C0		1	I/O
		T1F		2	O
		T3C0N		3	O
		LPCO		4	O
		T1C0		5	I/O
4	DIO1	GPIO1	I/O	0	I/O
		CAN0TX		1	O
		T1C0		2	I/O
		T2C0		3	I/O
		UART0TXD		4	O
		T1C1		5	I/O
		DTB15		7	O
5	DIO2	GPIO2	I/O	0	I/O
		CAN0RX		1	I
		T1C1		2	I/O
		T0PE		3	O
		UART0RXD		4	I
		T1C2		5	I/O
		DTB14		7	O
6	DIO3	GPIO3	I/O	0	I/O
		SPI0SCLK		1	I/O
		I2S0SCLK		2	I/O
		T2PE		3	O
		UART1TXD		4	O
		T2C0		5	I/O
		DTB13		7	O
7	DIO4	GPIO4	I/O	0	I/O
		SPI0PICO		1	I/O
		SPI0POCI		2	I/O
		T1C2		3	I/O
		UART1RXD		4	I
		T2C1		5	I/O
		DTB12		7	O
8	DIO5	GPIO5	I/O	0	I/O
		SPI0POCI		1	I/O
		SPI0PICO		2	I/O
		T2C1		3	I/O
		T3C1N		4	O
		T2C2		5	I/O
		DTB11		7	O

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Table 6-3. RHA (QFN40) Peripheral Pin Mapping (continued)

PIN NO. QFN40	PIN NAME	SIGNAL NAME	SIGNAL TYPE[1]	PIN MUX ENCODING	SIGNAL DIRECTION
9	VDDIO	VDDIO	—	N/A	N/A
10	DIO7	GPIO7	I/O	0	I/O
		SPI0CSN		1	I/O
		T2C2		2	I/O
		I2S0WS		3	I/O
		T3C2N		4	O
		DTB10		7	O
11	DIO9_SWDIO	GPIO9	I/O	0	I/O
		T0C1		1	I/O
		T2C0N		2	O
		I2S0SD0		3	I/O
		T0PE		4	O
		I2C0SCL		5	I/O
12	DIO10_SWDCK	GPIO10	I/O	0	I/O
		T0C2		1	I/O
		T2C1N		2	O
		I2S0SD1		3	I/O
		T2PE		4	O
		I2C0SDA		5	I/O
13	DIO11	GPIO11	I/O	0	I/O
		SPI1POCI		1	I/O
		SPI1PICO		2	I/O
		SWO		3	O
		T3C0		4	I/O
		T1F		5	O
		DTB9		7	O
14	DIO12	GPIO12	I/O	0	I/O
		SPI1PICO		1	I/O
		SPI1POCI		2	I/O
		T2C2N		3	O
		T3C1		4	I/O
		T3C2		5	I/O
		DTB8		7	O
15	DIO15	GPIO15	I/O	0	I/O
		SPI1SCLK		1	I/O
		T3C2		2	I/O
		T1C0N		3	O
		LPCO		4	O
		T3C1		5	I/O

Table 6-3. RHA (QFN40) Peripheral Pin Mapping (continued)

PIN NO. QFN40	PIN NAME	SIGNAL NAME	SIGNAL TYPE[1]	PIN MUX ENCODING	SIGNAL DIRECTION
16	DIO16	GPIO16	I/O	0	I/O
		I2S0MCLK		1	O
		SPI1CSN		2	I/O
		EXTCI		3	I
		T1F		4	I
		T3C0		5	I/O
		DTB7		7	O
17	VDDIO	VDDIO	—	N/A	N/A
18	VDDS	VDDS	—	N/A	N/A
19	DIO17_A8	GPIO17	I/O	0	I/O
		I2S0SCLK		1	I/O
		UART0RTS		2	O
		CAN0TX		3	O
		T0C0		4	I/O
		LRFD0		5	O
		ADC8		6	I
		DTB6		7	O
20	DIO18_A7	GPIO18	I/O	0	I/O
		I2S0WS		1	I/O
		UART0CTS		2	I
		CAN0RX		3	I
		T0C1		4	I/O
		LRFD1		5	O
		ADC7		6	I
		DTB5		7	O
21	DIO19_A6	GPIO19	I/O	0	I/O
		SPI0CSN		1	I/O
		UART0TXD		2	O
		UART0RXD		3	I
		I2S0SD0		4	I/O
		LRFD2		5	O
		ADC6/LPC+		6	I
		DTB4		7	O
22	DIO20_A6	GPIO20	I/O	0	I/O
		SPI0SCLK		1	I/O
		UART0RXD		2	I
		UART0TXD		3	O
		I2S0SD1		4	I/O
		LRFD3		5	O
		ADC5/LPC+/LPC-		6	I
		DTB3		7	O

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Table 6-3. RHA (QFN40) Peripheral Pin Mapping (continued)

PIN NO. QFN40	PIN NAME	SIGNAL NAME	SIGNAL TYPE[1]	PIN MUX ENCODING	SIGNAL DIRECTION
23	DIO21_A4	GPIO21	I/O	0	I/O
		SPI0PICO		1	I/O
		UART1TXD		2	O
		I2C0SCL		3	I/O
		T1C1N		4	O
		LRFD4		5	O
		ADC4/LPC+/LPC-		6	I
		DTB2		7	O
24	DIO22_A3	GPIO22	I/O	0	I/O
		SPI0POCI		1	I/O
		UART1RXD		2	I
		I2C0SDA		3	I/O
		T1C2N		4	O
		LRFD5		5	O
		ADC3		6	I
		DTB1		7	O
25	RTSN	RSTN	—	N/A	N/A
26	DIO23_X32P	GPIO23	I/O	0	I/O
		SPI1CSN		1	I/O
		UART1RTS		2	O
		LFCI		3	I
		T0C2		4	I/O
		T1C0		5	I/O
		LFXT_P		6	I
27	DIO24_X32N	GPIO24	I/O	0	I/O
		SPI1SCLK		1	I/O
		UART1CTS		2	I
		T0C0N		3	O
		LPCO		4	O
		T0C0		5	I/O
		LFXT_N		6	I
28	VDDD	VDDD	—	N/A	N/A
29	VDDS	VDDS	—	N/A	N/A
30	DCDC	DCDC	—	N/A	N/A
31	VDDS	VDDS	—	N/A	N/A
32	DIO27_A1	GPIO27	I/O	0	I/O
		SPI1PICO		1	I/O
		I2C0SCL		2	I/O
		CKMIN		3	I
		T0C1N		4	O
		LRFD6		5	O
		ADC1/AREF+		6	I
		DTB0		7	O

Table 6-3. RHA (QFN40) Peripheral Pin Mapping (continued)

PIN NO. QFN40	PIN NAME	SIGNAL NAME	SIGNAL TYPE(1)	PIN MUX ENCODING	SIGNAL DIRECTION
33	DIO28_A0	GPIO28	I/O	0	I/O
		SPI1POCI		1	I/O
		I2C0SDA		2	I/O
		T3C0N		3	O
		T0C2N		4	O
		LRFD7		5	O
		ADC0/AREF-		6	I
34	VDDR	VDDR	—	N/A	N/A
35	X48P	X48P	—	N/A	N/A
36	X48N	X48N	—	N/A	N/A
37	NC	NC	—	N/A	N/A
38	VDDS	VDDS	—	N/A	N/A
39	ANT	ANT	—	N/A	N/A
40	NC	NC	—	N/A	N/A
—	EGP	GND	—	N/A	N/A

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

ADVANCE INFORMATION

6.5 RHA Peripheral Signal Descriptions

Table 6-4. RHA (QFN40) Peripheral Signal Descrpitions

FUNCTION	SIGNAL NAME	Pin No. QFN40	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
ADC	ADC0	33	I/O	I	ADC channel 0 input
	ADC1	32			ADC channel 1 input
	ADC3	24			ADC channel 3 input
	ADC4	23			ADC channel 4 input
	ADC5	22			ADC channel 5 input
	ADC6	21			ADC channel 6 input
	ADC7	20			ADC channel 7 input
	ADC8	19			ADC channel 8 input
ADC Reference	AREF+	32	I/O	I	ADC external voltage reference, positive terminal
	AREF-	33			ADC external voltage reference, negative terminal
CAN	CAN0TX	4	I/O	O	CAN0 tranmit data output
		19			
	CAN0RX	5	I/O	I	CAN0 receive data input
		20			
Clock	X32P	26	I/O	I	32kHz crystal oscillator pin 1
	X32N	27	I/O	I	32kHz crystal oscillator pin 2
	X48P	35	—	I	48MHz crystal oscillator pin 1, Optional TCXO input
	X48N	36	—	I	48MHz crystal oscillator pin 2
	CKMIN	32	I/O	I	HFOSC tracking loop reference clock input
	LFCI	26	I/O	I	GPIO input for low frequency clock input (LFXT bypass clock from pin) or optional TCXO
Comparator	LPCO	3	I/O	O	Low power comparator output
		15			
		27			
	LPC+	21	I/O	I	Low power comparator positive input terminal
		22			
		23			
	LPC-	22			Lower power comparator negative input terminal
		23			

Table 6-4. RHA (QFN40) Peripheral Signal Descrpitions (continued)

FUNCTION	SIGNAL NAME	Pin No. QFN40	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Digital Test Bus	DTB0	32	I/O	O	Digital test bus output 0
	DTB1	24			Digital test bus output 1
	DTB2	23			Digital test bus output 2
	DTB3	22			Digital test bus output 3
	DTB4	21			Digital test bus output 4
	DTB5	20			Digital test bus output 5
	DTB6	19			Digital test bus output 6
	DTB7	16			Digital test bus output 7
	DTB8	14			Digital test bus output 8
	DTB9	13			Digital test bus output 9
	DTB10	10			Digital test bus output 10
	DTB11	8			Digital test bus output 11
	DTB12	7			Digital test bus output 12
	DTB13	6			Digital test bus output 13
	DTB14	5			Digital test bus output 14
	DTB15	4			Digitial test bus output 15
GPIO	GPIO0	3	I/O	I/O	General-purpose input or output
	GPIO1	4			
	GPIO2	5			
	GPIO3	6			
	GPIO4	7			
	GPIO5	8			
	GPIO7	10			
	GPIO9	11			
	GPIO10	12			
	GPIO11	13			
	GPIO12	14			
	GPIO15	15			
	GPIO16	16			
	GPIO17	19			
	GPIO18	20			
	GPIO19	21			
	GPIO20	22			
	GPIO21	23			
	GPIO22	24			
	GPIO23	26			
	GPIO24	27			
	GPIO27	32			
	GPIO28	33			

ADVANCE INFORMATION

Table 6-4. RHA (QFN40) Peripheral Signal Descrpitions (continued)

FUNCTION	SIGNAL NAME	Pin No. QFN40	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
I^2C	I2C0SCL	11	I/O	I/O	I^2C clock
		23			
		32			
	I2C0SDA	12	I/O	I/O	I^2C data
		24			
		33			
I^2S	I2S0MCLK	16	I/O	O	I^2S main clock
	I2S0SCLK	6	I/O	I/O	I^2S serial clock
		19			
	I2S0WS	10	I/O	I/O	I^2S word select
		20			
	I2S0SD0	11	I/O	I/O	I^2S serial data 0
		21			
	I2S0SD1	12	I/O	I/O	I^2S serial data 1
		22			
	EXTCI	16	I/O	I	I^2S external clock
LRF Digital Output	LRFD0	19	I/O	O	LRF digital output 0
	LRFD1	20			LRF digital output 1
	LRFD2	21			LRF digital output 2
	LRFD3	22			LRF digital ouptut 3
	LRFD4	23			LRF digital output 4
	LRFD5	24			LRF digital output 5
	LRFD6	32			LRF digital output 6
	LRFD7	33			LRF digital output 7
Power	VDDR	1	—	—	Internal supply
		2			
		34			
	VDDS	18	—	—	1.71V to 3.8V DIO supply
		29			
		31			
		38			
	VDDD	28	—	—	For decoupling of internal 1.32-V regulated core-supply.
	VDDIO	9	—	—	1.71V to 3.8V split rail I/O supply
		17			
	DCDC	30	—	—	Switching node of internal DC/DC converter
Reset	RSTN	25	—	—	Global master device reset (active low)
RF	ANT	39	—	—	50 ohm RF port

Table 6-4. RHA (QFN40) Peripheral Signal Descrpitions (continued)

FUNCTION	SIGNAL NAME	Pin No.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN40			
SPI	SPI0SCLK	6	I/O	I/O	SPI0 clock
		22			
	SPI0POCI	7	I/O	I/O	SPI0 peripheral out controller in
		8			
		24			
	SPI0CSN	10	I/O	I/O	SPI0 chip-select
		21			
	SPI0PICO	7	I/O	I/O	SPI0 peripheral in controller out
		8			
		23			
	SPI1SCLK	15	I/O	I/O	SPI1 clock
		27			
	SPI1POCI	13	I/O	I/O	SPI1 peripheral out controller in
		14			
		33			
	SPI1CSN	16	I/O	I/O	SPI1 chip select
		26			
	SPI1PICO	13	I/O	I/O	SPI1 peripheral in controller out
		14			
		32			
SWD	SWDIO	11	I/O	I/O	Serial wire data input/output
	SWDCK	12	I/O	I	Serial wire clock input
	SWO	13	I/O	O	Serial wire output

ADVANCE INFORMATION

Table 6-4. RHA (QFN40) Peripheral Signal Descrpitions (continued)

FUNCTION	SIGNAL NAME	Pin No.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN40			
Timers - Capture/ Compare	T0C0	3	I/O	I/O	Capture input-0 / compare output-0 of Timer-0
		19			
		27			
	T0C1	11			Capture input-1 / compare output-1 of Timer-0
		20			
	T0C2	12			Capture input-2 / compare output-2 of Timer-0
		26			
	T1C0	3	I/O	I/O	Capture input-0 / compare output-0 of Timer-1
		4			
		26			
	T1C1	4			Capture input-1 / compare output-1 of Timer-1
		5			
	T1C2	5			Capture input-2 / compare output-2 of Timer-1
		7			
	T2C0	4	I/O	I/O	Capture input-0 / compare output-0 of Timer-2
		6			
	T2C1	7			Capture input-1 / compare output-1 of Timer-2
		8			
	T2C2	8			Capture input-2 / compare output-2 of Timer-2
		10			
	T3C0	13	I/O	I/O	Capture input-0 / compare output-0 of Timer-3
		16			
	T3C1	14			Capture input-1 / compare output-1 of Timer-3
		15			
	T3C2	14			Capture input-2 / compare output-2 of Timer-3
		15			
Timers - Complementary Capture/PWM	T0C0N	27	I/O	O	Complementary compare/PWM output-0 from Timer-0
	T0C1N	32			Complementary compare/PWM output-1 from Timer-0
	T0C2N	33			Complementary compare/PWM output-2 from Timer-0
	T1C0N	15	I/O	O	Complementary compare/PWM output-0 from Timer-1
	T1C1N	23			Complementary compare/PWM output-1 from Timer-1
	T1C2N	24			Complementary compare/PWM output-2 from Timer-1
	T2C0N	11	I/O	O	Complementary compare/PWM output-0 from Timer-2
	T2C1N	12			Complementary compare/PWM output-1 from Timer-2
	T2C2N	14			Complementary compare/PWM output-2 from Timer-2
	T3C0N	3	I/O	O	Complementary compare/PWM output-0 from Timer-3
		33			
	T3C1N	8			Complementary compare/PWM output-1 from Timer-3
	T3C2N	10			Complementary compare/PWM output-2 from Timer-3
Timers - Fault input	T1F	3	I/O	I	Fault input for Timer-1
		13			
		16			

Table 6-4. RHA (QFN40) Peripheral Signal Descrpitions (continued)

FUNCTION	SIGNAL NAME	Pin No.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN40			
Timers - Prescaler Event	T2PE	6	I/O	O	Prescaler event ouput from Timer-2
		12			
	T0PE	5	I/O	O	Prescaler eveny ouput from Timer-0
		11			
UART	UART0TXD	4	I/O	O	UART0 TX data
		21			
		22			
	UART0RXD	5	I/O	I	UART0 RX data
		21			
		22			
	UART0CTS	20	I/O	I	UART0 clear-to-send input (active low)
	UART0RTS	19	I/O	O	UART0 request-to-send (active low)
	UART1TXD	6	I/O	O	UART1 TX data
		23			
	UART1RXD	7	I/O	I	UART1 RX data
		24			
	UART1CTS	27	I/O	I	UART1 clear-to-send input (active low)
	UART1RTS	26	I/O	O	UART1 request-to-send (active low)

ADVANCE INFORMATION

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

7.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, X is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RHA*).

For orderable part numbers of devices in the RHA (6mm × 6mm) package type, see the *Package Option Addendum* of this document, the Device Information in Section 3, the TI website (www.ti.com), or contact your TI sales representative.

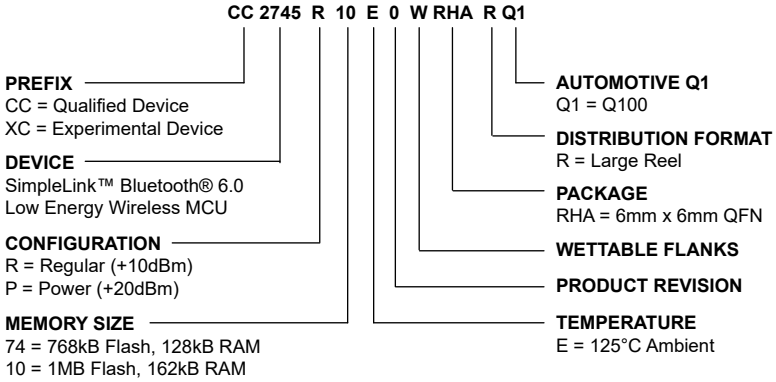

Figure 7-1. Device Nomenclature

7.2 Tools and Software

The CC274xR/P-Q1 devices are supported by a variety of software and hardware development tools.

Development Kit

CC2745R10-Q1 LaunchPad™ Development Kit	The CC2745R10-Q1 LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2745R10-Q1 SimpleLink Wireless MCU, which allows you to quickly evaluate and prototype 2.4GHz Bluetooth Low Energy wireless applications for up to +10dBm transmit

output power. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display and more.

Software

SimpleLink™ low power software development kit (SDK)

The SimpleLink low power software development kit (SDK) provides a complete package for the development of wireless applications on the CC27xx family of devices. The SDK includes a comprehensive software package for the CC274xR/P-Q1 device, including the following protocol stacks:

- Bluetooth Low Energy 6.0

The SimpleLink low power SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit https://www.ti.com/simplelink.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for Free-RTOS.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests send and receive packets between nodes
- Antenna and radiation tests set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

ADVANCE INFORMATION

CCS UniFlash — CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

7.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on Simplelink.

7.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder (CC274xR/Px-Q1). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer — Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC274xR/Px-Q1 Silicon Errata — The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC274xR-Q1 device are found on the device product folder (CC274xR/Px-Q1).

Technical Reference Manual (TRM)

CC27xx SimpleLink™ Wireless MCU TRM — The TRM provides a detailed description of all modules and peripherals available in the device family.

7.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.5 Trademarks

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7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2024	*	Initial Release

ADVANCE INFORMATION

9 Mechanical, Packaging, and Orderable Information

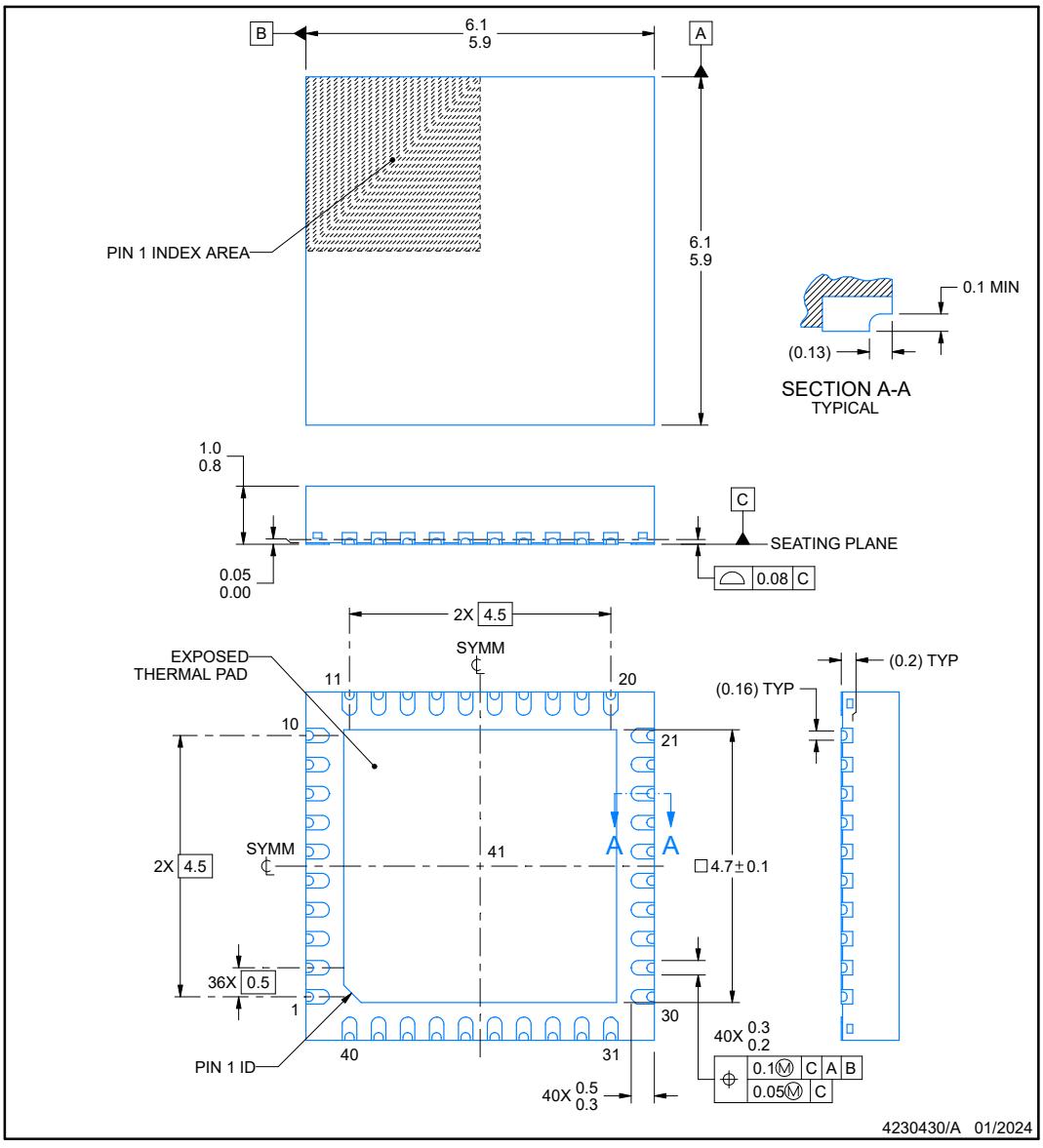
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RHA0040T

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

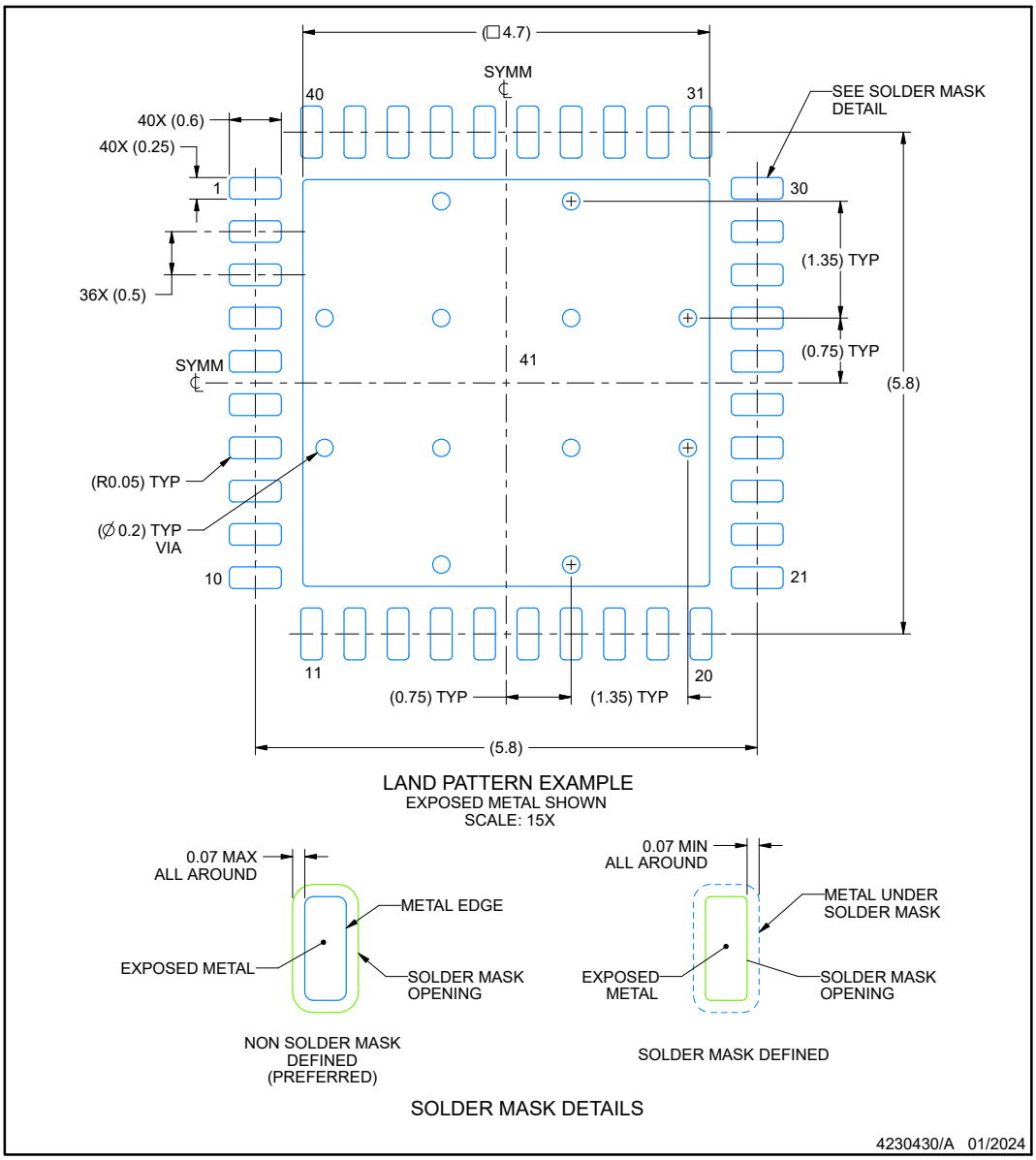
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RHA0040T — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



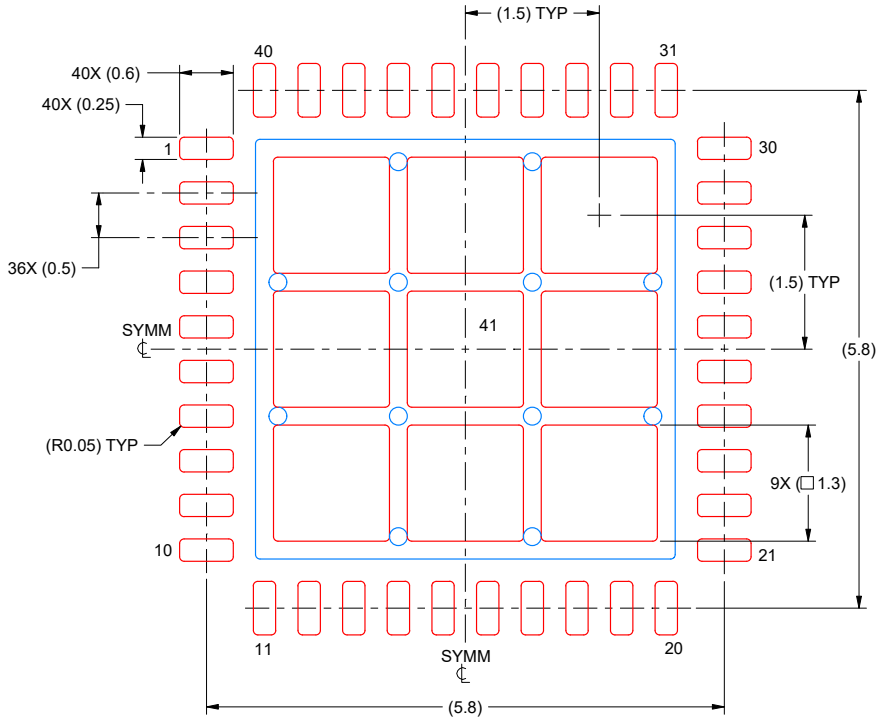
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0040T — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230430/A 01/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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