

# CSD15380F3 20-V N-Channel FemtoFET™ MOSFET

## 1 Features

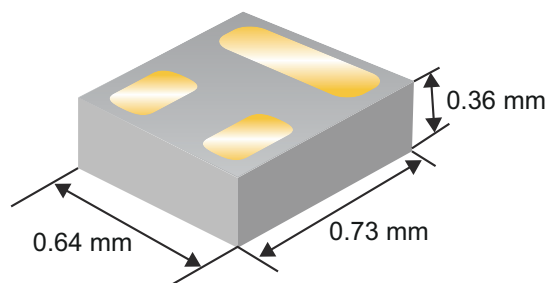
- Ultra-low  $C_{ISS}$  and  $C_{OSS}$
- Ultra-low  $Q_g$  and  $Q_{gd}$
- Ultra-small footprint
  - 0.73 mm × 0.64 mm
- Ultra-low profile
  - 0.36-mm max height
- Integrated ESD protection diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

## 2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

## 3 Description

This 20-V, 990-mΩ, N-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. Ultra-low capacitance improves switching speeds. When used in data line applications, the low capacitance minimizes noise coupling. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.



Typical Part Dimensions

## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	20	V
$Q_g$	Gate Charge Total (4.5 V)	0.216	nC
$Q_{gd}$	Gate Charge Gate-to-Drain	0.027	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}$	2220
		$V_{GS} = 4.5\text{ V}$	1170
		$V_{GS} = 8\text{ V}$	990
$V_{GS(th)}$	Threshold Voltage	1.1	V

## Device Information<sup>(1)</sup>

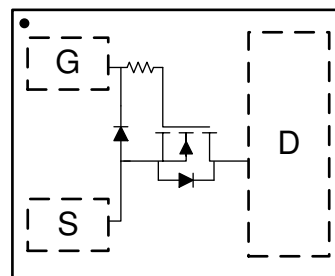
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD15380F3	3000	7-Inch Reel	Femto	Tape and Reel
CSD15380F3T	250		0.73-mm × 0.64-mm Land Grid Array (LGA)	

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ (unless otherwise stated)		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	20	V
$V_{GS}$	Gate-to-Source Voltage	10	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	0.9	A
	Continuous Drain Current <sup>(2)</sup>	0.5	
$I_{DM}$	Pulsed Drain Current <sup>(3)</sup>	1.6	A
$P_D$	Power Dissipation <sup>(1)</sup>	1.4	W
	Power Dissipation <sup>(2)</sup>	0.5	
$V_{(ESD)}$	Human-Body Model (HBM)	4	kV
	Charged-Device Model (CDM)	2	
$T_J, T_{stg}$	Operating Junction and Storage Temperature	–55 to 150	$^\circ\text{C}$

- (1) Typical  $R_{\theta JA} = 90^\circ\text{C/W}$  on 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB
- (2) Typical  $R_{\theta JA} = 255^\circ\text{C/W}$  on min Cu board
- (3) Pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .



Top View



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (July 2017) to Revision B (February 2022)</b>	<b>Page</b>
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.....	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm.....	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....	7
• Added FemtoFET Surface Mount Guide note.....	8

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## 5 Specifications

### 5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	20			V
$I_{DSS}$	Drain-to-Source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}$			50	nA
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 10\text{ V}$			25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = 2.5\ \mu\text{A}$	0.85	1.10	1.35	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 2.5\text{ V}, I_{DS} = 0.1\text{ A}$		2220	4000	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_{DS} = 0.1\text{ A}$		1170	1460	
		$V_{GS} = 8\text{ V}, I_{DS} = 0.1\text{ A}$		990	1190	
$g_{fs}$	Transconductance	$V_{DS} = 2\text{ V}, I_{DS} = 0.1\text{ A}$		0.64		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 10\text{ V}, f = 1\text{ MHz}$		8.1	10.5	pF
$C_{oss}$	Output capacitance			5.9	7.7	pF
$C_{riss}$	Reverse transfer capacitance			0.13	0.17	pF
$R_G$	Series gate resistance			9.6		$\Omega$
$Q_g$	Gate charge total (4.5 V)	$V_{DS} = 10\text{ V}, I_{DS} = 0.1\text{ A}$		0.216	0.281	nC
$Q_{gd}$	Gate charge gate-to-drain			0.027		nC
$Q_{gs}$	Gate charge gate-to-source			0.077		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			0.048		nC
$t_{d(on)}$	Turnon delay time			3		ns
$t_r$	Rise time	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_{DS} = 0.1\text{ A}, R_G = 0\ \Omega$		1		ns
$t_{d(off)}$	Turnoff delay time			7		ns
$t_f$	Fall time			7		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{SD} = 0.1\text{ A}, V_{GS} = 0\text{ V}$		0.85	1	V

### 5.2 Thermal Information

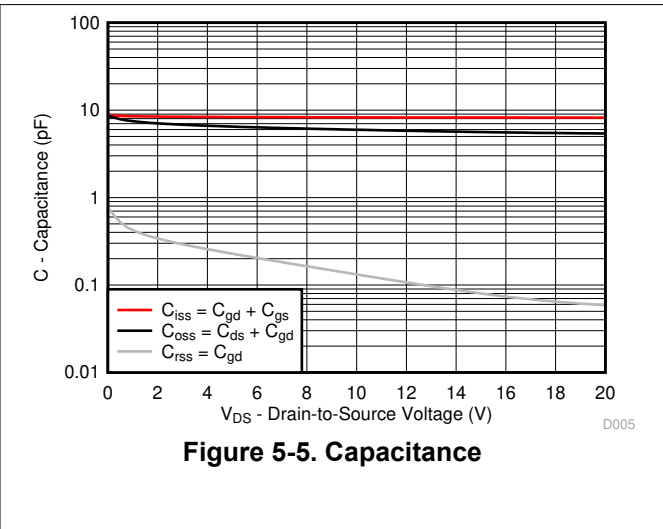
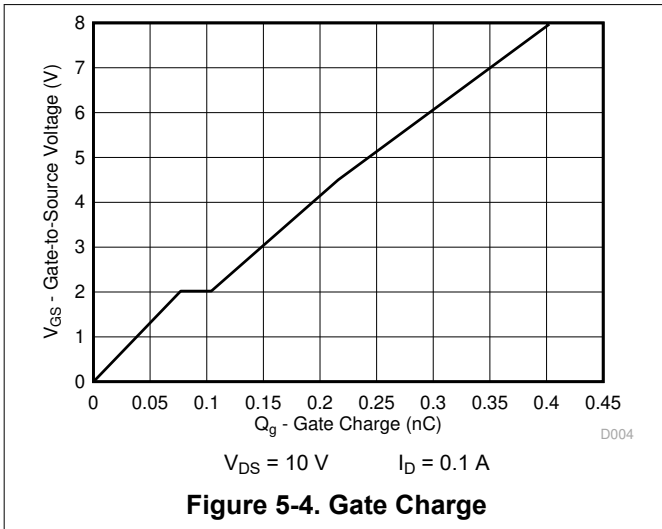
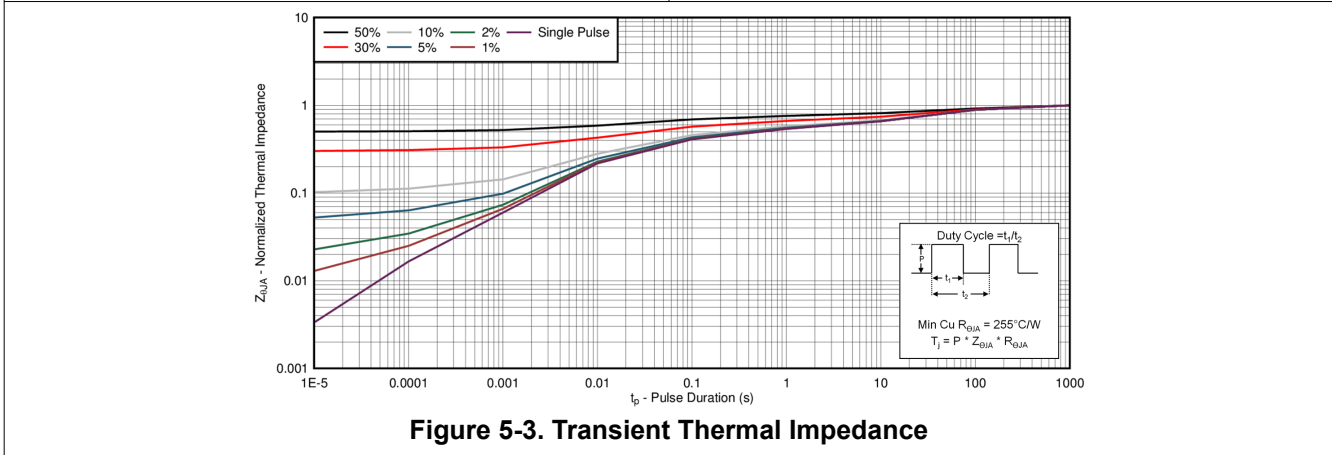
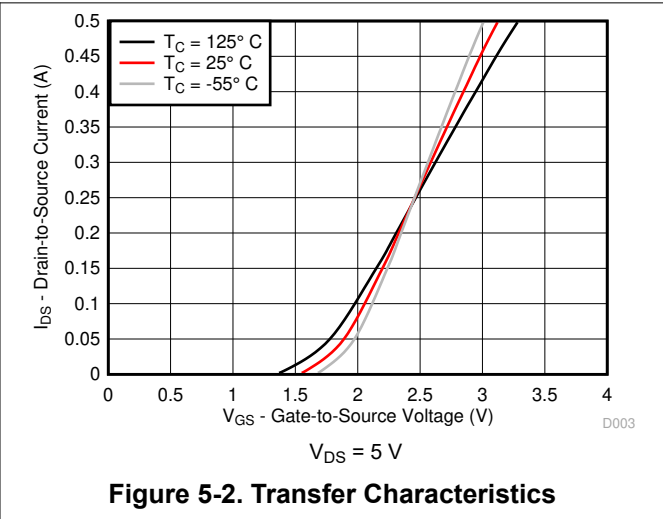
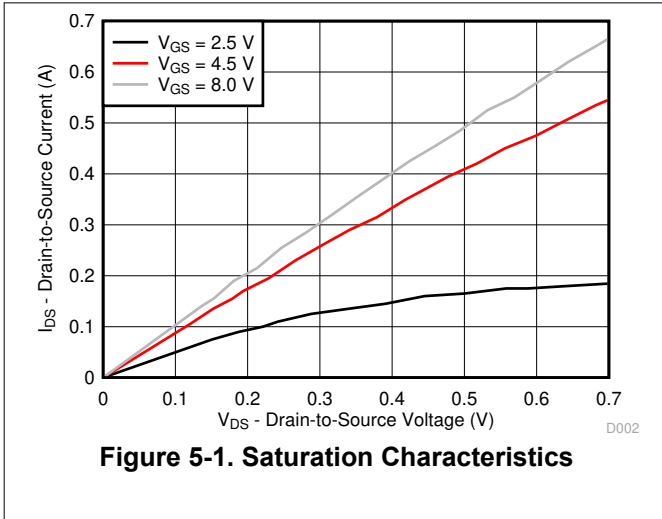
$T_A = 25^\circ\text{C}$  (unless otherwise stated)

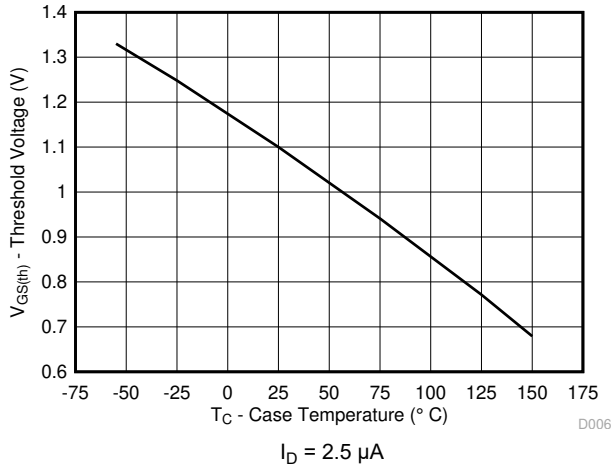
THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	90	$^\circ\text{C/W}$
	Junction-to-ambient thermal resistance <sup>(2)</sup>	255	

- (1) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.  
(2) Device mounted on FR4 material with minimum Cu mounting area.

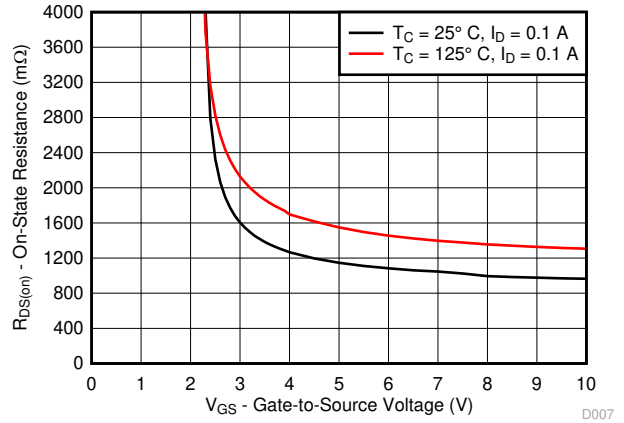
### 5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

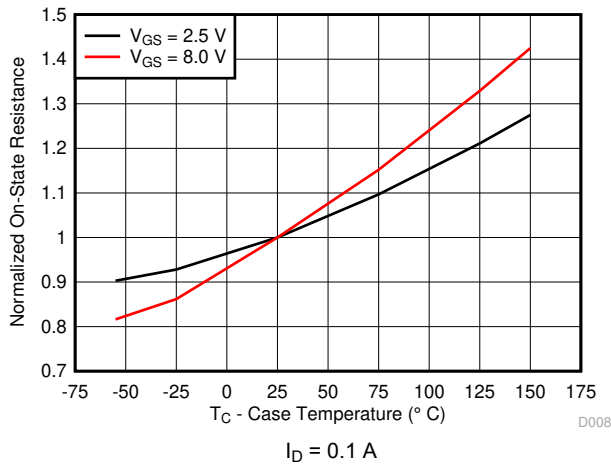




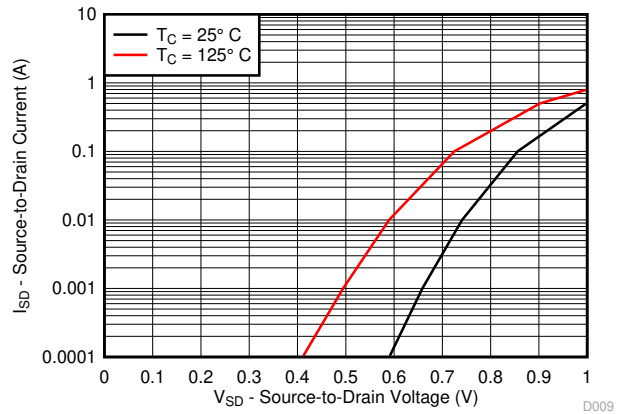
**Figure 5-6. Threshold Voltage vs Temperature**



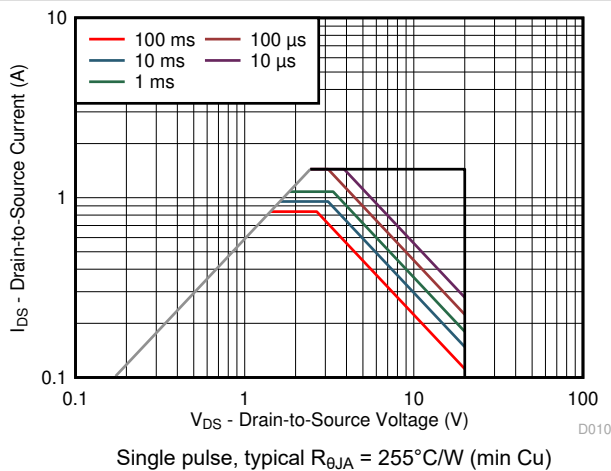
**Figure 5-7. On-State Resistance vs Gate-to-Source Voltage**



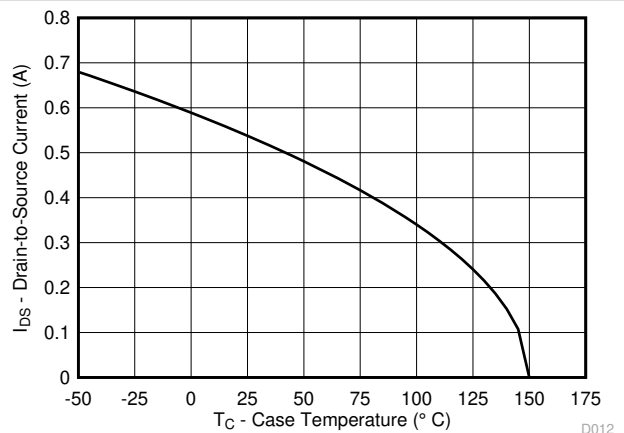
**Figure 5-8. Normalized On-State Resistance vs Temperature**



**Figure 5-9. Typical Diode Forward Voltage**



**Figure 5-10. Maximum Safe Operating Area**



**Figure 5-11. Maximum Drain Current vs Temperature**

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Trademarks

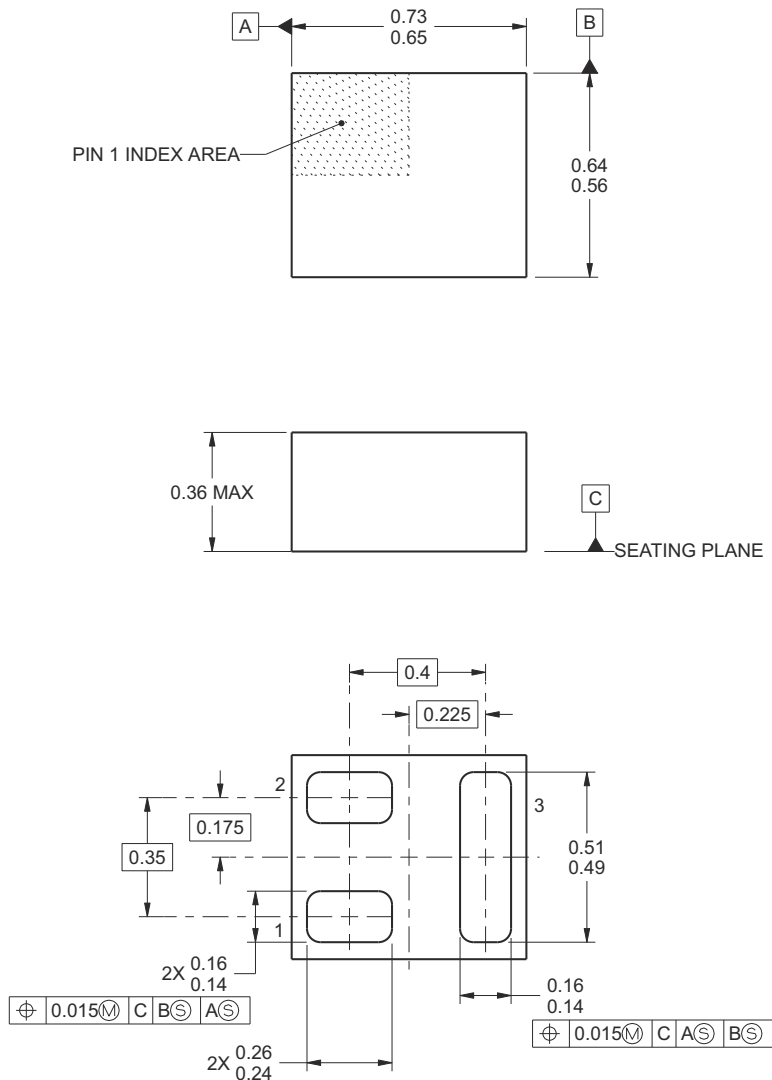
FemtoFET™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Mechanical Dimensions

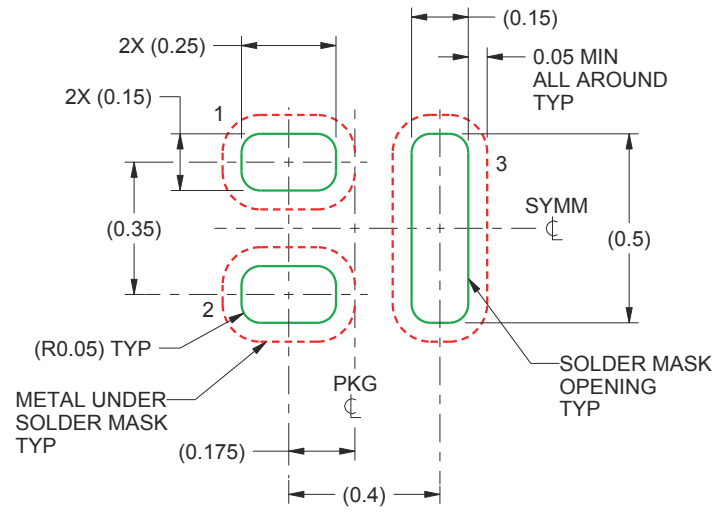


- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a lead-free solder land design.

**Table 7-1. Pin Configuration**

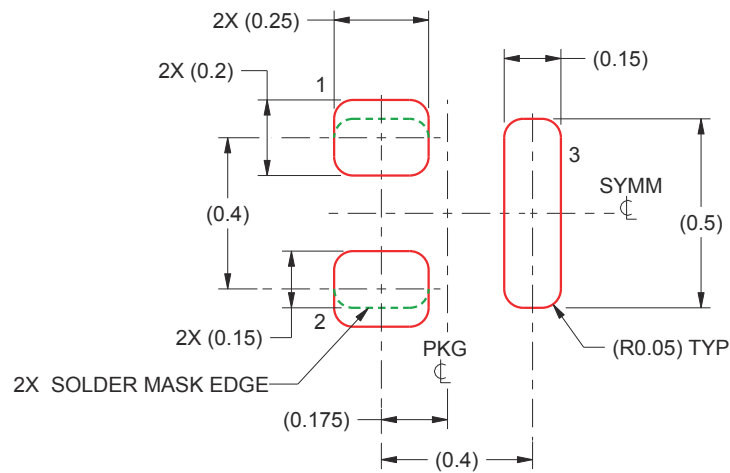
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

## 7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

## 7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD15380F3	ACTIVE	PICOSTAR	YJM	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	6	<a href="#">Samples</a>
CSD15380F3T	ACTIVE	PICOSTAR	YJM	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	6	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

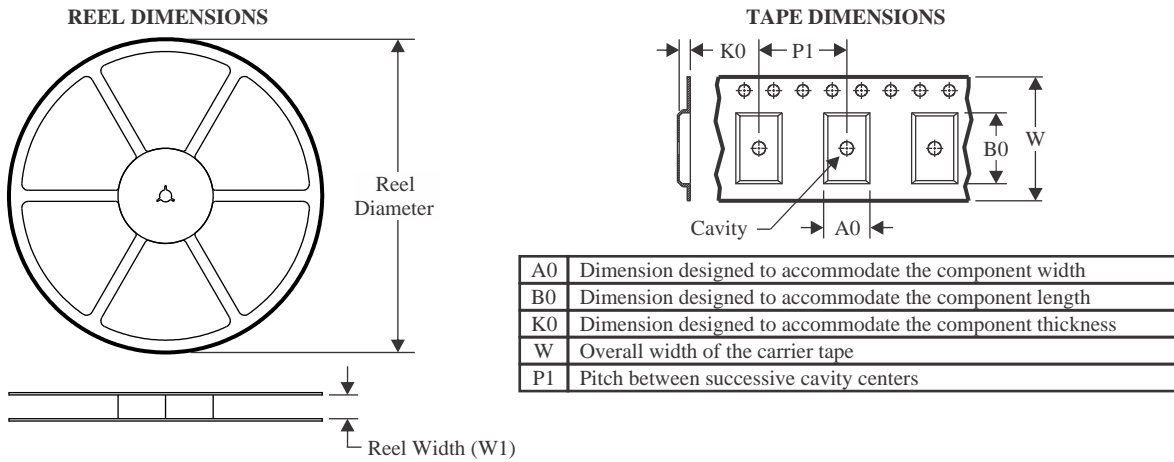
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

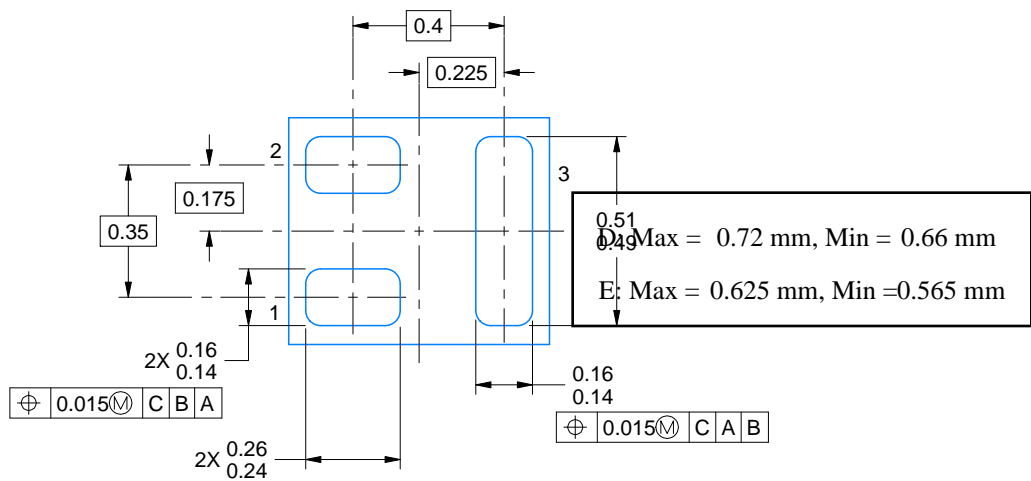
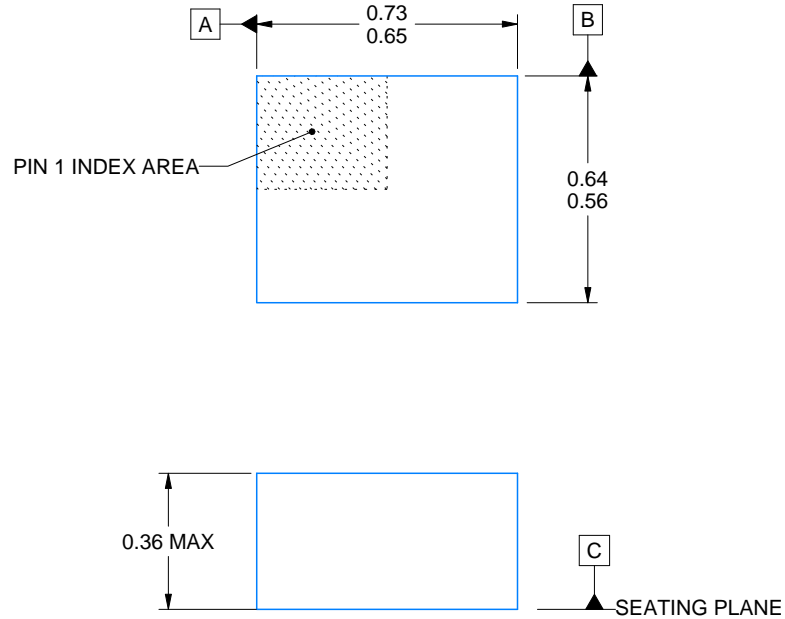

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD15380F3	PICOSTAR	YJM	3	3000	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
CSD15380F3T	PICOSTAR	YJM	3	250	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD15380F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD15380F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0



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NOTES:

PicoStar is a trademark of Texas Instruments.

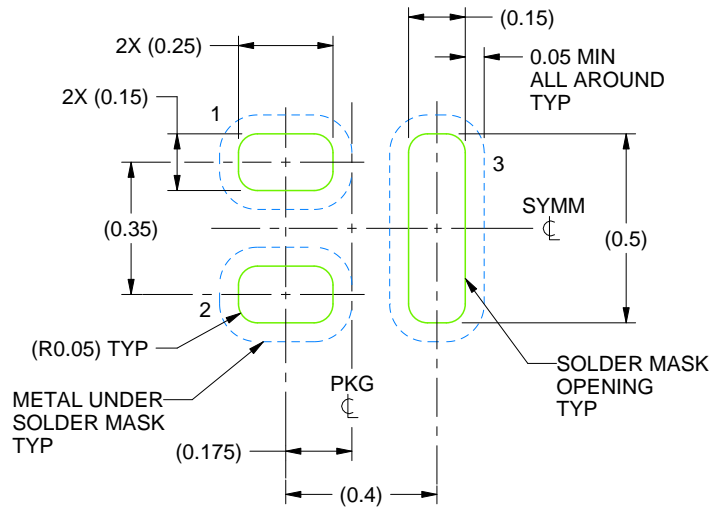
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

# EXAMPLE BOARD LAYOUT

YJM0003A

PicoStar™ - 0.36 mm max height

PicoStar™



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:50X

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NOTES: (continued)

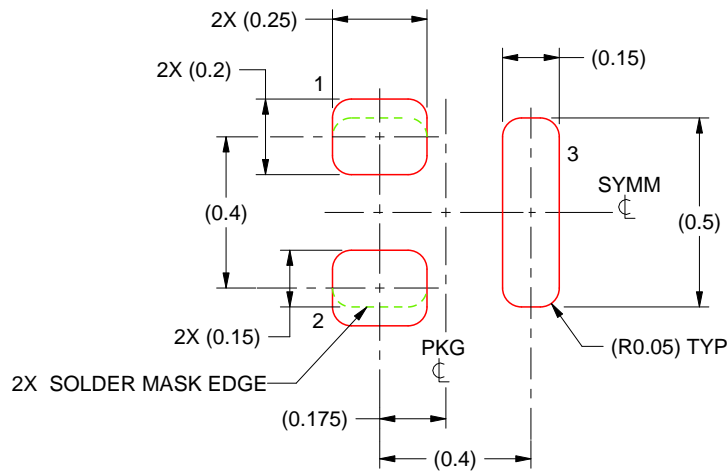
4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

YJM0003A

PicoStar™ - 0.36 mm max height

PicoStar™



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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