CSD95430RRB Synchronous Buck NexFET™ Smart Power Stage

1 Features

- Active current balancing between paralleled phases sharing a single PWM input
- Peak continuous current: 90-A
- System efficiency: > 95% at 30-A
- High-frequency operation: 1.25-MHz
- Diode emulation function to enable efficiency discontinuous conduction mode (DCM) operation
- Temperature compensated bi-directional current sense
- Analog temperature output
- Fault monitoring
- PWM signal compatible: 3.3 V and 5 V
- Tri-state PWM input
- Integrated bootstrap switch
- Optimized dead-time for shoot-through protection
- High-density industry common QFN 5-mm x 6-mm footprint
- Ultra-low inductance package
- System-optimized PCB footprint
- Thermally enhanced topside cooling
- RoHS compliant - lead-free terminal plating
- Halogen free

2 Applications

- Multiphase synchronous buck converters
  - Greater than 500-A
  - High-frequency
- Memory and graphic cards
- Data center and network switches
- Campus and branch switches
- Core and edge routers
- Hardware accelerator cards
- High-performance CPU/ASIC/FPGA power

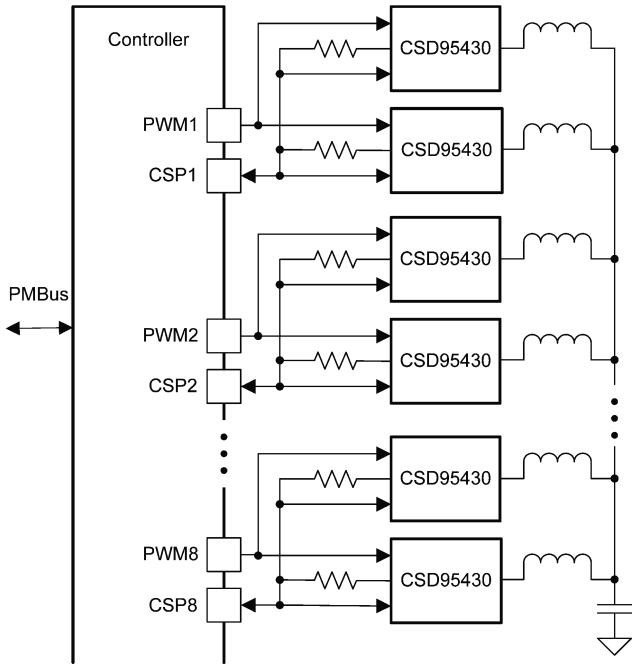
3 Description

The CSD95430RRB NexFET™ power stage is a highly optimized design for use in a high-power, high-density synchronous buck converter. This product integrates the driver IC and power MOSFETs to complete the power stage switching function. This combination produces high-current, high-efficiency, and high-speed switching capability in a small 5-mm × 6-mm outline package. It also integrates the accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design. This power stage features an active current balance feature which allows multiple power stages to be paralleled off a single PWM input. This enables phase multiplication for very high current applications without the need for a similarly high phase count controller. The active current balance ensures that the multiplied phases share current evenly so no significant derating of current capability is needed when paralleling phases.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CSD95430RRB	VQFN-CLIP	5.00 mm x 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2023	*	Initial release

5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

5.1 Documentation Support

5.1.1 Related Documentation

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.4 Trademarks

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5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 Package Option Addendum

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(4) (5)
CSD95430RRB	ACTIVE	QFN	RRB	41	2500	RoHS-Exempt & Green	CU NIPDAU/ Matte-Tin	Level-2-260C-1 YEAR	–55 to 150	95430RRB

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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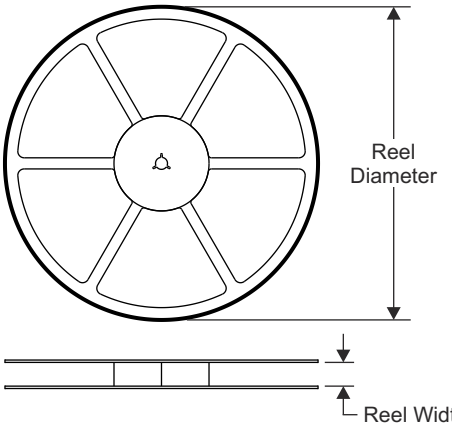
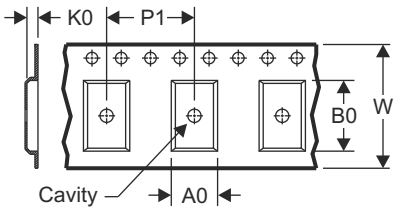
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

6.2 Tape and Reel Information

REEL DIMENSIONS

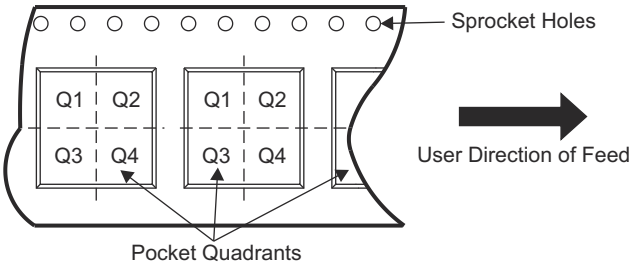


TAPE DIMENSIONS



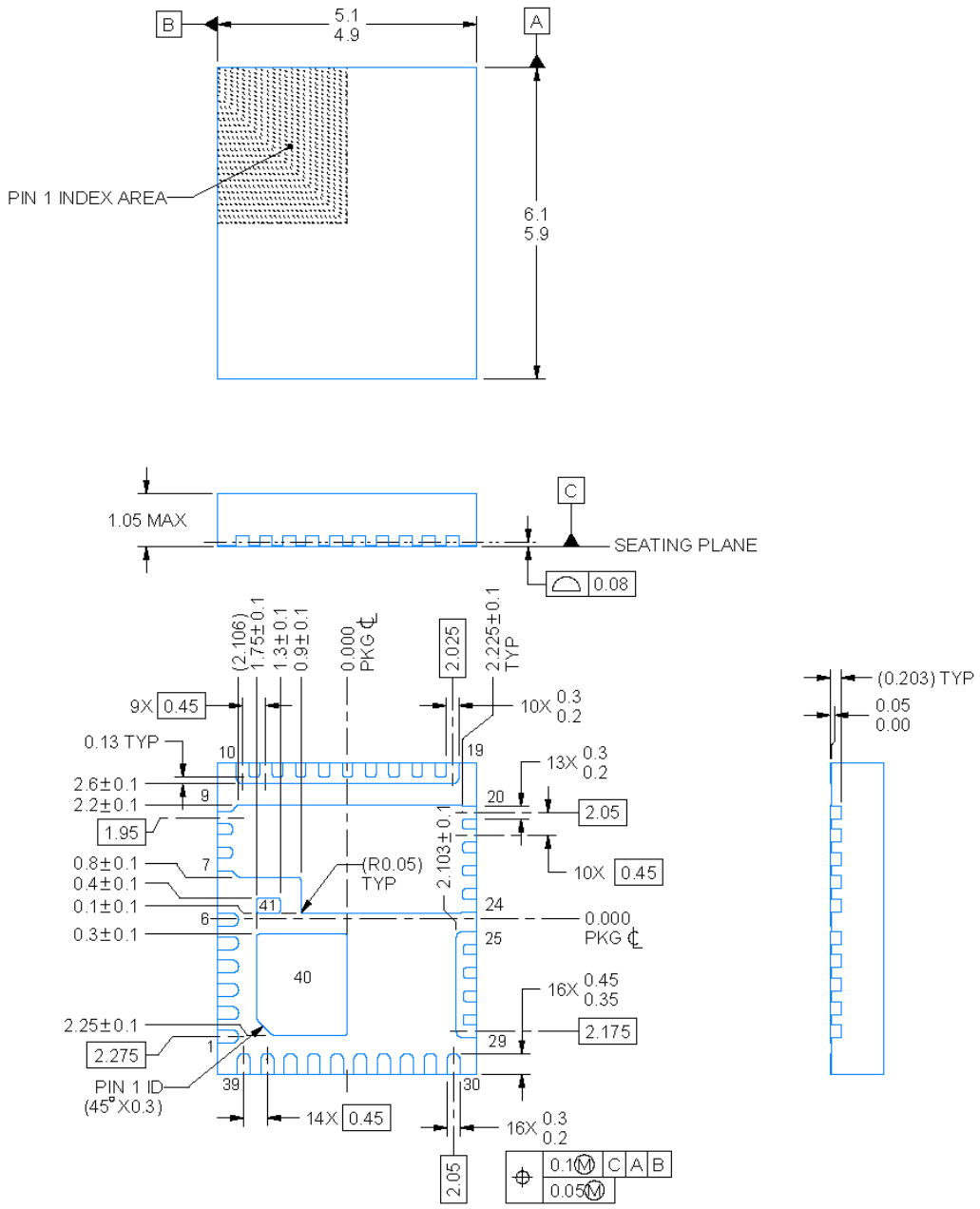
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



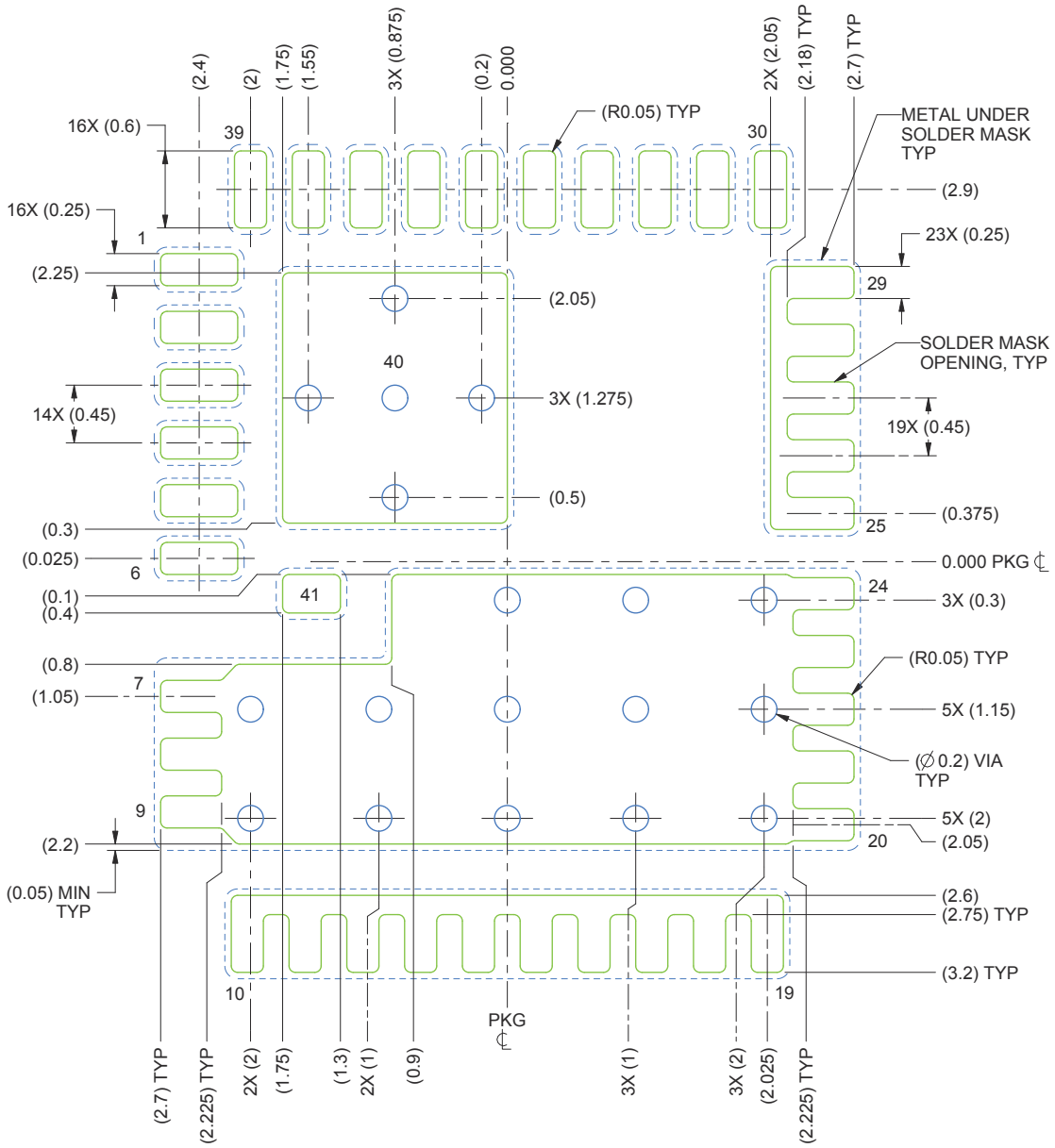
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95430RRB	QFN	RRB	41	2500	330	12.4	5.30	6.30	1.20	8.00	12.0	Q1

6.3 Mechanical Drawing



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

6.4 Recommended PCB Land Pattern

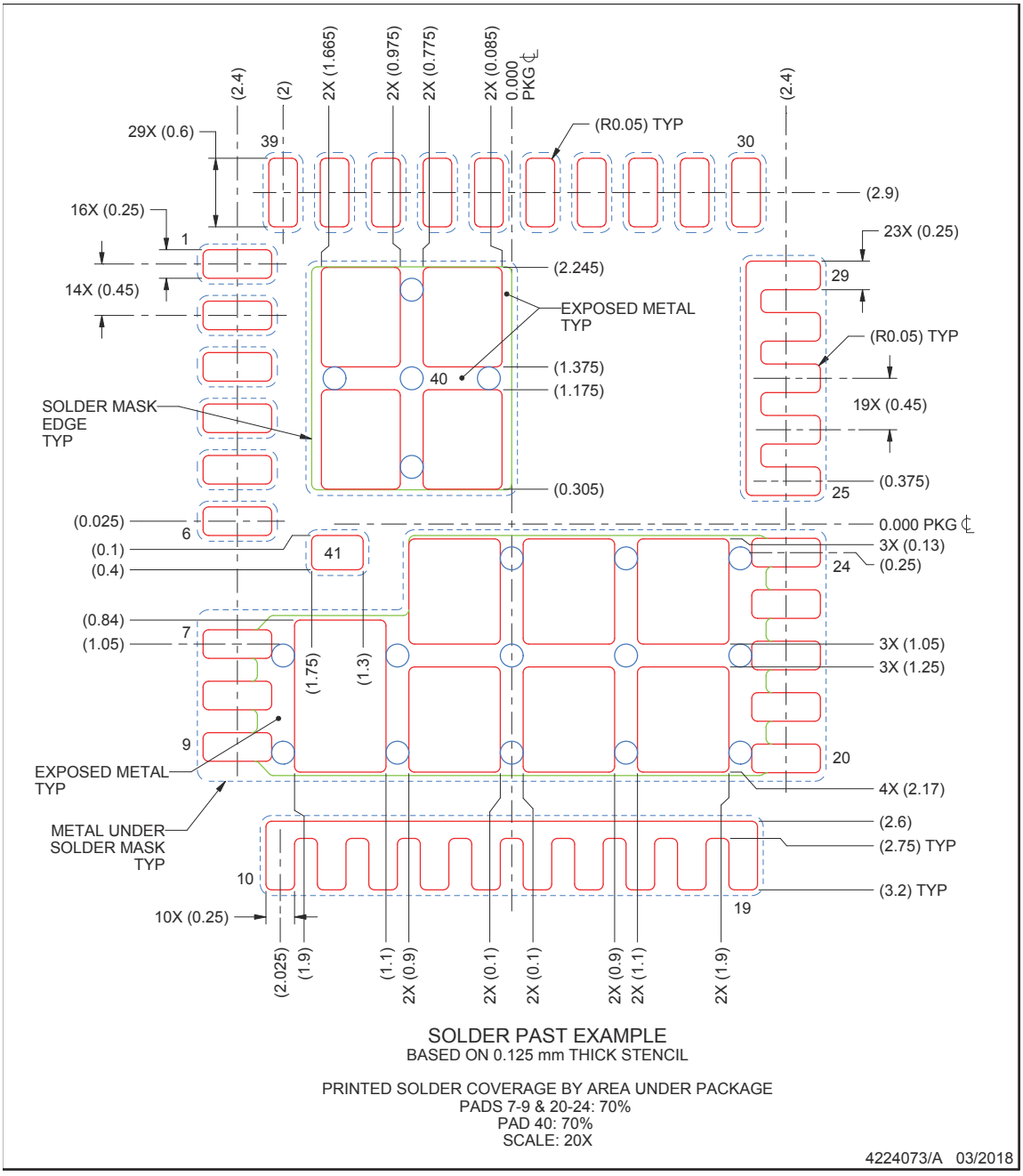


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 20X

4224073/A 03/2018

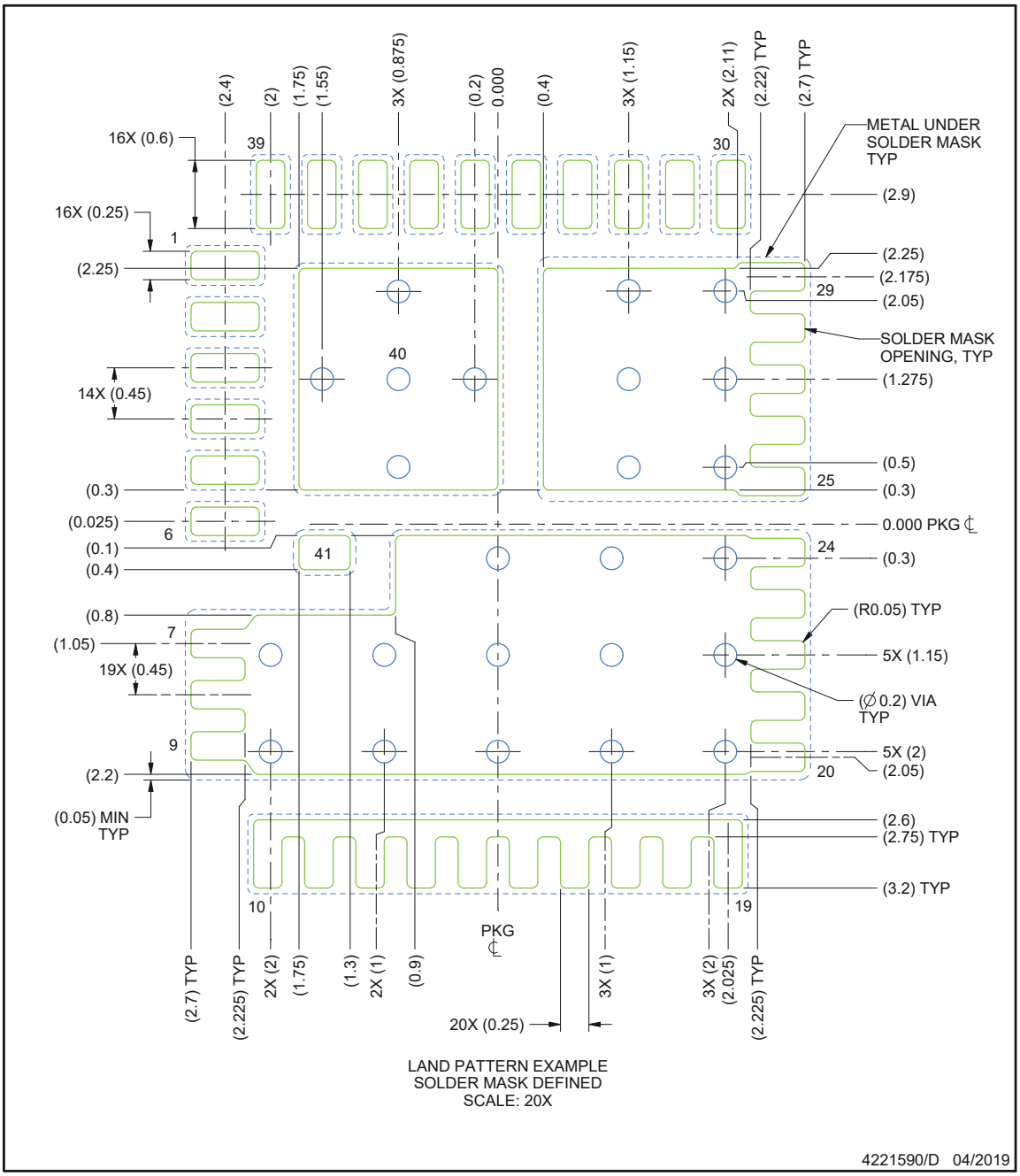
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is designed to be soldered to thermal pads on the board. For more information, see *QFN/SON PCB Attachment* (SLUA271).

6.5 Recommended Stencil Opening



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

6.6 Alternate Industry Standard Compatible PCB Land Pattern



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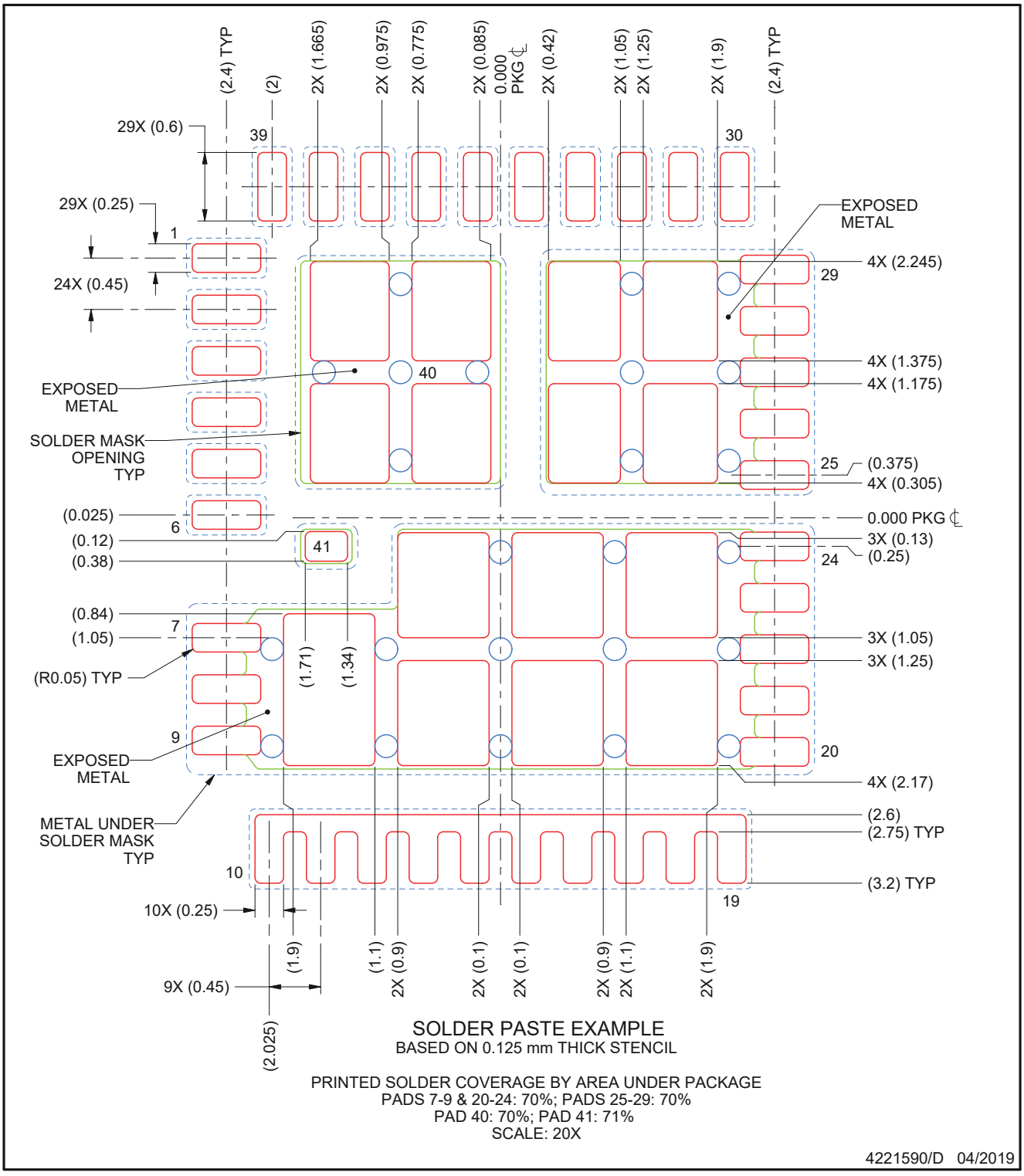
6.7 Alternate Industry Standard Compatible Stencil Opening



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