DACx1401 Single-Channel, 16-Bit and 12-Bit, High-Voltage Output DACs With Precision Internal Reference

1 Features

- Exceptional performance: 1LSB INL/DNL (maximum)
- Ultra-low glitch energy: 1nV-s
- Wide power supply:
  - Unipolar mode: +4.5V to +41.5V
  - Bipolar mode: ±4.5V to ±21.5V
- 14 user-programmable output ranges
  - ±5V, ±10V, ±20V
  - 0V to 5V, 0V to 10V, 0V to 20V, 0V to 40V
  - 20% overrange (except ±20V and 0V to 40V)
- Integrated 10ppm/°C, 2.5V precision reference
- Reliability features:
  - Cyclic redundancy check (CRC)
  - Fault pin
- 50MHz, 4-wire SPI-compatible interface
  - Readback
  - Daisy-chain
- Temperature range: –55°C to +125°C
- Packages:
  - 20-pin TSSOP (PW)
  - 16-pin WQFN (RTE)

2 Applications

- Semiconductor test and ATE
- Lab and field instrumentation
- PLC, DCS, and PAC
- Analog output module
- Servo drive control module

3 Description

The 16-bit DAC81401 and 12-bit DAC61401 (DACx1401) devices are a pin-compatible family of single-channel, buffered, high-voltage-output digital-to-analog converters (DACs) with an integrated 2.5V internal reference. These devices are specified monotonic and provide an exceptional linearity of less than 1LSB (maximum).

The DACx1401 offer bipolar output voltages of ±20V, ±10V, ±5V, and full-scale unipolar output voltages of 40V, 10V, and 5V. The DAC output range is programmable.

The DACx1401 incorporate a power-on-reset (POR) circuit that powers up the DAC output and keeps the devices in power-down mode until the outputs enable.

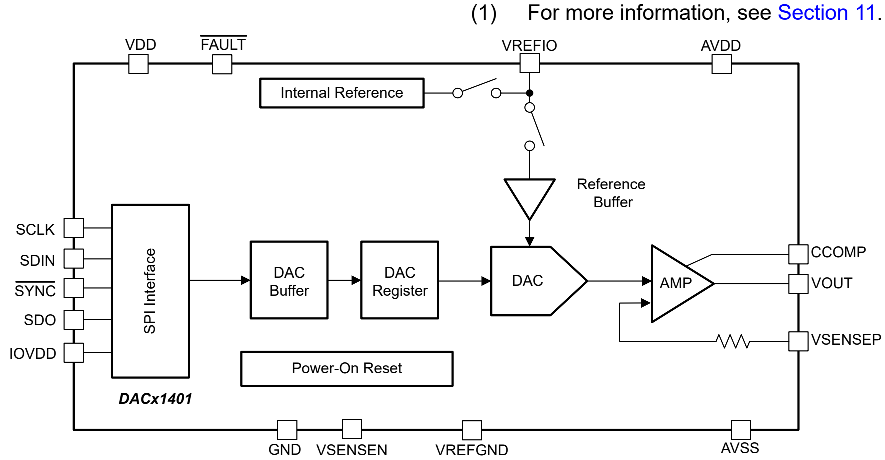
Communication to the devices is done through a high-speed, 4-wire serial interface compatible with industry-standard microprocessors and microcontrollers supporting 1.7V to 5.5V operation.

The DACx1401 are characterized for operation over the temperature range of –55°C to +125°C, and are available in a small 16-pin QFN and 20-pin TSSOP package.

Device Information

PART NUMBER	RESOLUTION	PACKAGE(1)
DAC61401	12-bit	PW (TSSOP, 20)
		RTE (WQFN, 16)
DAC81401	16-bit	PW (TSSOP, 20)
		RTE (WQFN, 16)

(1) For more information, see Section 11.



DACx1401 Block Diagram

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4 Pin Configuration and Functions

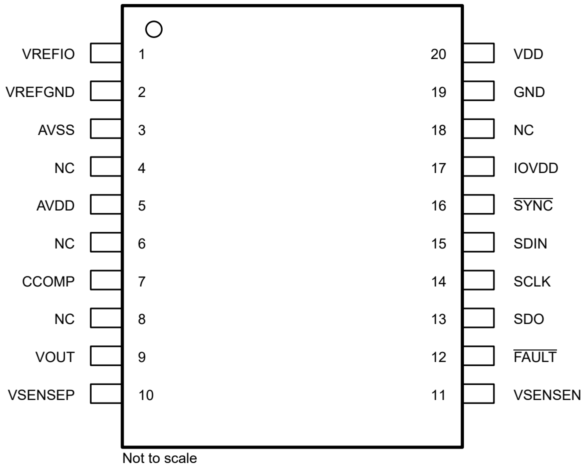


Figure 4-1. PW Package, 20-Pin TSSOP (Top View)

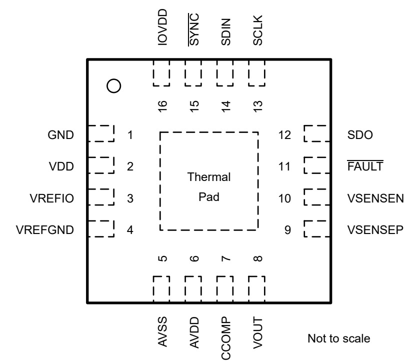


Figure 4-2. RTE Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	PW (TSSOP)	RTE (WQFN)		
AVDD	5	6	Power	Power supply
AVSS	3	5	Power	Negative power supply
CCOMP	7	7	Input	External compensation capacitor connection pin for VOUT. Addition of the external capacitor (470pF, typical) improves the stability with high capacitive loads (up to 1µF) at the VOUT pin by reducing the bandwidth of the output amplifier at the expense of increased settling time.
$\overline{\text{FAULT}}$	12	11	Output	$\overline{\text{FAULT}}$ pin. Open drain output. External 10kΩ pullup resistor required. The pin goes low (active) when the $\overline{\text{FAULT}}$ condition is detected.
GND	19	1	Ground	Digital and analog ground, connects to 0V
IOVDD	17	16	Input	IO pin power supply
NC	4, 6, 8, 18	—	—	Must be left unconnected, pin floating
SCLK	14	13	Input	Serial clock input of serial peripheral interface (SPI). Data can be transferred at rates up to 50MHz. Schmitt-trigger logic input
SDIN	15	14	Input	Serial data input. Data are clocked into the register on the falling edge of the serial clock input. Schmitt-trigger logic input
SDO	13	12	Output	Serial data output. Data are valid on the rising or falling edge of SCLK set by FSDO.
$\overline{\text{SYNC}}$	16	15	Input	SPI bus chip select input (active low). Data bits are not clocked into the serial shift register unless $\overline{\text{SYNC}}$ is low. When $\overline{\text{SYNC}}$ is high, SDO is in Hi-Z.
VDD	20	2	Power	Digital and analog power supply
VOUT	9	8	Output	DAC voltage output pin
VREFGND	2	4	Input	Reference ground, connects to 0V
VREFIO	1	3	Input/output	Internal reference output or external reference input. Connect a 150nF capacitor to ground.
VSENSEN	11	10	Input	Connect to 0V
VSENSEP	10	9	Input	Sense output pin for the positive voltage output load connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
	Supply voltage	VDD to GND	–0.3	6	V
		IOVDD to GND	–0.3	6	
		AVDD to GND	–0.3	44	
		AVSS to GND	–22	0.3	
		AVDD to AVSS	–0.3	44	
	Pin voltage	VOUT / VSENSEP to GND	AV_{SS} – 0.3	AV_{DD} + 0.3	V
		VREFIO to GND	–0.3	V_{DD} + 0.3	
		VREFGND / VSENSEN to GND	–0.3	0.3	
		Digital inputs to GND	–0.3	IOV_{DD} + 0.3	
		SDO to GND	–0.3	IOV_{DD} + 0.3	
		$\overline{\text{FAULT}}$ to GND	–0.3	6	
	Input current	Current into any digital pin (SCLK, SDIN, SDO, $\overline{\text{SYNC}}$)	–10	10	mA
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001[1]	±1000	V
		Human body model (HBM), per ANSI/ ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
POWER SUPPLY					
	VDD to GND	4.5		5.5	V
	IOVDD to GND	1.7		5.5	V
	AVDD to GND	4.5		41.5	V
	AVSS to GND	–21.5		0	V
	AVDD to AVSS	4.5		43	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		DACx1401 PW (TSSOP) 20 PINS	DACx1401 RTE (WQFN) 16 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	83.1	56.6	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	21.7	30.2	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	36.0	19.0	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	0.9	0.3	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	35.4	18.9	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report*.

5.5 Electrical Characteristics

all minimum and maximum values at T_A = –40°C to +125°C; all typical values at T_A = 25°C, A_{VDD} = 4.5V to 41.5V, A_{VSS} = –21.5V to 0V, V_{DD} = 5.0V, V_{REFIO} = 2.5V (external reference), IOV_{DD} = 1.7V, V_{SENSEN} = 0V, DAC output unloaded, CCOMP unconnected, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE[(1)]						
	Resolution	DAC81401	16			Bits
		DAC61401	12			Bits
INL	Relative accuracy[(1)]	DAC81401, all ranges except 0V to 40V range	–1	±0.4	1	LSB
		DAC81401, 0V to 40V range	–2		2	LSB
		DAC61401	–1		1	LSB
DNL	Differential nonlinearity		–1	±0.3	1	LSB
TUE	Total unadjusted error[(1)]	Unipolar ranges, AV_{SS} = 0V	–0.09		0.09	%FSR
		Unipolar ranges, AV_{SS} = 0V, 0°C ≤ T_A ≤ 50°C	–0.07		0.07	
		Bnipolar ranges, –21.5V ≤ AV_{SS} < 0V	–0.095		0.095	
OE	Offset error[(1)]	Unipolar ranges, AV_{SS} = 0V Bipolar ranges, –21.5V ≤ AV_{SS} < 0V	–0.05		0.05	%FSR
OE-TC	Offset error temperature coefficient	Unipolar ranges, AV_{SS} = 0V Bipolar ranges, –21.5V ≤ AV_{SS} < 0V		±2		ppmFSR/°C
ZCE	Zero-code (negative full scale) error	Unipolar ranges, AV_{SS} = 0V			0.15	%FSR
		Bipolar ranges, –21.5V ≤ AV_{SS} < 0V			0.05	
ZCE-TC	Zero-code (negative full scale) error temperature coefficient	Unipolar ranges, AV_{SS} = 0V Bipolar ranges, –21.5V ≤ AV_{SS} < 0V		±2		ppmFSR/°C
FSE	Full-scale error[(2)]	Unipolar ranges, AV_{SS} = 0V Bipolar ranges, –21.5V ≤ AV_{SS} < 0V	–0.08		0.08	%FSR
FSE-TC	Full-scale error temperature coefficient[(2)]			±3		ppmFSR/°C
GE	Gain error[(1)]	Unipolar ranges, AV_{SS} = 0V	–0.075		0.075	%FSR
BPGE	Bipolar Gain error[(1)]	Bipolar ranges, –21.5V ≤ AV_{SS} < 0V	–0.065		0.065	%FSR
GE-TC	Gain error temperature coefficient			±2		ppmFSR/°C
BPZE	Bipolar zero (midscale) error	Bipolar ranges, –21.5V ≤ AV_{SS} < 0V	–0.04		0.04	%FSR
BPZE-TC	Bipolar zero (midscale) error temperature coefficient	Bipolar ranges, –21.5V ≤ AV_{SS} < 0V		±2		ppmFSR/°C
	Output voltage drift over time	T_A = 40°C, DAC code at full-scale, 1000 hours		±6		ppm FSR

5.5 Electrical Characteristics (continued)

all minimum and maximum values at T_A = –40°C to +125°C; all typical values at T_A = 25°C, A_{VDD} = 4.5V to 41.5V, A_{VSS} = –21.5V to 0V, V_{DD} = 5.0V, V_{REFIO} = 2.5V (external reference), IOV_{DD} = 1.7V, V_{SENSEN} = 0V, DAC output unloaded, CCOMP unconnected, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage		0		5	V
		20% overrange of 0V to 5V	0		6	
			0		10	
		20% overrange of 0V to 10V	0		12	
			0		20	
		20% overrange of 0V to 20V	0		24	
			0		40	
			–5		5	
		20% overrange of –5V to +5V	–6		6	
			–10		10	
		20% overrange of –10V to +10V	–12		12	
			–20		20	
	Output voltage headroom (to AVDD) and footroom (to AVSS)(4)	–10mA ≤ load current ≤ 10mA	1.25			
		5.5V < AV_{DD} ≤ 41.5V, −15mA ≤ load current ≤ +15mA	1.5			V
I_{OS}	Short-circuit current(3)	Full-scale output shorted to AV_{SS}		40		mA
		Full-scale output shorted to AV_{DD}, 5.5V < AV_{DD} ≤ 41.5V,		40		
		Zero-scale output shorted to AV_{DD}, 4.5V ≤ AV_{DD} ≤ 5.5V		25		
	Load regulation	DAC at midscale, –15mA ≤ load current ≤ +15mA		50		µV/mA
C_L	Capacitive load(4)	R_{LOAD} = open, CCOMP pin left floating	0		2	nF
		R_{LOAD} = open, CCOMP pin = 470pF ±10% to V_{OUT}			1	µF
I_L	Load current(4)	5.5V < AV_{DD} ≤ 41.5V			15	mA
		4.5V < AV_{DD} ≤ 5.5V			10	
	V_{OUT} dc output impedance	DAC code at midscale, DAC unloaded		0.05		Ω
		DAC code at full scale, DAC unloaded		0.05		
		DAC code at zero scale, DAC unloaded, unipolar output		35		
		DAC code at negative full scale, DAC unloaded, bipolar output		0.05		
	V_{SENSEP} dc output impedance	DAC code at midscale, 10V span		55		kΩ
		DAC disabled		45		

5.5 Electrical Characteristics (continued)

all minimum and maximum values at T_A = –40°C to +125°C; all typical values at T_A = 25°C, A_{VDD} = 4.5V to 41.5V, A_{VSS} = –21.5V to 0V, V_{DD} = 5.0V, V_{REFIO} = 2.5V (external reference), IOV_{DD} = 1.7V, V_{SENSEN} = 0V, DAC output unloaded, CCOMP unconnected, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
	Output voltage settling time	5V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2LSB		7		µs
		10V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2LSB		8		µs
		20V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2LSB		12		µs
		40V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2LSB		22		µs
		5V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2LSB, C_L = 1µF, C_{COMP} = 470pF to V_{OUT}		0.6		ms
		10V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2LSB, C_L = 1µF, C_{COMP} = 470pF to V_{OUT}		0.6		ms
		20V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2LSB, C_L = 1µF, C_{COMP} = 470pF to V_{OUT}		0.6		ms
		40V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2LSB, C_L = 1µF, C_{COMP} = 470pF to V_{OUT}		1.2		ms
SR	Slew rate	0V to 5V range (10% to 90% of full-scale range)		0.8		V/µs
		All other output ranges except 40V span (10% to 90% of full-scale range)		4		
		0V to 5V range, C_L = 1µF, C_{COMP} = 470pF to V_{OUT}		0.04		
		All other ranges, C_L = 1µF, C_{COMP} = 470pF to V_{OUT}		0.04		
	Power-on glitch magnitude	AV_{SS} and AV_{DD} ramped symmetrically, ramp rate = 18V/ms, output unloaded, internal reference		0.1		V
	Output enable glitch magnitude	AV_{SS} and AV_{DD} ramped, output unloaded, internal reference		0.35		V
$V_{NOISEPP}$	Output noise	0.1Hz to 10Hz, DAC code at midscale, 10V span, external reference = 2.5V		25		µVpp
		0.1Hz to 10Hz, DAC code at midscale, 10V span, internal reference = 2.5V		30		
V_{NOISE}	Output noise density	1kHz, DAC code at midscale, 5V span, output unloaded, external reference		115		nV/Hz
		10kHz, DAC code at midscale, 5V span, output unloaded, external reference		105		
THD	Total harmonic distortion	1kHz sine wave on V_{OUT}, output unloaded, DAC update rate = 400kHz		93		dB

5.5 Electrical Characteristics (continued)

all minimum and maximum values at T_A = –40°C to +125°C; all typical values at T_A = 25°C, A_{VDD} = 4.5V to 41.5V, A_{VSS} = –21.5V to 0V, V_{DD} = 5.0V, V_{REFIO} = 2.5V (external reference), IOV_{DD} = 1.7V, V_{SENSEN} = 0V, DAC output unloaded, CCOMP unconnected, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR-AC	Power supply rejection ratio - ac	V_{OUT} = 0V (midscale), output unloaded, ±10V output, frequency = 60Hz, amplitude 200mV_{PP}, superimposed on AV_{DD}, V_{DD} or AV_{SS}		75		dB
PSRR-DC	Power supply rejection ratio - dc	V_{OUT} = 0V (midscale), ±10V output, V_{DD} = 5V, AV_{DD} = 15V ± 20%, AV_{SS} = –15V, output unloaded		5		µV/V
		V_{OUT} = 0V (midscale), ±10V output, V_{DD} = 5V, AV_{DD} = 15V, AV_{SS} = –15V ± 20%, output unloaded		10		µV/V
		V_{OUT} = 0V (midscale), ±10V output, V_{DD} = 5V ± 5%, AV_{DD} = 15V, AV_{SS} = –15V, output unloaded		0.2		mV/V
V_{GL}	Code change glitch impulse	1LSB change around midscale, 0V to 5V range, output unloaded		1		nV-s
		1LSB change around midscale, 0V to 10V range, output unloaded		2		
		1LSB change around midscale, –5V to +5V range, output unloaded		2		
		1LSB change around midscale, –10V to +10V range, output unloaded		4		
	Code change glitch amplitude	1LSB change around midscale, 0V to 5V, 0V to 10V, –5V to +5V, and –10V to +10V ranges, output unloaded		±1.5		mV
	Digital feedthrough	DAC code at midscale, f_{SCLK} = 1MHz, output unloaded		0.3		nV-s
EXTERNAL REFERENCE INPUT						
V_{REFIO}	Reference input voltage		2.49	2.5	2.51	V
I_{REF}	Reference input current			50		µA
Z_{IN}	Reference input impedance			50		kΩ
C_{REF}	Reference input capacitance			90		pF
INTERNAL REFERENCE						
V_{REFO}	Reference output voltage	T_A = 25°C	2.4975		2.5025	V
	Reference output drift(3)			5	10	ppm/°C
R_{ZO}	Reference output impedance			0.15		Ω
$V_{NOISEPP}$	Reference output noise	0.1Hz to 10Hz		12		µVpp
V_{NOISE}	Reference output noise density	10kHz, VREFIO pin = 10nF		240		nV/√Hz
I_L	Reference load current	Source		5		mA
	Reference load regulation	Source		120		µV/mA
	Reference line regulation			100		µV/V
	Reference output drift over time	T_A = 40°C, 1000 hours		±300		µV
	Reference thermal hysteresis	First cycle		±400		µV
		Additional cycle		±35		

5.5 Electrical Characteristics (continued)

all minimum and maximum values at T_A = –40°C to +125°C; all typical values at T_A = 25°C, A_{VDD} = 4.5V to 41.5V, A_{VSS} = –21.5V to 0V, V_{DD} = 5.0V, V_{REFIO} = 2.5V (external reference), IOV_{DD} = 1.7V, V_{SENSEN} = 0V, DAC output unloaded, CCOMP unconnected, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS AND OUTPUTS						
V_{IH}	SDIN, high-level input voltage		0.7 × IOV_{DD}			V
V_{IL}	SDIN, low-level input voltage				0.3 × IOV_{DD}	V
	Input current			±2		µA
	Input pin capacitance			2		pF
V_{OH}	SDO, high-level output voltage	SDO load current = 0.2mA	IOV_{DD} – 0.2			V
V_{OL}	SDO, low-level output voltage	SDO load current = 0.2mA			0.4	V
	$\overline{\text{FAULT}}$, low-level output voltage	$\overline{\text{FAULT}}$ load current = 10mA			0.4	V
	Output pin capacitance			5		pF
POWER REQUIREMENTS(5)						
I_{AVDD}	AV_{DD} supply current(5)	Normal mode, internal reference or external reference			1.6	mA
		Power down mode			10	µA
I_{VDD}	V_{DD} supply current(5)	Digital interface static, internal reference or external reference			2.5	mA
I_{AVSS}	AV_{SS} supply current(5)	Normal mode, internal reference or external reference	–1.6			mA
		Power-down mode	–10			µA
I_{IOVDD}	IOV_{DD} supply current(5)	SCLK toggling at 1MHz		10	120	µA

(1) End point fit between codes. 16bit: 512 to 65024 for A_{VDD} ≥ 5.5V, 512 to 63488 for A_{VDD} ≤ 5.5V, 0.2V headroom between V_{REFIO} and A_{VDD}; 12bit: 32 to 4064 for A_{VDD} ≥ 5.5V, 32 to 3968 for A_{VDD} ≤ 5.5V, 0.2V headroom between V_{REFIO} and A_{VDD}.
(2) Full-scale code written to the DAC for A_{VDD} ≥ 5.5V. 16bit: code 63488 written to the DAC for A_{VDD} ≤ 5.5V; 12bit: code 3968 written to the DAC for A_{VDD} ≤ 5.5V.
(3) Temporary overload condition protection. Junction temperature can be exceeded during current limit. Operation greater than the specified maximum junction temperature can impair device reliability.
(4) Specified by design and characterization, not production tested.
(5) Time to exit power down mode to normal operation. Measured from last rising edge of $\overline{\text{SYNC}}$ to 90% of DAC final value.

5.6 Timing Requirements - Write, IOV_{DD} = 1.7V to 2.7V

all specifications at T_A = –40°C to +125°C, input signals are specified with $t_R = t_F$ = 1ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of ($V_{IL} + V_{IH}$) / 2, SDO loaded with 20pF, 1.7V ≤ IOV_{DD} < 2.7V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			25	MHz
$t_{SCLKHIGH}$	SCLK high time	20			ns
$t_{SCLKLOW}$	SCLK low time	20			ns
t_{SDIS}	SDIN setup	10			ns
t_{SDIH}	SDIN hold	10			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup	30			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	10			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	50			ns
$t_{DACWAIT}$	Sequential DAC update wait time	2.4			µs

5.7 Timing Requirements - Write, IOV_{DD} = 2.7V to 5.5V

all specifications at T_A = –40°C to +125°C, input signals are specified with $t_R = t_F$ = 1ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of ($V_{IL} + V_{IH}$) / 2, SDO loaded with 20pF, 2.7V ≤ IOV_{DD} ≤ 5.5V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			50	MHz
$t_{SCLKHIGH}$	SCLK high time	10			ns
$t_{SCLKLOW}$	SCLK low time	10			ns
t_{SDIS}	SDIN setup	5			ns
t_{SDIH}	SDIN hold	5			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup	15			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	5			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	25			ns
$t_{DACWAIT}$	Sequential DAC update wait time	2.4			µs

5.8 Timing Requirements - Read and Daisy Chain, FSDO = 0, IOV_{DD} = 1.7V to 2.7V

all specifications at T_A = –40°C to +125°C, input signals are specified with t_R = t_F = 1ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20pF, 1.7V ≤ IOV_{DD} <2.7V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			12.5	MHz
$t_{SCLKHIGH}$	SCLK high time	33			ns
$t_{SCLKLOW}$	SCLK low time	33			ns
t_{SDIS}	SDIN setup	10			ns
t_{SDIH}	SDIN hold	10			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup	30			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	10			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	50			ns
t_{SDOZ}	SDO driven to tri-state mode	0		30	ns
t_{SDODLY}	SDO output delay from SCLK rising edge	0		30	ns

5.9 Timing Requirements - Read and Daisy Chain, FSDO = 1, IOV_{DD} = 1.7V to 2.7V

all specifications at T_A = –40°C to +125°C, input signals are specified with t_R = t_F = 1ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20pF, 1.7V ≤ IOV_{DD} < 2.7V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			25	MHz
$t_{SCLKHIGH}$	SCLK high time	20			ns
$t_{SCLKLOW}$	SCLK low time	20			ns
t_{SDIS}	SDIN setup	10			ns
t_{SDIH}	SDIN hold	10			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup	30			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	10			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	50			ns
t_{SDOZ}	SDO driven to tri-state mode	0		30	ns
t_{SDODLY}	SDO output delay from SCLK rising edge	0		30	ns

5.10 Timing Requirements - Read and Daisy Chain, FSDO = 0, IOV_{DD} = 2.7V to 5.5V

all specifications at T_A = –40°C to +125°C, input signals are specified with $t_R = t_F$ = 1ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$, SDO loaded with 20pF, 2.7V ≤ IOV_{DD} ≤ 5.5V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			20	MHz
$t_{SCLKHIGH}$	SCLK high time	25			ns
$t_{SCLKLOW}$	SCLK low time	25			ns
t_{SDIS}	SDIN setup	5			ns
t_{SDIH}	SDIN hold	5			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup	20			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	5			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	25			ns
t_{SDOZ}	SDO driven to tri-state mode	0		20	ns
t_{SDODLY}	SDO output delay from SCLK rising edge	0		20	ns

5.11 Timing Requirements - Read and Daisy Chain, FSDO = 1, IOV_{DD} = 2.7V to 5.5V

all specifications at T_A = –40°C to +125°C, input signals are specified with $t_R = t_F$ = 1ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$, SDO loaded with 20pF, 2.7V ≤ IOV_{DD} ≤ 5.5V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			35	MHz
$t_{SCLKHIGH}$	SCLK high time	14			ns
$t_{SCLKLOW}$	SCLK low time	14			ns
t_{SDIS}	SDIN setup	5			ns
t_{SDIH}	SDIN hold	5			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup	20			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	5			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	25			ns
t_{SDOZ}	SDO driven to tri-state mode	0		20	ns
t_{SDODLY}	SDO output delay from SCLK rising edge	0		20	ns

5.12 Timing Diagrams

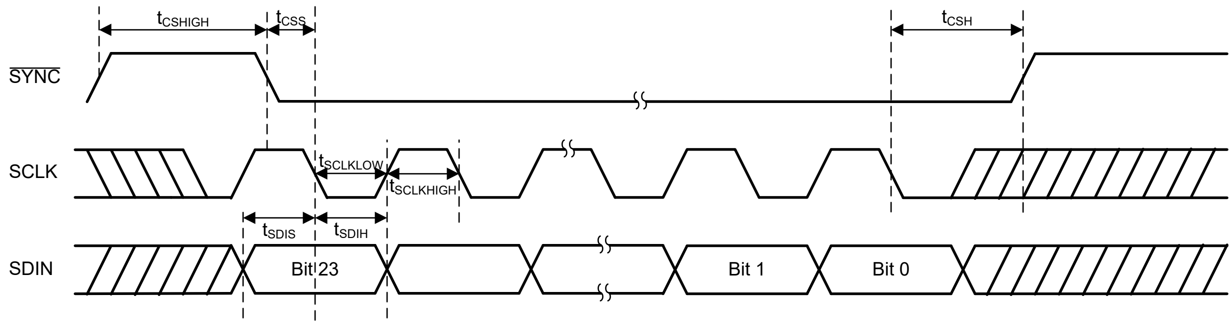


Figure 5-1. Serial Interface Write Timing Diagram

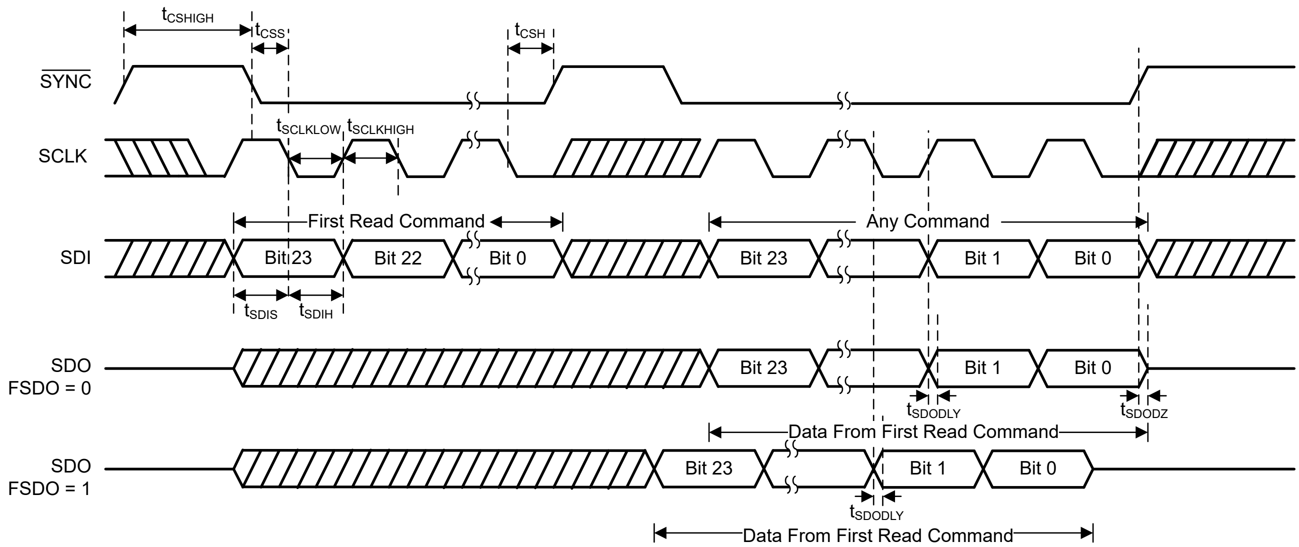


Figure 5-2. Serial Interface Read Timing Diagram

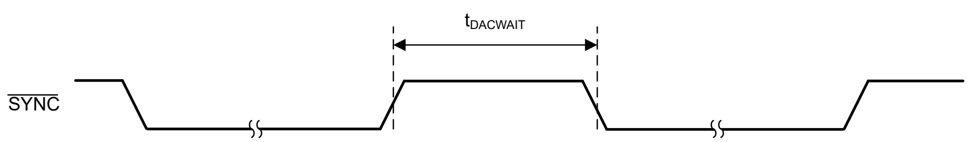


Figure 5-3. DAC Wait Time in Update Mode

5.13 Typical Characteristics

at T_A = 25°C, V_{DD} = 5.0V, IOV_{DD} = 1.8V, external reference, unipolar ranges: AV_{SS} = 0V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, and DAC output unloaded (unless otherwise noted)

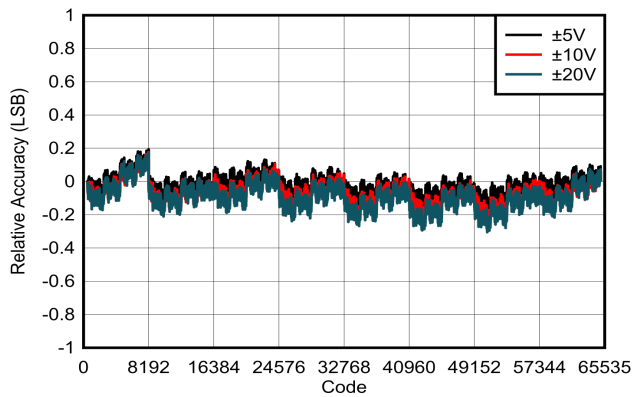


Figure 5-4. DAC81401 Relative Accuracy vs Digital Input Code (Bipolar Outputs)

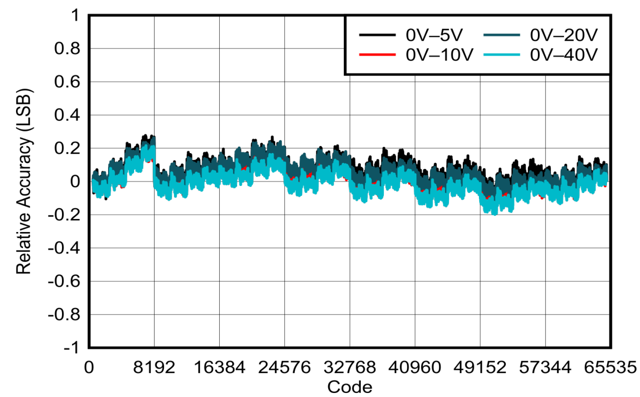


Figure 5-5. DAC81401 Relative Accuracy vs Digital Input Code (Unipolar Outputs)

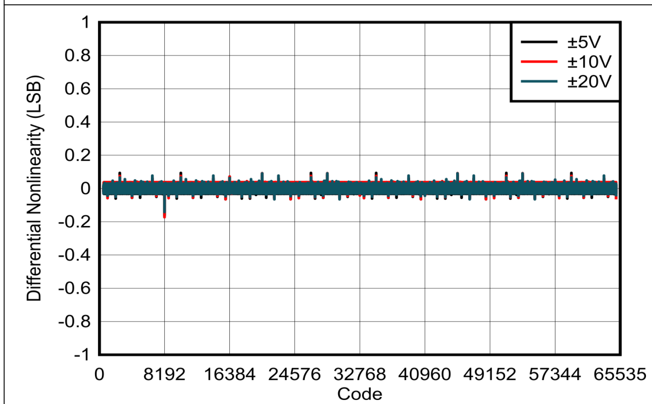


Figure 5-6. DAC81401 DNL vs Digital Input Code (Bipolar Outputs)

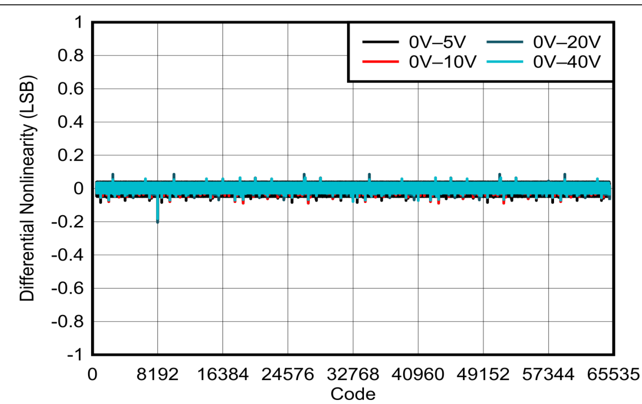


Figure 5-7. DAC81401 DNL vs Digital Input Code (Unipolar Outputs)

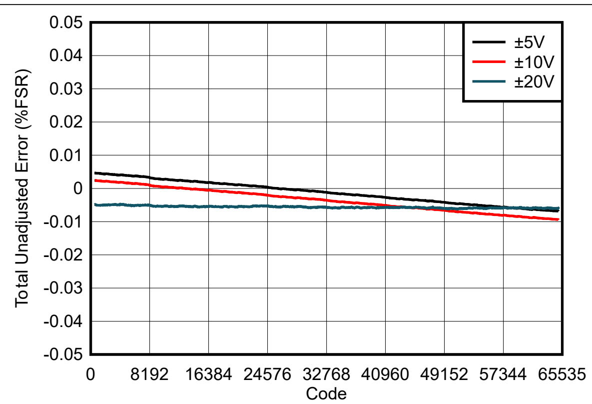


Figure 5-8. DAC81401 TUE vs Digital Input Code (Bipolar Outputs)

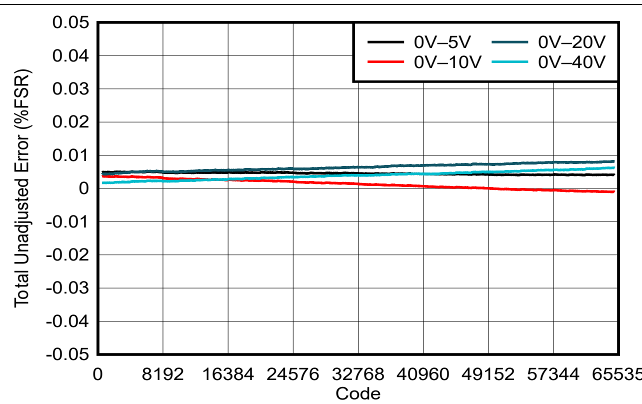


Figure 5-9. DAC81401 TUE vs Digital Input Code (Unipolar Outputs)

5.13 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.0V, IOV_{DD} = 1.8V, external reference, unipolar ranges: AV_{SS} = 0V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, and DAC output unloaded (unless otherwise noted)

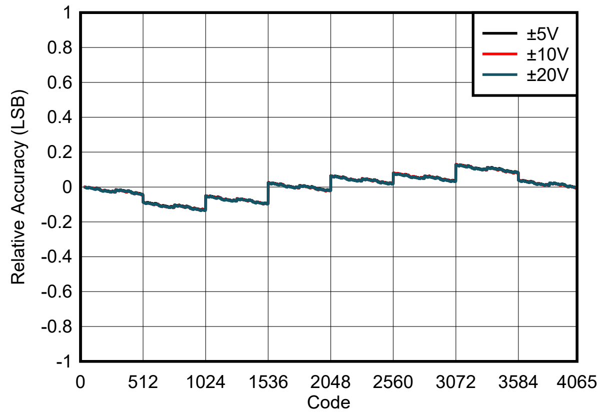


Figure 5-10. DAC61401 Relative Accuracy vs Digital Input Code (Bipolar Outputs)

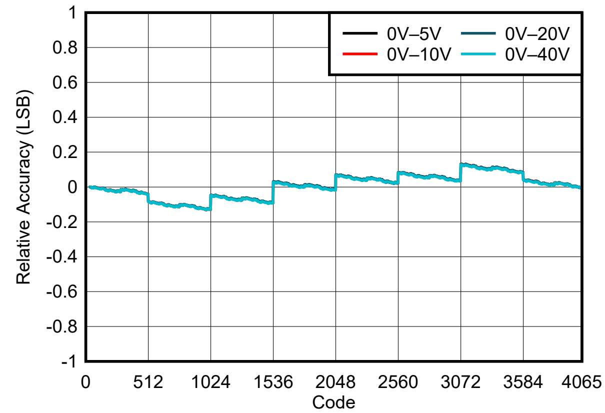


Figure 5-11. DAC61401 Relative Accuracy vs Digital Input Code (Unipolar Outputs)

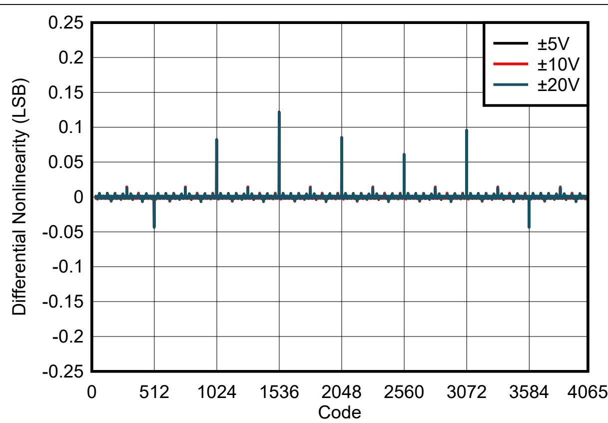


Figure 5-12. DAC61401 DNL vs Digital Input Code (Bipolar Outputs)

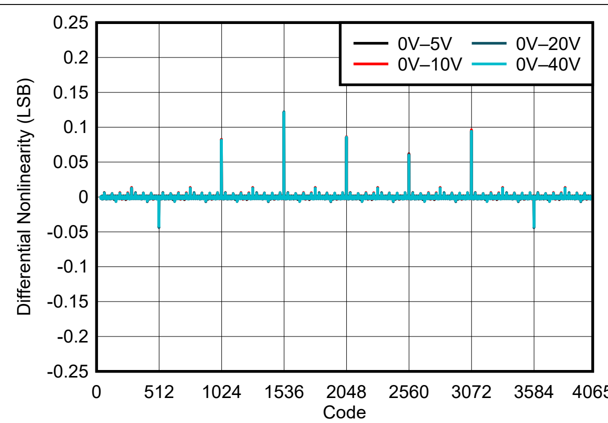


Figure 5-13. DAC61401 DNL vs Digital Input Code (Unipolar Outputs)

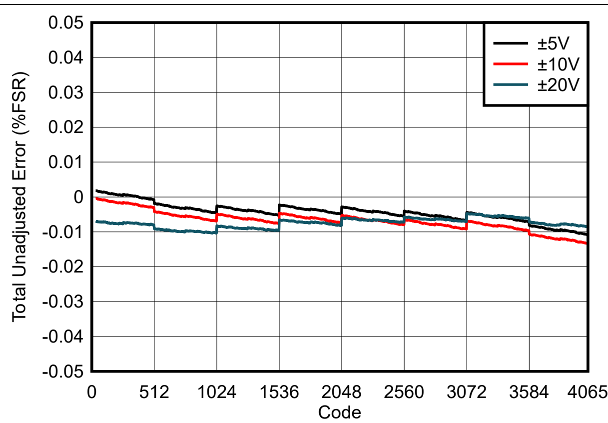


Figure 5-14. DAC61401 TUE vs Digital Input Code (Bipolar Outputs)

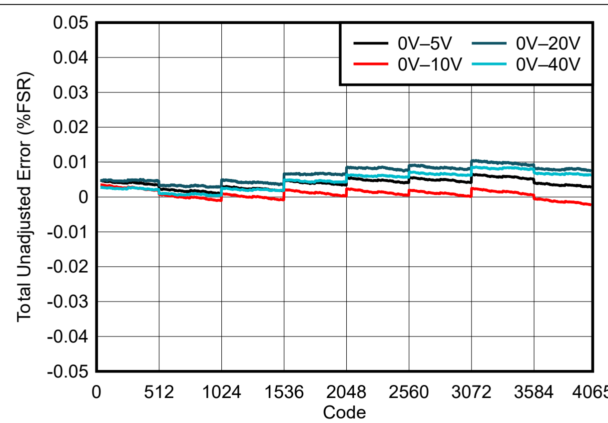


Figure 5-15. DAC61401 TUE vs Digital Input Code (Unipolar Outputs)

5.13 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.0V, IOV_{DD} = 1.8V, external reference, unipolar ranges: AV_{SS} = 0V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, and DAC output unloaded (unless otherwise noted)

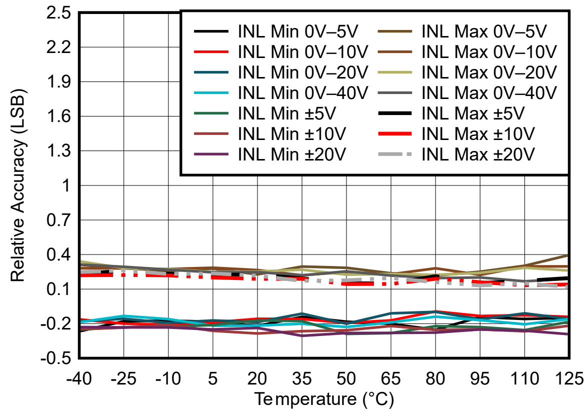


Figure 5-16. DAC81401 Relative Accuracy vs Temperature

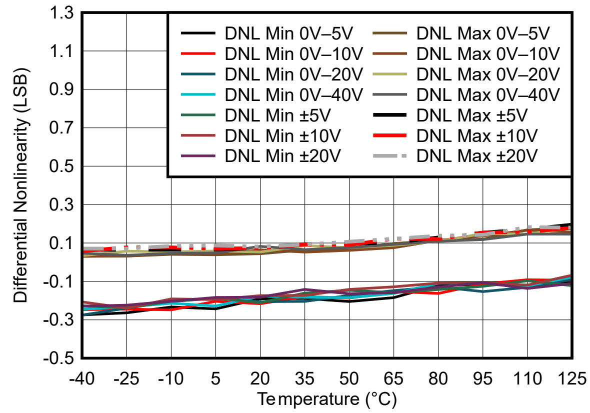


Figure 5-17. DAC81401 DNL vs Temperature

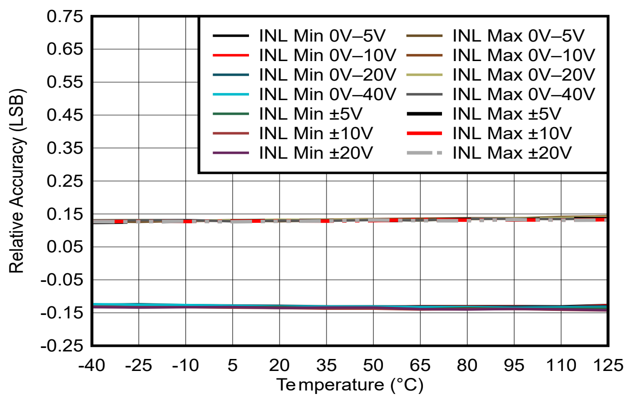


Figure 5-18. DAC61401 Relative Accuracy vs Temperature

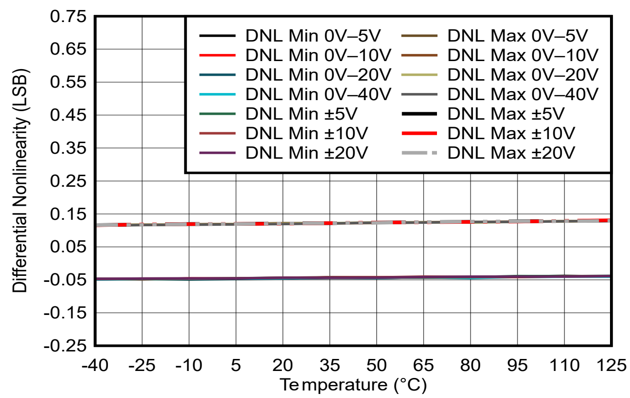


Figure 5-19. DAC61401 DNL vs Temperature

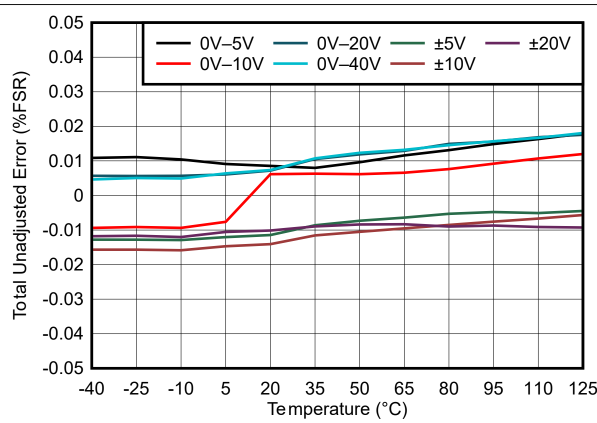


Figure 5-20. TUE vs Temperature

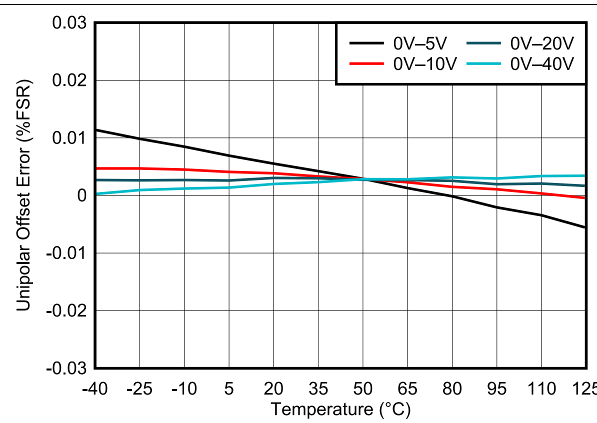


Figure 5-21. Unipolar Offset Error vs Temperature

5.13 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.0V, IOV_{DD} = 1.8V, external reference, unipolar ranges: AV_{SS} = 0V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, and DAC output unloaded (unless otherwise noted)

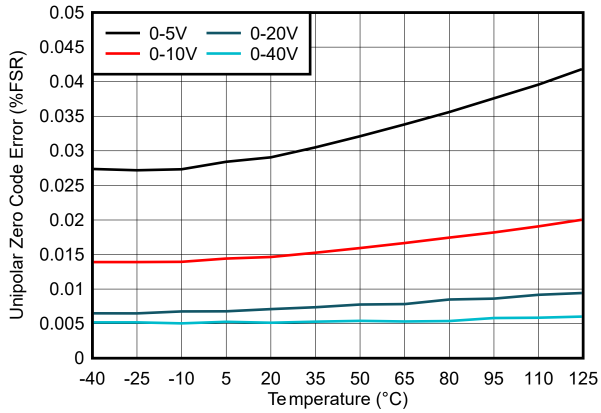


Figure 5-22. Unipolar Zero Code Error vs Temperature

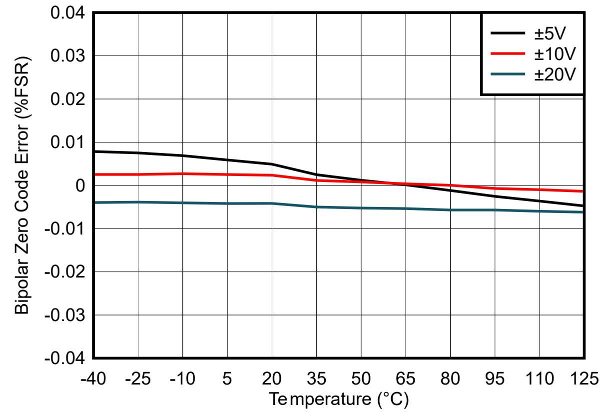


Figure 5-23. Bipolar Zero Code Error vs Temperature

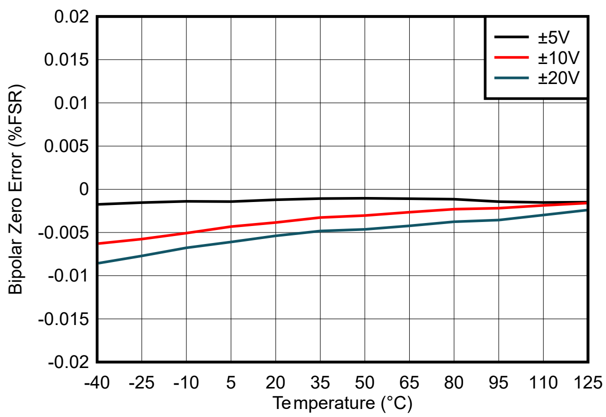


Figure 5-24. Bipolar Zero Error vs Temperature

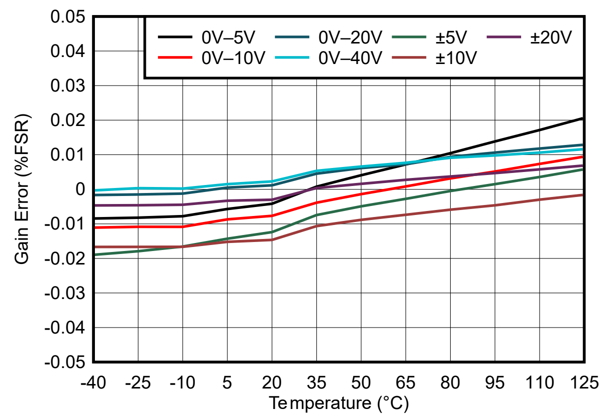


Figure 5-25. Gain Error vs Temperature

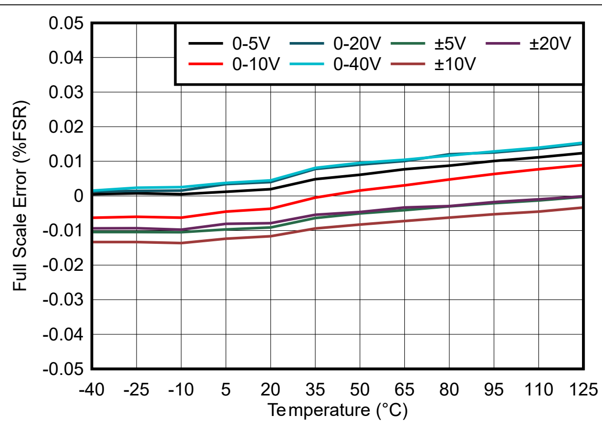


Figure 5-26. Full-Scale Error vs Temperature

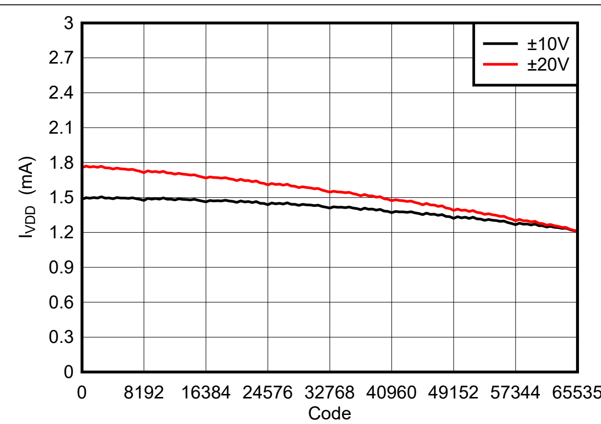


Figure 5-27. Supply Current (I_{VDD}) vs Digital Input Code

5.13 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.0V, IOV_{DD} = 1.8V, external reference, unipolar ranges: AV_{SS} = 0V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, and DAC output unloaded (unless otherwise noted)

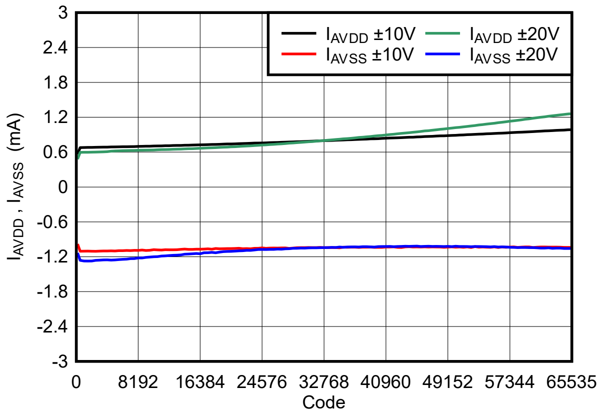


Figure 5-28. Supply Current (I_{AVDD}, I_{AVSS}) vs Digital Input Code

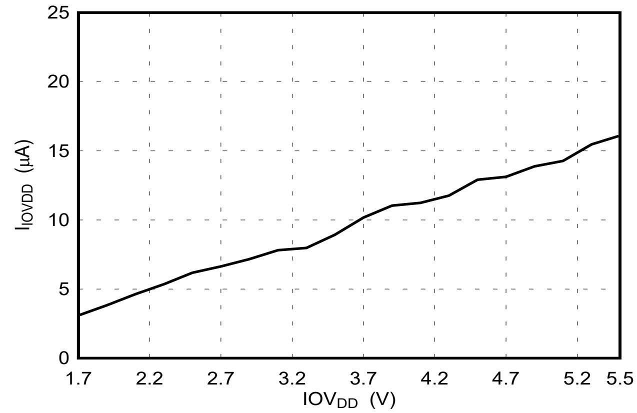
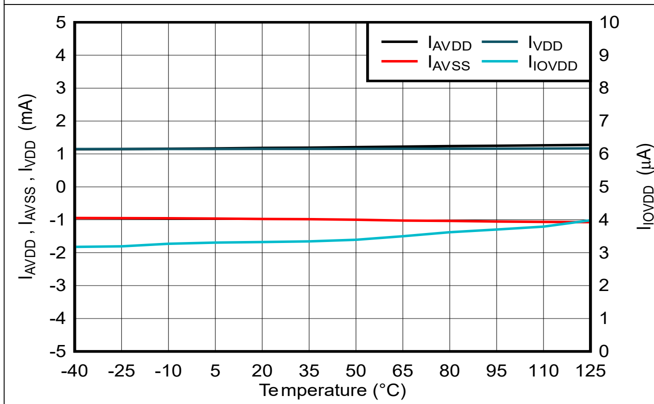
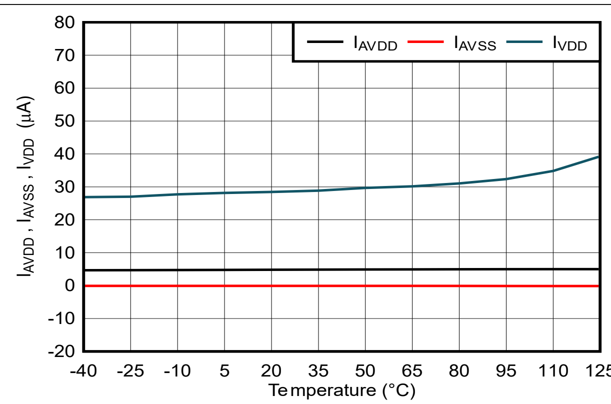


Figure 5-29. Supply Current (I_{IOVDD}) vs Supply Voltage



DAC range = ±20V

Figure 5-30. Supply Current vs Temperature



DAC range = ±20V

Figure 5-31. Power-Down Current vs Temperature

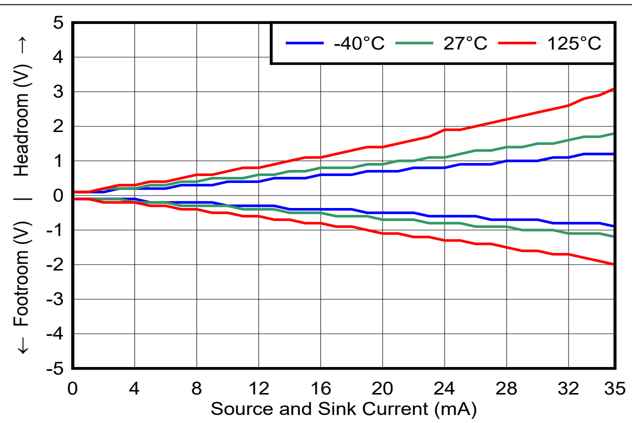


Figure 5-32. Headroom and Footroom From Supply vs Output Current

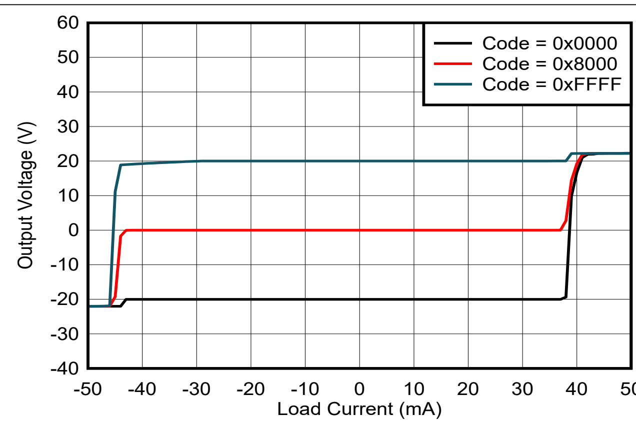
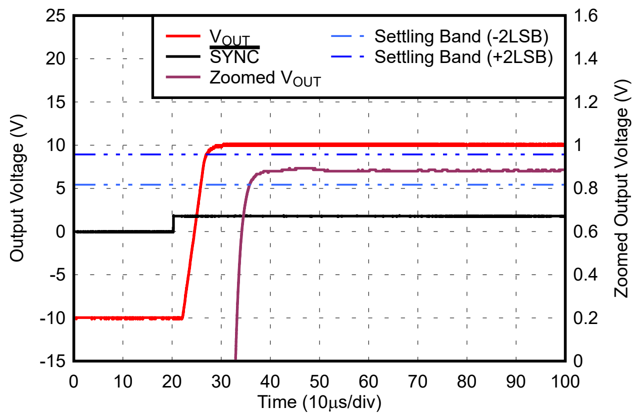


Figure 5-33. Source and Sink Capability

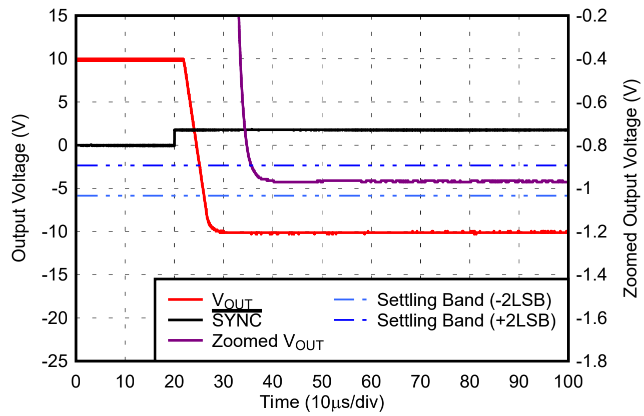
5.13 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.0V, IOV_{DD} = 1.8V, external reference, unipolar ranges: AV_{SS} = 0V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, and DAC output unloaded (unless otherwise noted)



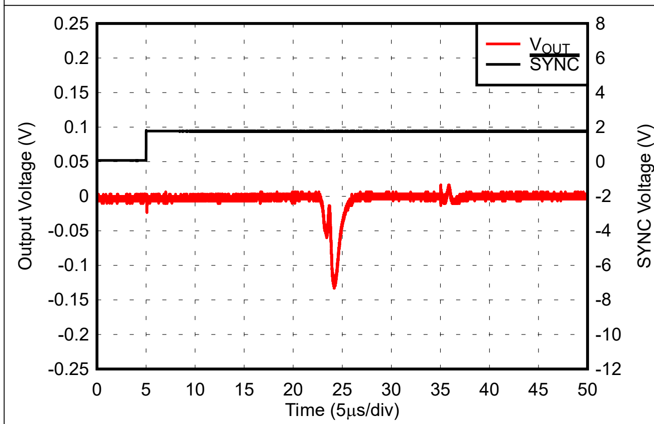
DAC range = ±10V

Figure 5-34. Full-Scale Settling Time, Rising Edge



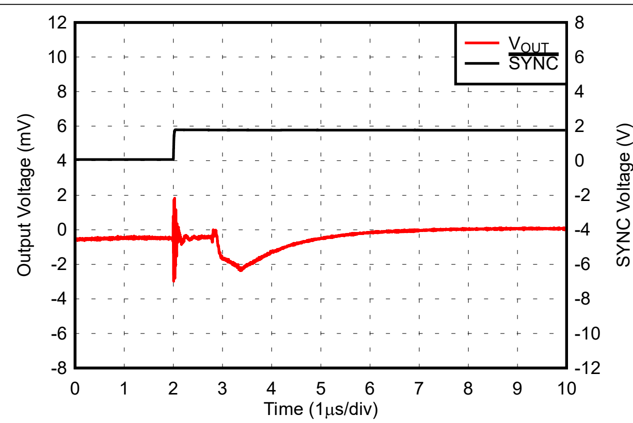
DAC range = ±10V

Figure 5-35. Full-Scale Settling Time, Falling Edge



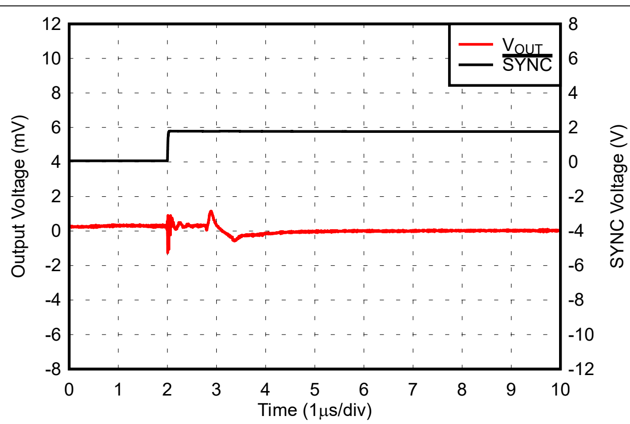
DAC range = ±20V

Figure 5-36. DAC Output Enable Glitch



DAC range = ±10V

Figure 5-37. Glitch Impulse, 1LSB Step, Rising Edge



DAC range = ±10V

Figure 5-38. Glitch Impulse, 1LSB Step, Falling Edge

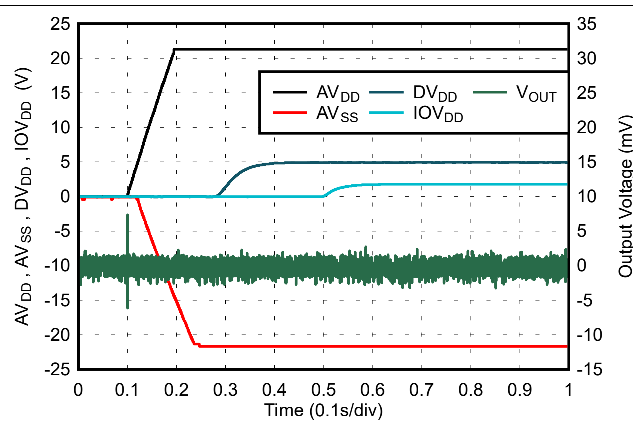


Figure 5-39. Power-Up Response

5.13 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.0V, IOV_{DD} = 1.8V, external reference, unipolar ranges: AV_{SS} = 0V and AV_{DD} ≥ V_{MAX} + 1.5V for the DAC range, bipolar ranges: AV_{SS} ≤ V_{MIN} − 1.5V and AV_{DD} ≥ V_{MAX} + 1.5V for the DAC range, and DAC output unloaded (unless otherwise noted)

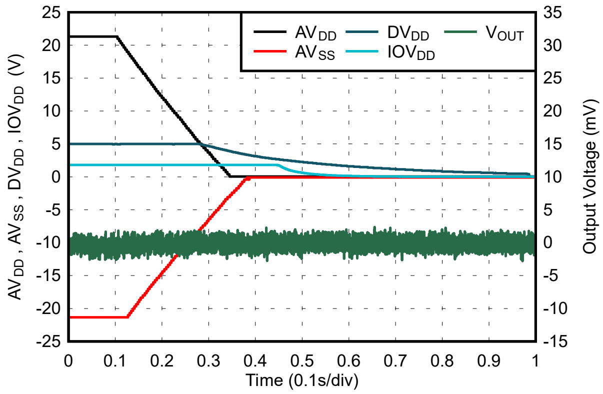
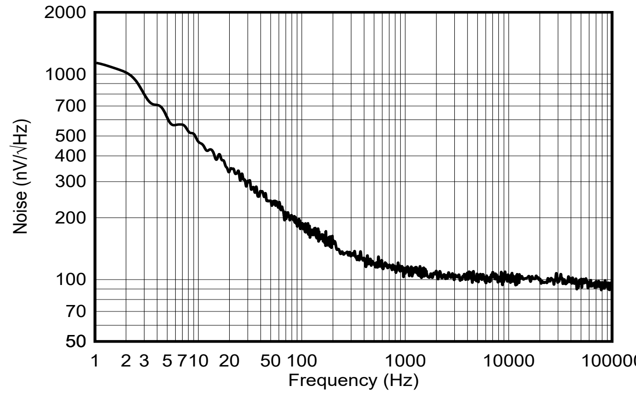
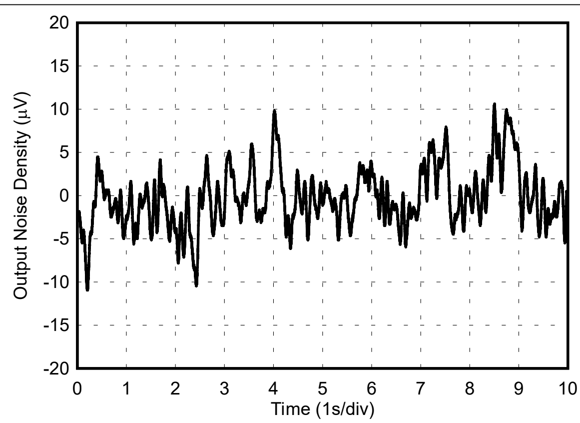


Figure 5-40. Power-Down Response



DAC range= 0V to 5V midscale code

Figure 5-41. DAC Output Noise Density vs Frequency



DAC range= 0V to 5V midscale code

Figure 5-42. DAC Output Noise

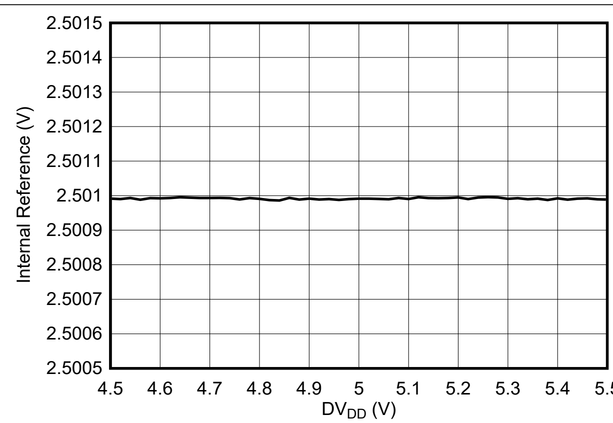


Figure 5-43. Internal Reference Voltage vs Supply Voltage

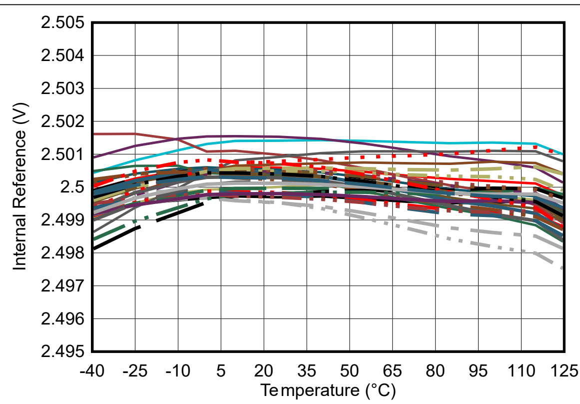


Figure 5-44. Internal Reference Voltage vs Temperature (TSSOP)

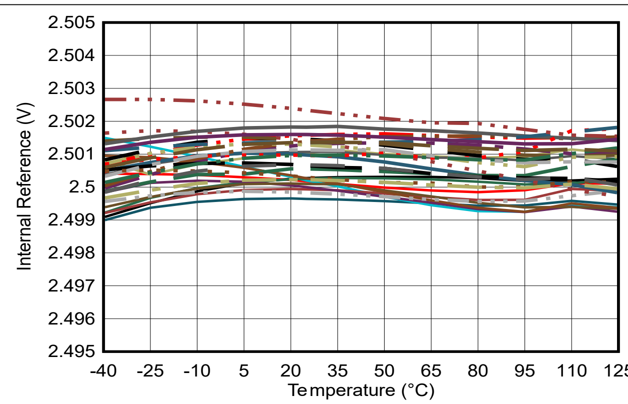


Figure 5-45. Internal Reference Voltage vs Temperature (WQFN)

5.13 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.0V, IOV_{DD} = 1.8V, external reference, unipolar ranges: AV_{SS} = 0V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5V and $AV_{DD} \geq V_{MAX}$ + 1.5V for the DAC range, and DAC output unloaded (unless otherwise noted)

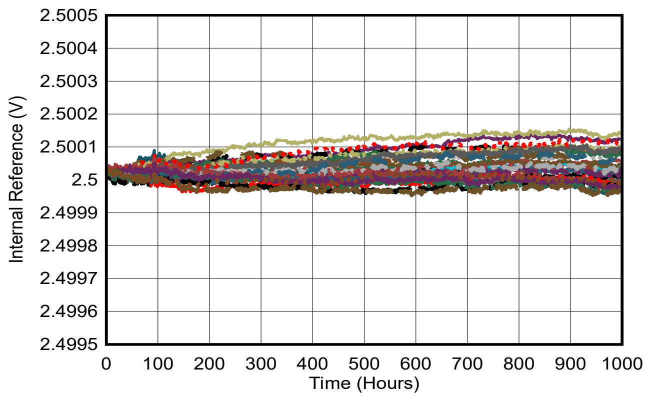


Figure 5-46. Internal Reference Voltage vs Time (TSSOP)

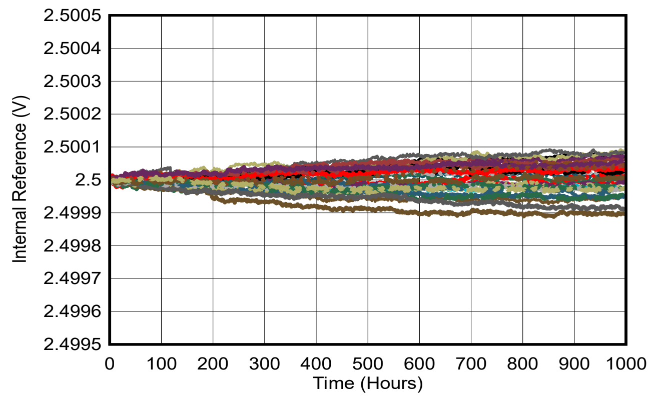


Figure 5-47. Internal Reference Voltage vs Time (WQFN)

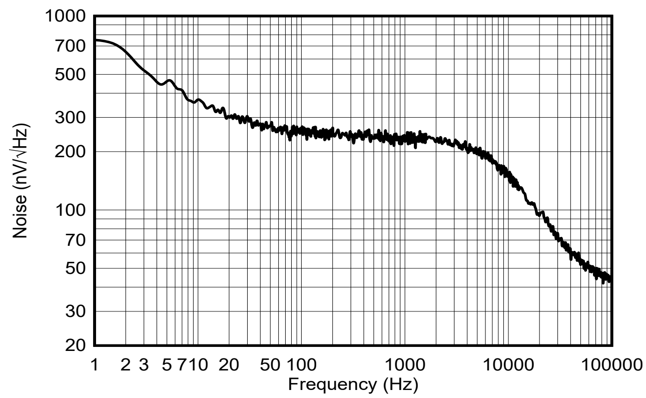


Figure 5-48. Internal Reference Noise Density vs Frequency

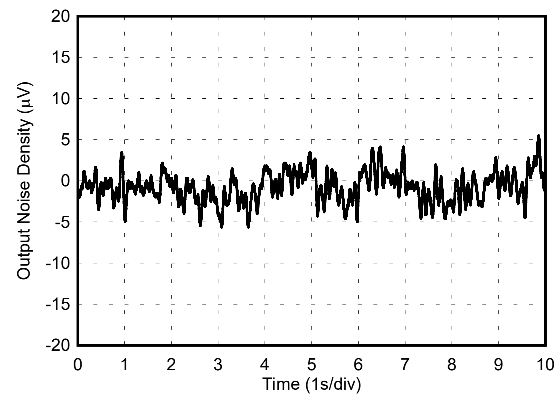


Figure 5-49. Internal Reference Noise

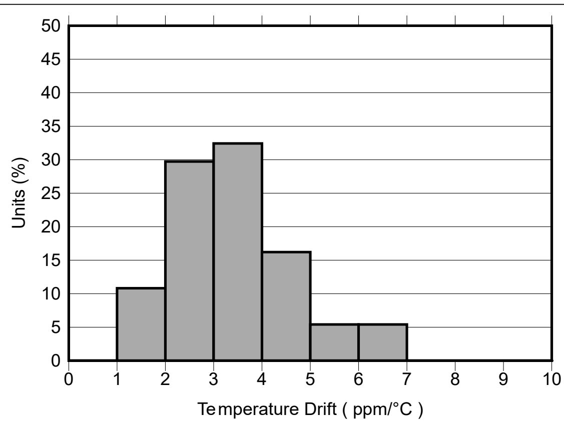
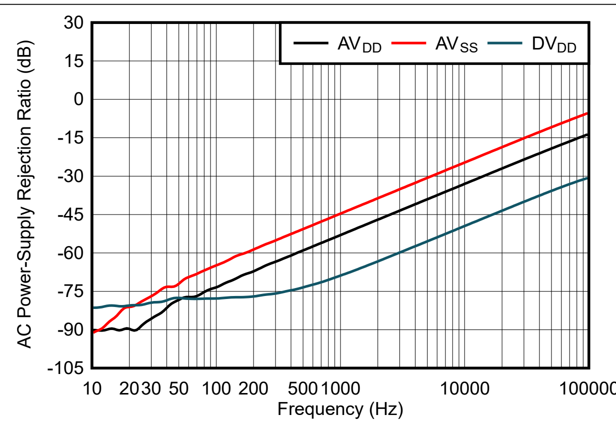


Figure 5-50. Internal Reference Temperature Drift Histogram



V_{OUT} = 0V (DAC code at midscale), output unloaded,
AV_{DD} = 10V, AV_{SS} = –10V, V_{DD} = 5V,
supply noise V_{PP} = 0.2V

Figure 5-51. AC Power Supply Rejection Ratio (PSSR-AC)

6 Detailed Description

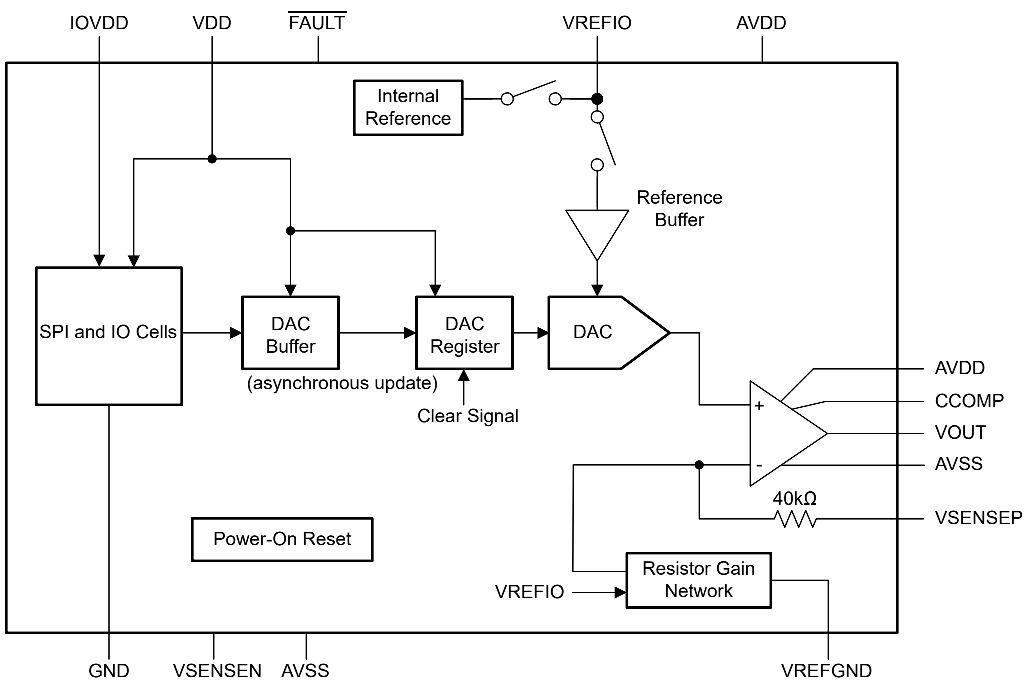
6.1 Overview

The 16-bit DAC81401 and 12-bit DAC61401 (DACx1401) are a pin-compatible family of single-channel, buffered, high-voltage output DACs. The DACx1401 offer bipolar output voltages of ±20V, ±10V, and ±5V, and full-scale unipolar output voltages of 40V, 10V, and 5V. The DAC output range is programmable. These devices are monotonic and provide exceptional linearity of less than 1LSB (maximum).

The DACx1401 integrate a 2.5V internal reference with maximum 10ppm/°C drift. The internal power-on reset circuit is designed to power the DAC output in power-down mode. The DAC remains in this mode until the output is enabled. The VSENSEP pin can sense the load voltage, while the CCOMP pin is used to connect an external compensation capacitor to support capacitive load larger than 2nF.

The digital interface of the DACx1401 uses a 4-wire serial peripheral interface (SPI) that operates at clock rates of up to 50MHz supporting 1.7V to 5.5V operation.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Digital-to-Analog Converter (DAC) Architecture

The DACx1401 devices consist of an R-2R ladder digital-to-analog converter (DAC) with ground buffer and a rail-to-rail output buffer amplifier. This device also includes an internal 2.5V reference. If the internal reference is not used, the reference voltage can be provided externally. Section 6.2 shows a simplified block diagram of the device architecture.

6.3.2 R-2R Ladder DAC

The DAC architecture consists of a voltage-output, segmented, R-2R ladder shown in Figure 6-1. The device incorporates a dedicated reference buffer that provides constant input impedance with code at the VREFIO pin. The output of the reference buffers drives the R-2R ladder. A production trim process provides excellent linearity and low glitch.

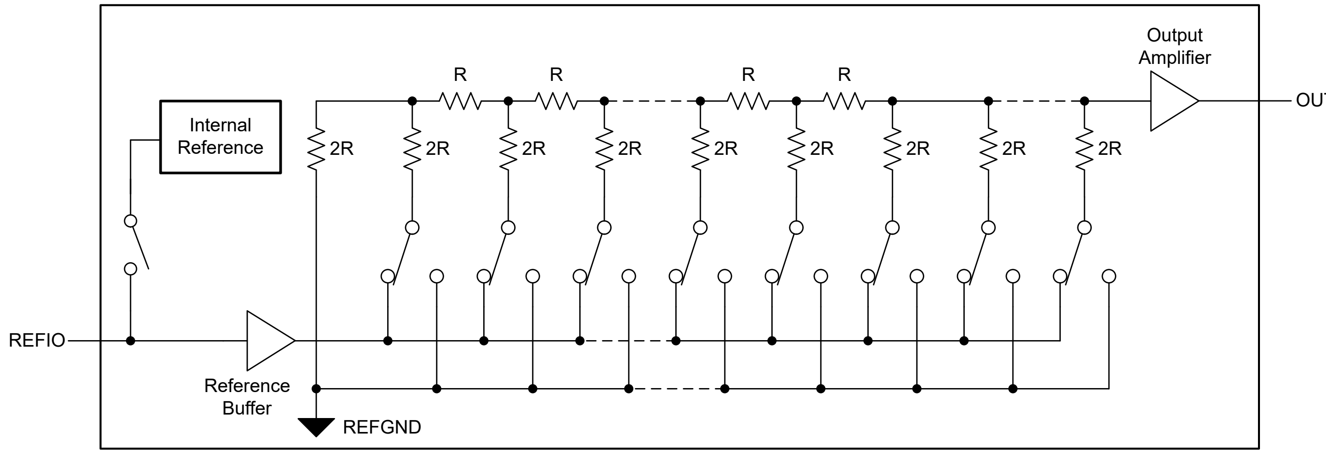


Figure 6-1. DACx1401 R-2R Ladder DAC

6.3.3 Programmable Gain Output Buffer

The voltage output stage, as conceptualized in Figure 6-2, provides the voltage output according to the DAC code and the output range setting.

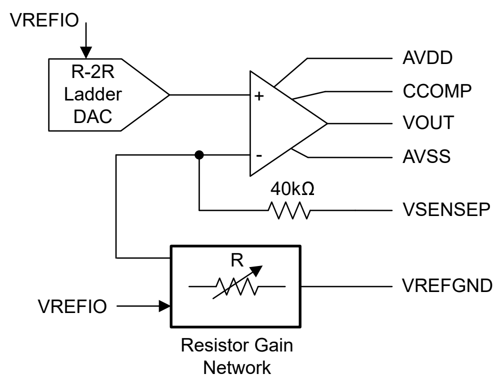


Figure 6-2. DACx1401 Voltage Output

The DAC output range can be programmed. Table 6-1 shows the range and corresponding gain.

Table 6-1. Voltage Output Range vs Gain Setting

MODE	VOLTAGE OUTPUT RANGE	GAIN
Unipolar	5V	2.0
	6V (20% overrange)	2.4
	10V	4.0
	12V (20% overrange)	4.8
	20V	8.0
	24V (20% overrange)	9.6
	40V	16.0
Bipolar	±5V	4.0
	±6V (20% overrange)	4.8
	±10V	8.0
	±12V (20% overrange)	9.6
	±20V	16.0

The output voltage (V_{OUT}) can be expressed as Equation 1 and Equation 2.

For unipolar output mode

$$V_{OUT} = V_{REFIO} \times GAIN \times \frac{CODE}{2^N} \tag{1}$$

For bipolar output mode

$$V_{OUT} = V_{REFIO} \times GAIN \times \frac{CODE}{2^N} - GAIN \times \frac{V_{REFIO}}{2} \tag{2}$$

Where:

- CODE is the decimal equivalent of the code loaded to the DAC register
- N is the bits of resolution: 16-bits for DAC81401, 12-bits for DAC61401
- VREFIO = 2.5V is the reference voltage (internal or external)
- GAIN is the gain factor assigned to each output voltage output range as shown in Table 6-1

The output amplifiers can drive up to ±15mA with 1.5V supply headroom while maintaining the specified total unadjusted error (TUE) specification for the device. The output stage has short-circuit current protection that limits the output current to 40mA. The device is designed to drive capacitive loads up to 2nF with the CCOMP pin unconnected. For capacitive loads greater than 2nF, an external compensation capacitor (470pF typical) must be connected between the CCOMP and VOUT pins to keep the output voltage stable, but at the expense of reduced bandwidth and increased settling time. With the external compensation capacitor, the device is able to drive capacitive loads up to 1µF (Section 5.5).

6.3.4 Sense Pins

The VSENSEP pin is provided to enable sensing of the load by connecting to points electrically closer to the load. This configuration allows the internal output amplifier to make sure that the correct voltage is applied across the load, as long as headroom is available on the power supply. The VSENSEP pin is used to correct for resistive drops on the system board, and are connected to VOUT at the pin. In some cases, both VOUT and VSENSEP are brought out through separate lines and connected remotely together at the load. In such cases, if the VSENSEP line is cut, then the amplifier loop is broken. Use a 5kΩ resistor between the VOUT and VSENSEP pins to maintain proper amplifier operation.

At device start up, the power-on reset circuit makes sure that all registers are at default values. The voltage output buffer is in a Hi-Z state. However, the VSENSEP pin connects to the amplifier inputs through an internal 40kΩ feedback resistor (Figure 6-2). If the VOUT and VSENSEP pins are connected together, the VOUT pin is also connected to the same node through the feedback resistor. This node is protected by internal circuitry and settles to a value between GND and the reference input.

6.3.5 DAC Register Structure

Data written to the DAC data registers are initially stored in the DAC buffer registers. The transfer of data from the DAC buffer registers to the active registers occurs immediately (asynchronous update). After the active registers are updated, the DAC output changes to the new values. After a power-on or reset event, the DAC data register sets to zero code, the DAC output amplifier powers down, and the DAC output connects to ground.

6.3.5.1 Output Update

The DAC double-buffered architecture enables data updates without disturbing the analog output. Data updates are performed asynchronously. In the update mode, a minimum wait time of 2.4µs ($t_{DACWAIT}$) is required between DAC output updates.

During update mode, a DAC data register write results in an immediate update of the DAC active register and the DAC output on a $\overline{SYNC}$ rising edge. The wait time is governed by $\overline{SYNC}$ timing (Figure 5-3).

6.3.5.2 Software Clear

The DAC output is set in clear mode through the SOFT-CLR bit in the TRIGGER register. In clear mode, the DAC data register is set to either zero code if configured for unipolar range operation or midscale code if set for bipolar range operation. A clear command forces the DAC to clear the contents of the buffer and active registers to the clear code.

6.3.5.2.1 Software Reset Mode

The DACx1401 implements a software reset feature. A device software reset is initiated by writing reserved code 0b1010 to SOFT-RESET in the TRIGGER register. The software reset command is triggered on the SYNC rising edge of the instruction.

6.3.6 Internal Reference

The device includes a precision 2.5V band-gap reference with a maximum temperature drift of 10ppm/°C. The internal reference is in power-down mode by default.

The internal reference voltage is available at the VREFIO pin and can source up to 5mA. To filter noise, place a minimum 150nF capacitor between the reference output and ground.

External reference operation is also supported. The external reference is applied to the VREFIO pin. If using an external reference, power down the internal reference.

6.3.7 Power-Supply Sequence

The DACx1401 has an internal power-on reset (POR) circuitry for both the digital and analog VDD and positive power AVDD supplies. This circuitry makes sure that the internal logic and power-on state of the DAC power up to the proper state independent of the supply sequence.

6.3.7.1 Power-On Reset (POR)

The device incorporates a power-on reset function. After the supplies reach the minimum specified values, a POR event is issued. Additionally, a POR event can be initiated by a SOFT-RESET command.

A POR event causes all registers to initialize to default values, and communication with the device is valid only after a 1ms POR delay. After a POR event, the device is set to power-down mode, where the DAC and internal reference are powered down and the DAC output is connected to ground through a 10kΩ internal resistor.

6.3.8 Thermal Alarm

The device incorporates a thermal shutdown that is triggered when the die temperature exceeds 140°C. A thermal shutdown sets the TEMP-ALM bit in the STATUS register, and causes the DAC output to power-down. However, the internal reference remains powered on. The $\overline{\text{FAULT}}$ pin can be configured to monitor a thermal shutdown condition by setting the TEMPALM-EN bit in the SPICONFIG register. After a thermal shutdown is triggered, the device stays in shutdown even after the device temperature lowers.

The die temperature must fall to less than 140°C before the device can be returned to normal operation. To resume normal operation, the thermal alarm must be cleared through the ALM-RESET bit in the TRIGGER register while the DAC channel is in power-down mode.

6.4 Device Functional Modes

6.4.1 Power Down Mode

The device output amplifiers and internal reference power-down status can be individually configured and monitored though the DAC-PWDWN bit. Setting DAC in power-down mode disables the output amplifier and clamps the output pin to ground through an internal 10kΩ resistor.

The DAC data registers are not cleared when the DAC goes into power-down mode. Upon return to normal operation, the DAC output voltages return to the same respective voltages prior to the device entering power-down mode. The DAC data registers can be updated while in power-down mode, which allows for changing the power-on voltage, if required.

After a power-on or reset event, the DAC output and the internal reference are in power-down mode. The entire device can be configured into power-down or active modes through the DEV-PWDWN bit.

6.5 Programming

The DACx1401 is controlled through a flexible four-wire serial interface that is compatible with SPI type interfaces used on many microcontrollers and DSP controllers. The interface provides read and write access to all registers of the DACx1401 device. Additionally, the interface can be configured to daisy-chain multiple devices for write operations.

6.5.1 Stand-Alone Operation

A serial interface access cycle is initiated by asserting the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, can be a continuous or gated clock. SDIN data are clocked in SCLK falling edges. A regular serial interface access cycle is 24 bits long with error checking disabled and 32 bits long with error checking enabled. Therefore, the $\overline{\text{SYNC}}$ pin must stay low for at least 24 or 32 SCLK falling edges. The access cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the first 24 or 32 bits are used by the device. When $\overline{\text{SYNC}}$ is high, the SCLK and SDIN signals are blocked, and SDO is in a Hi-Z state.

Table 6-2 describes the format for an error-checking-disabled access cycle (24-bits long). The first byte input to SDIN is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 6-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

Table 6-2. Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
23	R/W	Identifies the communication as a read or write command to the address register: R/W = 0 sets a write operation. R/W = 1 sets a read operation.
22	x	Don't care bit.
21-16	A[5:0]	Register address — specifies the register to be accessed during the read or write operation.
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values.

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit in the SPICONFIG register. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. The output data format is shown in Table 6-3. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit in the SPICONFIG register.

Table 6-3. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/W	Echo R/W from previous access cycle.
22	x	Echo bit 22 from previous access cycle.
21-16	A[5:0]	Echo address from previous access cycle.
15-0	DO[15:0]	Readback data requested on previous access cycle.

6.5.2 Daisy-Chain Operation

For systems that contain several DACx1401 devices, the SDO pin can be used to daisy-chain devices together. The daisy-chain feature is useful in reducing the number of serial interface lines. The SDO pin must be enabled by setting the SDO-EN bit in the SPICONFIG register before initiating daisy-chain operation.

The first falling edge on the $\overline{\text{SYNC}}$ pin starts the operation cycle (see Figure 6-4). If more than 24 clock pulses are applied while the $\overline{\text{SYNC}}$ pin is kept low, the data ripple out of the shift register and are clocked out on the SDO pin, either on the falling edge or rising edge of SCLK according to the FSDO bit. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed (Figure 6-3).

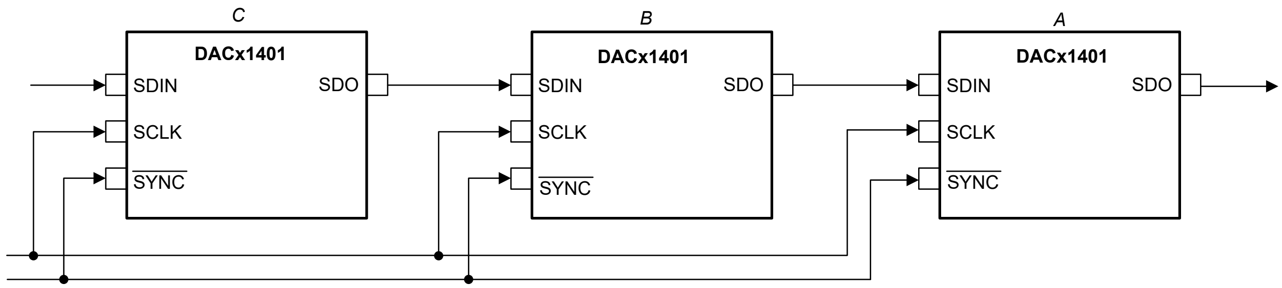


Figure 6-3. Daisy-Chain Setup

Each device in the system requires 24 clock pulses. As a result the total number of clock cycles must be equal to 24 × N, where N is the total number of devices in the daisy chain. When the serial transfer to all devices is complete the $\overline{\text{SYNC}}$ signal is taken high. This action transfers the data from the SPI shift registers to the internal register of each device in the daisy chain, and prevents any further data from being clocked into the input shift register.

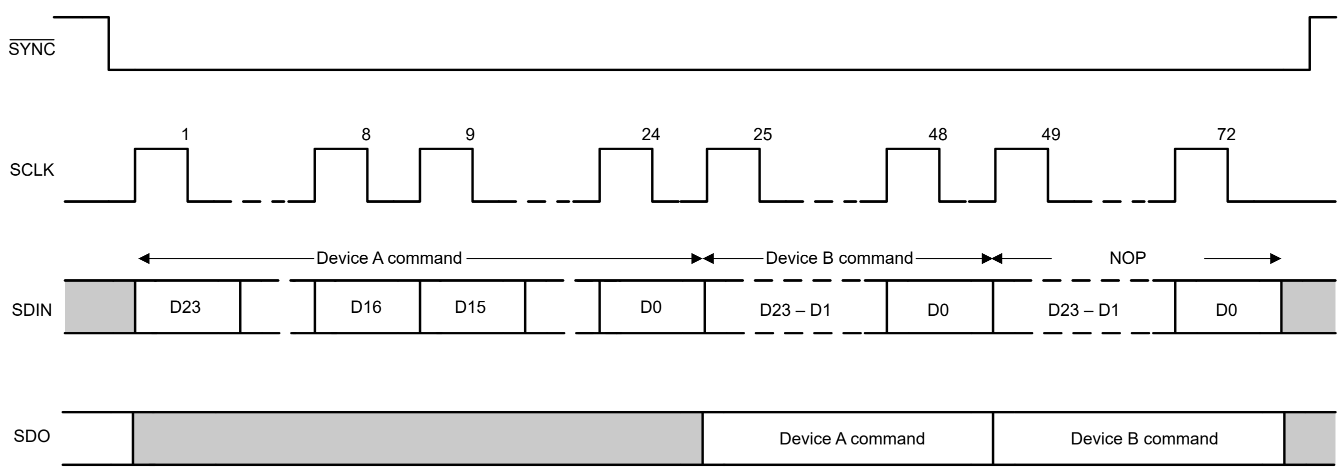


Figure 6-4. Serial Interface Daisy-Chain Write Cycle

6.5.3 Frame Error Checking

If the device is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature is enabled by setting the CRC-EN bit in the SPICONFIG register.

The error checking scheme is based on the CRC-8-ATM (HEC) polynomial: $x^8 + x^2 + x + 1$ (100000111). When error checking is enabled, the serial interface access cycle width is 32 bits. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding the data to the device. In all serial interface readback operations, the CRC polynomial is output on the SDO pin as part of the 32-bit cycle.

Table 6-4. Error Checking Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
31	R/W	Identifies the communication as a read or write command to the address register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
30	CRC-ERROR	Reserved bit. Set to zero.
29:24	A[5:0]	Register address. Specifies the register to be accessed during the read or write operation.
23:8	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values.
7:0	CRC	8-bit CRC polynomial.

The device decodes the 32-bit access cycle to compute the CRC remainder on $\overline{\text{SYNC}}$ rising edges. If no error exists, the CRC remainder is zero and data are accepted by the device.

A write operation failing the CRC check causes the data to be ignored by the device. After the write command, a second access cycle can be issued to determine the error checking results (CRC-ERROR bit) on the SDO pin.

If there is a CRC error, the CRC-ALM bit of the STATUS register is set to 1. The $\overline{\text{FAULT}}$ pin can be configured to monitor a CRC error by setting the CRCALM-EN bit in the SPICONFIG register.

Table 6-5. Write Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	R/W	Echo R/W from previous access cycle (R/W = 0).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, otherwise returns a 0.
29:24	A[5:0]	Echo address from previous access cycle.
23:8	DO[15:0]	Echo data from previous access cycle.
7:0	CRC	Calculated CRC value of bits 31:8.

A read operation must be followed by a second access cycle to get the requested data on the SDO pin. The error check result (CRC-ERROR bit) from the read command is output on the SDO pin.

As in the case of a write operation failing the CRC check, the CRC-ALM bit of the STATUS register is set to 1, and the $\overline{\text{FAULT}}$ pin, if configured for CRC alerts, is set low.

Table 6-6. Read Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	R/W	Echo R/W from previous access cycle (R/W = 1).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, otherwise returns a 0.
29:24	A[5:0]	Echo address from previous access cycle.
23:8	DO[15:0]	Readback data requested on previous access cycle.
7:0	CRC	Calculated CRC value of bits 31:8.

7 Register Map

Table 7-1 lists the memory-mapped registers for the device. Consider all register addresses not listed as reserved locations and do not modify the register contents.

Table 7-1. Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	NOP	W	0000	NOP[15:0]															
01	DEVICEID	R	029C (1) or 024C(2)	DEVICEID[13:0]														VERSIONID[1:0]	
02	STATUS	R	0000	RESERVED													CRC-ALM	DAC-BUSY	TEMP-ALM
03	SPICONFIG	R/W	0AA4	RESERVED				TEMPALM-EN	DACBUSY-EN	CRCALM-EN	RESERVED			DEV-PWDWN	CRC-EN	RSVD	SDO-EN	FSDO	RSVD
04	GENCONFIG	R/W	4000	RSVD	REF-PWDWN	RESERVED													
09	DACPWDWN	R/W	FFFF	RESERVED															DAC-PWDWN
0A	DACRANGE	W	0000	RESERVED												DAC-RANGE[3:0]			
0E	TRIGGER	R/W	0000	RESERVED						SOFT-CLR	ALM-RESET	RESERVED				SOFT-RESET[3:0]			
10	DAC	W	0000	DAC-DATA[15:0]															

(1) Reset code for DAC81401.
(2) Reset code for DAC61401.

7.1 Registers

Table 7-2 lists the memory-mapped registers for the device. All register offset addresses not listed in Table 7-2 are reserved locations. Do not modify the register contents.

Table 7-2. Registers

Offset	Acronym	Register Name	Section
00h	NOP	NOP Register	Go
01h	DEVICEID	DEVICE ID Register	Go
02h	STATUS	STATUS Register	Go
03h	SPICONFIG	SPI CONFIG Register	Go
04h	GENCONFIG	GENERAL CONFIG Register	Go
09h	DACPWDWN	DAC POWER DOWN Register	Go
0Ah	DACRANGE	DAC RANGE Register	Go
0Eh	TRIGGER	TRIGGER Register	Go
10h	DAC	DAC DATA Register	Go

7.1.1 NOP Register (Offset = 00h) [reset = 0000h]

NOP is shown in Figure 7-1 and described in Table 7-3.

Return to Summary Table.

Figure 7-1. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP[15:0]															
W-0000h															

Table 7-3. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	NOP	W	0000h	No operation. Write 0000h for proper no-operation command

7.1.2 DEVICEID Register (Offset = 01h) [reset = 0A70h or 0930h]

The device ID is shown in Figure 7-2 and described in Table 7-4.

Return to Summary Table.

Figure 7-2. DEVICEID Register

15	14	13	12	11	10	9	8
DEVICEID[13:6]							
R							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEVICEID[5:0]						VERSIONID[1:0]	
R-00h						R-0h	

Table 7-4. DEVICEID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	DEVICEID	R	029Ch or 024Ch	Device ID 029C: DAC81401 (16 Bits) 024C: DAC61401 (12 Bits)
1:0	VERSIONID	R	0h	Version ID. Subject to change

7.1.3 STATUS Register (Offset = 02h) [reset = 0000h]

The status register is shown in Figure 7-3 and described in Table 7-5.

Return to Summary Table.

Figure 7-3. STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	6	5	4	3	2	1	0
RESERVED					CRC-ALM	DAC-BUSY	TEMP-ALM
R-00h					R-0h	R-0h	R-0h

Table 7-5. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	N/A	0h	Reserved
2	CRC-ALM	R	0h	CRC Alarm 0: no error in CRC 1: CRC error indicated
1	DAC-BUSY	R	0h	DAC Busy 0: DAC is ready for update 1: DAC is not ready for update
0	TEMP-ALM	R	0h	Temperature Alarm 0: No thermal alarm 1: Die temperature is over +140°C. A thermal alarm event forces the DAC output to go into power-down mode

7.1.4 SPICONFIG Register (Offset = 03h) [reset = 0AA4h]

The SPI configuration register is shown in Figure 7-4 and described in Table 7-6.

Return to Summary Table.

Figure 7-4. SPICONFIG Register

15	14	13	12	11	10	9	8
RESERVED				TEMPALM-EN	DACBUSY-EN	CRCALM-EN	RESERVED
R-0h				R/W-1h	R/W-0h	R/W-1h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		DEV-PWDWN	CRC-EN	RESERVED	SDO-EN	FSDO	RESERVED
R-1h	R-0h	R/W-1h	R/W-0h	R-0h	R/W-1h	R/W-0h	R-0h

Table 7-6. SPICONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11	TEMPALM-EN	R/W	1h	Temperature alarm enable 0: Thermal alarm does not trigger the $\overline{\text{FAULT}}$ pin 1: Thermal alarm triggers the $\overline{\text{FAULT}}$ pin
10	DACBUSY-EN	R/W	0h	DAC busy indicator enable 0: No DAC busy indicator 1: The $\overline{\text{FAULT}}$ pin is set between DAC output updates. This alarm resets automatically
9	CRCALM-EN	R/W	1h	CRC alarm enable 0: No CRC alarm indicator 1: A CRC error triggers the $\overline{\text{FAULT}}$ pin
8:6	RESERVED	R	2h	Reserved
5	DEV-PWDWN	R/W	1h	Device power-down enable 0: The device is in active mode 1: The device is in power-down mode
4	CRC-EN	R/W	0h	CRC enable 0: No CRC 1: frame error checking is enabled
3	RESERVED	R	0h	Reserved
2	SDO-EN	R/W	1h	SDO pin enable 0: The SDO pin is not operational 1: The SDO pin is operational
1	FSDO	R/W	0h	Fast SDO bit enable 0: SDO updates on SCLK rising edges 1: SDO updates on SCLK falling edges
0	RESERVED	R	0h	Reserved

7.1.5 GENCONFIG Register (Offset = 04h) [reset = 0000h]

The general configuration register is shown in Figure 7-5 and described in Table 7-7.

Return to Summary Table.

Figure 7-5. GENCONFIG Register

15	14	13	12	11	10	9	8
RESERVED	REF-PWDWN	RESERVED					
R-0h	R/W-1h	R-00h					
7	6	5	4	3	2	1	0
RESERVED							
R-00h							

Table 7-7. GENCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	REF-PWDWN	R/W	1h	Reference power down 0: Internal reference enabled 1: Internal reference disabled
13:0	RESERVED	R	0000h	Reserved

7.1.6 DACPWDWN Register (Offset = 09h) [reset = FFFFh]

The DAC power-down register is shown in Figure 7-6 and described in Table 7-8.

Return to Summary Table.

Figure 7-6. DACPWDWN Register

15	14	13	12	11	10	9	8
RESERVED							
R-FFh							
7	6	5	4	3	2	1	0
RESERVED							DAC-PWDWN
R-FFh							R/W-1h

Table 7-8. DACPWDWN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED	N/A	FFFFh	Reserved
0	PDN	R/W	0h	DAC power down bit 0: DAC is enabled 1: DAC is powered down and the output is connected to ground through a 10kΩ internal resistor

7.1.7 DACRANGE Register (Offset = 0Ah) [reset = 0000h]

The DAC range register is shown in Figure 7-7 and described in Table 7-9.

Return to Summary Table.

Figure 7-7. DACRANGE Register

15	14	13	12	11	10	9	8
RESERVED							
N/A-0h							
7	6	5	4	3	2	1	0
RESERVED				DAC-RANGE3:0			
N/A-0h				R/W-0h			

Table 7-9. DACRANGE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	N/A	000h	Reserved
3:0	DAC-RANGE	R/W	0h	Sets the output range for the corresponding DAC. 0000: 0V to 5V 1000: 0V to 6V 0001: 0V to 10V 1001: 0V to 12V 0010: 0V to 20V 1010: 0V to 24V 0011: 0V to 40V 0101: –5.0V to +5.0V 1101: –6.0V to +6.0V 0110: –10.0V to +10.0V 1110: –12.0V to +12.0V 0111: –20.0V to +20.0V All other combinations invalid

7.1.8 TRIGGER Register (Offset = 0Eh) [reset = 0000h]

The trigger register is shown in Figure 7-8 and described in Table 7-10.

Return to Summary Table.

Figure 7-8. TRIGGER Register

15	14	13	12	11	10	9	8
RESERVED						SOFT-CLR	ALM-RESET
W-00h						W-0h	W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				SOFT-RESET[3:0]			
W-0h				W-0h			

Table 7-10. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	W	00h	Reserved
9	SOFT-CLR	W	0h	Software clear of the DAC output 0: DAC output remains unchanged 1: DAC output is cleared
8	ALM-RESET	W	0h	Set this bit to 1 to clear an alarm event. Not applicable for a DAC-BUSY alarm event
7-4	RESERVED	W	0h	Reserved
3:0	SOFT_RESET	W	0h	Set these bits to reserved code 0b1010 to reset the device to the default state

7.1.9 DAC Register (Offset = 10h) [reset = 0000h]

The DAC data register is shown in Figure 7-9 and described in Table 7-11.

Return to Summary Table.

Figure 7-9. DAC Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-DATA[15:0]															
W-0000h															

Table 7-11. DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
	DAC-DATA	W	0h	Stores the 16-bit data to be loaded to DAC in MSB-aligned straight-binary format. Data use the following format: DAC81401: {DATA[15:0]} DAC61401: {DATA[11:0], x, x, x, x} x – Don't care bits

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A primary application of the DACx1401 is programmable power supplies commonly used in automated test and laboratory equipment. With an excellent linearity of ±1 LSB INL and inherently monotonic design, the DACx1401 meets the requirement of high precision and provides a wide range of programmable voltage.

8.2 Typical Application

The DACx1401 output (VOUT) is capable of providing from –20V to +40V. However, some applications require even higher voltages. Figure 8-1 shows a simplified diagram to design the high-voltage requirement for this application using the DACx1401 with an external high-voltage gain stage.

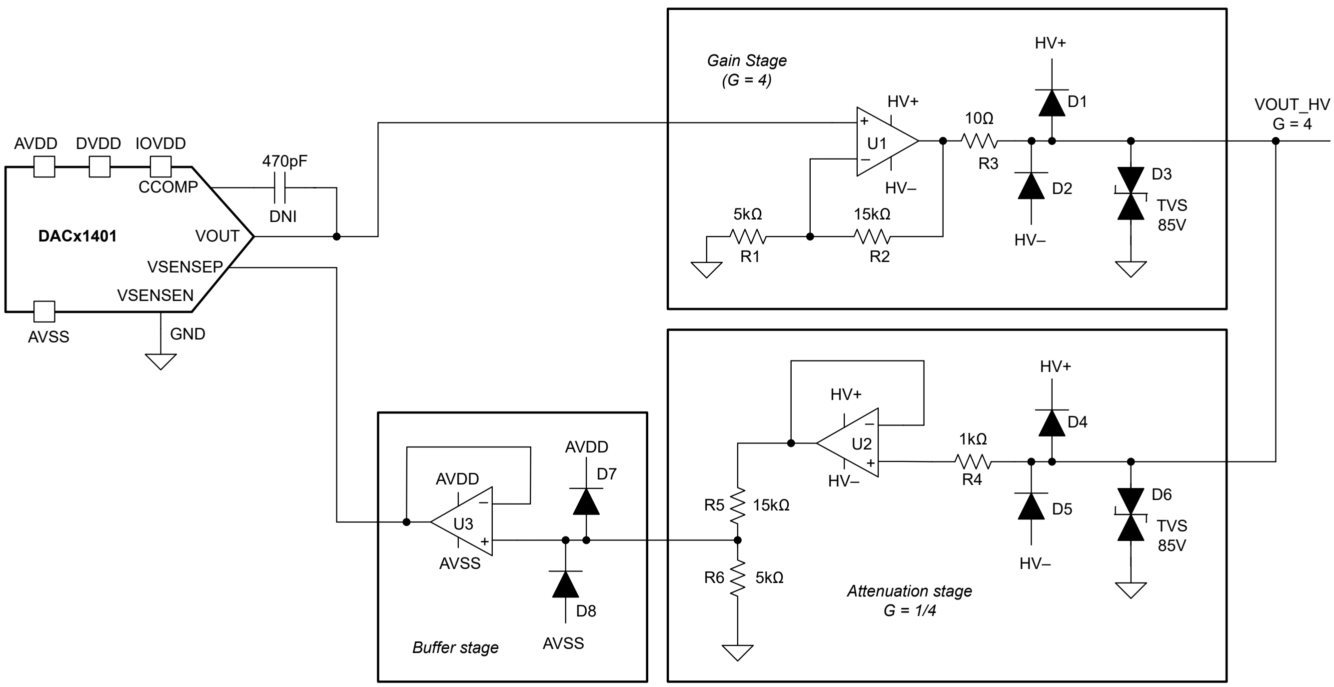


Figure 8-1. High-Voltage Gain-Stage Block Diagram

8.2.1 Design Requirements

- Voltage range: ±40V, 0V to 80V
- Minimum external power supplies: HV+ and HV–

8.2.2 Detailed Design Procedure

The DACx1401 devices are a great choice for this application because of the exceptional linearity and noise performance.

The DACx1401 are capable of providing output voltage 0V to 40V, or ±20V. In high-voltage applications where the voltage requirement is beyond 0V to 40V or ±20V, a high-voltage gain stage can be used to get a voltage ranging from 0V to 80V, or ±40V. This high-voltage gain stage requires an external high-voltage power supply.

8.2.2.1 Key Components

- U1, U2—OPA593 85V, low-offset, low-noise, 10MHz, 250mA output current, precision operational amplifier
- U3—OPA189 36V, low-offset, low-drift, low-noise, 14MHz precision operational amplifier
- D1, D2, D4, D5, D7, D8—Schottky diode 100V, 150mA, 0.7V forward voltage, fast switching
- D3, D6—85V standoff voltage, high-current, bidirectional TVS
- R1, R2—low temperature coefficient and high accuracy (< 0.01%) thin film resistors
- R5, R6—low temperature coefficient and high accuracy (< 0.01%) thin film resistors

8.2.2.2 Compensation Capacitor

The 470pF compensation capacitor is optional and the CCOMP pin can be left floating. This compensation capacitor is only required if the load capacitor at the DACx1401 VOUT node is greater than 2nF.

8.2.2.3 Gain Stage

The gain stage amplifies the DAC output voltage by 4 ×. This gain stage uses the OPA593 (U1), which supports an output voltage from 0V to 85V or ±42.5V. At the gain stage output, obtain 0V to 80V ±40V by programming the DAC output 0V to 20V or ±10V, respectively. For a given gain-stage output, calculate the DAC output by the Equation 3:

$$\mathrm{VOUT} = \frac{\mathrm{VOUT\_HV}}{4} \tag{3}$$

Where:

- VOUT: output voltage of DACx1401
- VOUT_HV: output of the gain stage (U1) in block diagram

The gain stage output vs DAC output plot is provided in Figure 8-2 and Figure 8-3 for both unipolar and bipolar modes, respectively.

8.2.2.4 Attenuation and Buffer Stage

To avoid any unintended I-R drop, connect VOUT and VSENSEP close to the load, and the voltage value for VSESNEP and VOUT must be same. Therefore, the gain stage output voltage is first buffered (U2) and then attenuated by a factor of 4 × with resistor divider R5 and R6.

VSENSEP has an input impedance of approximately 50kΩ, and the resistor divider voltage cannot be connected directly, which causes erroneous voltage due to loading. This voltage output is first buffered (U3) and then connected to VSENSEP node of DACx1401 to close the internal feedback loop with VOUT.

8.2.2.5 External Power Supply

An external high-voltage power supply is required for the OPA593 used in the gain stage (U1) and attenuation stage (U2). The power supply must meet the headroom and footroom requirements as per the OPA593 data sheet. These external power supplies needs to be provided from high voltage supply source. Typical values used for HV+ and HV– are +41V and –41V, or 81V and 0V, respectively.

$$\mathrm{HV+} = \max\left(\mathrm{VOUT\_HV}\right) + \mathrm{headroom}\left(\mathrm{OPA593}\right) \tag{4}$$

$$\mathrm{HV-} = \min\left(\mathrm{VOUT\_HV}\right) - \mathrm{footroom}\left(\mathrm{OPA593}\right) \tag{5}$$

Where VOUT_HV is output of the gain stage (U1) in block diagram.

8.2.2.6 Protection Design

If the device output pins are exposed to industrial transient testing without external protection components, the internal diode structures of the DACx1401 become forward biased and conduct current. If the conducted current is large, as is common in high-voltage industrial transient tests, the structures become permanently damaged and impact the device functionality.

The gain-stage output and attenuation-stage input includes an external electrical-overstress protection circuit for short-circuit events. Protection is achieved by the transient voltage suppressor (TVS) diodes D3 and D6, and clamp-to-rail diodes D1, D2, D4, D5.

The combined effects of both TVS and clamp-to-rail diodes limits the current flowing into the device internal diode structures to prevent permanent damage. If the Schottky diode clamps VOUT to ±1.5V from the rail, then the peak current entering the device is equal to 80mA, assuming R1 = 10Ω and the diode FB is 0.7V. Also include TVS diodes D3 and D6 at the gain-stage output and attenuation-stage input nodes to provide a discharge path for the energy sent to these nodes through diodes D3 and D6, and the internal diode structures. In the absence of these diodes, when current is diverted to these nodes, the decoupling capacitors charge, slowly increasing the voltage at these nodes, which can exceed the threshold limits of HV+ and HV–.

8.2.2.7 Design Accuracy

The gain stage output has an error contributed by mostly from:

- Offset voltage of U1 (OPA593): ±100µV offset voltage of OPA593 has a small error contribution to the static device performance. The error contribution from offset voltage is calculated to be 0.00025%FSR using Equation 6, considering a 40V span for the gain stage output.

$$\mathrm{error}\left(\%\mathrm{FSR}\right) = \frac{\text{offset voltage}}{\text{gain stage voltage span}} \times 100 \tag{6}$$

- Gain resistors R1 and R2: Mismatch in ratio of R1 and R2 causes a gain error at the gain stage output. The error contribution due to mismatch in the ratio R1 and R2, is calculated to be 0.02%FSR using Equation 7.

$$\mathrm{error}\left(\%\mathrm{FSR}\right) = \left(1 - \frac{(1 \pm \Delta\,\mathrm{R2})}{(1 \pm \Delta\,\mathrm{R1})}\right) \times 100 \tag{7}$$

The calculated error contributions from U1, R1, and R3 show that the final gain stage output is just as accurate as the DACx1401.

8.2.3 Application Curves

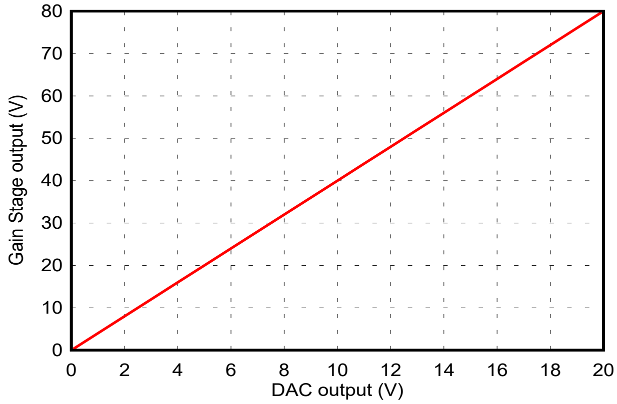


Figure 8-2. Gain Stage Output vs DAC Output (Unipolar Mode)

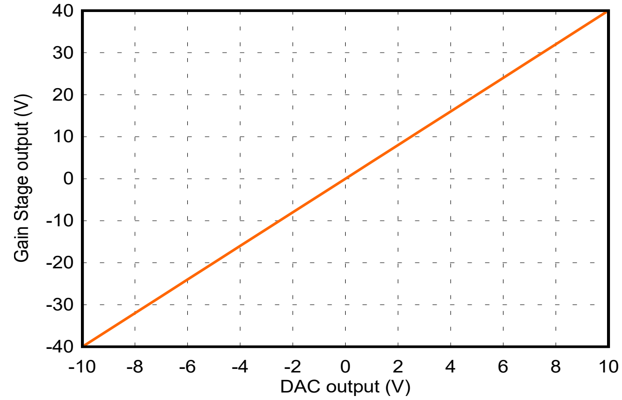


Figure 8-3. Gain Stage Output vs DAC Output (Bipolar Mode)

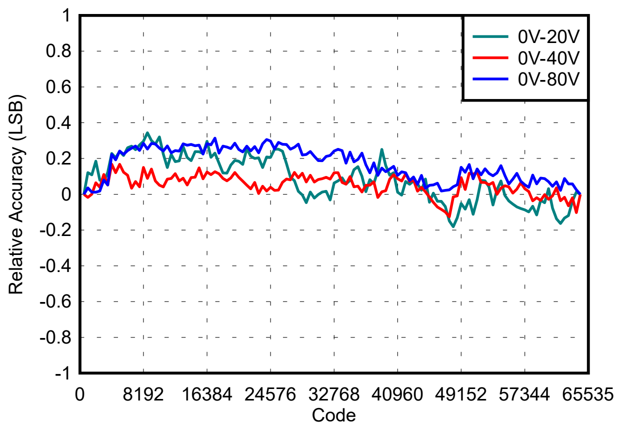


Figure 8-4. Relative Accuracy vs Digital Input Code (Unipolar Mode)

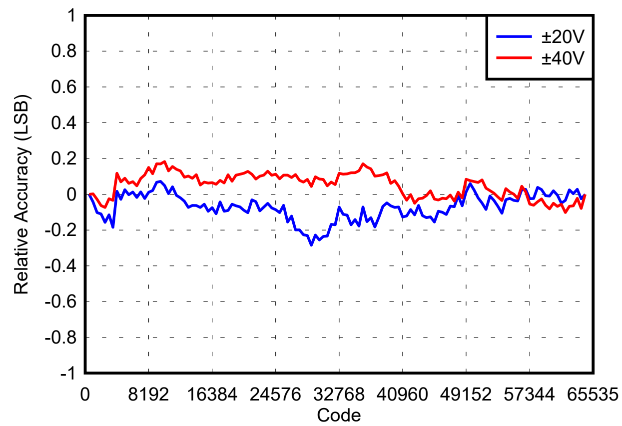


Figure 8-5. Relative Accuracy vs Digital Input Code (Bipolar Mode)

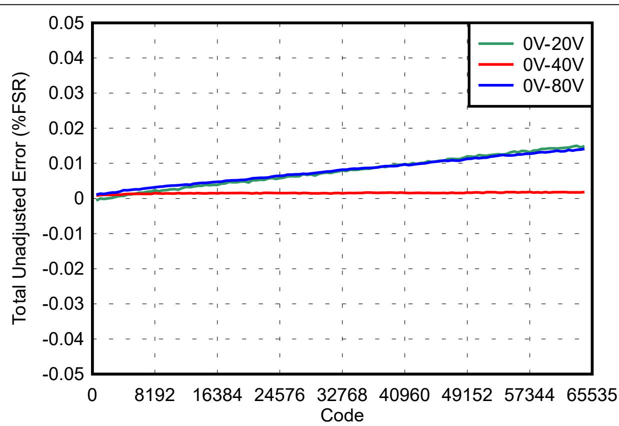


Figure 8-6. TUE vs Digital Input Code (Unipolar Mode)

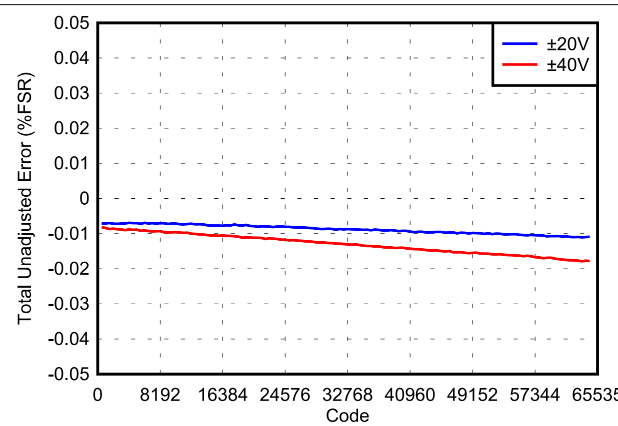


Figure 8-7. TUE vs Digital Input Code (Bipolar Mode)

8.3 Initialization Set Up

To check the basic functionality and working of the DACx1401, follow the steps as described here:

- Power up the device with supply values AVDD = 15V, AVSS = –15V, VDD = 5V and IOVDD = 3.3V (these are just recommendation and can be different as per device operating conditions)
- Write SPI frame in the following sequence:
  - Write 0x0A04 to the SPI_CONFIG (0x03) register to power up the device
  - Write 0x0000 to the GEN_CONFIG (0x04) register to power up the internal reference
  - Write 0xFFFE to the DAC_PWDWN (0x09) register to power up the DAC output
  - Write 0x0005 to the DACRANGE (0x0A) register to configure the DAC in ±5V range, default output range is 0V to 5V
  - Write 0x0000, 0x7FFF or 0xFFFF to the DAC (0x10) register to configure the DACx1401 VOUT to 2.5V, 0V, or 2.5V

8.4 Power Supply Recommendations

The device requires four power-supply inputs: IOVDD, VDD, AVDD, and AVSS. Connect a 0.1µF ceramic capacitor close to each power-supply pin. In addition, a 4.7µF or 10µF bulk capacitor is recommended for each power supply. Choose tantalum or aluminum types for the bulk capacitors.

External reference voltage of 2.5V can be supplied to VREFIO pin provided VDD supply is powered up beforehand.

The digital pins of the DACx1401 (SCLK, SDI, $\overline{\text{SYNC}}$ and SDO) are not fail safe. Pull the digital pins to logic level high with IOVDD supply or after IOVDD supply, but not before.

There is no sequencing requirement for the power supplies. The DAC output range is configurable; therefore, sufficient power-supply headroom is required to achieve linearity at codes close to the power-supply rails. When sourcing or sinking current from or to the DAC output, account for the effects of power dissipation on the temperature of the device, and the device must not exceed the maximum junction temperature.

8.5 Layout

8.5.1 Layout Guidelines

Printed circuit board (PCB) layout plays a significant role in achieving desired ac and dc performance from the device and this kind of precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. As a general rule, place digital traces as far away from analog traces as possible.

Place bypass capacitor and additional capacitor close to the device. The recommended capacitors for this device are listed below:

- 0.1μF capacitor close to the device and another 1μF to 10μF capacitor for AVDD
- 0.1μF capacitor close to the device and another 1μF to 10μF capacitor for AVSS
- 0.1μF capacitor close to the device and another 1μF to 10μF capacitor for VDD
- 0.1μF capacitor close to the device and another 1μF capacitor (optional) for IOVDD
- 0.15μF capacitor at VREFIO pin for internal reference noise filtering

For best power-supply bypassing, place the bypass capacitors close to the respective power-supply pins. Provide unbroken ground reference planes for the digital signal traces, especially for the SPI signals. The $\overline{\text{FAULT}}$ signal is static line; therefore, this line can lay on the analog side of the ground plane. Figure 8-8 and Figure 8-9 show example layouts.

8.5.2 Layout Examples

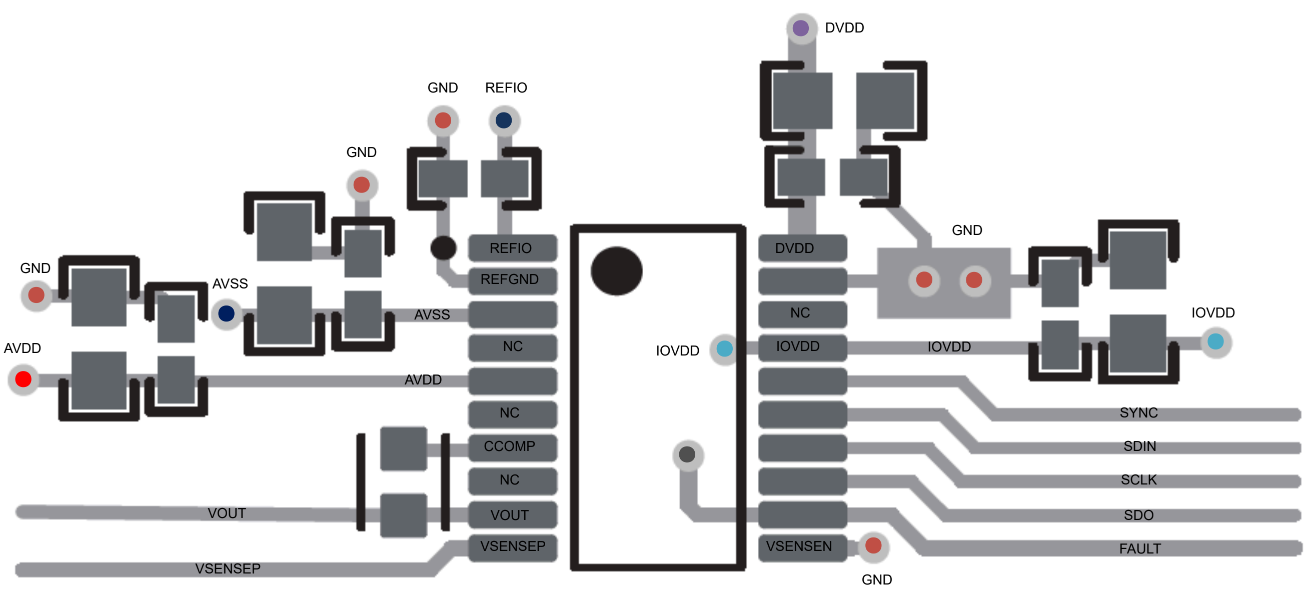


Figure 8-8. Layout Example: PW (TSSOP)

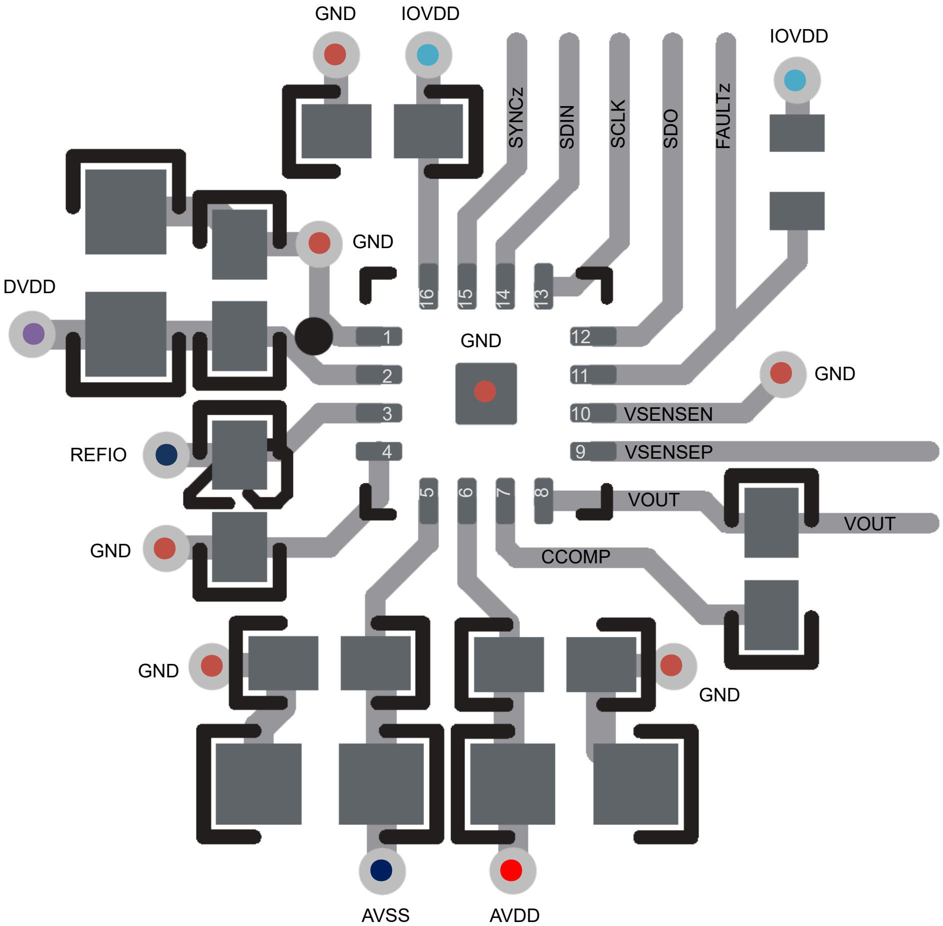


Figure 8-9. Layout Example: RTE (WQFN)

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2023) to Revision A (December 2024)	Page
• Added the WQFN package to data sheet	1
• Updated TUE in Bipolar ranges	5
• Updated ZCE in Unipolar ranges	5
• Updated Bipolar zero (midscale) error	5
• Updated Figure 5-18	14
• Added Figure 5-45 and Figure 5-47	14

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC61401PWR	ACTIVE	TSSOP	PW	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAC61401	Samples
DAC81401PWR	ACTIVE	TSSOP	PW	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAC81401	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

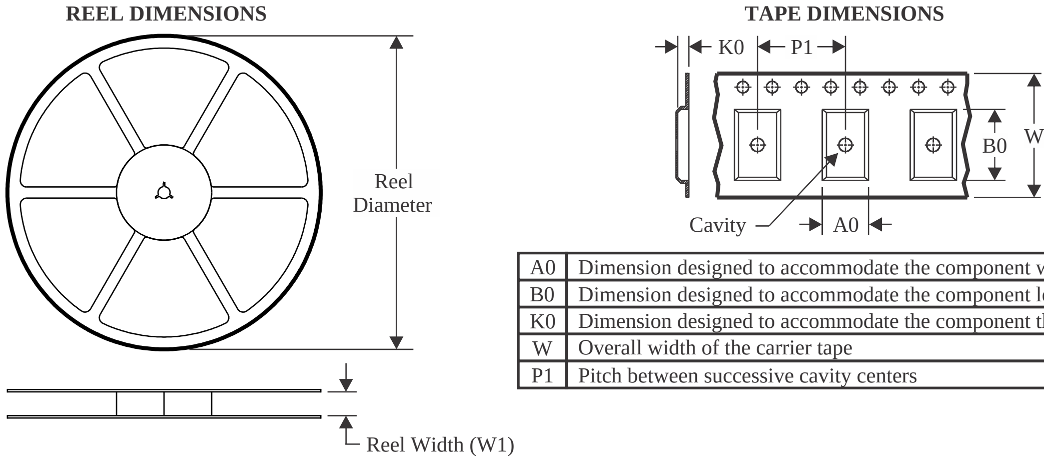
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

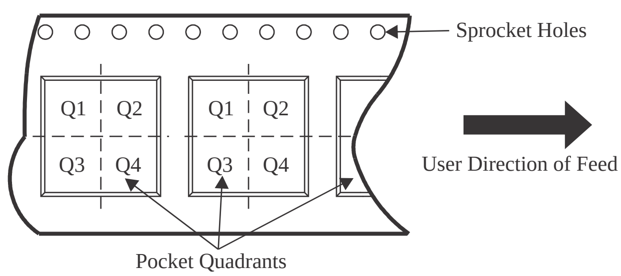
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION



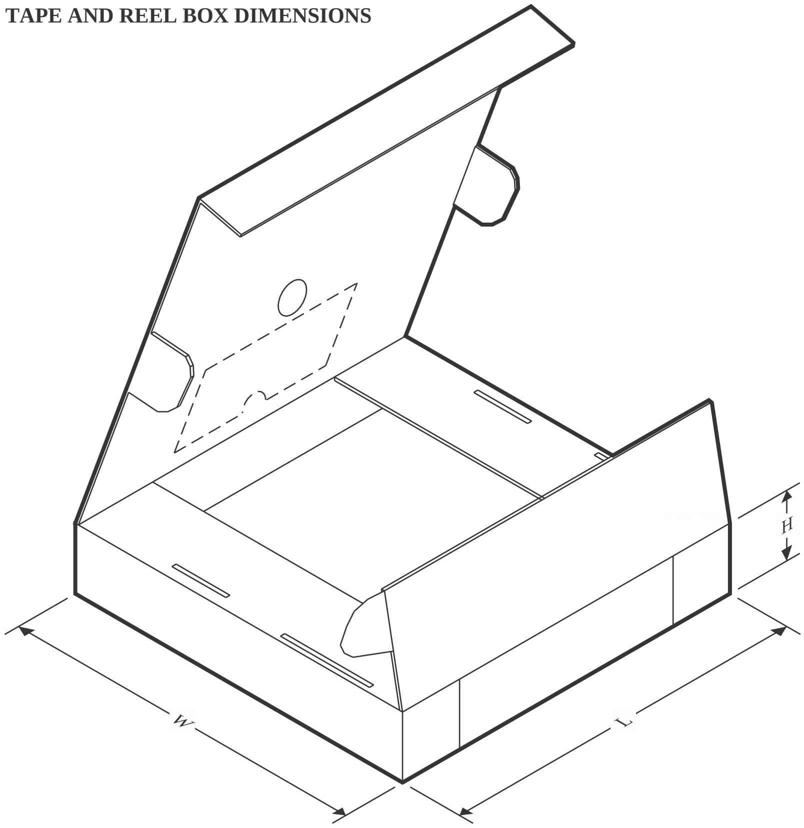
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

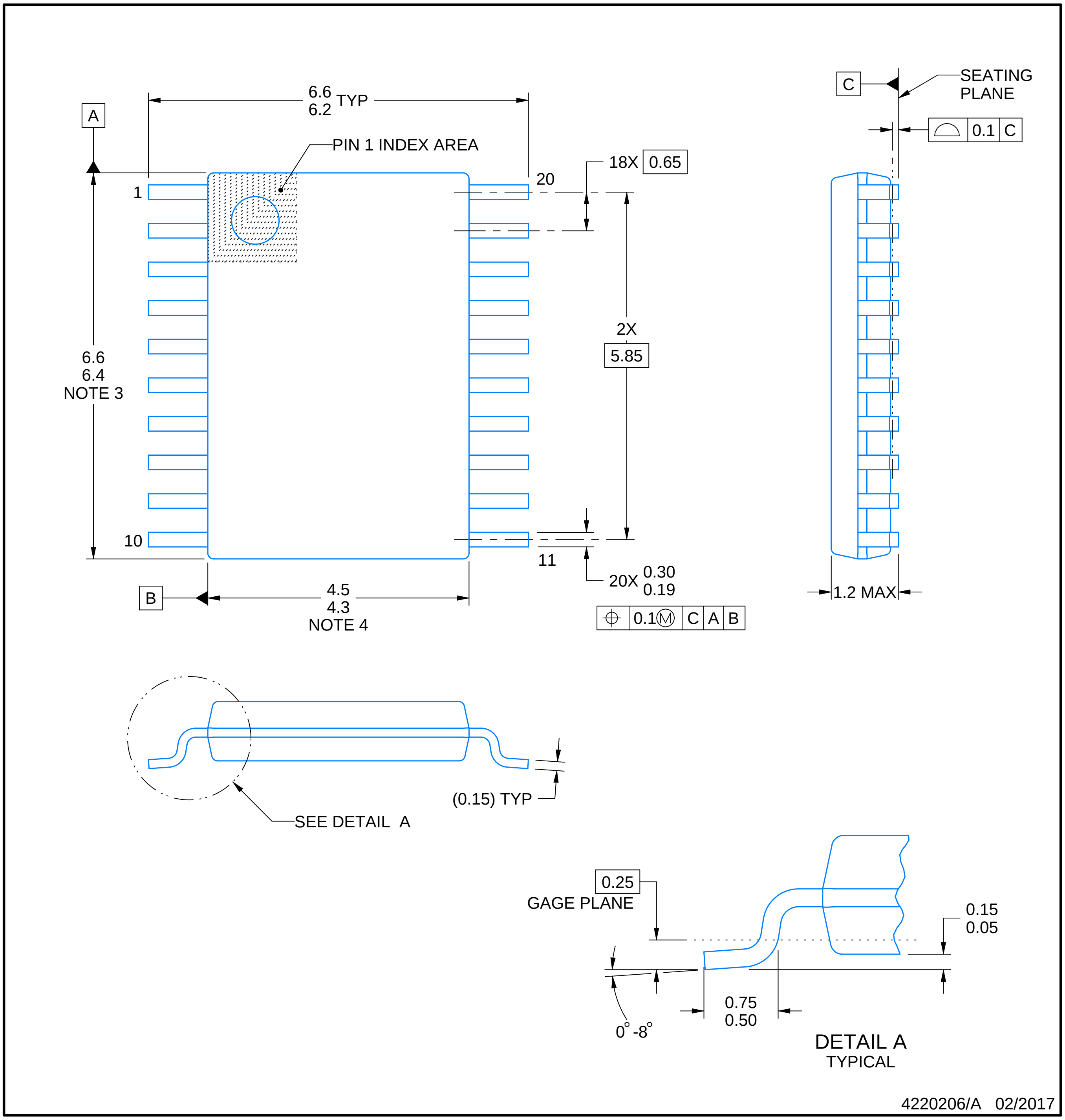
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC61401PWR	TSSOP	PW	20	3000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
DAC81401PWR	TSSOP	PW	20	3000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



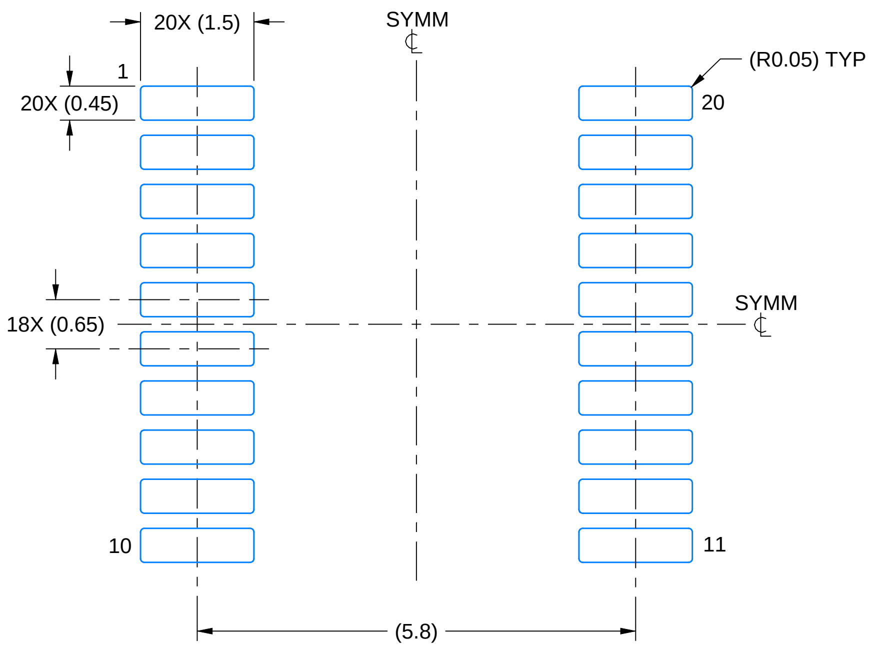
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC61401PWR	TSSOP	PW	20	3000	356.0	356.0	35.0
DAC81401PWR	TSSOP	PW	20	3000	356.0	356.0	35.0

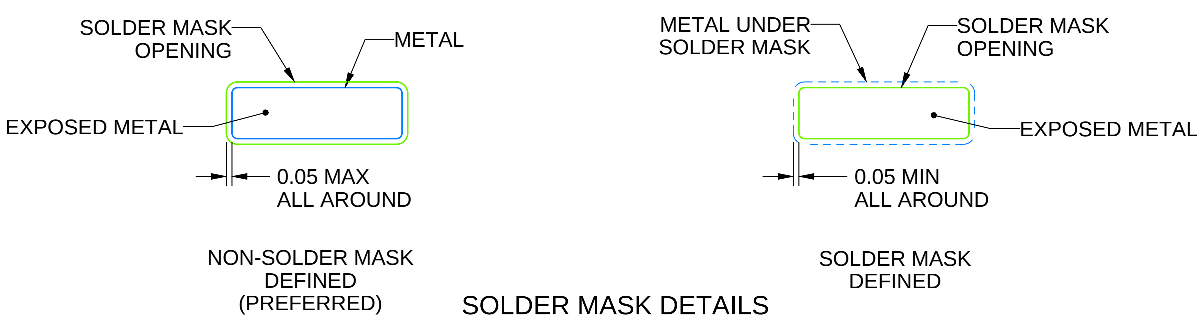


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

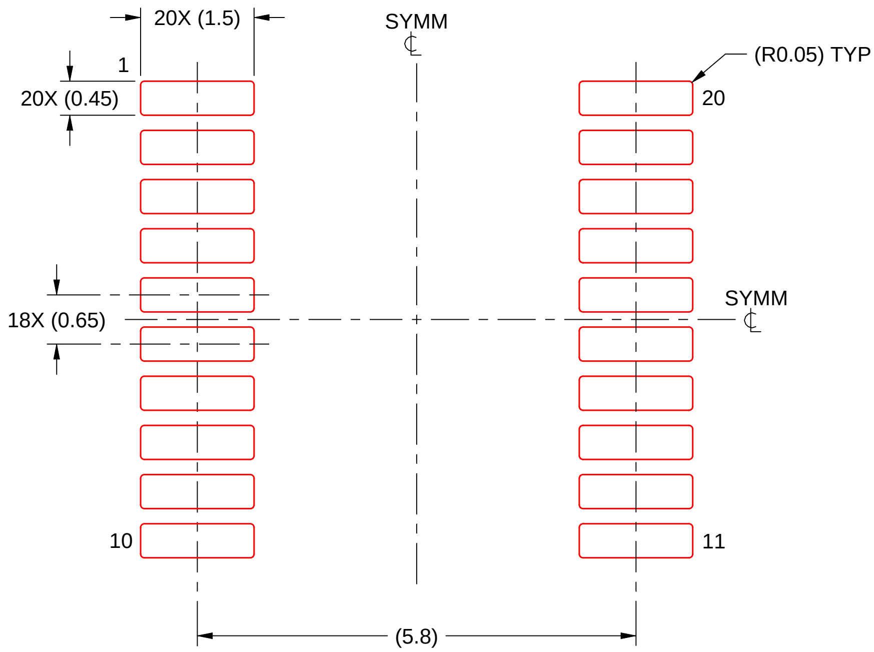


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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