LM324-MIL Quadruple Operational Amplifier

1 Features

- Wide Supply Ranges
  - Single Supply: 3 V to 32 V
  - Dual Supplies: ±1.5 V to ±16 V
- Low Supply-Current Drain Independent of Supply Voltage: 0.8 mA Typical
- Common-Mode Input Voltage Range Includes Ground, Allowing Direct Sensing Near Ground
- Low Input Bias and Offset Parameters
  - Input Offset Voltage: 3 mV Typical
  - Input Offset Current: 2 nA Typical
  - Input Bias Current: 20 nA Typical
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: 32 V
- Open-Loop Differential Voltage Amplification: 100 V/mV Typical
- Internal Frequency Compensation
- On Products Compliant to MIL-PRF-38535, All Parameters are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Blu-ray Players and Home Theaters
- Chemical and Gas Sensors
- DVD Recorders and Players
- Digital Multimeter: Bench and Systems
- Digital Multimeter: Handhelds
- Field Transmitter: Temperature Sensors
- Motor Control: AC Induction, Brushed DC, Brushless DC, High-Voltage, Low-Voltage, Permanent Magnet, and Stepper Motor
- Oscilloscopes
- TV: LCD and Digital
- Temperature Sensors or Controllers Using Modbus
- Weigh Scales

3 Description

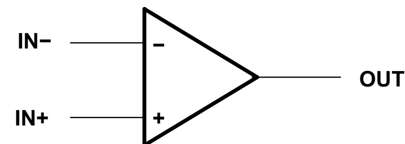
This device consist of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply or split supply over a wide range of voltages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM324-MIL	SOIC (14)	8.65 mm × 3.91 mm
	CDIP (14)	19.56 mm × 6.67 mm
	PDIP (14)	19.30 mm × 6.35 mm
	CFP (14)	9.21 mm × 5.97 mm
	TSSOP (14)	5.00 mm × 4.40 mm
	SO (14)	9.20 mm × 5.30 mm
	SSOP (14)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Symbol (Each Amplifier)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 **Features** 1
2 **Applications** 1
3 **Description** 1
4 **Revision History** 2
5 **Pin Configuration and Functions** 3
6 **Specifications** 4
6.1 Absolute Maximum Ratings 4
6.2 ESD Ratings 4
6.3 Recommended Operating Conditions 4
6.4 Thermal Information 4
6.5 Electrical Characteristics 5
6.6 Operating Conditions 5
6.7 Typical Characteristics 6
7 **Parameter Measurement Information** 7
8 **Detailed Description** 8
8.1 Overview 8
8.2 Functional Block Diagram 8
8.3 Feature Description 9
8.4 Device Functional Modes 9
9 **Application and Implementation** 10
9.1 Application Information 10
9.2 Typical Application 10
10 **Power Supply Recommendations** 12
11 **Layout** 13
11.1 Layout Guidelines 13
11.2 Layout Examples 13
12 **Device and Documentation Support** 14
12.1 Documentation Support 14
12.2 Receiving Notification of Documentation Updates 14
12.3 Community Resources 14
12.4 Trademarks 14
12.5 Electrostatic Discharge Caution 14
12.6 Glossary 14
13 **Mechanical, Packaging, and Orderable Information** 14

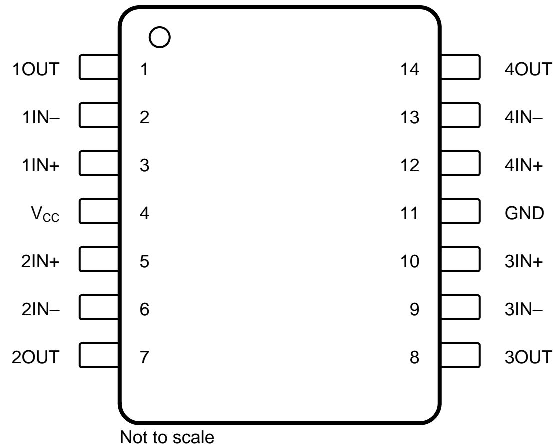
4 Revision History

DATE	REVISION	NOTES
June 2017	*	Initial release.

Copyright © 2017, Texas Instruments Incorporated

5 Pin Configuration and Functions

D, DB, J, N, NS, PW, W PACKAGE
14-Pin SOIC, SSOP, CDIP, PDIP, SO, TSSOP, CFP
(Top View)



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Negative input
1IN+	3	I	Positive input
1OUT	1	O	Output
2IN–	6	I	Negative input
2IN+	5	I	Positive input
2OUT	7	O	Output
3IN–	9	I	Negative input
3IN+	10	I	Positive input
3OUT	8	O	Output
4IN–	13	I	Negative input
4IN+	12	I	Positive input
4OUT	14	O	Output
GND	11	—	Ground
NC	—	—	Do not connect
V_{CC}	4	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (2)		±16	32	V
Differential input voltage, V_{ID} (3)			±32	V
Input voltage, V_I (either input)		–0.3	32	V
Duration of output short circuit (one amplifier) to ground at (or below) T_A = 25°C, V_{CC} ≤ 15 V (4)		Unlimited		
Operating virtual junction temperature, T_J			150	°C
Case temperature for 60 seconds	FK package		260	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+, with respect to IN−.
(4) Short circuits from outputs to VCC can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	30	V
V_{CM}	Common-mode voltage	0	V_{CC} – 2	V
T_A	Operating free air temperature	0	70	°C

6.4 Thermal Information

THERMAL METRIC(1)		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	J (CDIP)	W (CFP)	UNIT
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$ (2)(3)	Junction-to-ambient thermal resistance	86	86	80	76	113	—	—	°C/W
$R_{\theta JC}$ (4)	Junction-to-case (top) thermal resistance	—	—	—	—	—	15.05	14.65	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Short circuits from outputs to VCC can cause excessive heating and eventual destruction.
(3) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_{J(max)} – T_C)/R_{\theta JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

Copyright © 2017, Texas Instruments Incorporated

6.5 Electrical Characteristics

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		T_A[2]	MIN	TYP[3]	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR}min, V_O = 1.4 V		25°C		3	7	mV
				Full range			9	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		2	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–20	–250	nA
				Full range			–500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX		25°C	0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			
V_{OH}	High-level output voltage	R_L = 2 kΩ		25°C	V_{CC} – 1.5			V
		R_L = 10 kΩ		25°C				
		V_{CC} = MAX	R_L = 2 kΩ	Full range	26			
			R_L ≥ 10 kΩ	Full range	27	28		
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ		Full range		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ		25°C	25	100		V/mV
				Full range	15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C	65	80		dB
k_{SVR}	Supply-voltage rejection ratio (ΔV_{CC} /ΔVIO)			25°C	65	100		dB
V_{O1}/ V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	Source	25°C	–20	–30	–60	mA
				Full range	–10			
		V_{CC} = 15 V, V_{ID} = –1 V, V_O = 15 V	Sink	25°C	10	20		
				Full range	5			
		V_{ID} = –1 V, V_O = 200 mV		25°C	12	30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, V_O = 0, GND at –5 V		25°C		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, no load		Full range		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, no load		Full range		1.4	3	

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX V_{CC} for testing purposes is 30 V.
(2) Full range is 0°C to 70°C for LM324-MIL.
(3) All typical values are at T_A = 25°C

6.6 Operating Conditions

V_{CC} = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 30 pF, V_I = ±10 V (see Figure 7)	0.5	V/μs
B_1	Unity-gain bandwidth	R_L = 1 MΩ, C_L = 20 pF (see Figure 7)	1.2	MHz
V_n	Equivalent input noise voltage	R_S = 100 Ω, V_I = 0 V, f = 1 kHz (see Figure 8)	35	nV/√Hz

Copyright © 2017, Texas Instruments Incorporated

6.7 Typical Characteristics

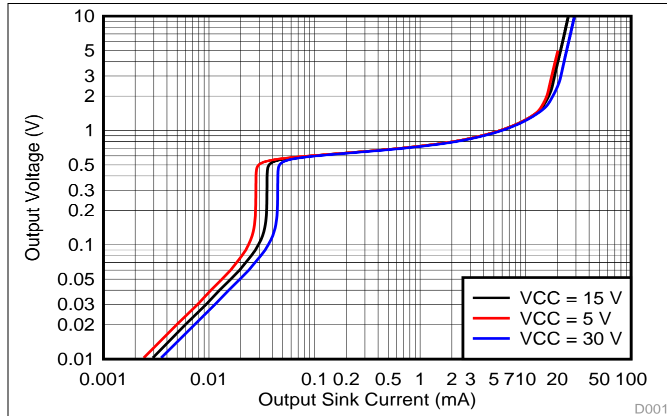


Figure 1. Output Sinking Characteristics

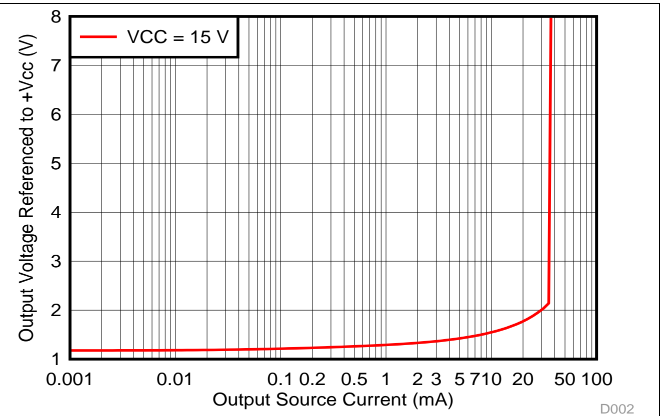


Figure 2. Output Sourcing Characteristics

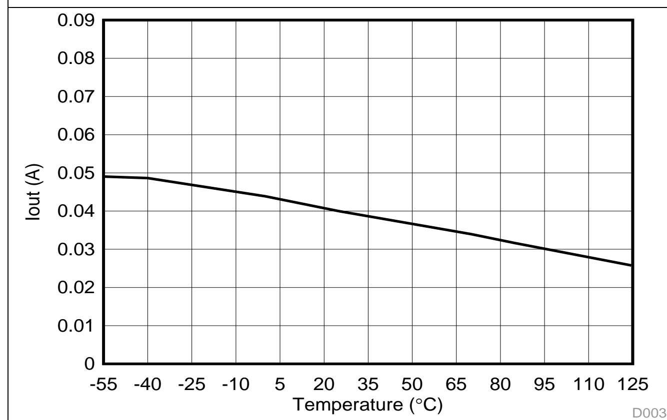


Figure 3. Source Current Limiting

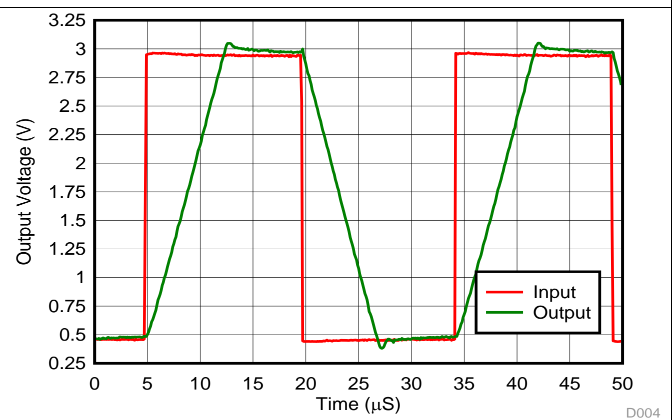


Figure 4. Voltage Follower Large Signal Response (50 pF)

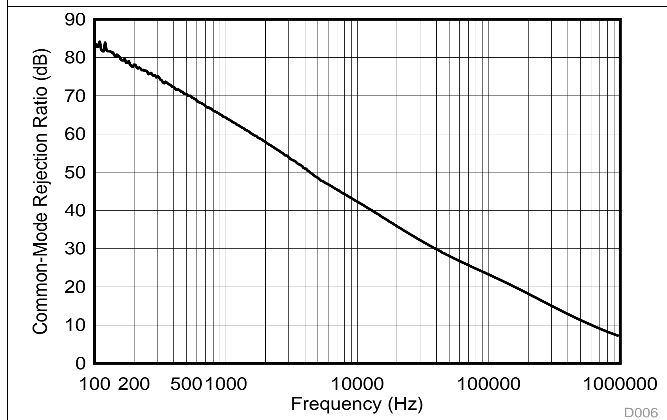


Figure 5. Common-Mode Rejection Ratio

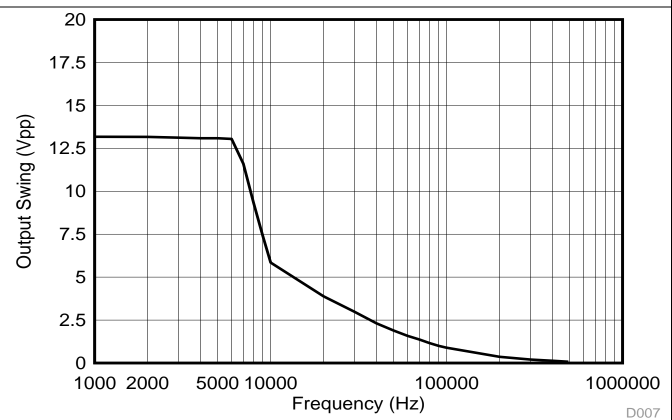


Figure 6. Maximum Output Swing vs. Frequency (VCC = 15 V)

Copyright © 2017, Texas Instruments Incorporated

7 Parameter Measurement Information

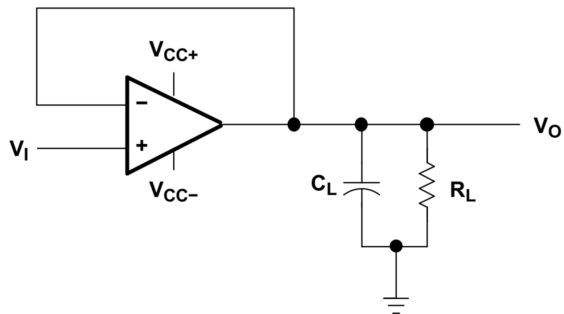


Figure 7. Unity-Gain Amplifier

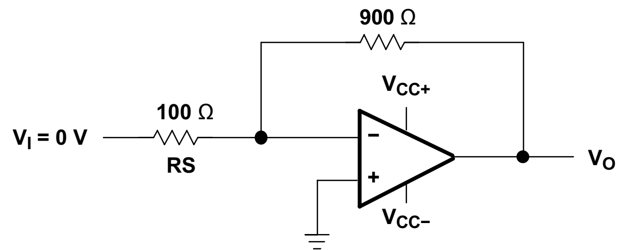


Figure 8. Noise-Test Circuit

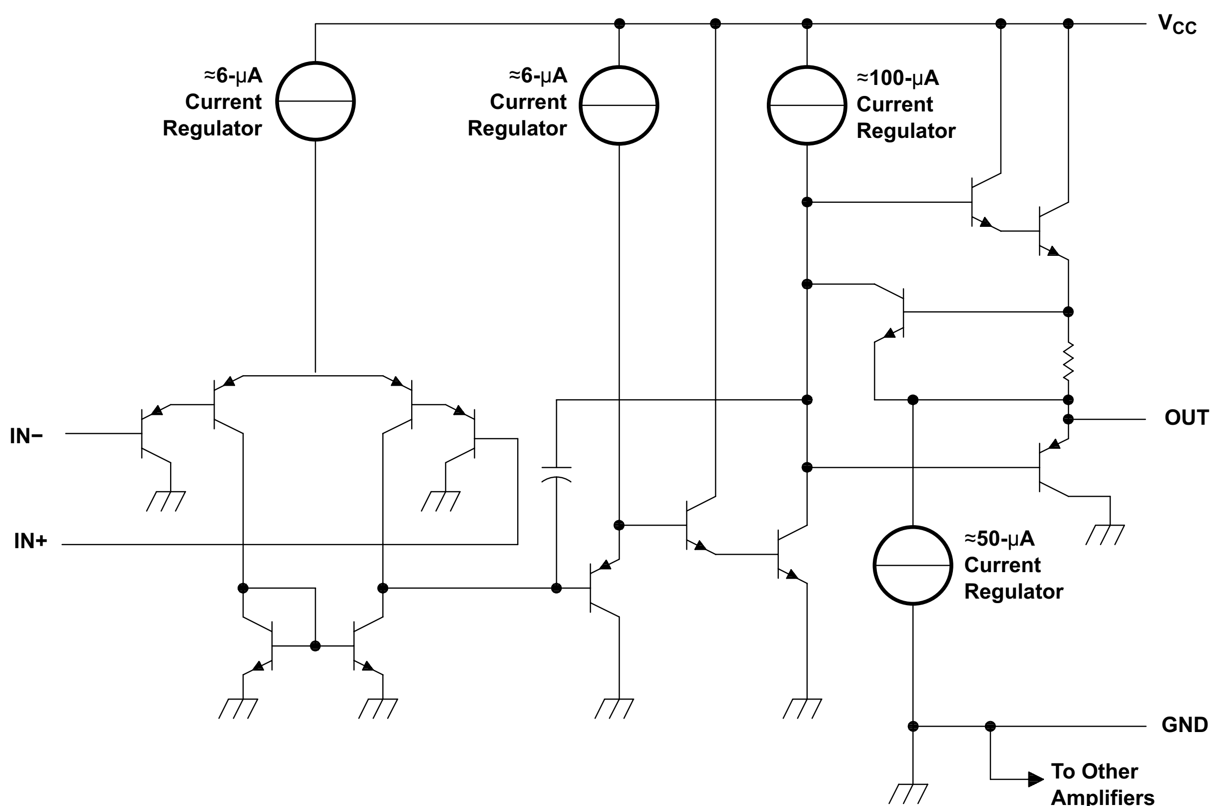
8 Detailed Description

8.1 Overview

The device consists of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is 3 V to 32 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, DC amplification blocks, and all the conventional operational-amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM324-MIL device can be operated directly from the standard 5-V supply that is used in digital systems and provides the required interface electronics, without requiring additional ±15-V supplies.

8.2 Functional Block Diagram



COMPONENT COUNT (total device)	
Epi-FET	1
Transistors	95
Diodes	4
Resistors	11
Capacitors	4

Copyright © 2017, Texas Instruments Incorporated

8.3 Feature Description

8.3.1 Unity-Gain Bandwidth

Gain bandwidth product is found by multiplying the measured bandwidth of an amplifier by the gain at which that bandwidth was measured. These devices have a high gain bandwidth of 1.2 MHz.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/μs slew rate.

8.3.3 Input Common Mode Range

The valid common mode range is from device ground to V_{CC} – 1.5 V (V_{CC} – 2 V across temperature). Inputs may exceed V_{CC} up to the maximum V_{CC} without device damage. At least one input must be in the valid input common mode range for output to be correct phase. If both inputs exceed valid range then output phase is undefined. If either input is less than –0.3 V then input current should be limited to 1 mA and output phase is undefined.

8.4 Device Functional Modes

The device is powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

Copyright © 2017, Texas Instruments Incorporated

9 Application and Implementation

NOTE

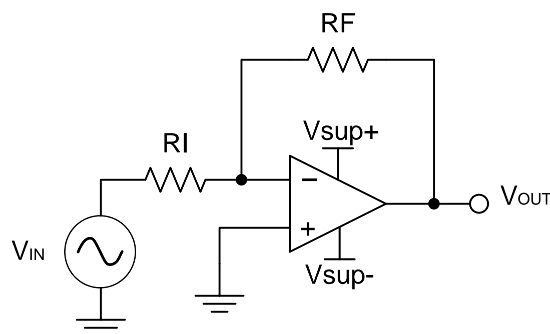
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM324-MIL operational amplifier is useful in a wide range of signal conditioning applications. Inputs can be powered before VCC for flexibility in multiple supply circuits.

9.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.



Copyright © 2016, Texas Instruments Incorporated

Figure 9. Application Schematic

9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{VOUT}{VIN} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kilohm range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_V = -\frac{RF}{RI} \tag{3}$$

Copyright © 2017, Texas Instruments Incorporated

Typical Application (continued)

9.2.3 Application Curve

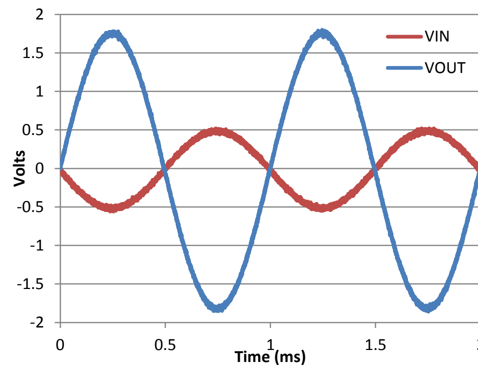


Figure 10. Input and Output Voltages of the Inverting Amplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 32 V for a single supply, or outside the range of ±16 V for a dual supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

Copyright © 2017, Texas Instruments Incorporated

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

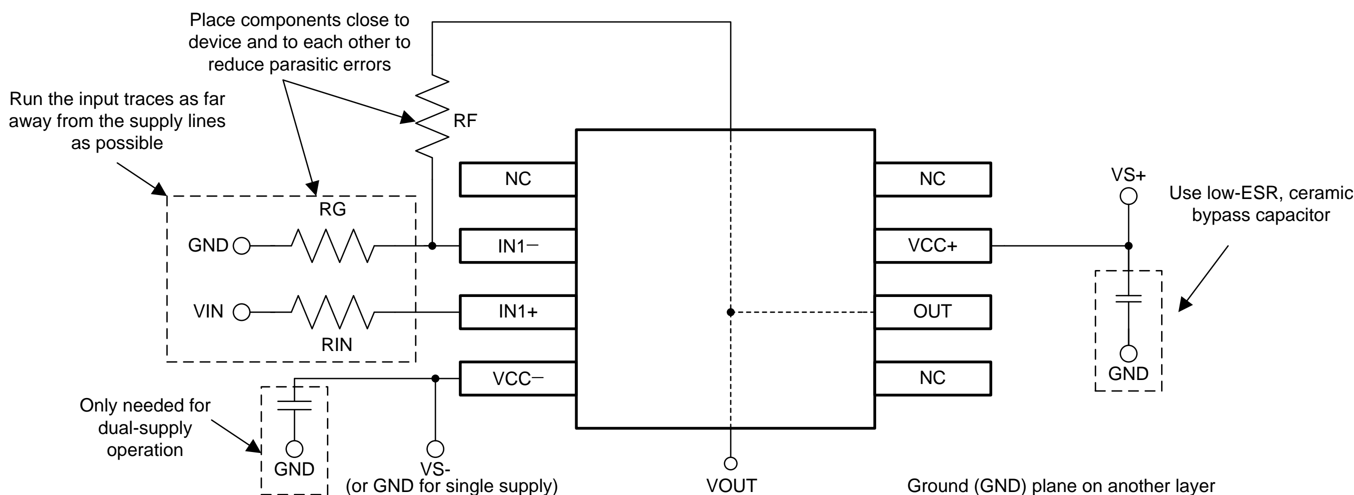


Figure 11. Operational Amplifier Board Layout for Noninverting Configuration

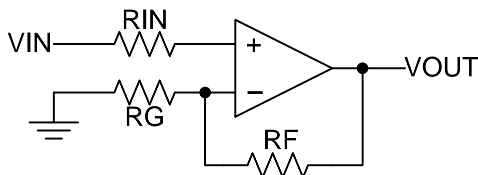


Figure 12. Operational Amplifier Schematic for Noninverting Configuration

Copyright © 2017, Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Circuit Board Layout Techniques, SLOA089

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

Copyright © 2017, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM324 MWA	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

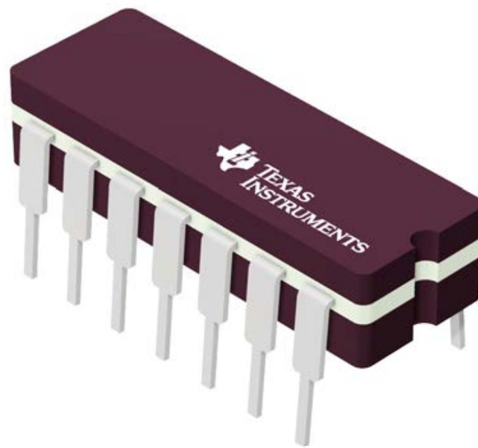
[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PIN 1 ID
(OPTIONAL)

A

4X .005 MIN
[0.13]

.015-.060 TYP
[0.38-1.52]

1

14

12X .100
[2.54]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⌖ .010 [0.25] C A B

.754-.785
[19.15-19.94]

7

8

B

.245-.283
[6.22-7.19]

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

SEATING PLANE

C

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015
[0.38]
GAGE PLANE

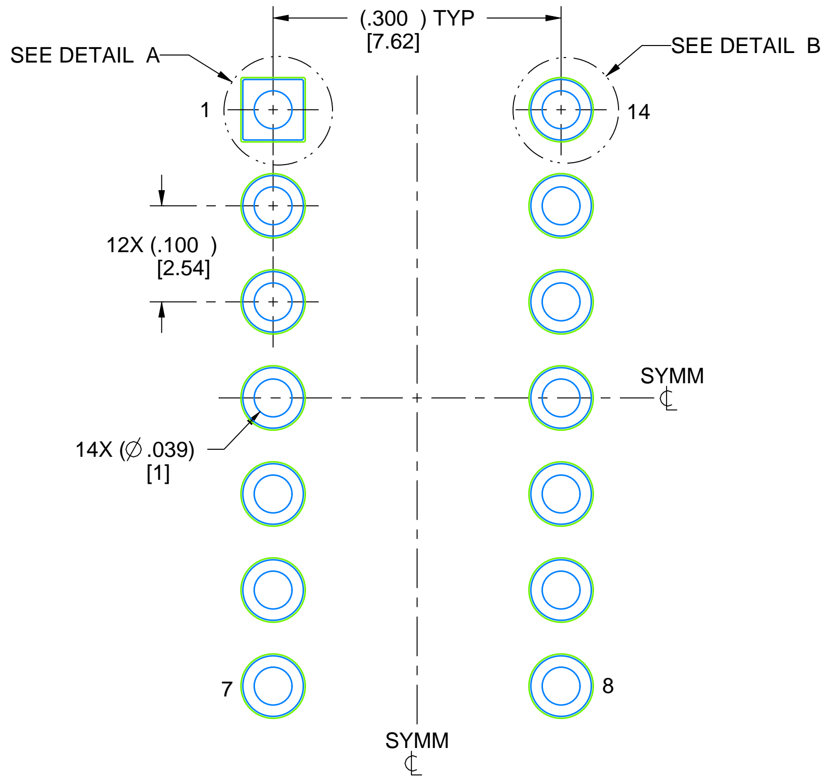
0°-15°
TYP

14X .008-.014
[0.2-0.36]

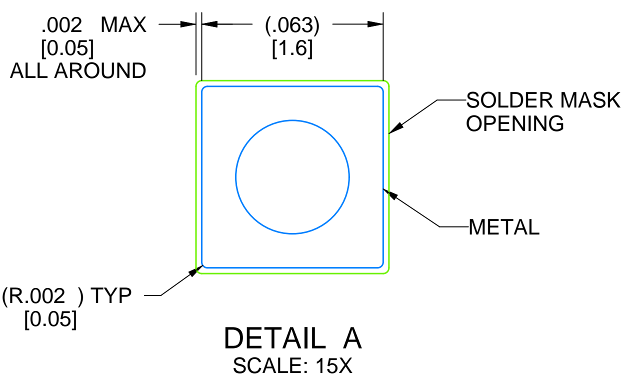
4214771/A 05/2017

NOTES:

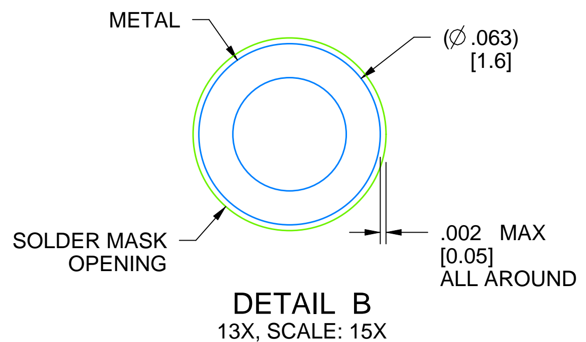
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X

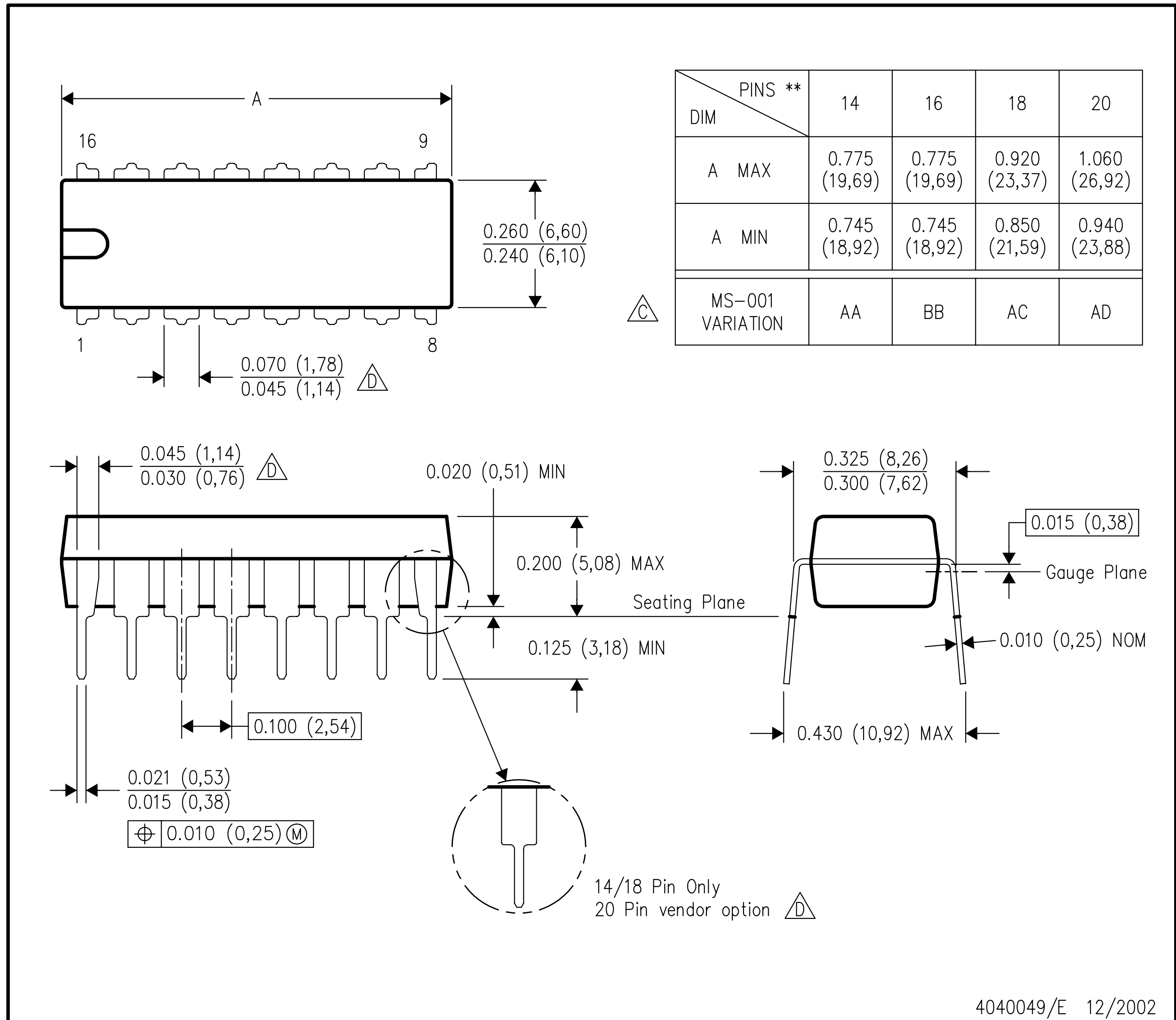


DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

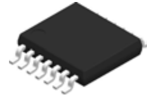
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

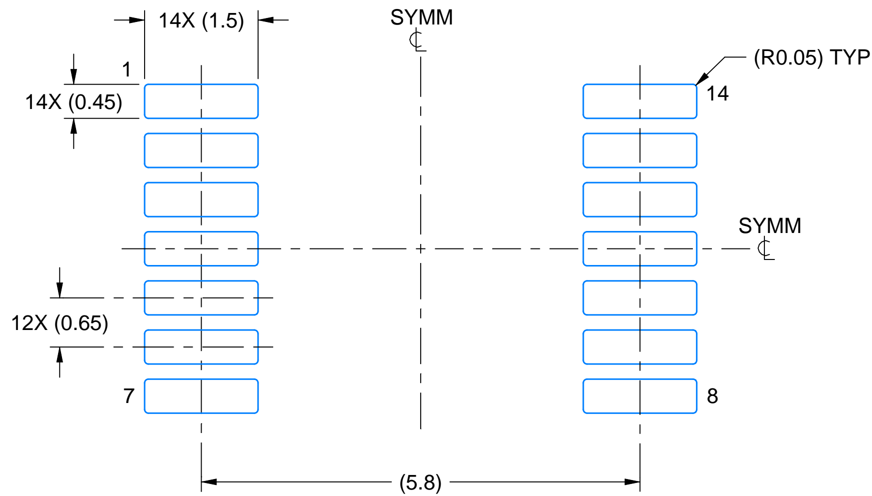
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.



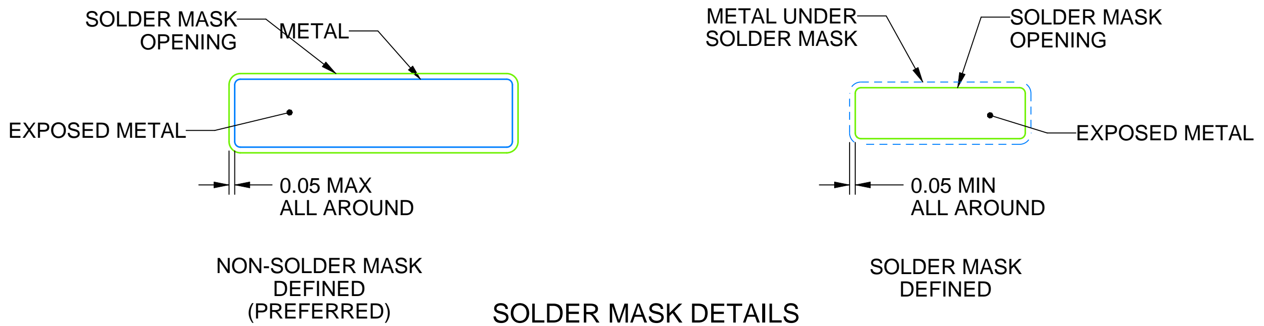
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

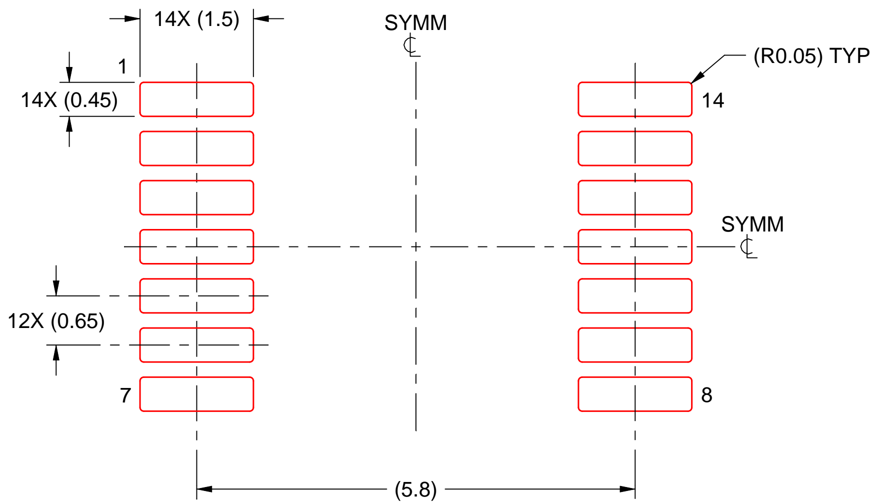
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

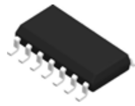


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

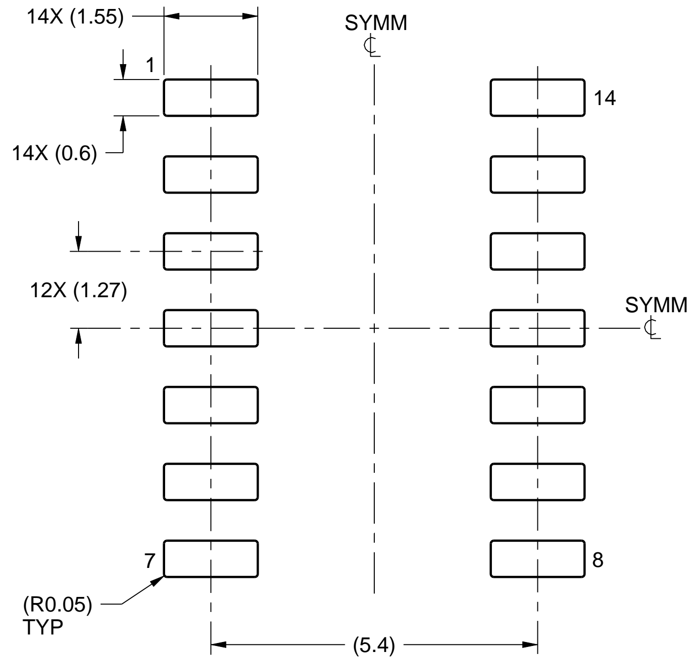
D0014A

SOIC - 1.75 mm max height

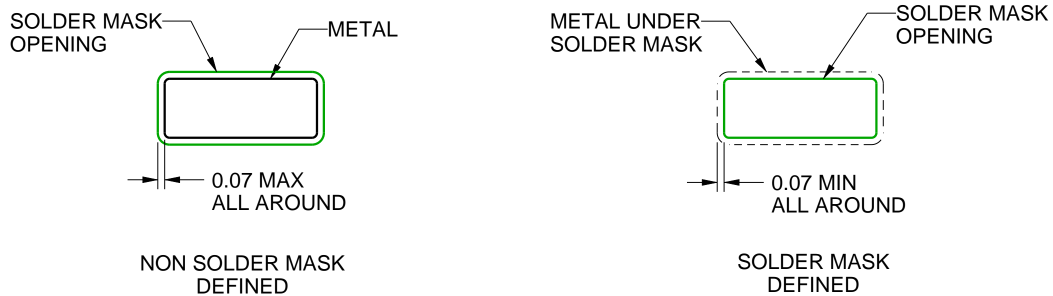
SMALL OUTLINE INTEGRATED CIRCUIT

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK DEFINED

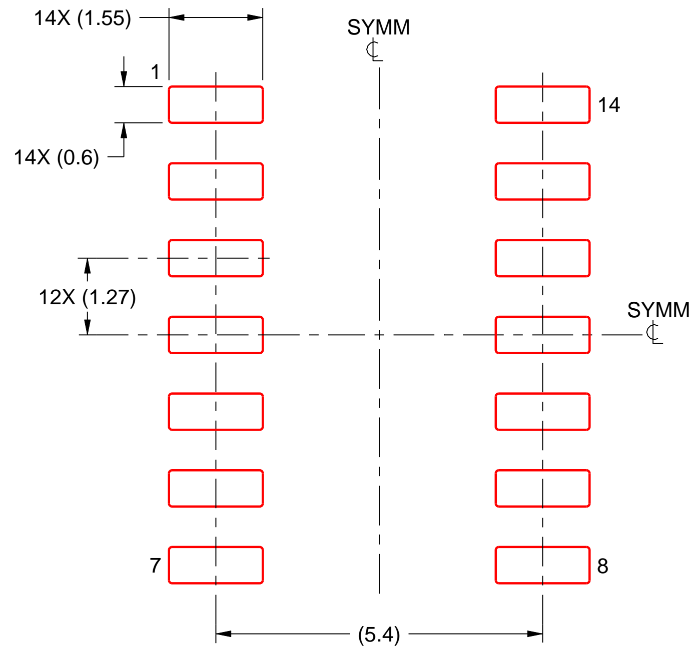
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

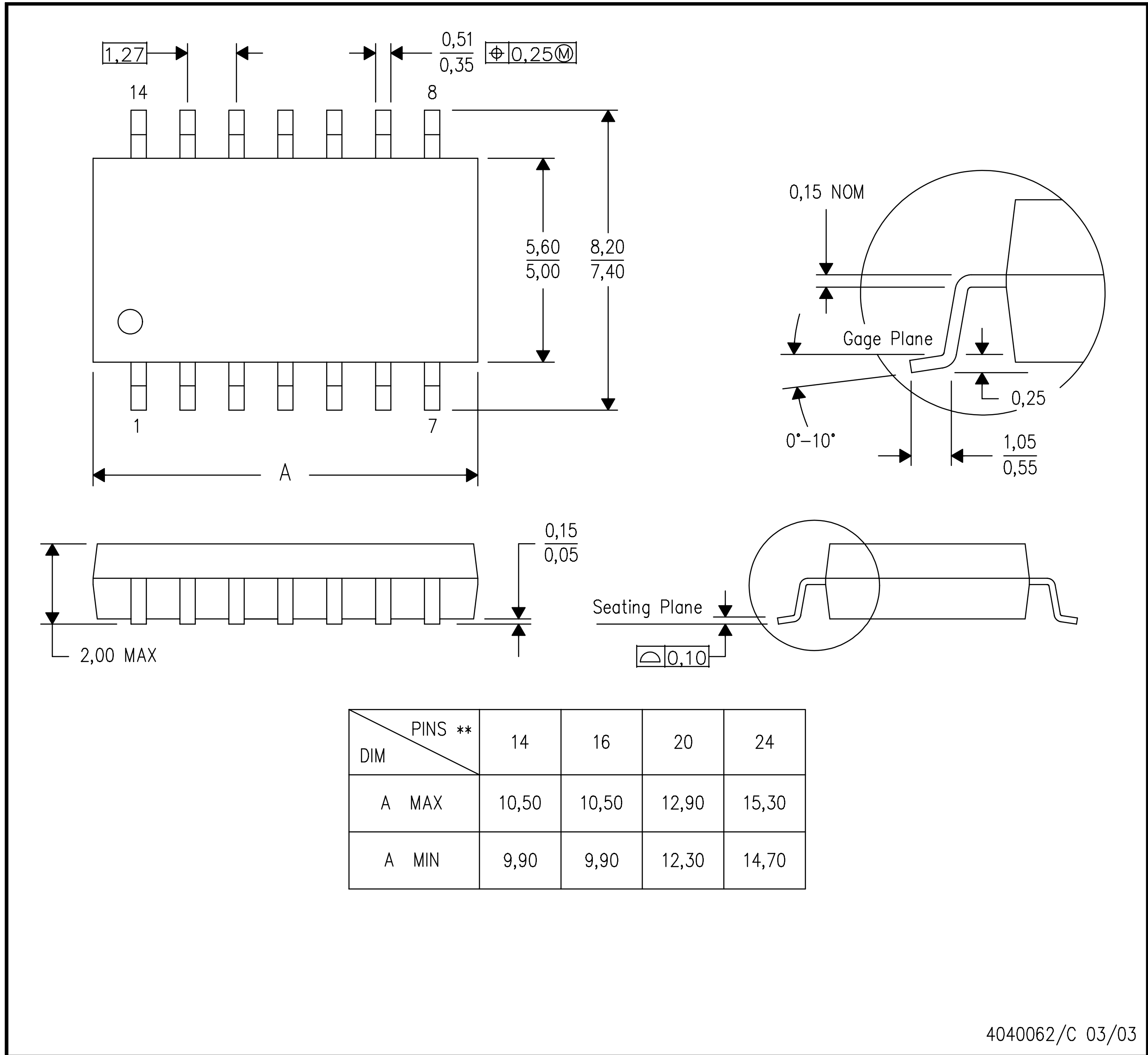
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

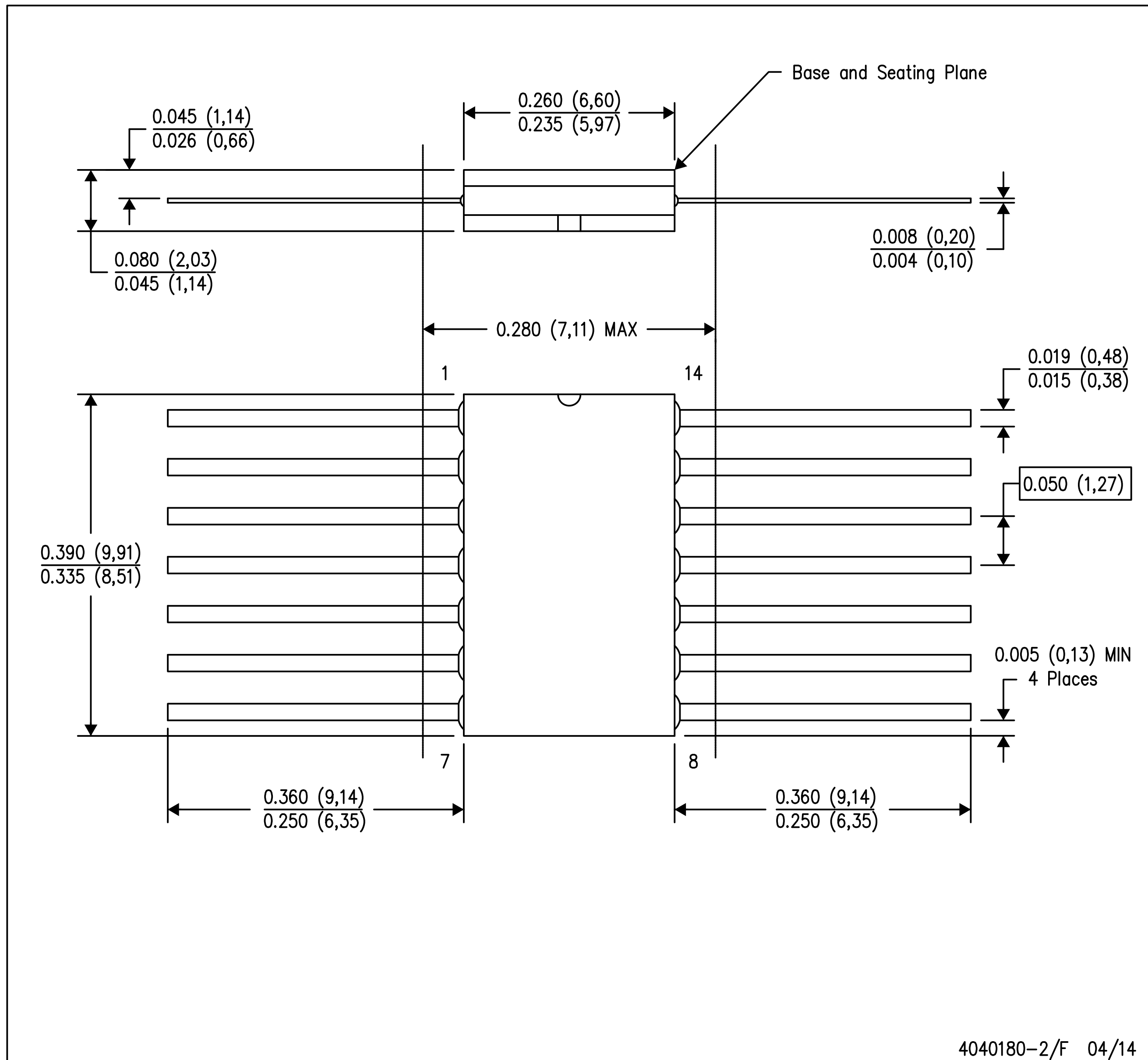
14-PINS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

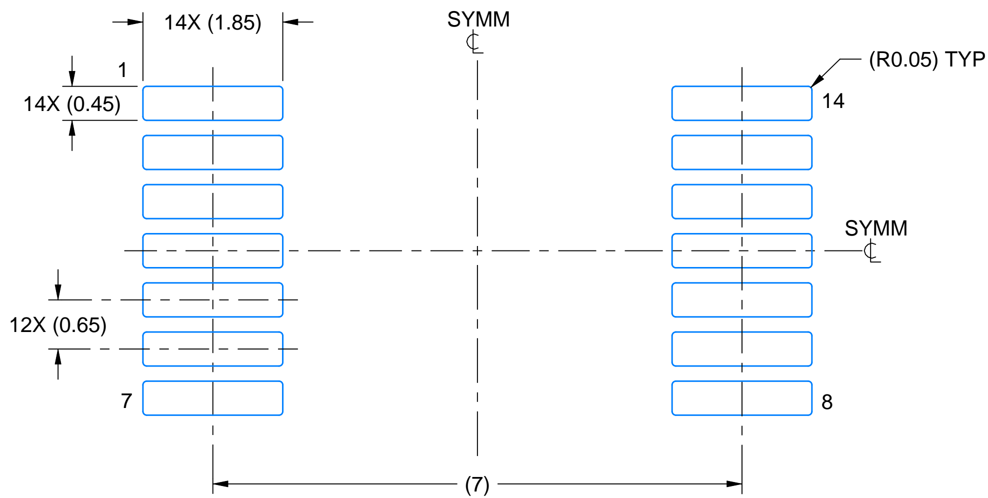
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



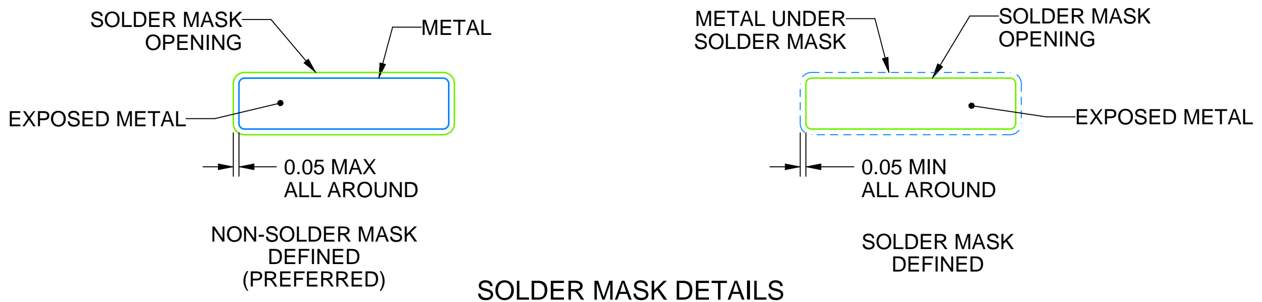
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1–F14

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

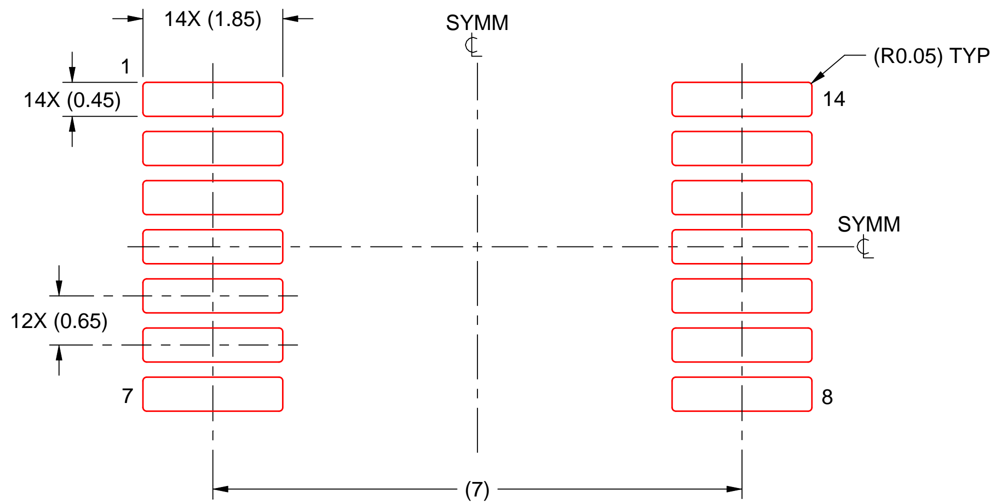


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024, Texas Instruments Incorporated