# Dynamic Headroom Controller with Thermal Control Interface and Individual Channel Dimming Control

**Check for Samples: LM3463**

## FEATURES

- **Dynamic Headroom Control Output to Maximize Efficiency**
- **6 Channels Current Regulated LED Driver**
- **High Precision Analog Dimming Control Interface**
- **4 Individual PWM Dimming Control Input**
- **Dimming Control via Digital Data Bus**
- **Built-In Maximum MOSFET Power Limiting Mechanism**
- **Allows Cascade Operation to Extend the Output Channels**
- **Fault Indicator Output**
- **Thermal Shutdown**
- **UVLO With Hysteresis**
- **48L WQFN Package**

## KEY SPECIFICATIONS

- **Wide supply voltage range (12V-95V)**
- **Thermal fold-back dimming control**
- **DHC regulates the lowest MOSFET drain voltage to 1V**

## APPLICATIONS

- **Streetlights**
- **Solid State Lighting Solutions**

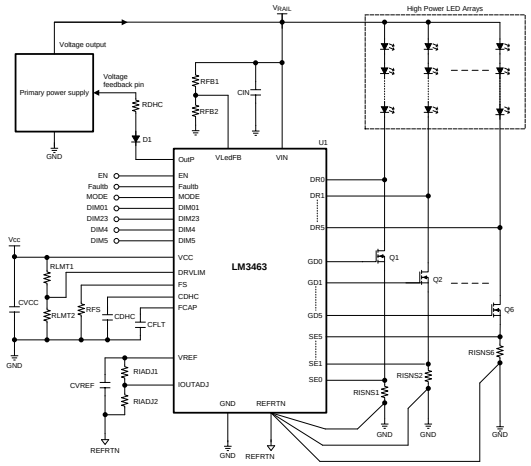
## DESCRIPTION

The LM3463 is a six channel linear LED driver with Dynamic Headroom Control (DHC) interface that is specialized for high power LED lighting applications. The variation of the output current of every output channel in the temperature range of -40°C to 125°C is well controlled to less than ±1%. The output current of every channel is accurately matched to each other with less than ± 1% difference as well.

By interfacing the LM3463 to the output voltage feedback node of a switching power supply via the DHC interface, the system efficiency is optimized automatically. The dynamic headroom control circuit in the LM3463 minimizes power dissipation on the external MOSFETs by adjusting the output voltage of the primary switching power supply according to the changing forward voltage of the LEDs. Comprising the advantages of linear and switching converters, the LM3463 delivers accurately regulated current to LEDs while maximizing the system efficiency.

The dimming control interface of the LM3463 accepts both analog and PWM dimming control signals. The analog dimming control input controls the current of all LEDs while the PWM control inputs control the dimming duty of output channels individually.

### Typical Application

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## DESCRIPTION CONTINUED

The LM3463 provides a sophisticated protection mechanism that secures high reliability and stability of the lighting system. The protection features include $V_{IN}$ Under-Voltage–Lock-Out (UVLO), thermal shut-down, LED short / open circuit protection and MOSFET drain voltage limiting. The LED short circuit protection protects both the LED and MOSFETS by limiting the power dissipation on the MOSFETS.

### Connection Diagram

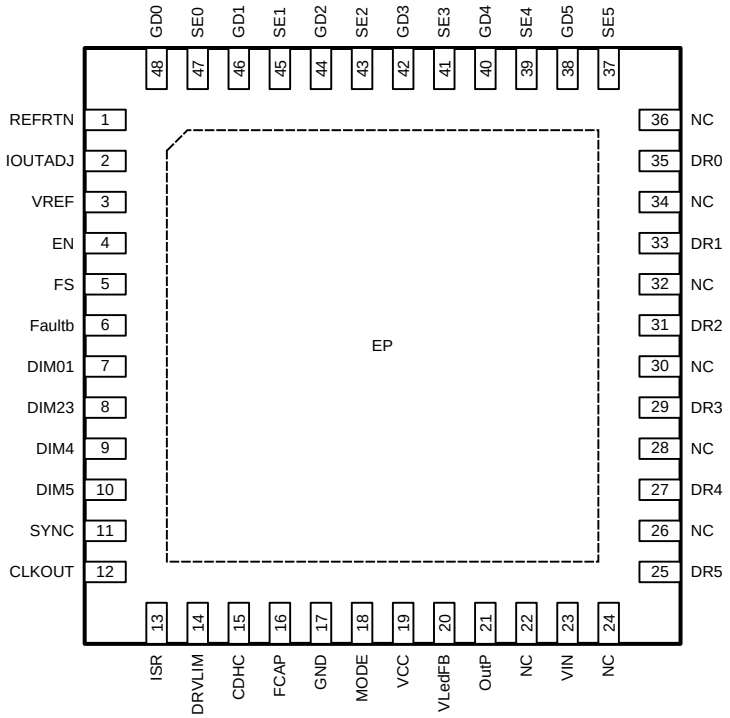



**Figure 1. TOP VIEW**
**48-Lead Plastic WQFN**
**Package Number RHS**

### PIN DESCRIPTIONS

| Pin | Name | Description | Application information |
|---|---|---|---|
| 1 | REFRTN | 0V reference for small signal return paths | This pin should connect to the end points of current sensing resistors with individual connections to ensure channel to channel current accuracy. |
| 2 | IOUTADJ | Output current level adjust pin | The current of all output channels (defined by $R_{ISNSn}$) reduces according to the voltage at this pin. This pin should connect to the VREF pin when output current reduction is not required. |
| 3 | VREF | Precision reference voltage output | This pin is the output of a precision reference voltage regulator. This pin must be bypassed through a ceramic capacitor to REFRTN. |
| 4 | EN | Enable input | Device enable pin with internal pull-up |
| | | | Enable: $V_{EN}$ = Floating |
| | | | Disable: $V_{EN}$ = GND |
| 5 | FS | Internal oscillator control or external clock input pin | Frequency setting pin. Connect a resistor across this pin to GND to set the internal oscillator frequency. |
| | | | The internal clock frequency can be defined by forcing an external clock signal to this pin. |
| 6 | Faultb | Fault indicator output | Fault indicator output. This pin is an open-drain output and is pulled low when an open circuit of LED string is identified. |

## PIN DESCRIPTIONS (continued)

| Pin | Name | Description | Application information |
|---|---|---|---|
| 7 | DIM01 | Multi-function input pin. | The function of this pin differs depending on the selected operation mode that sets by the MODE pin. |
| | | Channel 0/1 PWM dimming control | Direct PWM mode: Apply a bi-level PWM signal (TTL logic high and low) to this pin to enable/disable ch0 and ch1. Apply logic high to this pin to enable channel 0 and 1. |
| | | Serial data input | In serial interface mode, this pin is configured as the serial data input. |
| | | DC voltage dimming control | In DC interface mode, the voltage on this pin is converted into PWM dimming duty for channel 0 and 1. |
| 8 | DIM23 | Multi-function input pin. | The function of this pin differs depending on the selected operation mode that sets by the MODE pin. |
| | | Channel 2/3 PWM dimming control | Direct PWM mode: apply bi-level PWM signal (TTL logic high and low) to this pin to enable/disable ch2 and ch3. Apply a logic high to this pin to enable both channel 2 and 3. |
| | | Serial clock input | In serial interface mode, this pin is configured as the serial clock signal input. |
| | | DC voltage dimming control | In DC interface mode, the voltage on this pin is converted into PWM dimming duty for channel 2 and 3. |
| 9 | DIM4 | Multi-function input pin. | The function of this pin differs depending on the selected operation mode that sets by the MODE pin. |
| | | Channel 4 dimming control | Direct PWM mode: apply bi-level PWM signal to this pin to enable/disable channel 4. Apply logic high to this pin to enable channel 4. |
| | | Load data control pin | In serial interface mode, this pin is configured as load pulse input, pulling this pin low will latch the shifted-in data into internal register of the LM3463. This pin is pulled low if the requested load operation is not completed. User should check the status of this pin before writing data into the LM3463 through this pin. |
| | | DC voltage dimming control | In DC interface mode, the voltage on this pin is converted into PWM dimming duty for channel 4. |
| 10 | DIM5 | Multi-function input pin. | The function of this pin differs depending on the selected operation mode that sets by the MODE pin. |
| | | Channel 5 dimming control | Direct PWM mode: Apply a bi-level PWM signal (TTL logic high and low) to this pin to enable/disable channel 5. Apply a logic high to this pin to enable channel 5. |
| | | Serial operation mode | This pin should connect to GND when serial operation mode is selected. |
| | | DC voltage dimming control | In DC interface mode, the voltage on this pin is converted into PWM dimming duty for channel 5. |
| 11 | SYNC | Serial data output for cascade operation | Serial control signal output pin for cascade operation. This signal synchronizes with the rising edge of the CLKOUT signal and carries information to the slave devices to turn on LEDs. |
| | | Sync. pulse input in direct PWM mode | This is a synchronization signal input pin for the slave device to perform LED pretest upon system startup. |
| 12 | CLKOUT | Dimming clock output for cascade operation / Sync pulse output for Direct PWM mode | Dimming clock output for cascade operation. The frequency at this pin equal to 1/2 of the internal clock or externally applied clock frequency. |
| 13 | ISR | Start up current control pin | Connect a resistor from this pin to GND to set the additional bias current to the $C_{DHC}$ upon system startup. |
| 14 | DRVLIM | MOSFET power limit setting input | The voltage on this pin defines the threshold of the drain voltage of the external MOSFETs ($V_{DRn}$) to begin output current reduction. |
| | | | As the $V_{DRn}$ exceeds $V_{DRVLIM}$, the LED driving current reduces according to the increasing of $V_{DRn}$ at certain fixed rate. This function prevents the MOSFET from over-heating. The maximum power dissipation is limited to $V_{DRVLIM} * I_{LED}$(per ch.). |
| 15 | CDHC | Dynamic headroom control time constant capacitor | Connect a capacitor ($C_{DHC}$) from this pin to ground to program the DHC loop response. |
| 16 | FCAP | Fault de-bounce capacitor | Connect a capacitor, $C_{FLT}$ from this pin to ground to program the fault de-bounce time. |
| 17 | GND | System ground | This pin should connect to the system ground |

## PIN DESCRIPTIONS (continued)

| Pin | Name | Description | Application information |
|---|---|---|---|
| 18 | MODE | Mode select input pin | Operation mode selection input pin. Bias this pin externally to set the LM3463 in different operation mode. |
| | | | Direct PWM mode: $V_{MODE}$ = GND |
| | | | Serial interface mode: $V_{MODE}$ = No Connection |
| | | | DC interface mode: $V_{MODE}$ = VCC |
| 19 | VCC | Internal regulator output | Output terminal of the internal voltage regulator. This pin should be bypassed to GND through a 1uf ceramic capacitor. |
| 20 | VLedFB | Rail voltage detection input pin | This pin detects the output voltage of the primary power supply ($V_{RAIL}$). LEDs will be turned on when the voltage at this pin reaches 2.5V. |
| | | | Connect this pin to VCC to set a device as a slave. |
| 21 | OutP | DHC output Driver | This pin is an open drain output (current sink) which should connect to the output voltage feedback node of the primary power supply through a resistor and a diode to realize rail voltage adjustment. |
| 22 | NC | | No connection |
| 23 | VIN | System supply | Supply voltage input pin. This pin should be bypassed to GND using a 1uF ceramic capacitor. |
| 24 | NC | | No connection |
| 25 | DR5 | Channel 5 drain voltage feedback input to facilitate DHC | Connect to the junction of the drain terminal of the external MOSFET and the cathode of the LED string. This pin is connected to the internal comparator to facilitate DHC. |
| 26 | NC | | No connection |
| 27 | DR4 | Channel 4 drain voltage feedback input to facilitate DHC | Connect to the junction of the drain terminal of the external MOSFET and the cathode of the LED string. This pin is connected to the internal comparator to facilitate DHC. |
| 28 | NC | | No connection |
| 29 | DR3 | Channel 3 drain voltage feedback input to facilitate DHC | Connect to the junction of the drain terminal of the external MOSFET and the cathode of the LED string. This pin is connected to the internal comparator to facilitate DHC. |
| 30 | NC | | No connection |
| 31 | DR2 | Channel 2 drain voltage feedback input to facilitate DHC | Connect to the junction of the drain terminal of the external MOSFET and the cathode of the LED string. This pin is connected to the internal comparator to facilitate DHC. |
| 32 | NC | | No connection |
| 33 | DR1 | Channel 1 drain voltage feedback input to facilitate DHC | Connect to the junction of the drain terminal of the external MOSFET and the cathode of the LED string. This pin is connected to the internal comparator to facilitate DHC. |
| 34 | NC | | No connection |
| 35 | DR0 | Channel 0 drain voltage feedback input to facilitate DHC | Connect to the junction of the drain terminal of the external MOSFET and the cathode of the LED string. Voltage on this pin is being fed to the internal comparator to facilitate DHC. |
| 36 | NC | | No connection |
| 37 | SE5 | Channel 5 LED driver sense input pin | Connect to the junction of the source terminal of the external MOSFET and the sense resistor to facilitate current regulation for channel 5. |
| 38 | GD5 | channel 5 gate drive output pin | Gate driver output. Connect to the gate terminal of the external MOSFET. |
| 39 | SE4 | Channel 4 LED driver sense input pin | Connect to the junction of the source terminal of the external MOSFET and the sense resistor to facilitate current regulation for channel 4. |
| 40 | GD4 | channel 4 gate drive output pin | Gate driver output. Connect to the gate terminal of the external MOSFET. |
| 41 | SE3 | Channel 3 LED driver sense input pin | Connect to the junction of the source terminal of the external MOSFET and the sense resistor to facilitate current regulation for channel 3. |
| 42 | GD3 | channel 3 gate drive output pin | Gate driver output. Connect to the gate terminal of the external MOSFET. |
| 43 | SE2 | Channel 2 LED driver sense input pin | Connect to the junction of the source terminal of the external MOSFET and the sense resistor to facilitate current regulation for channel 2. |
| 44 | GD2 | channel 2 gate drive output pin | Gate driver output. Connect to the gate terminal of the external MOSFET. |
| 45 | SE1 | Channel 1 LED driver sense input pin | Connect to the junction of the source terminal of the external MOSFET and the sense resistor to facilitate current regulation for channel 1. |

## PIN DESCRIPTIONS (continued)

| Pin | Name | Description | Application information |
|---|---|---|---|
| 46 | GD1 | channel 1 gate drive output pin | Gate driver output. Connect to the gate terminal of the external MOSFET. |
| 47 | SE0 | Channel 0 LED driver sense input pin | Connect to the junction of the source terminal of the external MOSFET and the sense resistor to facilitate current regulation for channel 0. |
| 48 | GD0 | channel 0 gate drive output pin | Gate driver output. Connect to the gate terminal of the external MOSFET. |
| | EP | Thermal Pad | Connect to the GND pin. The EP has no internal connection to ground and must connect to the GND pin externally. Place 9 vias from EP to copper ground plane. |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)

| | |
|---|---|
| VIN to GND | -0.3V to 100V |
| DR0, DR1, DR2, DR3, DR4, DR5 to GND | -0.3V to 100V |
| EN | -0.3V to 5.5V |
| DRVLIM | -0.3V to 6V |
| Faultb | -0.3V to 20V |
| All other pins | -0.3V to 7V |
| ESD Rating, Human Body Model(3) | ±2 kV |
| Storage Temperature | −65°C to +150°C |
| Junction Temperature ($T_J$) | −40°C to +125°C |

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114-C.

## Operating Ratings

| | |
|---|---|
| Supply Voltage Range (VIN) | 12V to 95V |
| Junction Temperature Range ($T_J$) | −40°C to + 125°C |
| Thermal Resistance ($\theta_{JA}$) | 24°C/W |
| Thermal Resistance ($\theta_{JC}$)(1) | 2.5°C/W |

(1) $\theta_{JC}$ measurements are performed in general accordance with Mil-Std 883B, Method 1012.1 and utilize the copper heat sink technique. Copper Heat Sink @ 60°C.

## Electrical Characteristics

Specification with standard type are for $T_A = T_J = +25°C$ only; limits in **boldface** type apply over the full Operating Junction Temperature ($T_J$) range. Minimum and Maximum are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = +25°C$, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{IN} = 48V$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $I_{IN}$ | $V_{IN}$ Quiescent Current | $V_{EN}$ pin floating | | 9.75 | **15** | mA |
| $I_{SD}$ | $V_{IN}$ Shut-Down Current | $V_{EN}$ = 0V | | 550 | **800** | µA |
| **VIN UVLO** | | | | | | |
| $V_{IN-UVLO}$ | $V_{IN}$ Turn-on Threshold | | | 7.4 | **10** | V |
| | $V_{IN}$ Turn-off Threshold | | **4.5** | 7.1 | | V |
| | $V_{IN}$ UVLO Hysteresis | | | 300 | | mV |
| **VCC Regulator** | | | | | | |
| $V_{CC}$ | $V_{CC}$ Regulated Voltage | $C_{VCC}$ = 1 µF, $I_{VCC}$=1mA | **6.240** | 6.475 | **6.760** | V |
| | | $I_{CC}$ = 10 mA | **6.230** | 6.462 | **6.741** | V |
| $I_{VCC-LIM}$ | $V_{CC}$ Current Limit | $V_{CC}$ = 0V | | 28 | **45** | mA |
| $V_{CC-UVLO}$ | $V_{CC}$ Turn-on Threshold | | | 4.5 | **4.7** | V |
| | $V_{CC}$ Turn-off Threshold | | **3.75** | 4.20 | | V |
| | $V_{CC}$ UVLO hysteresis | $V_{CC}$ Decreasing | | 300 | | mV |
| **Internal Reference Voltage Regulator** | | | | | | |
| $V_{VREF}$ | Reference Voltage Regulator Output Voltage | $C_{VREF}$ = 0.47 µF, No Load | **2.453** | 2.499 | **2.564** | V |
| | | $I_{VREF}$ = 2mA | **2.443** | 2.496 | **2.545** | V |
| $I_{VREF-SC}$ | VREF Pin Short-Circuit Current | $V_{VREF} = V_{REFRTN}$ | **7.0** | 8.2 | **10.5** | mA |

## Electrical Characteristics (continued)

Specification with standard type are for $T_A = T_J = +25°C$ only; limits in **boldface** type apply over the full Operating Junction Temperature ($T_J$) range. Minimum and Maximum are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = +25°C$, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{IN} = 48V$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Dimming Control Interfaces** | | | | | | |
| **Analog Mode** | | | | | | |
| $V_{DIMn-MAX}$ | DIMn Voltage at 100% Output Duty Cycle | MODE = VCC | | 5.65 | | V |
| $V_{DIMn-MIN}$ | DIMn Voltage at 0% Output Duty Cycle | MODE = VCC | | 807 | | mV |
| $V_{DIMn-001H}$ | DIMn Voltage at data code = 001h | MODE = VCC | | 826 | | mV |
| **PWM Mode** | | | | | | |
| $V_{DIM-LED-ON}$ | DIMn Voltage Threshold at LED ON | MODE = GND | | 1.50 | **1.75** | V |
| $V_{DIM-LED-OFF}$ | DIMn Voltage Threshold at LED OFF | | **1.1** | 1.4 | | V |
| $V_{DIM-LED-HYS}$ | DIMn Voltage Hysteresis at LED ON to OFF | | | 100 | | mV |
| **System Clock Generator** | | | | | | |
| $V_{FS}$ | FS Pin Voltage | FS Pin = Open | **1.173** | 1.235 | **1.297** | V |
| $I_{FS-SC}$ | FS Pin Short-Circuit Current | $V_{FS} = 0V$ | | 110 | **140** | µA |
| $f_{OSC}$ | System Clock Frequency | $R_{FS} = 14 kΩ$ | **0.90** | 1.00 | **1.15** | MHz |
| **Bus Interface Mode** | | | | | | |
| $V_{SCLK-HIGH (DIM23)}$ | SCLK (Serial CLK) Logic High Threshold | MODE = Hi-Z | | 1.50 | **1.75** | V |
| $V_{SCLK-LOW (DIM23)}$ | SCLK (Serial CLK) Logic Low Threshold | MODE = Hi-Z | **1.1** | 1.4 | | V |
| $V_{SCLK-HYS (DIM23)}$ | SCLK (Serial CLK) Hysteresis | MODE = Hi-Z | | 100 | | mV |
| $V_{SDA-HIGH (DIM01)}$ | SDA (Serial Data) Logic High Threshold | MODE = Hi-Z | | 1.50 | **1.75** | V |
| $V_{SDA-LOW (DIM01)}$ | SDA (Serial Data) Logic Low Threshold | MODE = Hi-Z | **1.1** | 1.4 | | V |
| $V_{SDA-HYS (DIM01)}$ | SDA (Serial Data) Hysteresis | MODE = Hi-Z | | 100 | | mV |
| **Dynamic headroom Control** | | | | | | |
| $V_{DRn-DHC-STDEAY}$ | The lowest VDRn when DHC is under steady state | Measure at DRn pin | | 0.95 | | V |
| $V_{VLedFB-TH}$ | VLedFB Voltage Threshold for Turning LEDs ON | $V_{VLedFB}$ Increasing | **2.325** | 2.500 | **2.625** | V |
| $V_{VLedFB-HYS}$ | VLedFB Voltage Hysteresis | $V_{VLedFB}$ decreasing | | 1.21 | | V |
| $V_{VLedFBEN-SLAVE}$ | VLedFB Pin Voltage Threshold for Slave Mode | Measure at VLedFB pin | **5.15** | 5.39 | **5.60** | V |
| $V_{OutP-MAX}$ | OutP Max. Output Voltage | $I_{OutP} = 1mA$ Current Sink $V_{CDHC} = 0.5V$ | **2.90** | 3.10 | **3.25** | V |
| $V_{OutP-MIN}$ | OutP Min. Output Voltage | $I_{OutP} = 1mA$ Current Sink $V_{CDHC} = 3.5V$ | **0.050** | 0.120 | **0.235** | V |
| $V_{ISR}$ | ISR Pin Voltage | $I_{ISR} = 1µA$ Current Sink to GND | **1.226** | 1.307 | **1.382** | V |
| | | $I_{ISR} = 10µA$ Current Sink to GND | **1.195** | 1.240 | **1.285** | V |
| | | $I_{ISR} = 100µA$ Current Sink to GND | **1.075** | 1.125 | **1.175** | V |
| $I_{CDHC-SOURCE}$ | CDHC Pin Max. Sourcing Current | Any $V_{DRn} < 0.9V$ | **15** | 26 | **35** | µA |
| $I_{CDHC-SINK}$ | CDHC Pin Max. Sinking Current | Any $V_{DRn} > 0.9V$ | **20** | 33 | **45** | µA |
| $R_{CDHC-SOURCE}$ | CDHC Pin Output Impedance | Sourcing current from CDHC pin | **1.20** | 1.70 | **2.25** | MΩ |
| $R_{CDHC-SINK}$ | CDHC Pin Output Impedance | Sinking current from CDHC pin | **0.7** | 1.1 | **1.4** | MΩ |
| $gm_{CDHC-OTA}$ | CDHC Pin OTA Transconductance | $V_{DRn} ≥ 0.9V$ | | 75 | | µmho |
| | | $V_{DRn} < 0.9V$ | | 17 | | µmho |

## Electrical Characteristics (continued)

Specification with standard type are for $T_A = T_J = +25°C$ only; limits in **boldface** type apply over the full Operating Junction Temperature ($T_J$) range. Minimum and Maximum are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = +25°C$, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{IN} = 48V$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **LED Current Regulator** | | | | | | |
| $V_{GDn-MAX}$ | GDn Gate Driver Maximum Output Voltage | $V_{SEn} = 0V$ | **5.30** | 5.75 | **6.20** | V |
| $I_{GDn-MAX}$ | GDn Gate Driver Short Circuit Current | $V_{GDn} = 0V$ | | 10 | **16** | mA |
| $I_{DRn-MAX}$ | DRn pin Maximum Input Current | $V_{DRn} = 80V$ | **35** | 50 | **65** | µA |
| $V_{SEn}$ | Output Current Sensing Reference Voltage w.r.t $V_{REFRTN}$ | $V_{IOUTADJ} = V_{VREF}$ | **190** | 200 | **210** | mV |
| | | $V_{IOUTADJ} = V_{VREF} / 2$ | **85** | 100 | **115** | mV |
| | | $V_{IOUTADJ} = V_{REFRTN}$ | **2.0** | 4.6 | **6.5** | mV |
| **Fault Detection and Handling** | | | | | | |
| $V_{SEn-LED-OPEN-FLT}$ | LED Open Fault Detection Voltage Threshold at SEn Pin | Measure at SEn pin | | 43 | | mV |
| $I_{SEn-LED-OPEN-FLT}$ | LED Open Fault Detection Current Threshold at SEn Pin | Measure at SEn pin | **15** | 22 | **30** | µA |
| $V_{DRn-LED-NORMAL}$ | LED Open Fault Detection Voltage Threshold at DRn Pin | Measure at DRn pin | | 330 | | mV |
| $I_{FCAP-CHG}$ | Fault Cap. Charging Current | Fault = True | **20** | 28 | **40** | µA |
| $V_{FCAP-FLT-TH}$ | FCAP Pin Fault Confirm Voltage Threshold | Measure at FCAP pin | **3.3** | 3.6 | **3.9** | V |
| $V_{FCAP-RST-TH}$ | FCAP Pin Fault Reset Voltage Threshold | Measure at FCAP pin | **85** | 157 | **230** | mV |
| **Device Enable** | | | | | | |
| $V_{EN-ENABLE}$ | EN Pin Voltage Threshold for Device Enable | | | 2.6 | **3.3** | V |
| $V_{EN-DISABLE}$ | EN Pin Voltage Threshold for Device Disable | | **1.9** | 2.5 | | V |
| $V_{EN-HYS}$ | Device Enable Hysteresis | | | 100 | | mV |
| **Thermal Protection** | | | | | | |
| $T_{SD}$ | Thermal shutdown temperature | $T_J$ Rising | | 165 | | °C |
| $T_{SD-HYS}$ | Thermal shutdown temperature hysteresis | $T_J$ Falling | | 20 | | °C |

## Typical Performance Characteristics

All curves taken at $V_{IN}$ = 48V with configuration in typical application for driving twelve power LEDs with six output channels active and 350 mA output current per channel. $T_A$ = 25°C, unless otherwise specified.

**$V_{SEn}$ vs Temperature, $V_{IOUTADJ}$=$V_{REF}$**

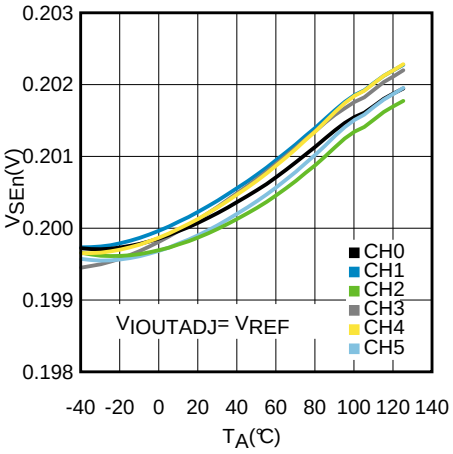



**Figure 2.**

**$V_{SEn}$ vs Temperature, $V_{IOUTADJ}$=0.5 $V_{REF}$**

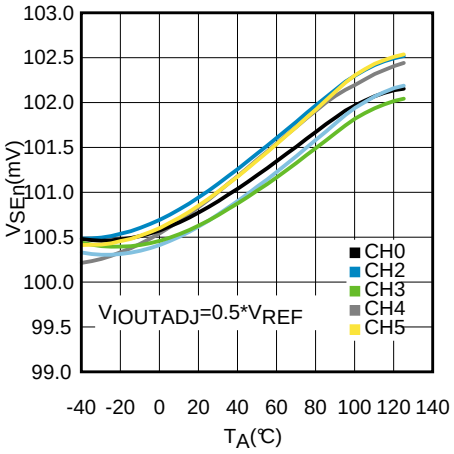



**Figure 3.**

**Variation of $V_{SEn}$ vs Temperature, $V_{IOUTADJ}$=$V_{REF}$**

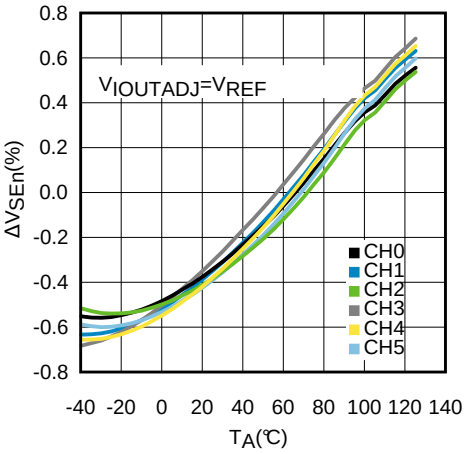



**Figure 4.**

**Variation of $V_{SEn}$ vs Temperature, $V_{IOUTADJ}$=0.5 $V_{REF}$**

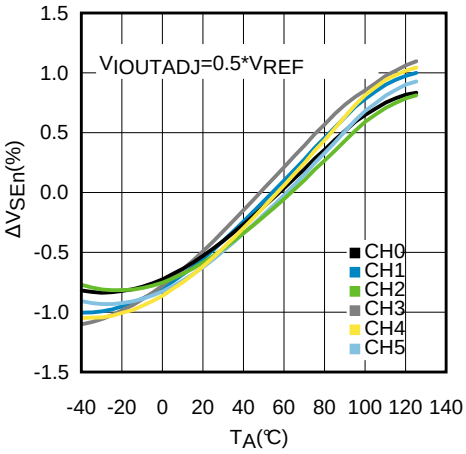



**Figure 5.**

**CH-CH Variation of $V_{SEn}$ vs Temperature, $V_{IOUTADJ}$=$V_{REF}$**

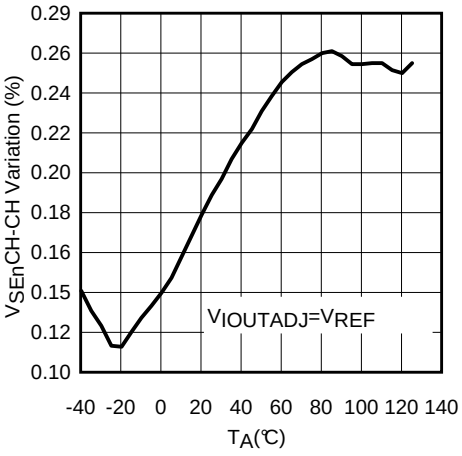



**Figure 6.**

**CH-CH Variation of $V_{SEn}$ vs Temperature, $V_{IOUTADJ}$=0.5 $V_{REF}$**

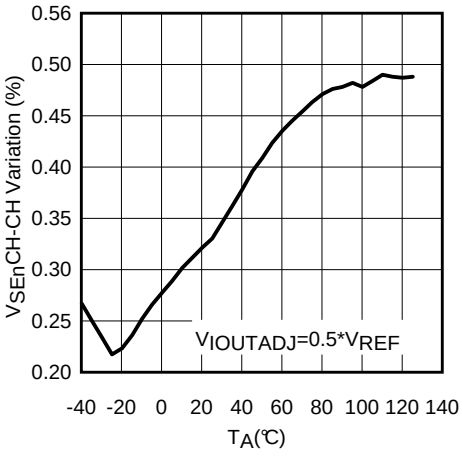



**Figure 7.**

## Typical Performance Characteristics (continued)

All curves taken at $V_{IN}$ = 48V with configuration in typical application for driving twelve power LEDs with six output channels active and 350 mA output current per channel. $T_A$ = 25°C, unless otherwise specified.

**$V_{SEn}$ vs $V_{IOUTADJ}$, $T_A$=125°C**

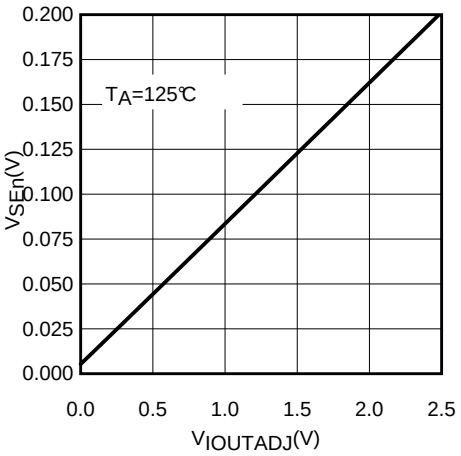



**Figure 8.**

**$V_{SEn}$ vs $V_{IOUTADJ}$ ($V_{IOUTADJ}$ < 60 mV), $T_A$=125°C**

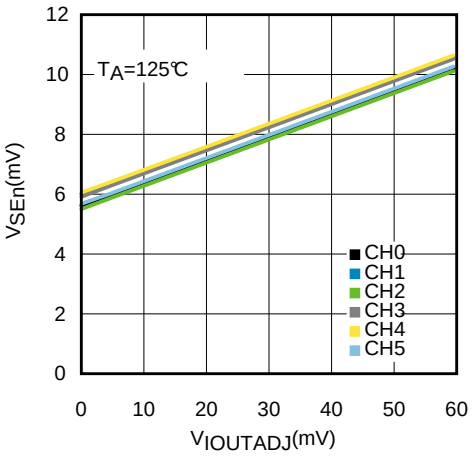



**Figure 9.**

**$V_{SEn}$ vs $V_{IOUTADJ}$, $T_A$=25°C**

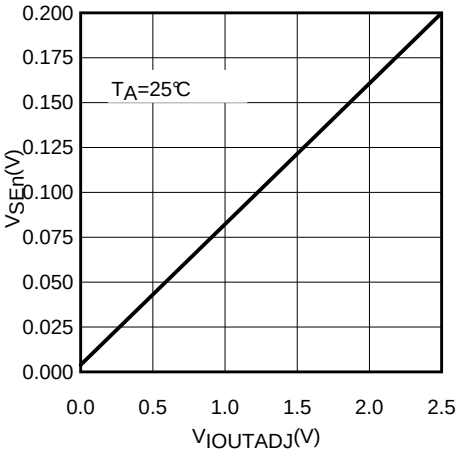



**Figure 10.**

**$V_{SEn}$ vs $V_{IOUTADJ}$ ($V_{IOUTADJ}$ < 60 mV), $T_A$=25°C**

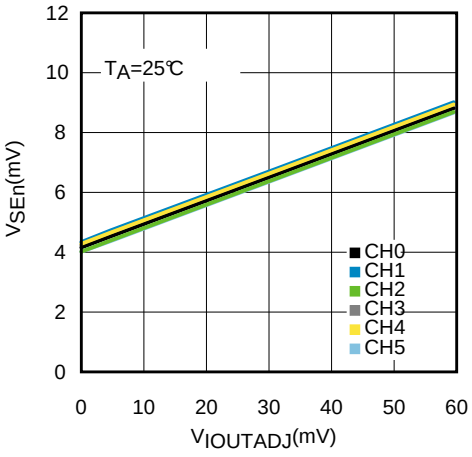



**Figure 11.**

**$V_{SEn}$ vs $V_{IOUTADJ}$, $T_A$=–40°C**

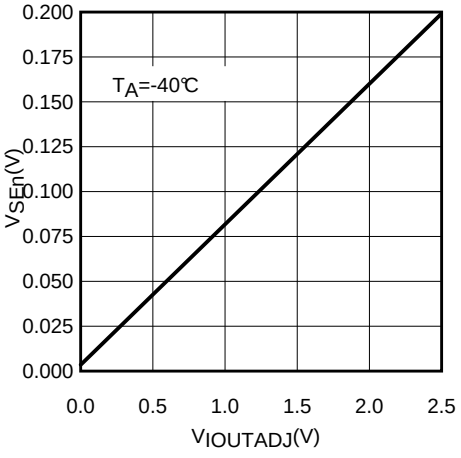



**Figure 12.**

**$V_{SEn}$ vs $V_{IOUTADJ}$ ($V_{IOUTADJ}$ < 60 mV), $T_A$=–40°C**

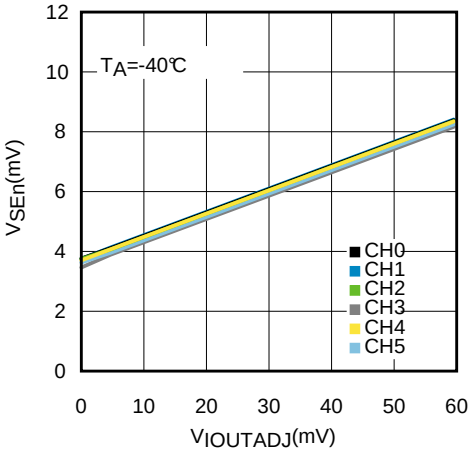



**Figure 13.**

## Typical Performance Characteristics (continued)

All curves taken at $V_{IN}$ = 48V with configuration in typical application for driving twelve power LEDs with six output channels active and 350 mA output current per channel. $T_A$ = 25°C, unless otherwise specified.

**$V_{OutP-MAX}$ vs Temperature**

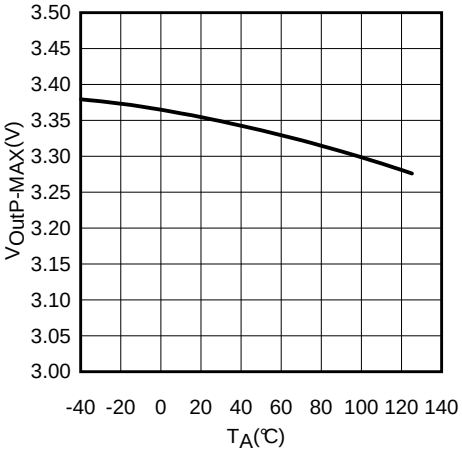



**Figure 14.**

**$V_{REF}$ vs Temperature**

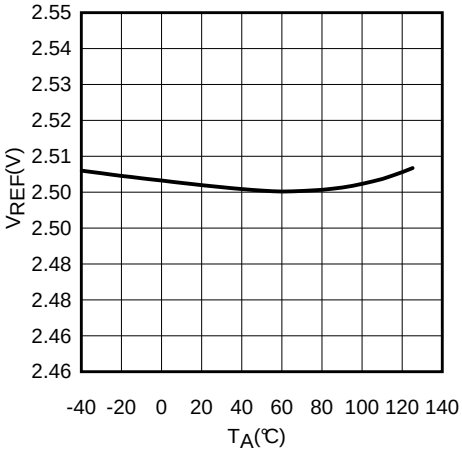



**Figure 15.**

**$V_{CC}$ vs Temperature**

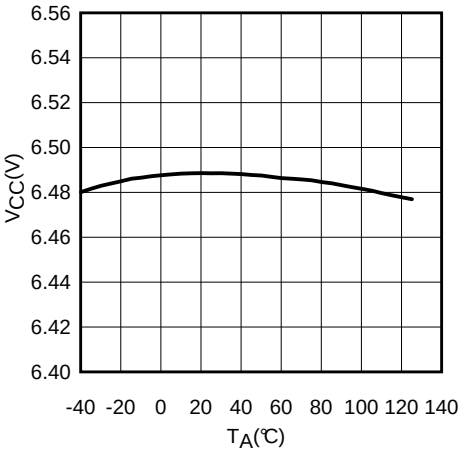



**Figure 16.**

**Operating $I_{IN}$ vs Temperature**

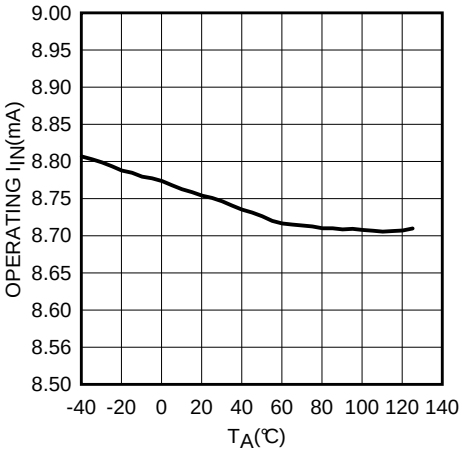
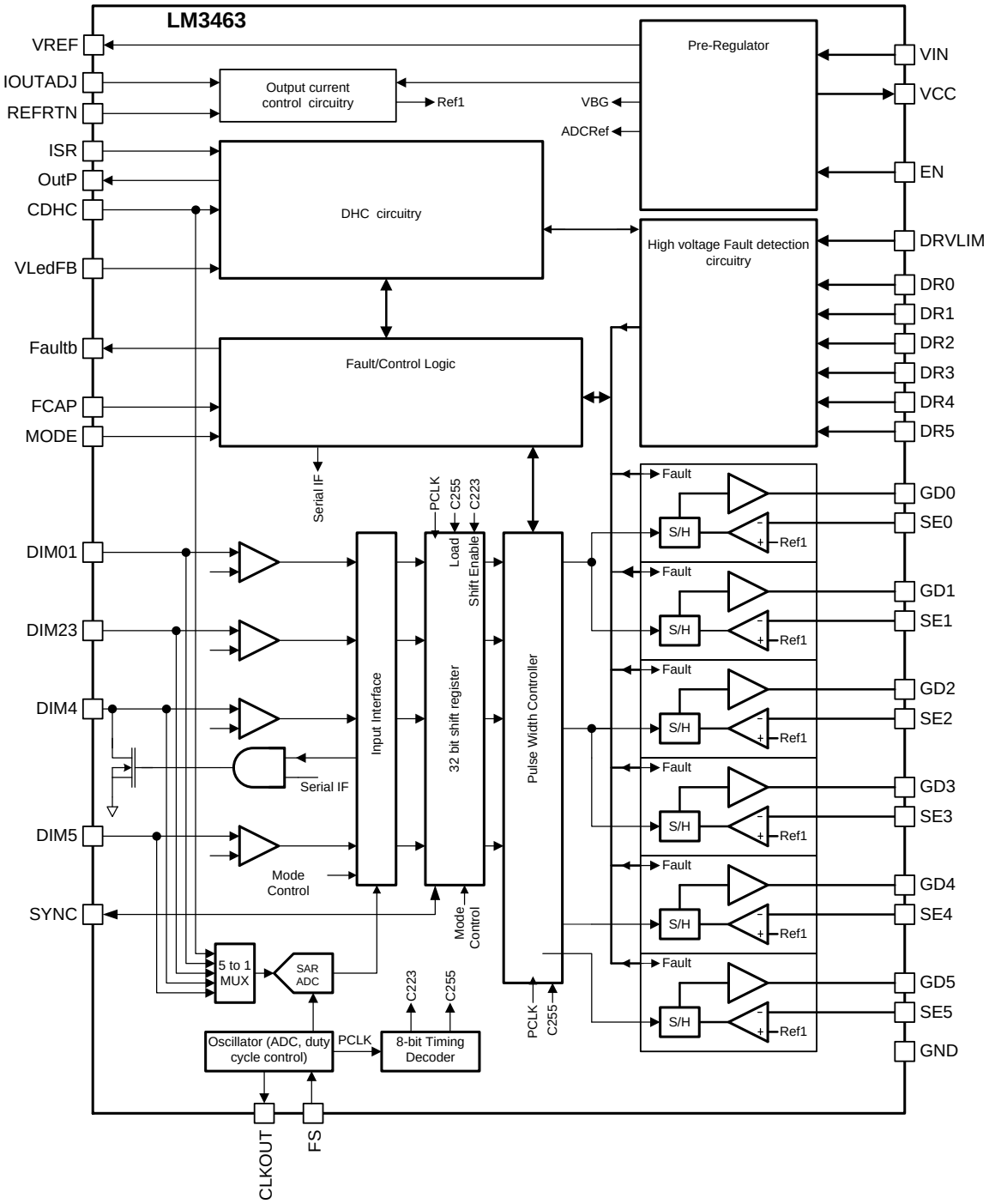



**Figure 17.**

## Block Diagram



## Overview

The LM3463 is a six channel linear current regulator which designed for LED lighting applications. The use of the Dynamic Headroom Control (DHC) method secures high system power efficiency and prolongs system operation lifetime by minimizing the power stress on critical components. The output currents of the LM3463 driver stage are regulated by six individual low-side current regulators.

The current regulators are accompanied by a high precision current sensing circuit. In order to ensure excellent current matching among output channels, the current sensing inputs are corresponding to a dedicated reference point, the REFRTN pin to insulate the ground potential differences due to trace resistances. With this current sensing circuit, the channel to channel output current difference is well controlled below ±10% when the output current is reduced (DC LED current reduction) to 5%.

### LED Current Regulators and Analog Dimming Control

The LM3463 provides six individual linear current regulators to perform LED current regulation. Each current regulator includes an internal MOSFET driver and error amplifier and an external MOSFET and current sensing resistor. The output current of every output channel is defined by the value of an external current sensing resistor individually. The reference voltage of the regulators can be adjusted by changing the bias voltage at the IOUTADJ pin.

When analog dimming control applies, the output current of all channels reduces proportional to the voltage being applied to the IOUTADJ pin. Figure 18 shows the simplified block diagram of a current regulator.

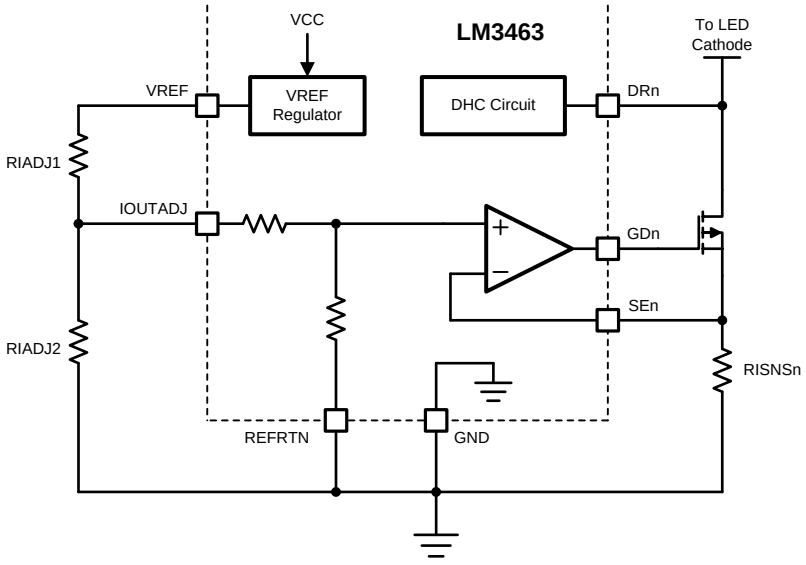



**Figure 18. Block diagram of a linear current regulator**

Since the driving current of a LED string is determined by the resistance of the current sensing resistor $R_{ISNSn}$ individually, every channel can have different output current by using different value of $R_{ISNSn}$. The LED current, $I_{OUTn}$ is calculated using the following expression:

$$V_{SEn} = [(V_{IOUTADJ} \times 0.0782) + 4.3 \times 10^{-3}] \quad (1)$$

AND since:

$$I_{OUTn} = \left(\frac{V_{SEn}}{R_{ISNSn}}\right) A \quad (2)$$

Thus,

$$I_{OUTn} = \frac{[(V_{IOUTADJ} \times 0.0782) + 4.3 \times 10^{-3}]}{R_{ISNSn}} \quad (3)$$

The above equations apply when $V_{IOUTADJ}$ is equal to or below $V_{REF}$ (2.5V). Generally the $V_{IOUTADJ}$ should not be set higher than $V_{REF}$. Applying a voltage high than $V_{REF}$ to the IOUTADJ pin could result in inaccurate LED driving currents which fall out of the specification. Figure 19 shows the relationship of $V_{IOUTADJ}$ and $V_{SEn}$.

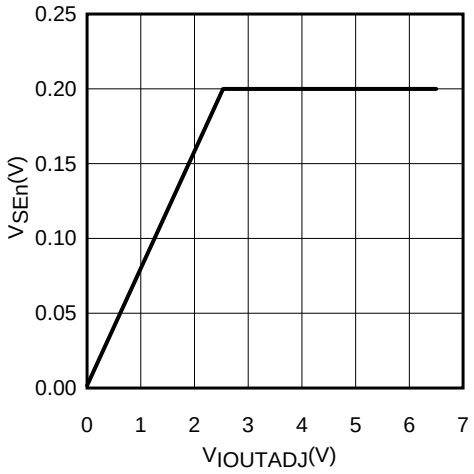



**Figure 19. $V_{SEn}$ versus $V_{IOUTADJ}$**

Since the analog dimming control interface is designed for slow brightness control only, the rate of change of the voltage at the IOUTADJ pin must not be higher than 1.25V/sec to allow good tracking of the output current and changing of the $V_{IOUTADJ}$. The voltage at the IOUTADJ pin can be provided by an external voltage source as shown in Figure 20.

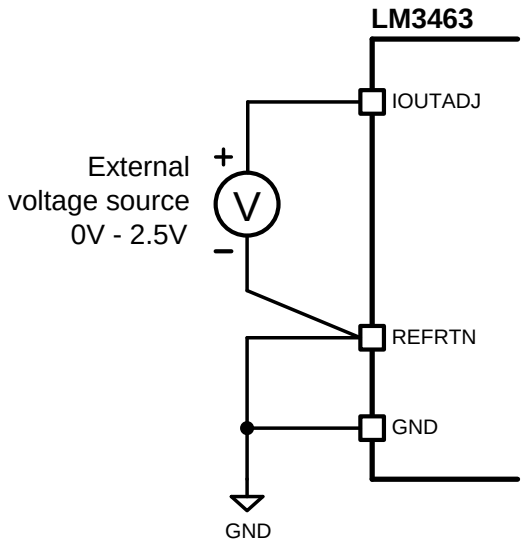



**Figure 20. Adjust $V_{SEn}$ by external voltage**

To secure high accuracy and linearity of dimming control, the voltage of the IOUTADJ pin can be provided by a voltage divider connecting across the VREF and REFRTN pins as shown in Figure 21.

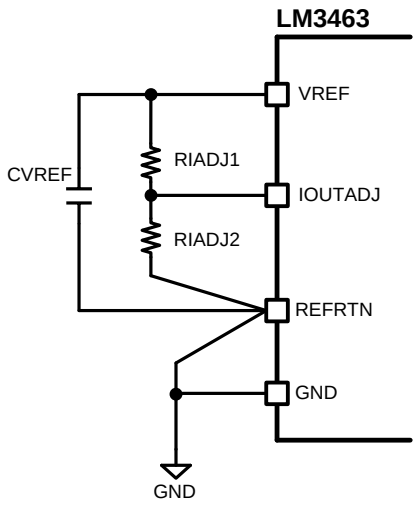



**Figure 21. Biasing IOUTADJ from VREF**

## $V_{CC}$ Regulator

The $V_{CC}$ regulator accepts an input voltage in the range of 12V to 95V from the VIN pin and delivers a 6.5V typical constant voltage at the VCC pin to provide power and bias voltages to the internal circuits. The VCC pin should be bypassed to ground by a low ESR capacitor across the VCC and GND pins. A 1uF 10V X7R capacitor is suggested.

The output current of the VCC regulator is limited to 20 mA which includes the biasing currents to the internal circuit. When using the VCC regulator to bias external circuits, it is suggested to sink no more than 10 mA from the VCC regulator to prevent over-heating of the device.

## VREF Regulator

The VREF regulator is used to provide precision reference voltage to internal circuits and the IOUTADJ pin. Other than providing bias voltage to the IOUTADJ pin, the VREF pin should not be used to provide power to external circuit. The VREF pin must be bypassed to ground by a low ESR capacitor across the VREF and RETRTN pins. A 0.47uF 10V X7R capacitor is suggested.

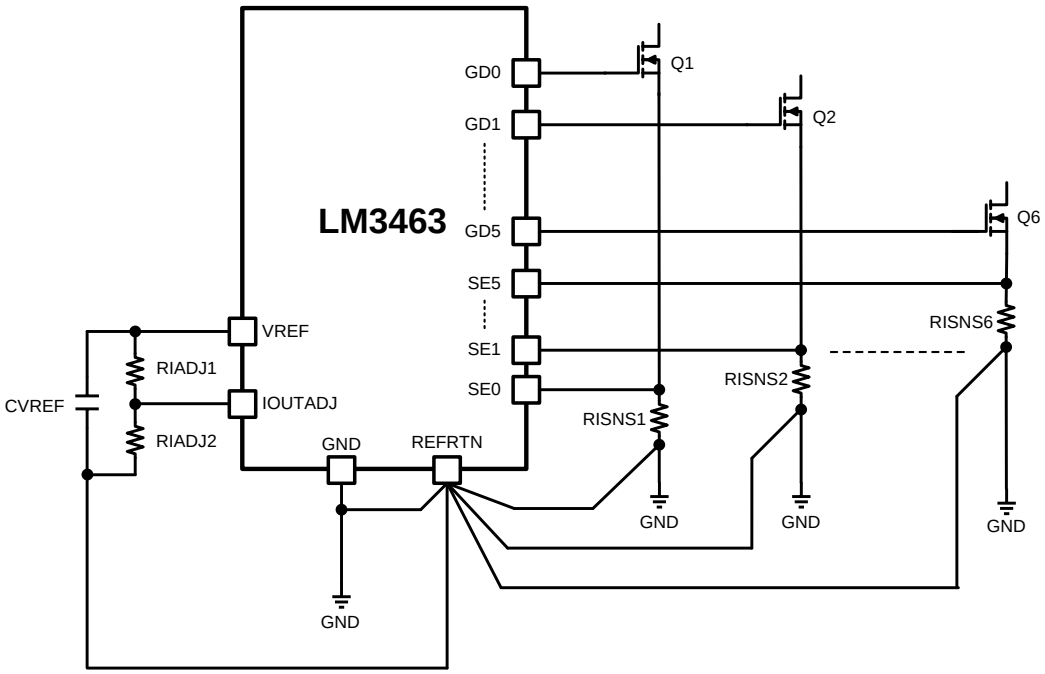



**Figure 22. Individual connections to REFRTN**

## REFRTN and GND

The REFRTN pin is the reference point for the high precision and low noise internal circuits. The pins which referenced to the REFRTN are VREF, IOUTADJ, SE0, SE1, SE2, SE3, SE4 and SE5. To secure accurate current regulations, the current sensing resistors, $R_{ISNSn}$ should connect to the REFRTN pin directly using dedicated connections. And the REFRTN and GND pins should be connected together using dedicated connection as shown in Figure 22.

## Device Enable

The LM3463 can be disabled by pulling the EN pin to ground. The EN pin is pulled up by an internal weak-pull-up circuit, thus the LM3463 is enabled by default. Pulling the EN pin to ground will reset all fault status. A system restart will be undertaken when the EN pin is released from pulling low.

## Open Circuit of LED String(s)

When a LED string is disconnected, the LM3463 pulls the Faultb low to indicate a fault condition. The Faultb is an open-drain output pin. An open circuit of a LED string is detected when a $V_{SEn}$ is below 43 mV and the $V_{DRn}$ of the corresponding channel is below 300mV simultaneously. When the fault conditions are fulfilled, the LM3463 waits for a delay time to recognize whether there is a disconnected LED or not. If the conditions of open circuit of LED is sustained longer than the delay time, a real fault is recognized. The delay time for fault recognition is defined by the value of an external capacitor, $C_{FLT}$, and governed by the following equation:

$$t_{FLT\text{-}RECOG} = \left(\frac{3.62V \times C_{FLT}}{28.1\,\mu A}\right) second \quad (4)$$

The fault indication can be reset by either applying a falling edge to the EN pin or performing a system re-powering.

## System Clock Generator

The LM3463 includes an internal clock generator which is used to provide clock signal to the internal digital circuits. The clock frequency at the CLKOUT pin is equal to 1/2 of the frequency of the internal system clock generator. The system clock generator governs the rate of operation of the following functions:

- PWM dimming frequency in Serial Interface Mode
- PWM dimming frequency in DC Interface Mode
- Clock frequency in cascade operation (CLKOUT pin)

The system clock frequency is defined by the value of an external resistor, $R_{FS}$ following the equation:

$$f_{CLKOUT} = \left[\frac{15.44 \times 10^6}{R_{FS} + 548.6} + 10.08\right] kHz \quad (5)$$

| Operation Mode | CLKOUT Freq. | Dimming Freq. | $R_{FS}$ |
|---|---|---|---|
| Serial Interface Mode | 125 kHz | 488. 3Hz | 125 kΩ |
| DC Interface Mode | 625 kHz | 488.3Hz | 62.2 kΩ |
| Direct PWM Mode | 625 kHz | Virtually no limit | 62.2 kΩ |

## Dynamic Headroom Control (DHC)

The Dynamic Headroom Control (DHC) is a control method which aimed at minimizing the voltage drops on the linear regulators to optimize system efficiency. The DHC circuit inside the LM3463 controls the output voltage of the primary power supply ($V_{RAIL}$) until the voltage at any drain voltage sensing pin ($V_{DRn}$) equals 1V. The LM3463 interacts with the primary power supply through the OutP pin in a slow manner which determined by the capacitor, $C_{DHC}$. Generally, the value of the $C_{DHC}$ defines the frequency response of the LM3463. The higher the capacitance of the $C_{DHC}$, the lower the frequency response of the DHC loop, and vice versa. Since the $V_{RAIL}$ is controlled by the LM3463 via the DHC loop, the response of the LM3463 driver stage must be set one decade lower than the generic response of the primary power supply to secure stable operation.

The cut-off frequency of the DHC loop is governed by the following equation:

$$f_{C(LM3463)} = \left(\frac{1}{2\Pi \times CDHC \times R_{CDHC\text{-}SOURCE}}\right) Hz \quad (6)$$

Practically, the frequency response of the primary power supply might not be easily identified (e.g. off-the-shelf AC/DC power supply). For the situations that the primary power supply has an unknown frequency response, it is suggested to use a 2.2uF 10V X7R capacitor for CDHC as an initial value and decrease the value of the $C_{DHC}$ to increase the response of the whole system as needed.

## Holding $V_{RAIL}$ In Analog Dimming Control

Due to the V-I characteristic of the LED, the forward voltage of the LED strings decreases when the forward current is decreased. In order to compensate the rising of the voltage drop on the linear regulators when performing analog dimming control (due to the reduction of LED forward voltages), the DHC circuit in the LM3463 reduces the rail voltage ($V_{RAIL}$) to maintain minimum voltage headroom (i.e. minimum $V_{DRn}$).

In order to ensure good response of analog dimming control, the $V_{RAIL}$ is maintained at a constant level to provide sufficient voltage headroom when the output currents are adjusted to a very low level. When the voltage at the IOUTADJ pin is decreased from certain level to below 0.63V, the DHC circuit stops to react to the changing of $V_{DRn}$ and maintains the $V_{RAIL}$ at the level while $V_{IOUTADJ}$ equals 0.63V. DHC resumes when the $V_{IOUTADJ}$ is increased to above 0.63V. Figure 23 shows the relationship of the $V_{RAIL}$, $V_{SEn}$ and $V_{IOUTADJ}$.

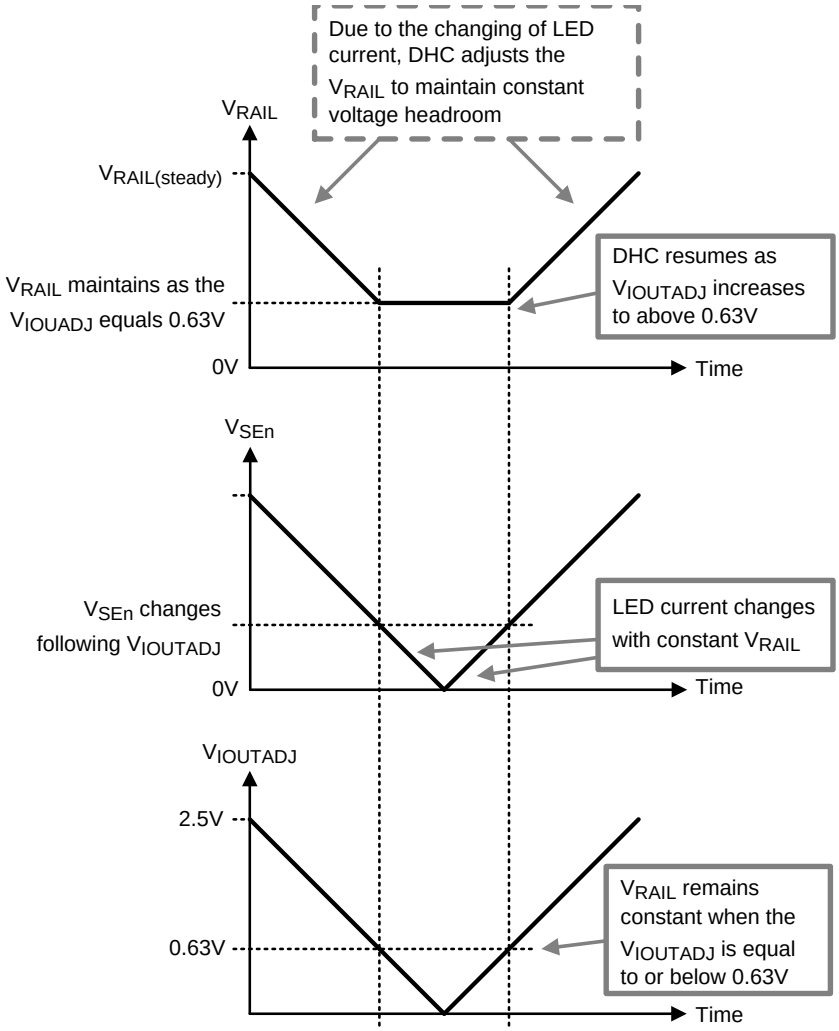



**Figure 23. Holding $V_{RAIL}$ when $V_{IOUTADJ}$ is below 0.63V**

## System Startup

When the LM3463 is powered, the internal Operational Transconductance Amplifier (OTA) charges the capacitor $C_{DHC}$ through the CDHC pin. As the voltage at the CDHC pin increases, the voltage at the OutP pin starts to reduce from $V_{CC}$. When the voltage of the OutP pin falls below $V_{FB}$ + 0.7V, the OutP pin sinks current from the $V_{FB}$ node and eventually pulls up the output voltage of the primary power supply ($V_{RAIL}$). As the $V_{RAIL}$ reaches $V_{DHC\_READY}$, the LM3463 performs a test to identify the status of the LED strings (short / open circuit of LED strings). The $V_{DHC\_REDAY}$ is defined by an external voltage divider which consists of $R_{FB1}$ and $R_{FB2}$. The $V_{DHC\_READY}$ is calculated following the equation:

$$V_{DHC\_READY} = \left(\frac{RFB1 + RFB2}{RFB2}\right) \times 2.5V \tag{7}$$

After the test is completed, the LM3463 turns on the LED strings with regulated output currents. At the moment that the LM3463 turns the LEDs on, the OutP pin stops sinking current from the $V_{FB}$ node and in turn $V_{RAIL}$ slews down. Along with the decreasing of $V_{RAIL}$, the voltage at the $V_{DRn}$ pins falls to approach 1V. When a $V_{DRn}$ is decreased to 1V, the DHC loop enters a steady state to maintain the lowest $V_{DRn}$ to 1V average at a slow manner defined by $C_{DHC}$. Figure 24 presents the changes of $V_{RAIL}$ from system power up to DHC loop enters steady state.

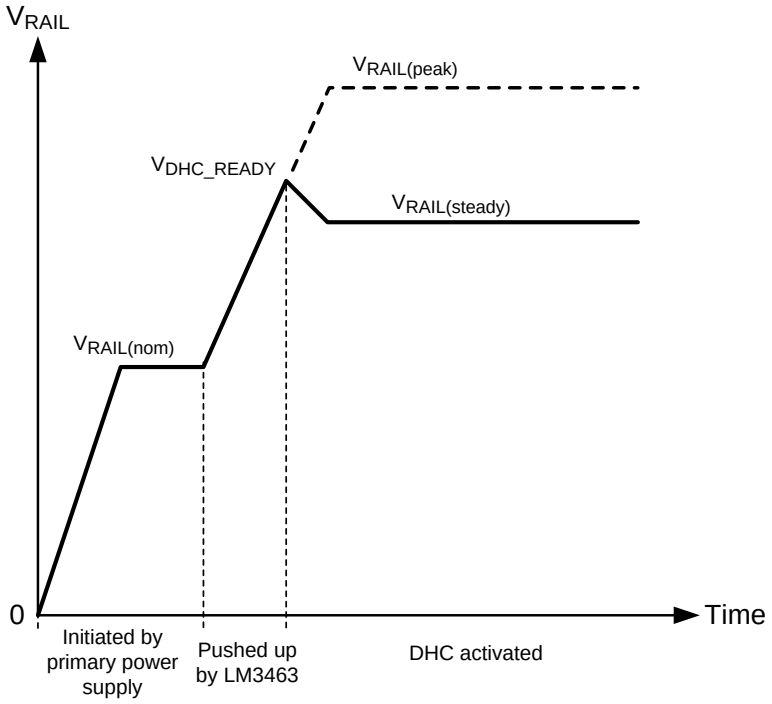



**Figure 24. Changes of $V_{RAIL}$ during system startup**

## Shortening System Startup Time

The system startup time can be shortened by sinking current from the ISR pin to ground through a resistor, $R_{ISR}$. The lower resistance the $R_{ISR}$ carries, the shorter time the system startup takes. Sinking current from the ISR pin increases the charging current to the capacitor, $C_{DHC}$and eventually increases the rate of the increasing of $V_{RAIL}$ during startup ($V_{RAIL}$ ramps up from $V_{RAIL(nom)}$ to $V_{DHC\_READY}$). Figure 25 shows how the system startup time is shortened by using different value of $R_{ISR}$.

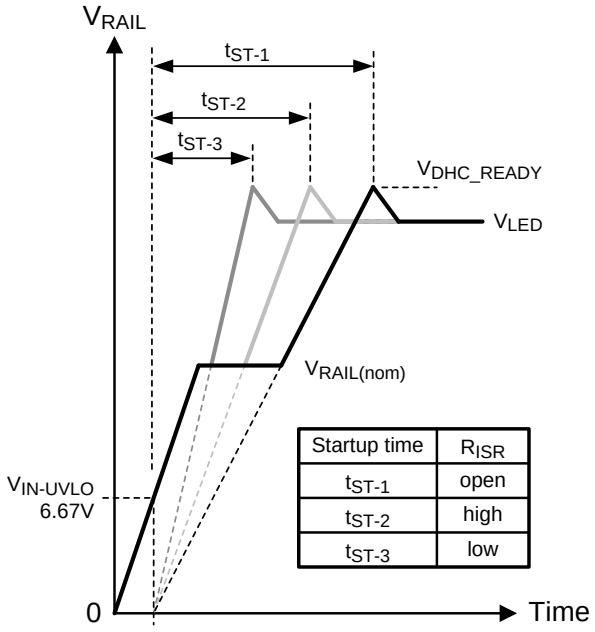



**Figure 25. Setting different startup time using different $R_{ISR}$**

Generally, the system startup time $t_{ST}$ is the longest when the ISR pin is left open ($t_{ST-1}$). The amount of the decreasing of the startup time is inversely proportional to the current being drawn from the ISR pin, thus determined by the value of the resistor, $R_{ISR}$. The rate of decreasing of the startup time is governed by the following equation.

$$t_{ST} = \left[ \frac{1}{\left( 1 + \frac{170503}{R_{ISR}} \right)} \right] \times t_{ST-1} \tag{8}$$

The practical startup time varies according to the settings of the $V_{DHC\_READY}$, $V_{FB}$, $C_{DHC}$ and $R_{ISR}$ with respect to the following equations.

$$t_{ST} = \left[ \frac{3.6V - V_{OutP}}{\left( 7.33\,\mu A + \frac{1.25V}{R_{ISR}} \right)} \right] \times C_{CDHC} \text{ in sec.} \tag{9}$$

where

$$V_{OutP} = \left[ V_{FB} - 0.6V - R_{DHC} \times \left( \frac{V_{DHC-READY} - V_{FB}}{R_1} - \frac{V_{FB}}{R_2} \right) \right] \tag{10}$$

Sinking higher than 100 µA from the ISR pin could damage the device. The value of the $R_{ISR}$ should be no lower than 13 kΩ to prevent potential damages.

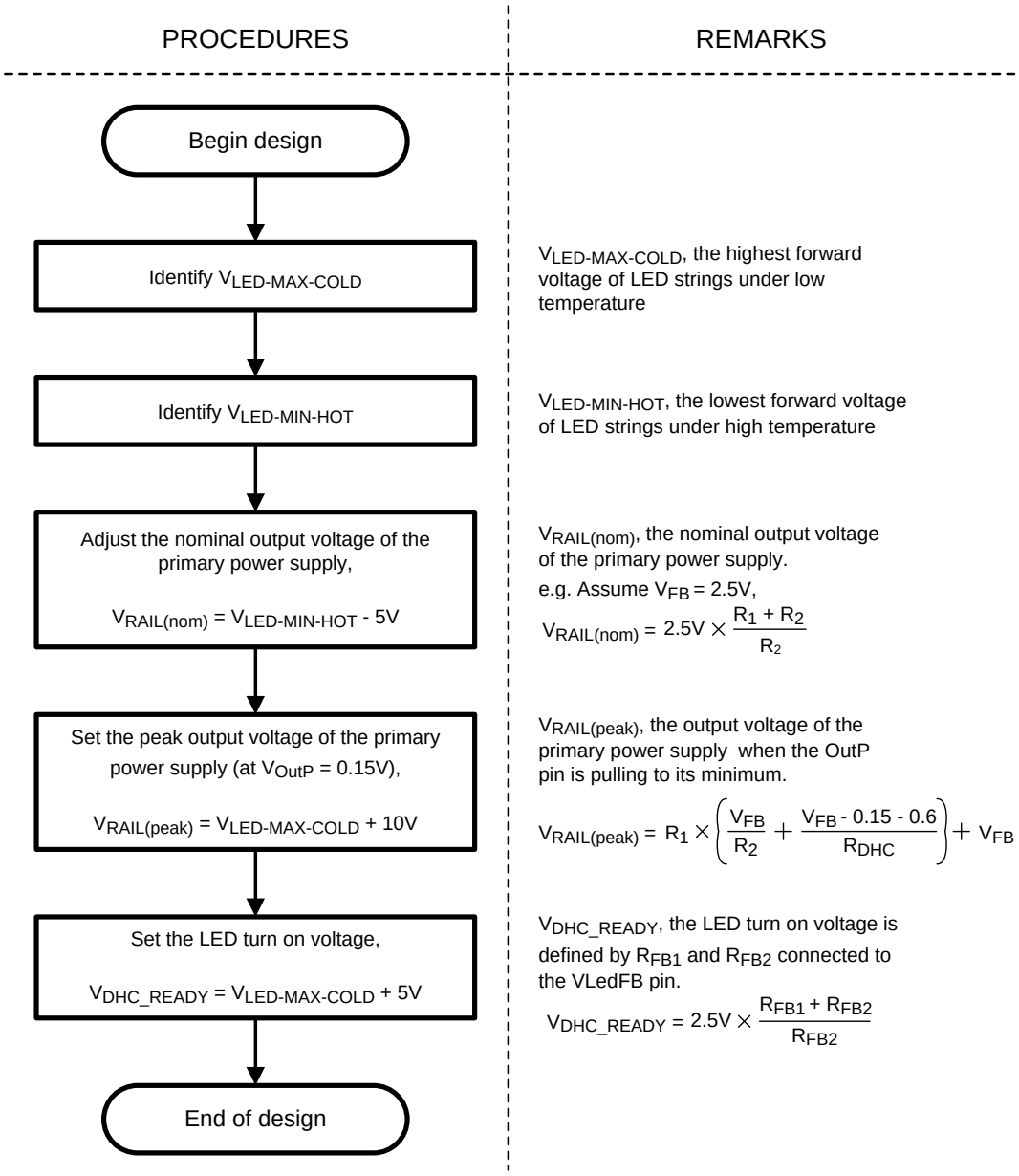



**Figure 26. Procedure of defining startup parameters**

## Setting the $R_{DHC}$ and $V_{RAIL}$

Prior to defining the parameters for the operations in steady state, the value of the $R_{DHC}$ and different levels of the supply rail voltage ($V_{RAIL}$) during system startup must be determined. Figure 26 illustrates the procedures of determining the value of the $R_{DHC}$ and voltage levels of the $V_{RAIL(nom)}$, $V_{RAIL(peak)}$ and $V_{DHC\_READY}$.

In Figure 26, the $V_{LED-MAX-COLD}$ and $V_{LED-MIN-HOT}$ are the maximum and minimum forward voltages of the LED strings under the required lowest and highest operation temperatures respectively. In order to ensure all the LED string are supplied with adequate forward current when turning on the LEDs, the $V_{DHC\_READY}$ must be set higher than the $V_{LED-MAX-COLD}$. For most applications, the $V_{DHC\_READY}$ can be set 5 V higher than the $V_{LED-MAX-COLD}$.

In order to reserve voltage headroom to perform DHC under high operation temperature, the nominal output voltage of the primary power supply must be set lower than the $V_{LED-MIN-HOT}$. For most applications, the $V_{RAIL(nom)}$ can be set 5 V lower than the $V_{LED-MIN-HOT}$. Figure 27 shows an example connection diagram of interfacing the LM3463 to a power supply of 2.5V feedback reference voltage.

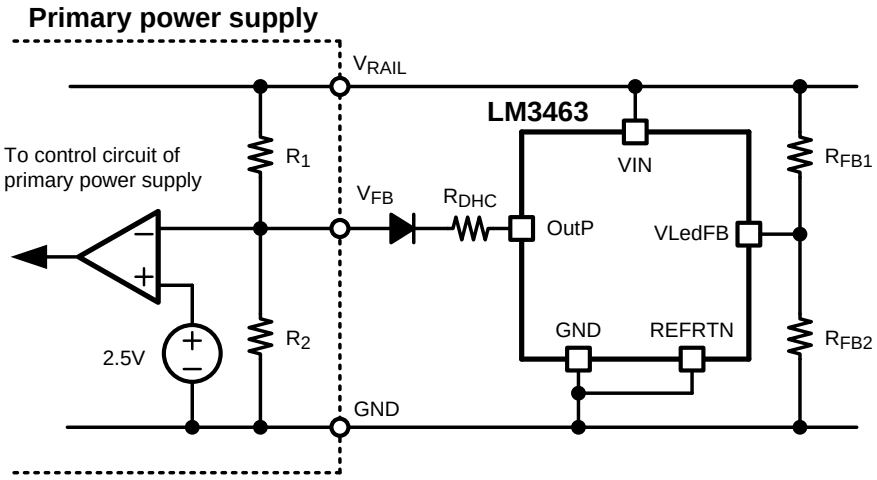



**Figure 27. Connecting the LM3463 to a power supply**

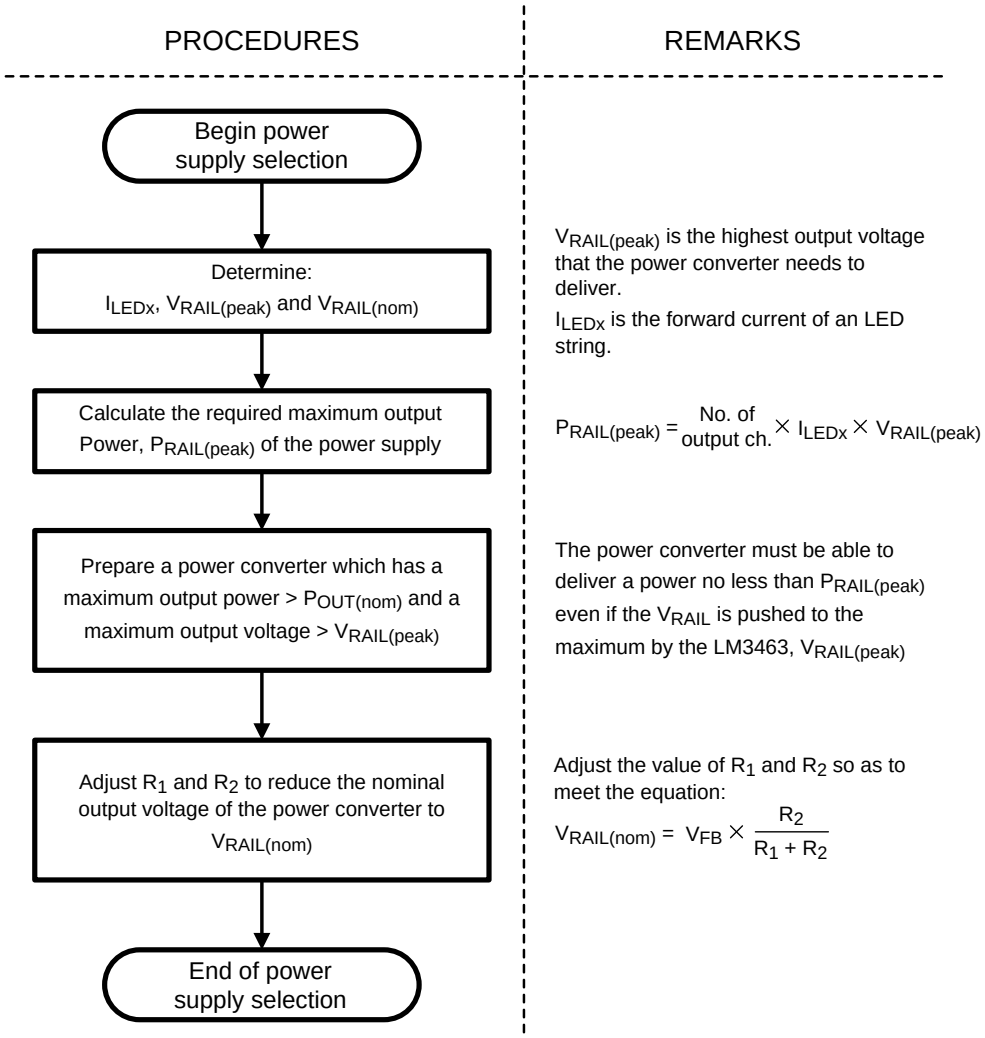



**Figure 28. Procedures of selecting the primary power supply**

## Choosing the proper Primary Power Supply

If the primary power supply is an off-the-shelf power converter, it is essential to make certain that the power converter is able to withstand the $V_{RAIL(peak)}$. In order to allow DHC, the nominal output voltage of the primary power supply needs to be adjusted to below $V_{LED-MIN-HOT}$ as well. The suggested procedures for selecting the proper power supply are as shown in Figure 28.

## Selection of External MOSFET

The selection of external MOSFET is dependent on the highest current and the highest voltage that could be applied to the drain terminal of the MOSFET. Generally, the Drain-to-Source breakdown voltage ($V_{DSS}$) and the continuous drain current ($I_D$) of the external MOSFET must be higher than the defined peak supply rail voltage ($V_{RAIL(peak)}$) and the maximum output LED current ($I_{OUTn}$) respectively.

## Testing LEDs at System Startup

As $V_{RAIL}$ increases to $V_{DHC\_READY}$, the voltage at the VLedFB pin equals 2.5V. When the voltage at the VLedFB pin rises to 2.5V, the LM3463 sinks 100 µA through every LED strings from the supply rail into the DRn pins for certain period of time to determine the status of the LED strings. The time for checking LED strings is defined by the value of the external capacitor, $C_{FLT}$ and is governed by the following equation:

$$t_{LED-TEST} = \left( \frac{3.62V \times C_{FLT}}{28.1\,\mu A} \right) \text{second} \tag{11}$$

If the voltage at any DRn pin is detected lower than 350 mV in the LED test period, that particular output channel will be disabled and excluded from the DHC loop. All disabled output channels will remain in OFF state until a system restarting is undertaken. The LED test performs only once after the voltage at VLedFB pin hits 2.5V. The disabled channel can be re-enabled by pulling the EN pin to GND for 10 ms (issuing a system restart) or re-powering the entire system.

## MOSFET Power Dissipation Limit

In order to protect the MOSFETs from thermal break down when a short circuit of the LED sting(s) is encountered, the LM3463 reduces the output current according to the increment of the drain voltage of the MOSFET ($V_{DRn}$) when the drain voltage exceeds a certain preset threshold voltage to limit the power dissipation on the MOSFETs. This threshold voltage is defined by the voltage being applied to the DRVLIM pin, $V_{DRVLIM}$ and is roughly four times the voltage of the $V_{DRVLIM}$. For example, if the desired drain threshold voltage to perform output current reduction is 16V, the DRVLIM pin voltage should be biased to 4V. Figure 29 shows the relation between $V_{SEn}$, $V_{DRn}$ and $V_{DRVLIM}$.

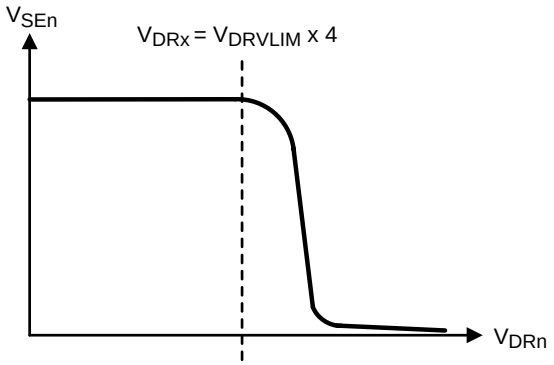



**Figure 29. $V_{SEn}$ reduces as $V_{DRn}$ exceeds $V_{DRVLIM}$ x4**

## Dimming Mode Control

The LM3463 provides three modes of PWM dimming control. The three modes are: Direct PWM dimming mode, Serial interface mode and DC interface mode. Selection of the mode of dimming mode is made by leaving the MODE pin open or connecting the MODE pin to GND or VCC. Regardless of the selection of the mode of PWM dimming control, the output channels 0 and 1 are controlled commonly by the signal at the DIM01 pin and the output channels 2 and 3 are controlled commonly by the PWM signal at the DIM23 pin. The dimming duty of the channel 4 and 5 are controlled by the signals on DIM4 and DIM5 pins respectively.

The DIM01, DIM23, DIM4 and DIM5 pins are pulled down by an internal 2 MΩ weak pull-downs to prevent the pins from floating. Thus the dimming control input pins are default to 'LED OFF' state and need external pulled up resistors when the pins are connected to open collector/drain signal sources. Figure 30 shows a suggested circuit for connecting the LM3463 to an open collector/drain dimming signal sources.

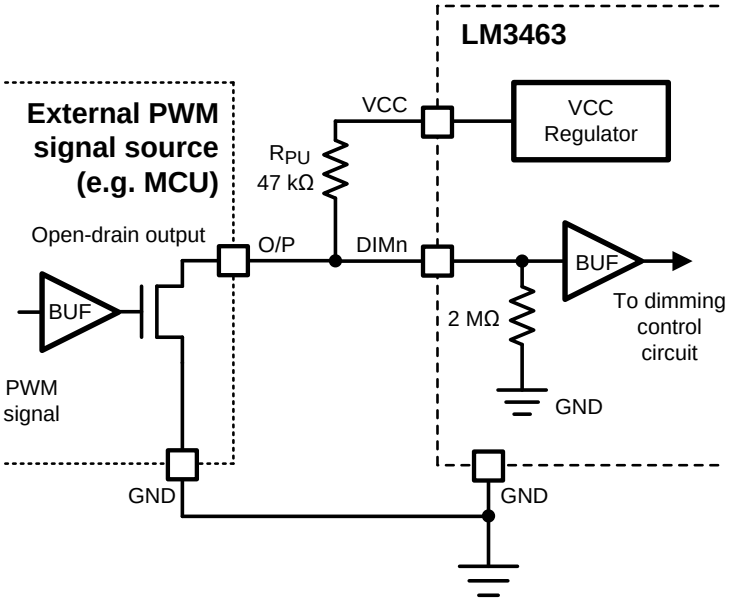



**Figure 30. Adding an external pull-up resistor to the DIMn pin**

### Direct PWM Dimming Mode

Connecting the MODE pin to ground enables direct PWM dimming mode. Every dimming control pin (DIM01 to DIM5) in direct PWM control mode accepts active high TTL logic level signal. In direct PWM dimming mode, the six output channels are separated into four individual groups to accept external PWM dimming signals. The configuration of output channels are as listed in the following table:

| | |
|---|---|
| Group A | CH0 and CH1, controlled by DIM01 pin |
| Group B | CH2 and CH3, controlled by DIM23 pin |
| Group C | CH4, controlled by DIM4 pin |
| Group D | CH5, controlled by DIM5 pin |

In order to secure accurate current regulation, the pull-up time of every dimming control input must not be shorter than 8 µs. If a 256 level (8-bit resolution) brightness control is needed, the PWM dimming frequency should be no higher than 488Hz.

### Serial Interface Mode

Leaving MODE pin floating enables serial interface mode. In serial interface mode, the DIM01, DIM23 and DIM4 pins are used together as a serial data interface to accept external dimming control data frames serially. The following table presents the functions of the DIM01, DIM23 and DIM4 pins in serial interface mode:

| | |
|---|---|
| DIM01 | Serial data packet input (8-bit packet size) |
| DIM23 | Clock signal input for data bit latching |
| DIM4 | End Of Frame (EOF) signal input for data packet loading |

The DIM5 pin is not used in this mode and should connect to GND. Every data frame contains four 8–bit wide data byte for PWM dimming control. Every data byte controls the PWM dimming duty of its corresponding output channel(s): A hexadecimal 000h gives 0% dimming duty; a hexadecimal 0FFh gives 100% dimming duty. Respectively, the first byte being loaded into the LM3463 controls the dimming duty of CH0 and CH1, the second byte controls the dimming duty of CH2 and CH3, the third byte controls the dimming duty of CH4 and the forth byte controls the dimming duty of CH5.

In serial interface mode, the six output channels are separated into four individual groups as listed in the following table:

| | |
|---|---|
| Group A | CH0 and CH1, controlled by the first byte |
| Group B | CH2 and CH3, controlled by the second byte |
| Group C | CH4, controlled by the third byte |
| Group D | controlled by the forth byte |

A data bit is latched into the LM3463 by applying a rising edge to the DIM02 pin. After clocking 32 bits (4 data bytes) into the LM3463, a falling edge should be applied to the DIM4 pin to indicate an EOF and load data bytes from data buffer to output channels accordingly. Figure 31 shows the serial input waveforms to the LM3463 to facilitate in serial interface mode. Figure 32 shows the timing parameters of the serial data interface. The PWM dimming duty in the serial interface mode is governed by the following equation:

$$D_{SERIAL\text{-}DIM} = \left( \frac{\text{data byte value} + 1}{256} \right) \times 100\% \tag{12}$$

The PWM dimming duty at decimal data codes 01 (001h) and 02 (002h) are rounded up to 2/256. Thus the minimum dimming duty in the serial interface mode is 2/256 or 0.781%. Figure 33 shows the relationship of the PWM dimming duty and the code value of a data byte in the serial interface mode. The PWM dimming frequency in serial interface mode is defined by the system clock of the LM3463. The dimming frequency in the serial interface mode is equal to the system clock frequency divided by 256 which follows the equation below:

$$f_{SERIAL\text{-}DIM} = \frac{f_{CLKOUT}}{256} = \left[ \frac{15.44 \times 10^6}{R_{FS} + 548.6} + 10.08 \right] \times \frac{1}{256} \tag{13}$$

In order to achieve a 256 level (8–bit resolution) brightness control, the minimum on time of every channel ($1/(f_{SERIAL\text{-}DIM}*256)$) should be no shorter than 8us, thus a dimming frequency of 488Hz is suggested to use.

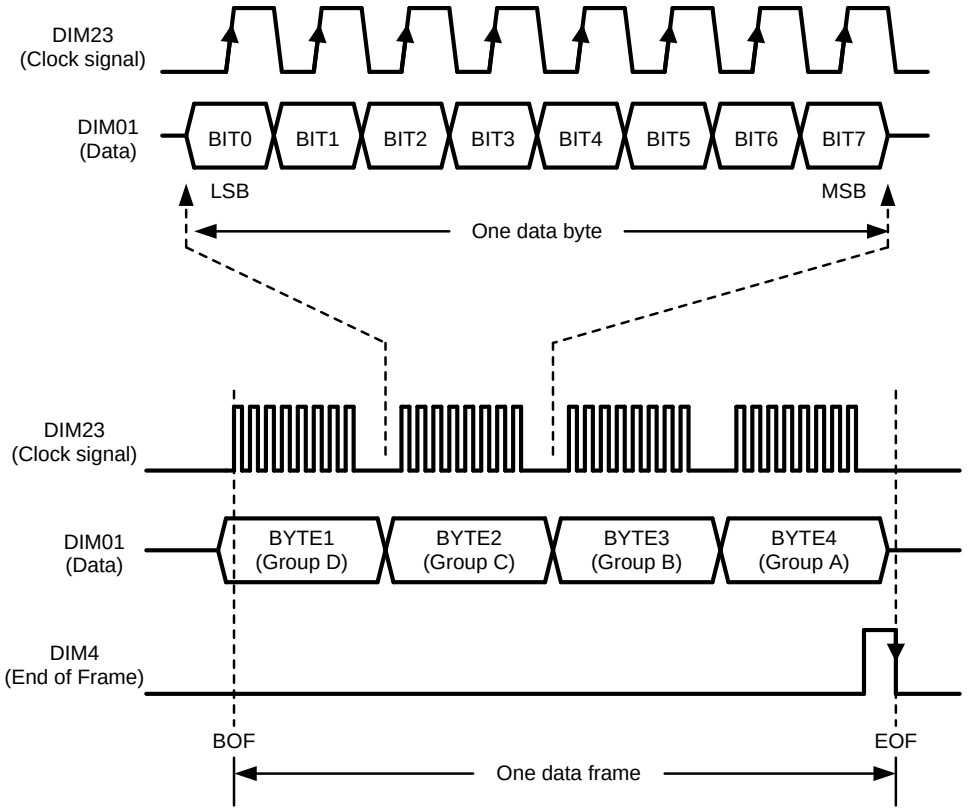



**Figure 31. Input waveform to the LM3463 in serial interface mode**

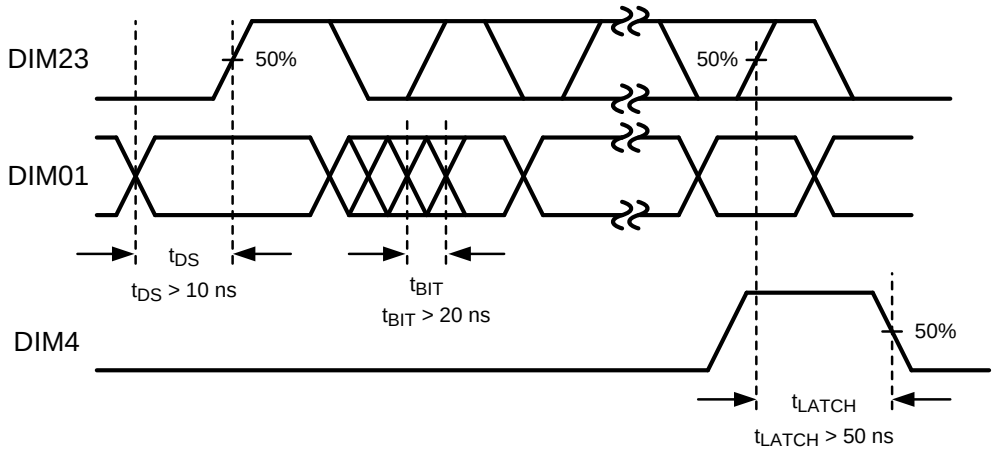



**Figure 32. Timing parameters of the serial data interface**

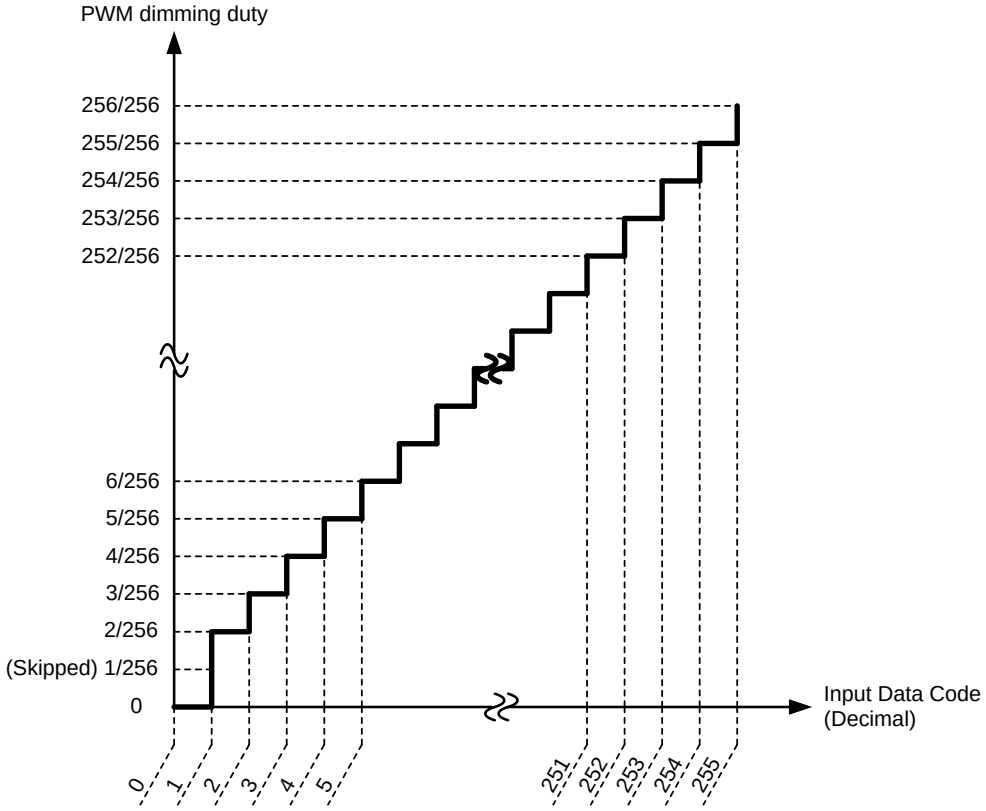



**Figure 33. PWM dimming duty vs code value of a data byte**

### DC Interface Mode

Connecting the MODE pin to VCC enables DC interface mode. In this mode the LM3463 converts the voltage on the dimming signal input pins into PWM dimming duty to the corresponding output channels. The six output channels are separated into four individual groups to accept external PWM dimming signals as listed in the following table:

| | |
|---|---|
| Group A | CH0 and CH1, controlled by the voltage at DIM01 pin |
| Group B | CH2 and CH3, controlled by the voltage at DIM23 pin |
| Group C | CH4, controlled by the voltage at DIM4 pin |
| Group D | CH5, controlled by the voltage at DIM5 pin |

In DC interface mode, the DIM01, DIM23, DIM4 and DIM5 pins accept DC voltages in the range of 0.8V to 5.7V to facilitate PWM dimming control. The voltage at the DIMn pins ($V_{DIMn}$) and the PWM dimming duty in the DC interface mode ($D_{DC\text{-}DIM}$) are governed by the following equation. Figure 34 shows the correlation of $V_{DIMn}$ and $D_{DC\text{-}DIM}$. The conversion characteristic is shown in Figure 35.

$$D_{DC\text{-}DIM} = \left[ \left( V_{DIMn} - 0.8V \right) \times 20.4082 \right] \%$$

where

- $0.8V < V_{DIMn} < 5.7V$ (14)

The PWM dimming frequency in the DC interface mode is defined by the system clock of the LM3463. The dimming frequency in the DC interface mode is equal to the system clock frequency divided by 1280 which follows the equation below:

$$f_{DC\text{-}DIM} = \frac{f_{CLKOUT}}{256} = \left[\frac{15.44 \times 10^6}{R_{FS} + 548.6} + 10.08\right] \times \frac{1}{256} \quad (15)$$

In order to achieve a 256 level (8–bit resolution) brightness control, the minimum on time of every channel ($1/(f_{SERIAL\text{-}DIM}*256)$) should be no shorter than 8 us, thus a dimming frequency of 488Hz is suggested to use.

The LM3463 samples the analog voltage at the DIMn pins and updates the dimming duty of each output channel at a rate of 1280 system clock cycle ($1280/f_{CLKOUT}$). In order to ensure correct conversion of analog voltage to PWM dimming duty, the slew rate of the analog voltage for dimming control is limited the following equation:

$$\frac{dV_{DIMn(DC\text{-}DIM)}}{dt} = < V_{LSB} \times \frac{f_{CLKOUT}}{1280} \quad (16)$$

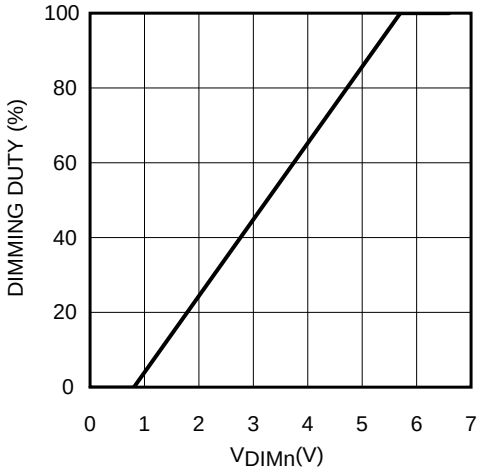



**Figure 34. Dimming Duty vs $V_{DIMn}$ in DC interface mode**

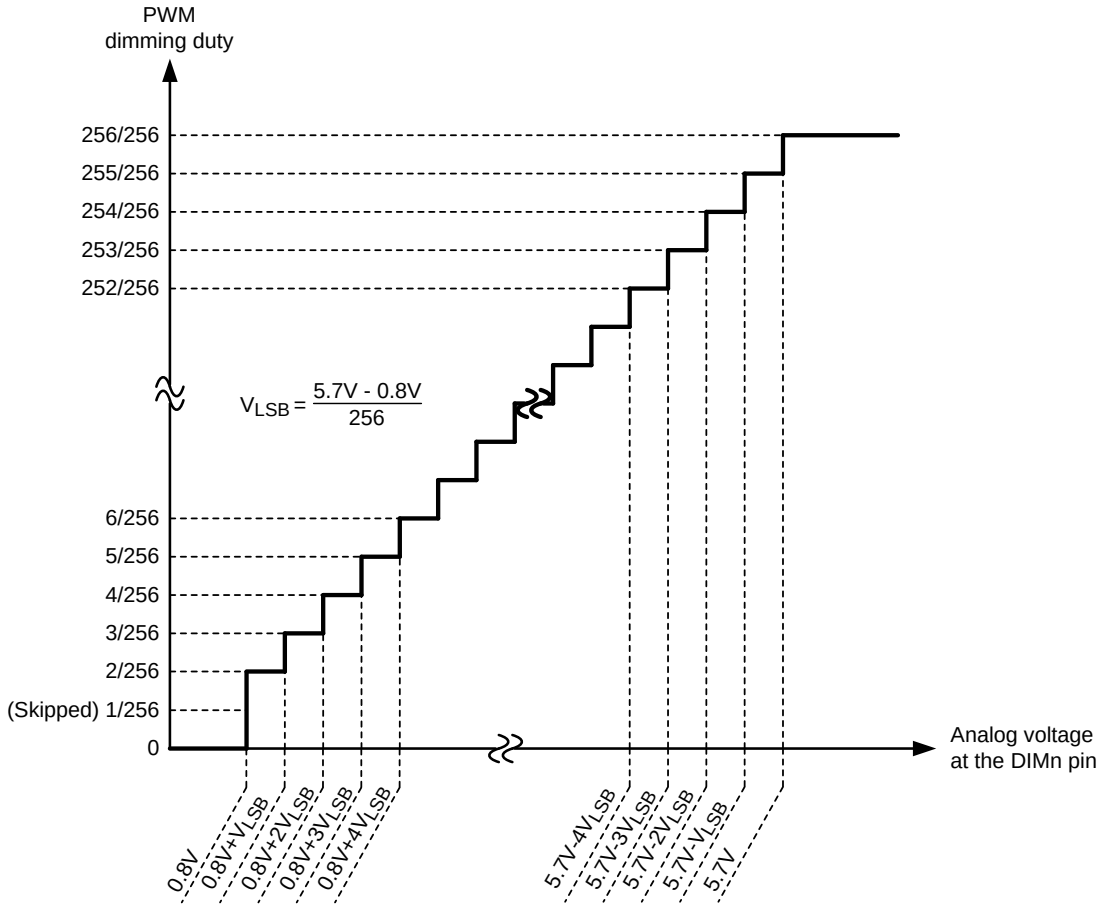



**Figure 35. Conversion characteristic of the analog voltage to PWM dimming control circuit**

## Using Less than Six Output Channels

If less than 6 output channels are needed, the unused output channel(s) of the LM3463 can be disabled by not installing the external MOSFET and current sensing resistor. The drain voltage sensing pin (DRn), gate driver output pin (GDn) and current sensing input pin (SEn) of a disabled channel must be left floating to secure proper operation. The output channel(s) which has no external MOSFET and current sensing resistor installed is disabled and excluded from DHC loop at system startup while the $V_{RAIL}$ reaches $V_{DHC\_READY}$.

A total of five output channels of the LM3463 can be disabled. The channel 0 must be in use regardless of the number of disabled channel. This feature also applies in cascade operation.

## Cascading of LM3463

For the applications that require more than six output channels, two or more pieces of LM3463 can be cascaded to expand the number of output channel. Dimming control is allowed in cascade operation. The connection diagrams for cascade operation in different modes of dimming control are as shown in Figure 36.

### Serial interface mode in cascade operation

In the serial interface mode, the master LM3463 accepts external data frames through the serial data interface which consists of the DIM01, DIM23 and DIM4 pins and passes the frames to the following slave LM3463 through its serial data output interface (SYNC and CLKOUT pins). Every slave unit shifts data in and out bit by bit to its following slave unit.

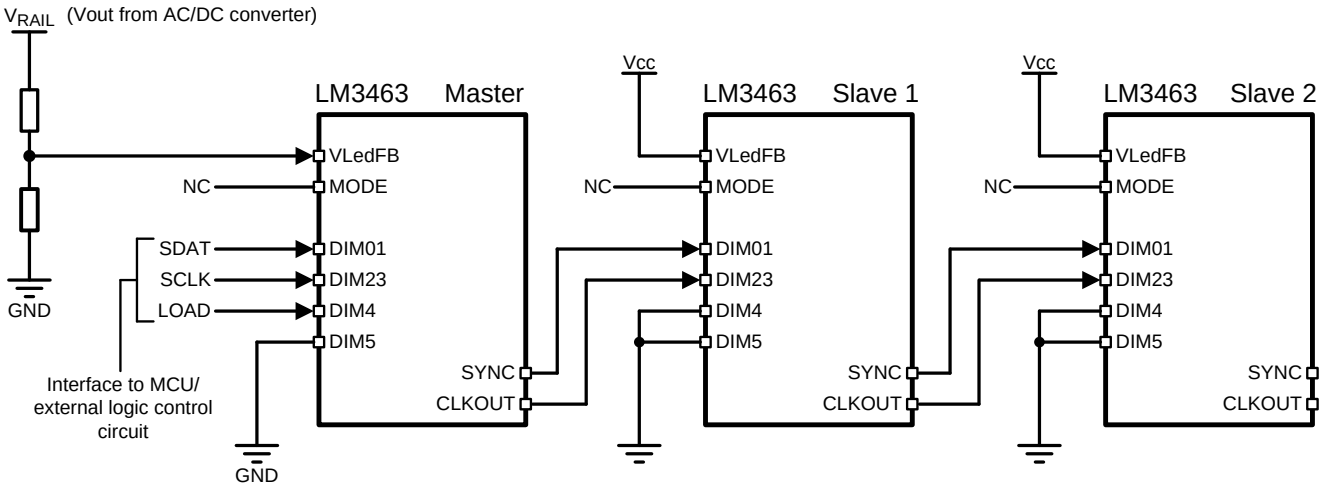
### DC interface mode in cascade operation

In the DC interface mode, the master unit accepts four individual analog dimming control signals from external signal sources (via the DIM01, DIM23, DIM4 and DIM5 pins) and encodes the analog signals into 8-bit serial dimming control signals. The master LM3463 passes the encoded dimming control signals serially to the following slave unit through its serial data output interface (SYNC and CLKOUT pins). Every slave unit shifts data in and out bit by bit to its following slave unit.

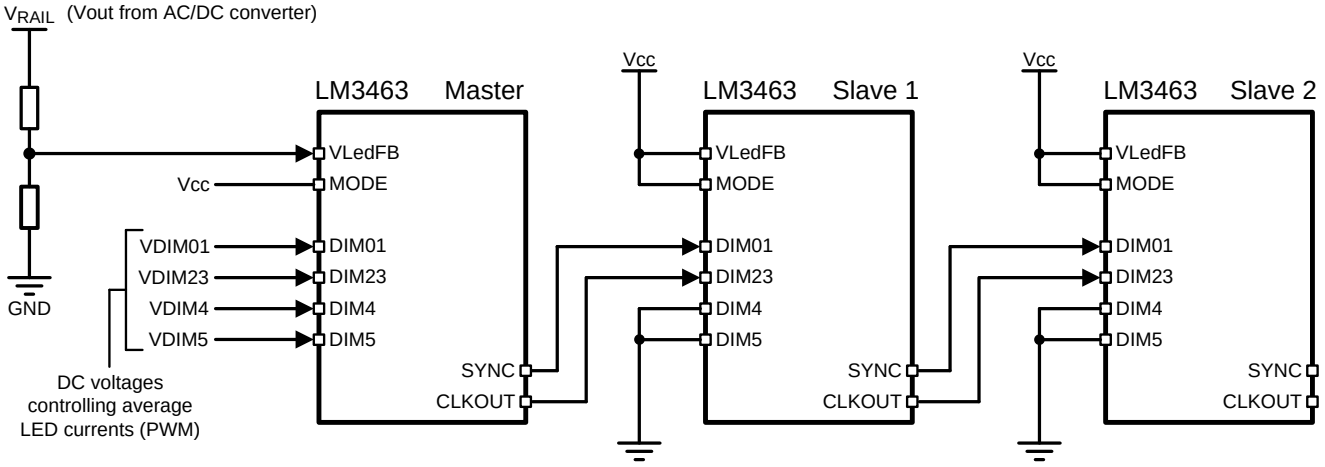
### Direct PWM dimming mode in cascade operation

In the Direct PWM Dimming mode, the master and slave units share the PWM dimming control signals at the DIM01, DIM23, DIM4 and DIM5 pin to facilitate dimming control. In this mode, the SYNC and CLKOUT of all slave units should be connected to the SYNC and CLKOUT pin of the master unit accordingly to perform startup synchronization. Since the dimming control signal inputs of all the LM3464 are connected in parallel to share the control signals, it is essential to ensure the signal source is strong enough to drive all the LM3463 in parallel.

**Serial Data Interface**




**DC Voltage Dimming Control Interface**




**Direct PWM Diming Control Interface**

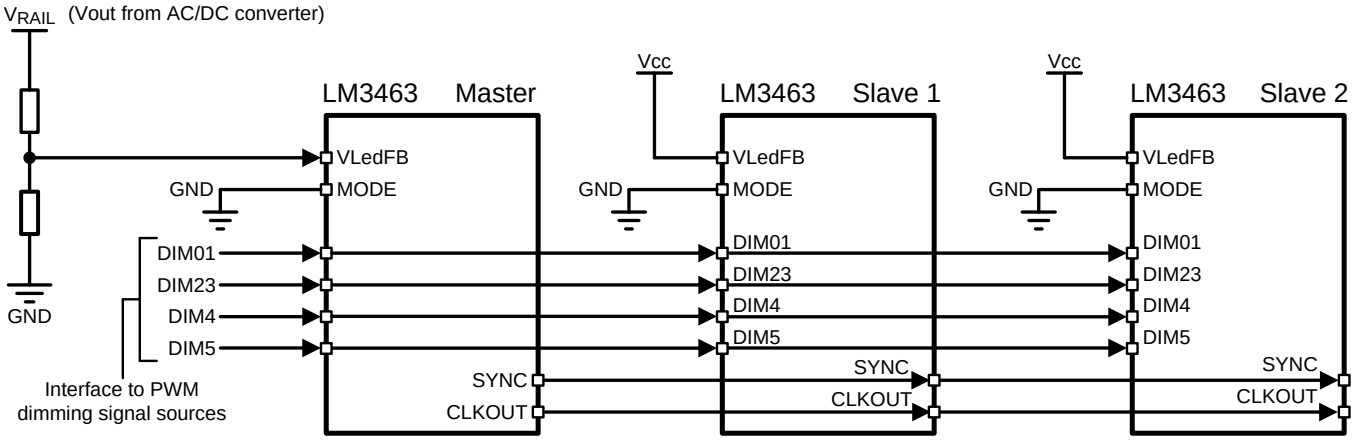



**Figure 36. Connect diagram for cascade operations in different modes of dimming control**

## APPLICATION EXAMPLES

**Figure 37. LM3463 typical application circuit for stand alone operation**

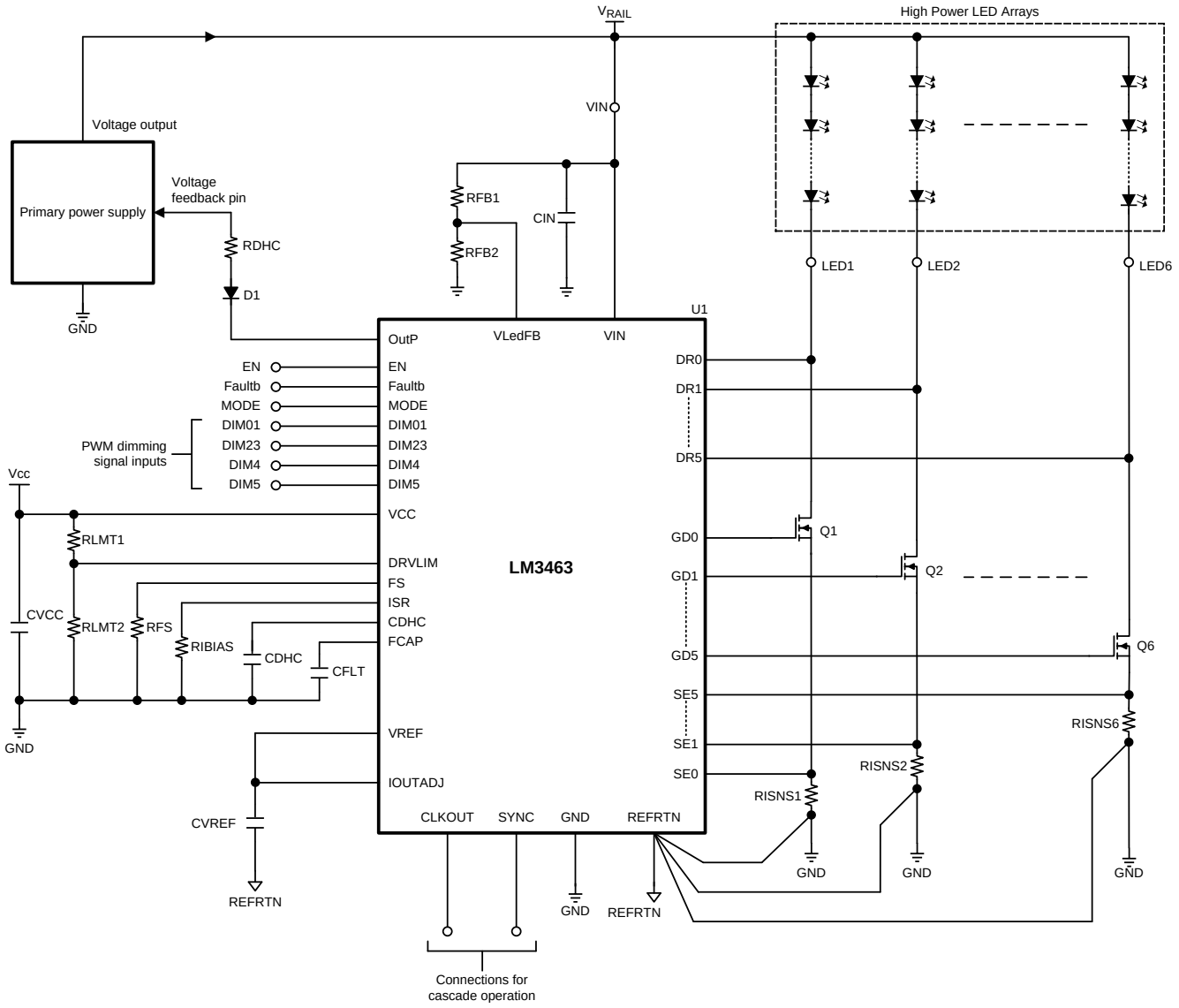


**Figure 38. LM3463 typical application circuit for true analog dimming control**

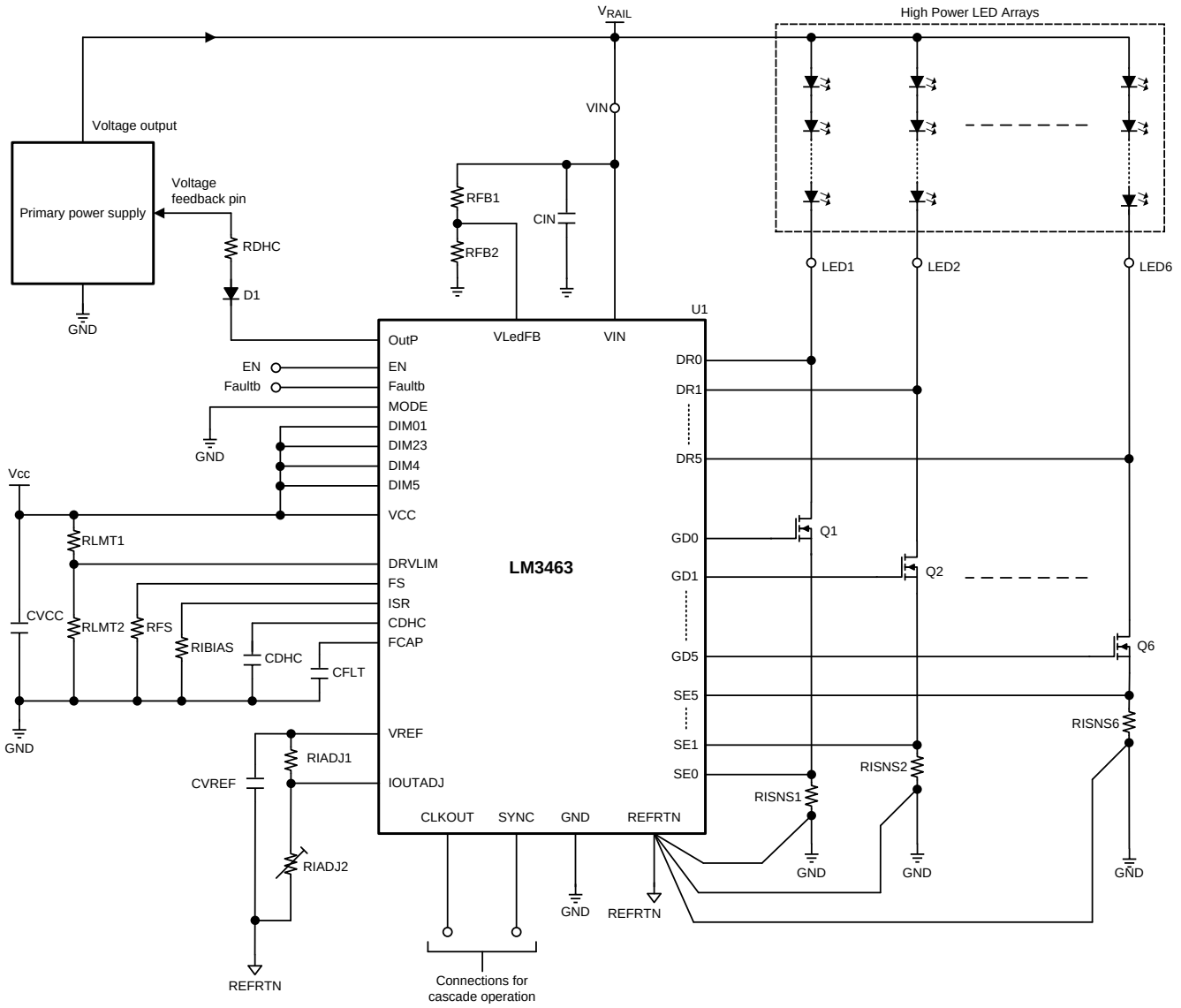


**Figure 39. White LEDs Only**

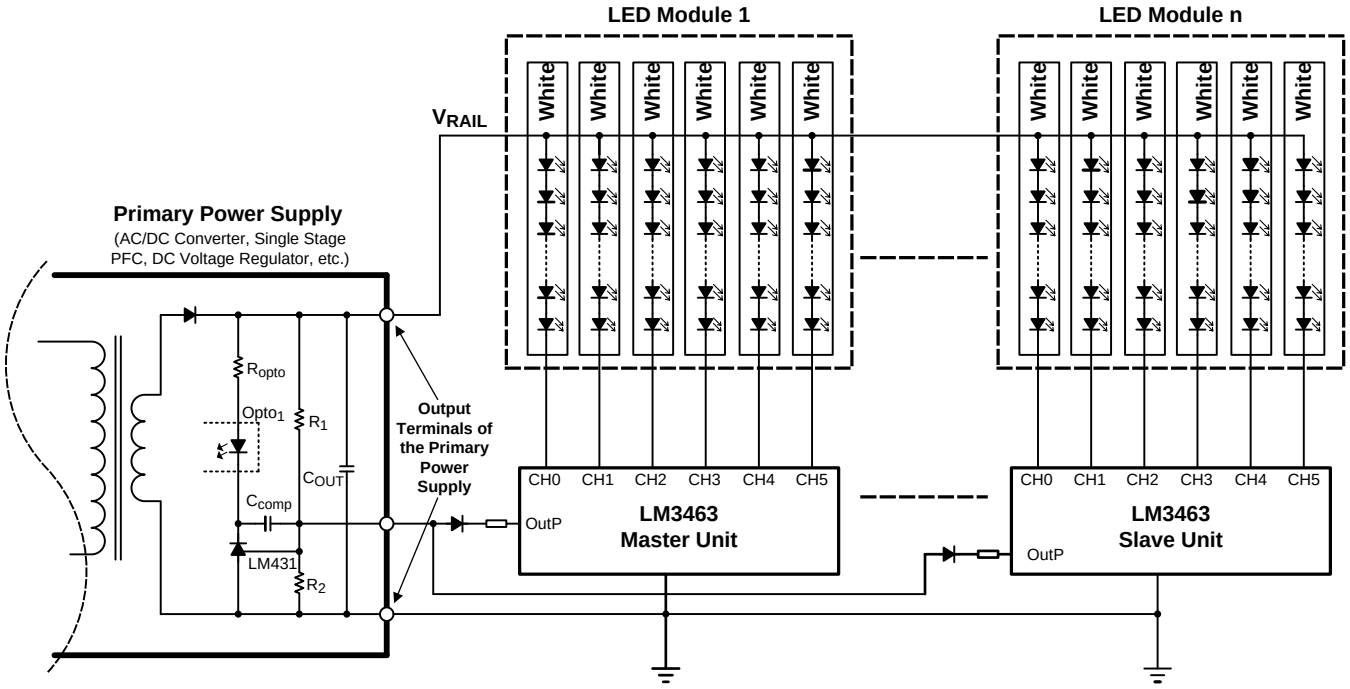



**Figure 40. White + Amber LEDs for Color Temperature Adjustment**

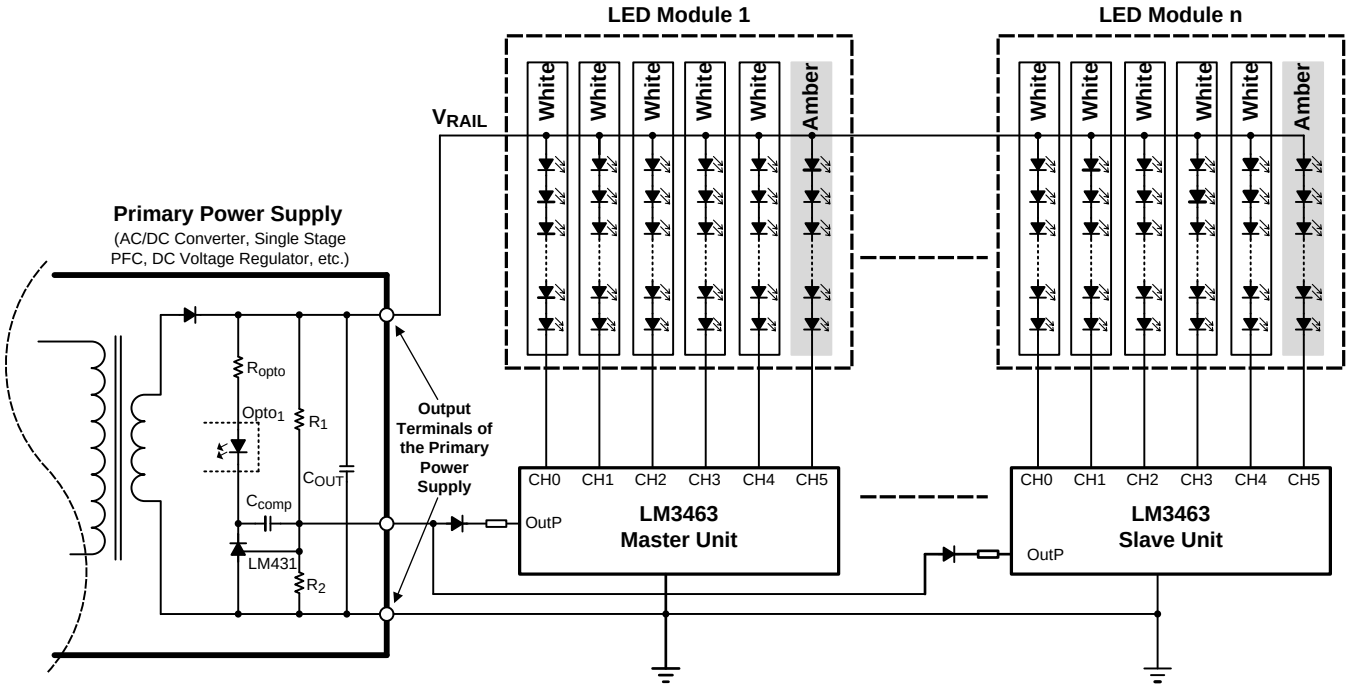


**Figure 41. White + Red + Green LEDs for CRI Adjustment**

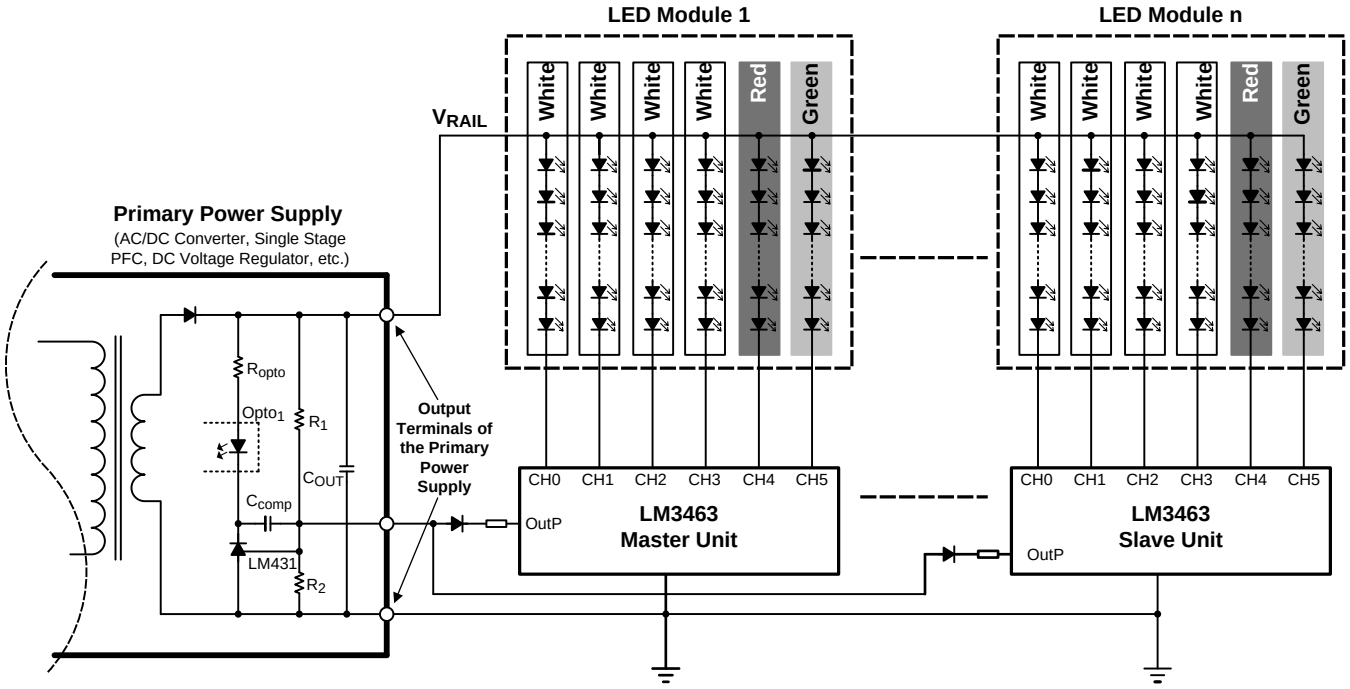
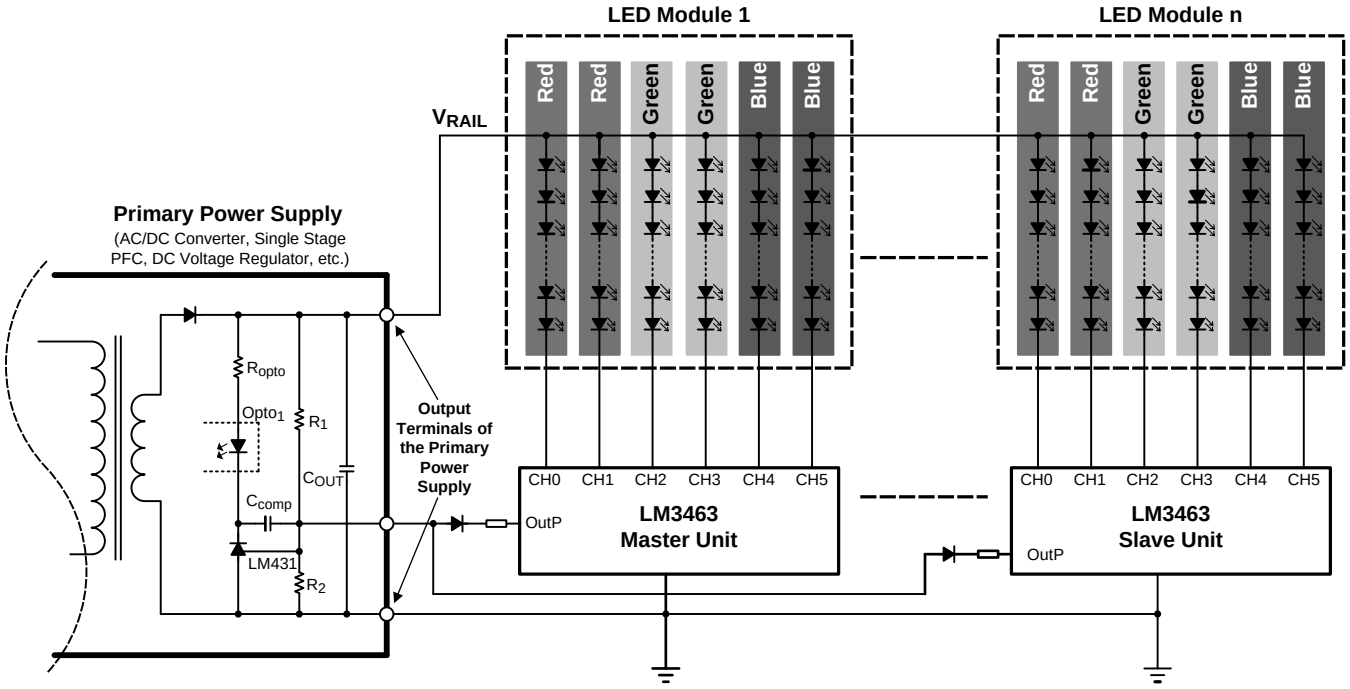



**Figure 42. Red + Green + Blue LEDs for Color Mixing**



## REVISION HISTORY

| Changes from Original (May 2013) to Revision A | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 35 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3463SQ/NOPB | ACTIVE | WQFN | RHS | 48 | 1000 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 125 | LM3463 | Samples |
| LM3463SQX/NOPB | ACTIVE | WQFN | RHS | 48 | 2500 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 125 | LM3463 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

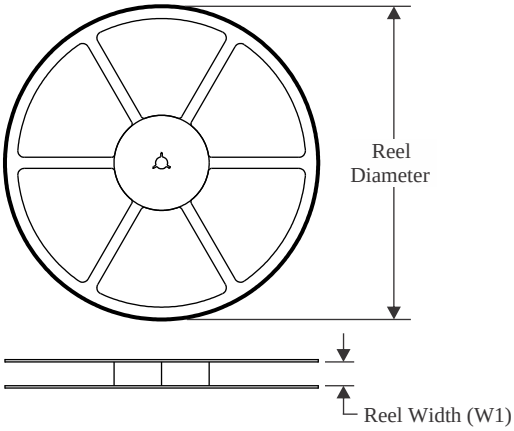
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

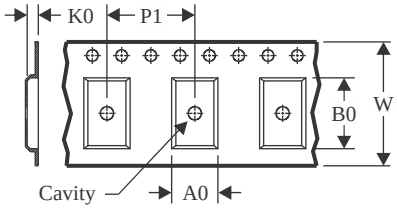
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

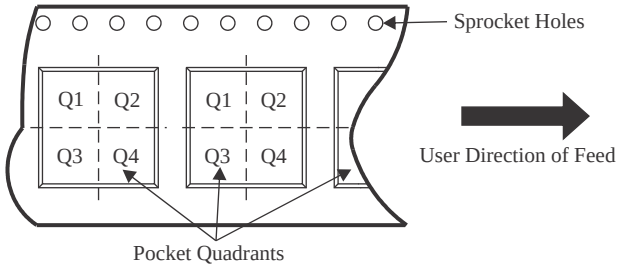



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

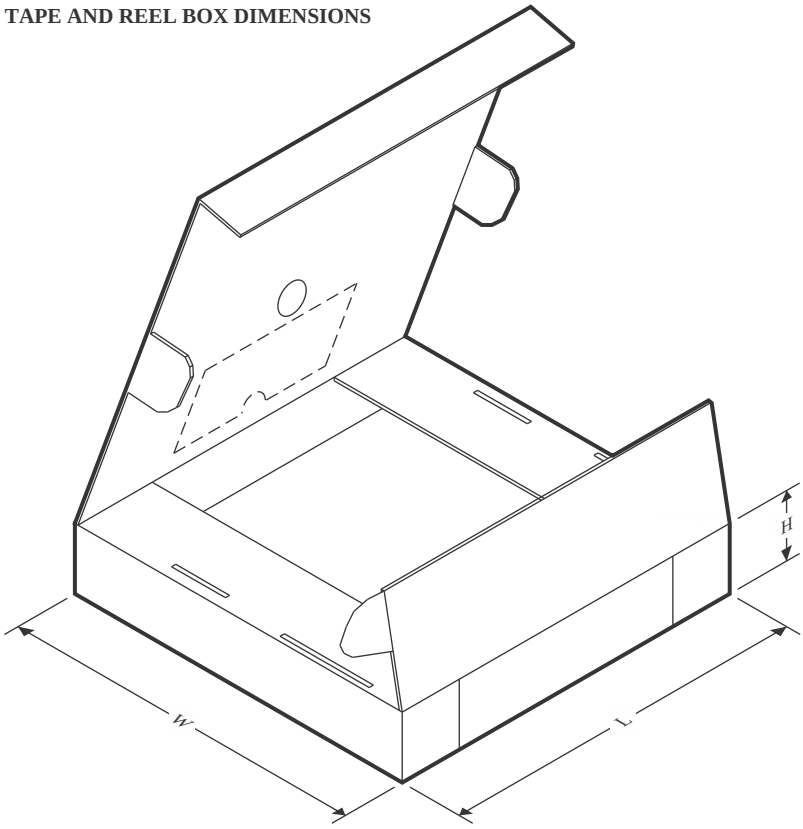
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3463SQ/NOPB | WQFN | RHS | 48 | 1000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LM3463SQX/NOPB | WQFN | RHS | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

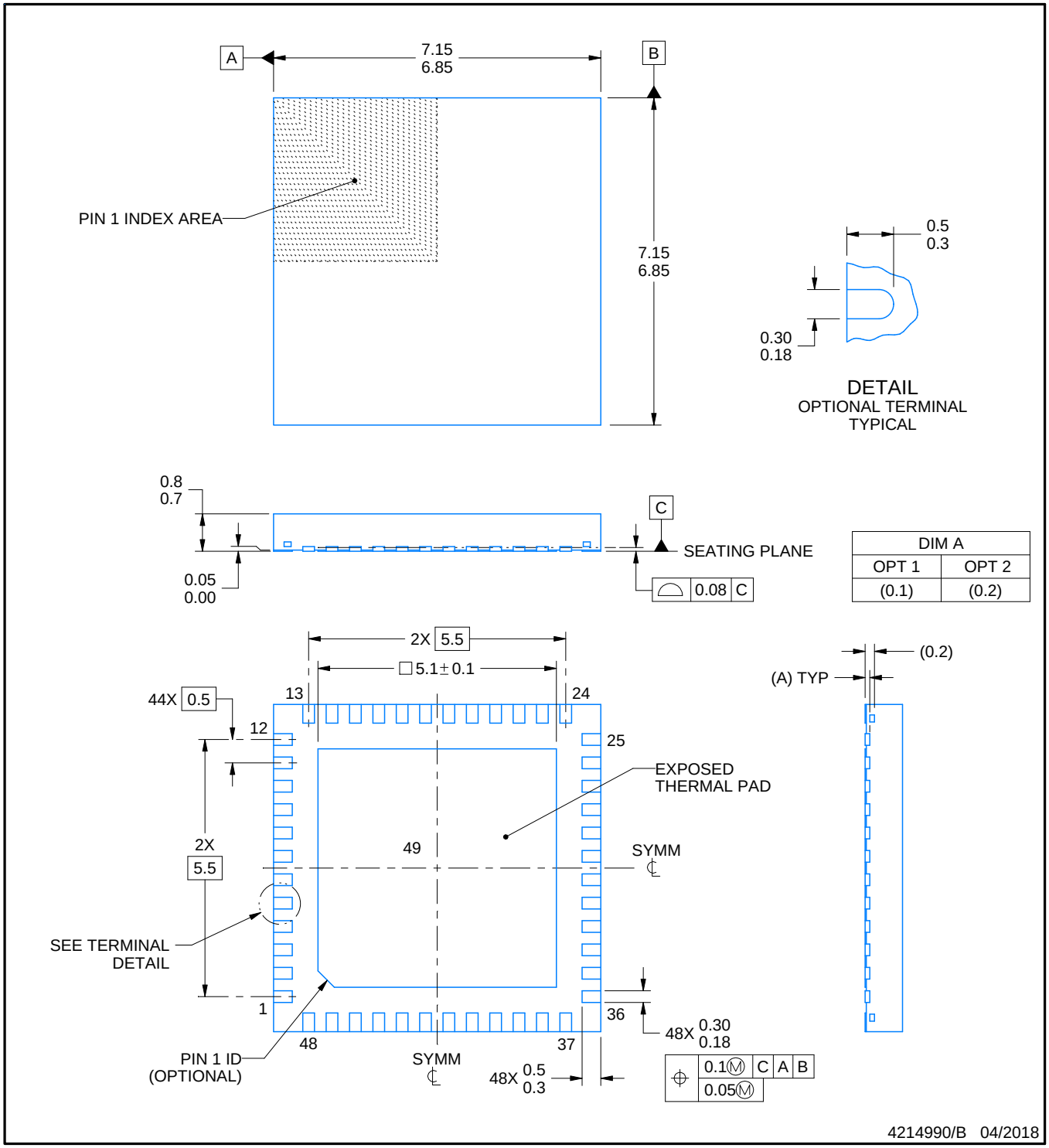
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM3463SQ/NOPB | WQFN | RHS | 48 | 1000 | 356.0 | 356.0 | 36.0 |
| LM3463SQX/NOPB | WQFN | RHS | 48 | 2500 | 356.0 | 356.0 | 36.0 |

# PACKAGE OUTLINE

## RHS0048A

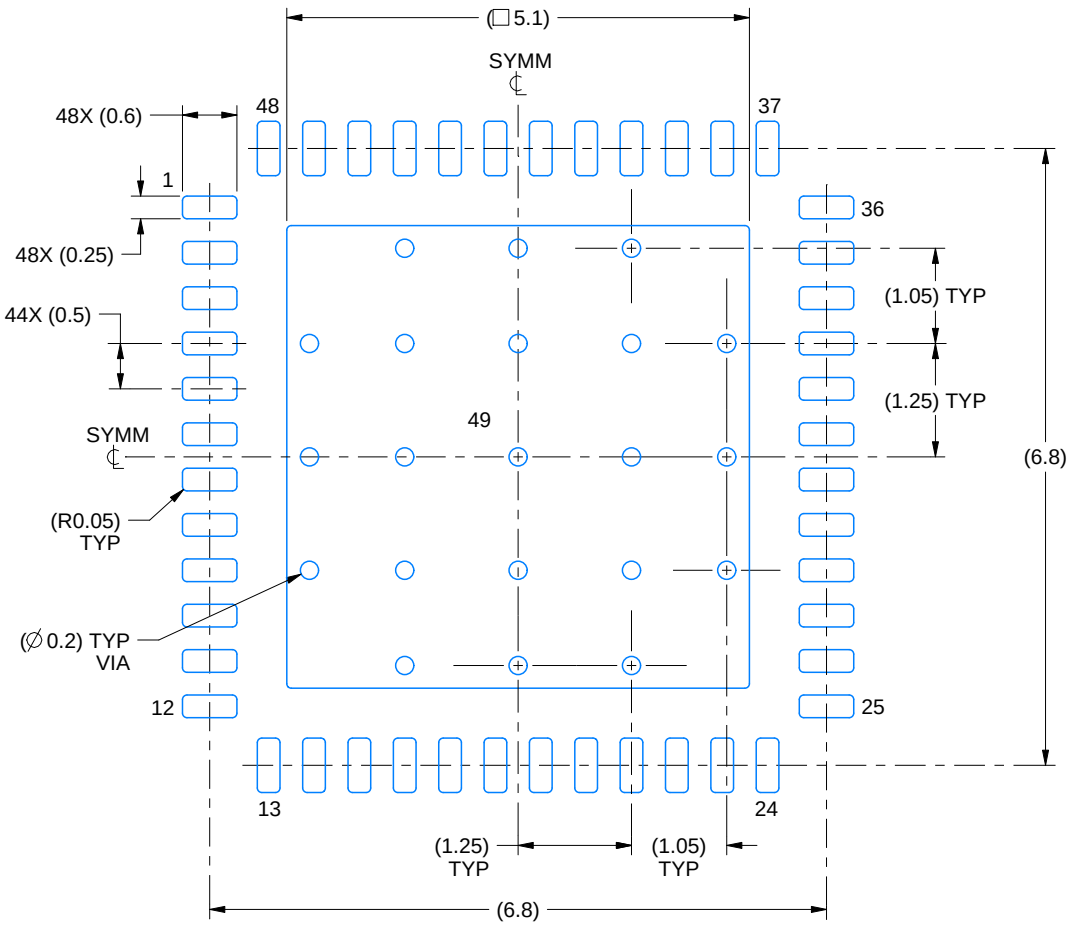
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

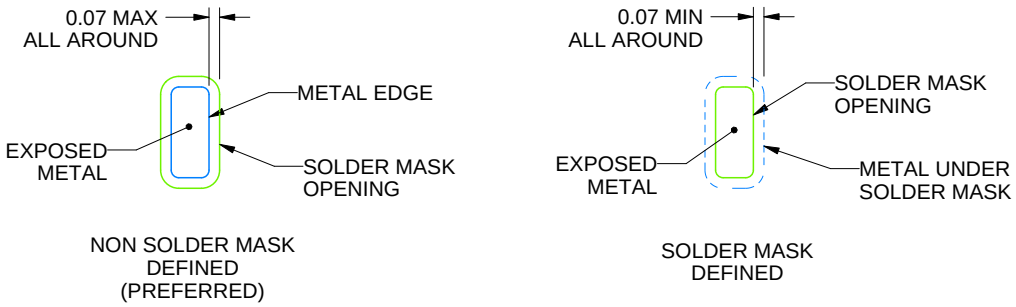



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

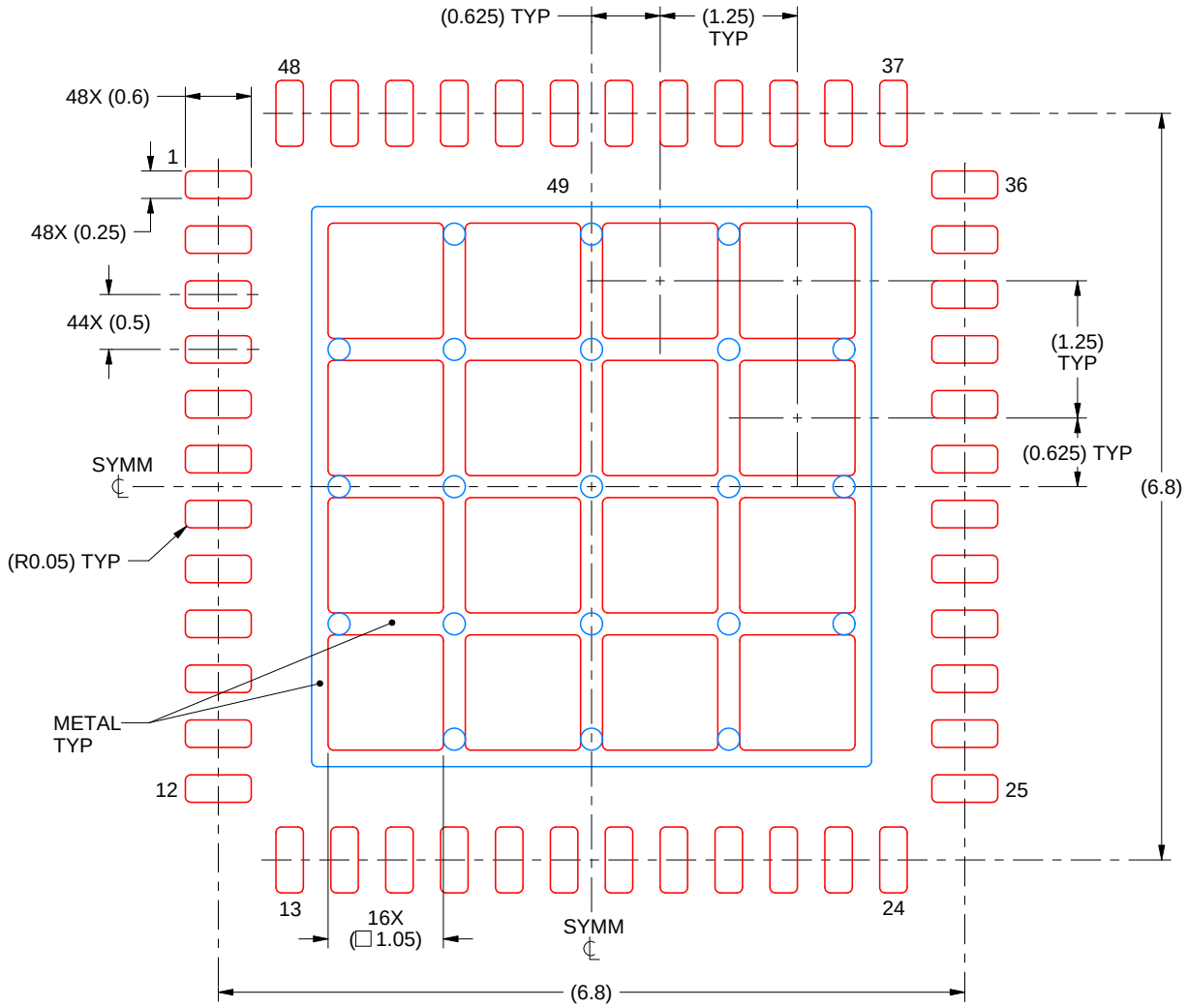



SOLDER MASK DETAILS

4214990/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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