LMH6682/6683 190MHz Single Supply, Dual and Triple Operational Amplifiers

Check for Samples: LMH6682, LMH6683

FEATURES

V_S = ±5V, T_A = 25°C, R_L = 100Ω, A = +2 (Typical Values Unless Specified)

- **DG error 0.01%**
- **DP error 0.08°**
- **−3dB BW (A = +2) 190MHz**
- **Slew rate (V_S = ±5V) 940V/μs**
- **Supply Current 6.5mA/amp**
- **Output Current +80/−90mA**
- **Input Common Mode Voltage 0.5V Beyond V^-,1.7V from V^+**
- **Output Voltage Swing (R_L = 2kΩ) 0.8V from Rails**
- **Input Voltage Noise (100KHz) 12nV/$\sqrt{Hz}$**

APPLICATIONS

- **CD/DVD ROM**
- **ADC Buffer Amp**
- **Portable Video**
- **Current Sense Buffer**
- **Portable Communications**

DESCRIPTION

The LMH6682 and LMH6683 are high speed operational amplifiers designed for use in modern video systems. These single supply monolithic amplifiers extend TI's feature-rich, high value video portfolio to include a dual and a triple version. The important video specifications of differential gain (± 0.01% typ.) and differential phase (±0.08 degrees) combined with an output drive current in each amplifier of 85mA make the LMH6682 and LMH6683 excellent choices for a full range of video applications.

Voltage feedback topology in operational amplifiers assures maximum flexibility and ease of use in high speed amplifier designs. The LMH6682/83 is fabricated in TI's VIP10 process. This advanced process provides a superior ratio of speed to quiescent current consumption and assures the user of high-value amplifier designs. Advanced technology and circuit design enables in these amplifiers a −3db bandwidth of 190MHz, a slew rate of 940V/μsec, and stability for gains of less than −1 and greater than +2.

The input stage design of the LM6682/83 enables an input signal range that extends below the negative rail. The output stage voltage range reaches to within 0.8V of either rail when driving a 2kΩ load. Other attractive features include fast settling and low distortion. Other applications for these amplifiers include servo control designs. These applications are sensitive to amplifiers that exhibit phase reversal when the inputs exceed the rated voltage range. The LMH6682/83 amplifiers are designed to be immune to phase reversal when the specified input range is exceeded. See applications section. This feature makes for design simplicity and flexibility in many industrial applications.

The LMH6682 dual operational amplifier is offered in miniature surface mount packages, SOIC-8, and VSSOP-8. The LMH6683 triple amplifier is offered in SOIC-14 and TSSOP-14.

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Connection Diagram

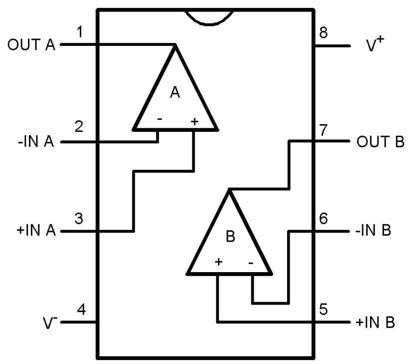

Figure 1. SOIC-8/VSSOP-8 (LMH6682) Top View

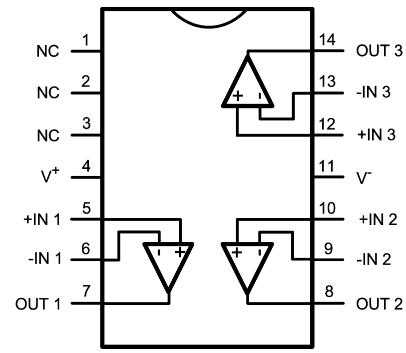

Figure 2. SOIC-14/TSSOP-14 (LMH6683) Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance	Human Body Model	2KV(3)
	Machine Model	200V(4)
V_{IN} Differential		±2.5V
Output Short Circuit Duration		See(5)(6)
Input Current		±10mA
Supply Voltage (V^+ - V^-)		12.6V
Voltage at Input/Output pins		V^+ +0.8V, V^- −0.8V
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C
Storage Temperature Range		−65°C to +150°C
Junction Temperature(7)		+150°C

(1) Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Machine Model, 0Ω in series with 200pF.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(7) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings(1)

Supply Voltage (V^+ – V^-)		3V to 12V
Operating Temperature Range(2)		−40°C to +85°C
Package Thermal Resistance(2)	SOIC-8	190°C/W
	VSSOP-8	235°C/W
	SOIC-14	145°C/W
	TSSOP-14	155°C/W

(1) Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

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5V Electrical Characteristics

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_O = V_{CM} = $V^+/2$, and R_L = 100Ω to $V^+/2$, R_F = 510Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
SSBW	−3dB BW	A = +2, V_{OUT} = 200mV_{PP}	140	180		MHz
		A = −1, V_{OUT} = 200mV_{PP}		180		
GFP	Gain Flatness Peaking	A = +2, V_{OUT} = 200mV_{PP} DC to 100MHz		2.1		dB
GFR	Gain Flatness Rolloff	A = +2, V_{OUT} = 200mV_{PP} DC to 100MHz		0.1		dB
LPD 1°	1° Linear Phase Deviation	A = +2, V_{OUT} = 200mV_{PP}, ±1°		40		MHz
$GF_{0.1dB}$	0.1dB Gain Flatness	A = +2, ±0.1dB, V_{OUT} = 200mV_{PP}		25		MHz
FPBW	Full Power −1dB Bandwidth	A = +2, V_{OUT} = 2V_{PP}		110		MHz
DG	Differential Gain NTSC 3.58MHz	A = +2, R_L = 150Ω to $V^+/2$ Pos video only V_{CM} = 2V		0.03		%
DP	Differential Phase NTSC 3.58MHz	A = +2, R_L = 150Ω to $V^+/2$ Pos video only V_{CM} = 2V		0.05		deg
Time Domain Response						
T_r/T_f	Rise and Fall Time	20-80%, V_O = 1V_{PP}, A_V = +2		2.1		ns
		20-80%, V_O = 1V_{PP}, A_V = −1		2		
OS	Overshoot	A = +2, V_O = 100mV_{PP}		22		%
T_s	Settling Time	V_O = 2V_{PP}, ±0.1%, A_V = +2		49		ns
SR	Slew Rate (3)	A = +2, V_{OUT} = 3V_{PP}		520		V/μs
		A = −1, V_{OUT} = 3V_{PP}		500		
Distortion and Noise Response						
HD2	2^{nd} Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 2kΩ		−60		dBc
		f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 100Ω		−61		
HD3	3^{rd} Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 2kΩ		−77		dBc
		f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 100Ω		−54		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 2kΩ		−60		dBc
		f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 100Ω		−53		
e_n	Input Referred Voltage Noise	f = 1kHz		17		nV/√Hz
		f = 100kHz		12		
i_n	Input Referred Current Noise	f = 1kHz		8		pA/√Hz
		f = 100kHz		3		
CT	Cross-Talk Rejection (Amplifier)	f = 5MHz, A = +2, SND: R_L = 100Ω RCV: R_F = R_G = 510Ω		−77		dB
Static, DC Performance						
A_{VOL}	Large Signal Voltage Gain	V_O = 1.25V to 3.75V, R_L = 2kΩ to $V^+/2$	85	95		dB
		V_O = 1.5V to 3.5V, R_L = 150Ω to $V^+/2$	75	85		
		V_O = 2V to 3V, R_L = 50Ω to $V^+/2$	70	80		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB	−0.2 **−0.1**	−0.5		V
			3.0 **2.8**	3.3		

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_O = V_{CM} = V^+/2, and R_L = 100Ω to V^+/2, R_F = 510Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			±1.1	±5 **±7**	mV
TC V_{OS}	Input Offset Voltage Average Drift	See (4)		±2		μV/°C
I_B	Input Bias Current	See (5)		−5	−20 **−30**	μA
TC $_{IB}$	Input Bias Current Drift			0.01		nA/°C
I_{OS}	Input Offset Current			50	300 **500**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.0V	72	82		dB
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 4.5V to 5.5V, V_{CM} = 1V	70	76		dB
I_S	Supply Current (per channel)	No load		6.5	9 **11**	mA
Miscellaneous Performance						
V_O	Output Swing High	R_L = 2kΩ to V^+/2	4.10 **3.8**	4.25		V
		R_L = 150Ω to V^+/2	3.90 **3.70**	4.19		
		R_L = 75Ω to V^+/2	3.75 **3.50**	4.15		
	Output Swing Low	R_L = 2kΩ to V^+/2		800	920 **1100**	mV
		R_L = 150Ω to V^+/2		870	970 **1200**	
		R_L = 75Ω to V^+/2		885	1100 **1250**	
I_{OUT}	Output Current	V_O = 1V from either supply rail	±40	+80/−75		mA
I_{SC}	Output Short Circuit Current (6) (7) (8)	Sourcing to V^+/2	−100 **−80**	−155		mA
		Sinking from V^+/2	100 **80**	220		
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			1.6		pF
R_{OUT}	Output Resistance Closed Loop	f = 1kHz, A = +2, R_L = 50Ω		0.02		Ω
		f = 1MHz, A = +2, R_L = 50Ω		0.12		

(4) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Short circuit test is a momentary test. See next note.
(7) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(8) Positive current corresponds to current flowing into the device.

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±5V Electrical Characteristics

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_O = V_{CM} = 0V, and R_L = 100Ω to 0V, R_F = 510Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
SSBW	−3dB BW	A = +2, V_{OUT} = 200mV_{PP}	150	190		MHz
		A = −1, V_{OUT} = 200mV_{PP}		190		
GFP	Gain Flatness Peaking	A = +2, V_{OUT} = 200mV_{PP} DC to 100MHz		1.7		dB
GFR	Gain Flatness Rolloff	A = +2, V_{OUT} = 200mV_{PP} DC to 100MHz		0.1		dB
LPD 1°	1° Linear Phase Deviation	A = +2, V_{OUT} = 200mV_{PP}, ±1°		40		MHz
$GF_{0.1dB}$	0.1dB Gain Flatness	A = +2, ±0.1dB, V_{OUT} = 200mV_{PP}		25		MHz
FPBW	Full Power −1dB Bandwidth	A = +2, V_{OUT} = 2V_{PP}		120		MHz
DG	Differential Gain NTSC 3.58MHz	A = +2, R_L = 150Ω to 0V		0.01		%
DP	Differential Phase NTSC 3.58MHz	A = +2, R_L = 150Ω to 0V		0.08		deg
Time Domain Response						
T_r/T_f	Rise and Fall Time	20-80%, V_O = 1V_{PP}, A = +2		1.9		ns
		20-80%, V_O = 1V_{PP}, A = −1		2		
OS	Overshoot	A = +2, V_O = 100mV_{PP}		19		%
T_s	Settling Time	V_O = 2V_{PP}, ±0.1%, A = +2		42		ns
SR	Slew Rate (3)	A = +2, V_{OUT} = 6V_{PP}		940		V/μs
		A = −1, V_{OUT} = 6V_{PP}		900		
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 2kΩ		−63		dBc
		f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 100Ω		−66		
HD3	3rd Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 2kΩ		−82		dBc
		f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 100Ω		−54		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 2kΩ		−63		dBc
		f = 5MHz, V_O = 2V_{PP}, A = +2, R_L = 100Ω		−54		
e_n	Input Referred Voltage Noise	f = 1kHz		18		nV/√Hz
		f = 100kHz		12		
i_n	Input Referred Current Noise	f = 1kHz		6		pA/√Hz
		f = 100kHz		3		
CT	Cross-Talk Rejection (Amplifier)	f = 5MHz, A = +2, SND: R_L = 100Ω RCV: R_F = R_G = 510Ω		−78		dB
Static, DC Performance						
A_{VOL}	Large Signal Voltage Gain	V_O = −3.75V to 3.75V, R_L = 2kΩ to V^+/2	87	100		dB
		V_O = −3.5V to 3.5V, R_L = 150Ω to V^+/2	80	90		
		V_O = −3V to 3V, R_L = 50Ω to V^+/2	75	85		
CMVR	Input Common Mode Voltage Range	CMRR ≥ 50dB	−5.2 **−5.1**	−5.5		V
			3.0 **2.8**	3.3		

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_O = V_{CM} = 0V, and R_L = 100Ω to 0V, R_F = 510Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [1]	Typ [2]	Max [1]	Units
V_{OS}	Input Offset Voltage			±1	±5 **±7**	mV
TC V_{OS}	Input Offset Voltage Average Drift	See [4]		±2		μV/°C
I_B	Input Bias Current	See [5]		−5	−20 **−30**	μA
TC I_B	Input Bias Current Drift			0.01		nA/°C
I_{OS}	Input Offset Current			50	300 **500**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −5V to 3.0V	75	84		dB
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 8.5V to 9.5V, V^- = −1V	75	82		dB
−PSRR	Negative Power Supply Rejection Ratio	V^- = −4.5V to −5.5V, V^+ = 5V	78	85		dB
I_S	Supply Current (per channel)	No load		6.5	9.5 **11**	mA
Miscellaneous Performance						
V_O	Output Swing High	R_L = 2kΩ to 0V	4.10 **3.80**	4.25		V
		R_L = 150Ω to 0V	3.90 **3.70**	4.20		
		R_L = 75Ω to 0V	3.75 **3.50**	4.18		
	Output Swing Low	R_L = 2kΩ to 0V		−4.19	−4.07 **−3.80**	mV
		R_L = 150Ω to 0V		−4.05	−3.89 **−3.65**	
		R_L = 75Ω to 0V		−4.00	−3.70 **−3.50**	
I_{OUT}	Output Current	V_O = 1V from either supply rail	±45	+85/−80		mA
I_{SC}	Output Short Circuit Current [6][7][8]	Sourcing to 0V	−120 **−100**	−180		mA
		Sinking from 0V	120 **100**	230		
R_{IN}	Common Mode Input Resistance			4		MΩ
C_{IN}	Common Mode Input Capacitance			1.6		pF
R_{OUT}	Output Resistance Closed Loop	f = 1kHz, A = +2, R_L = 50Ω		0.02		Ω
		f = 1MHz, A = +2, R_L = 50Ω		0.12		

(4) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Short circuit test is a momentary test. See next note.
(7) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(8) Positive current corresponds to current flowing into the device.

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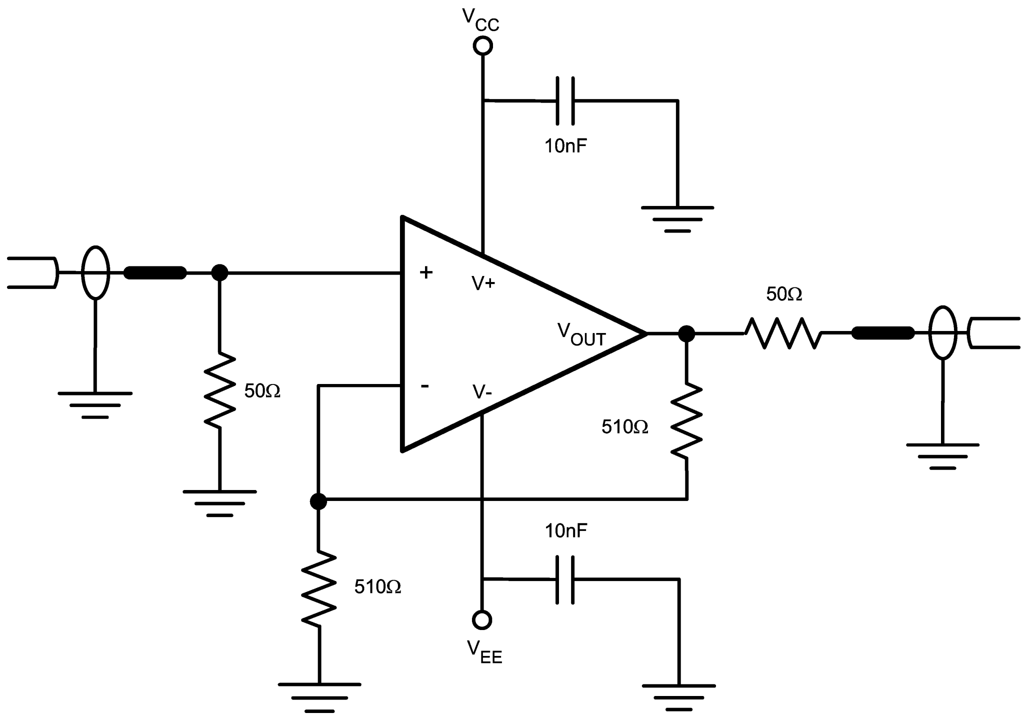
Typical Schematic



Typical Performance Characteristics

At T_A = 25°C, V^+ = +5V, V^- = −5V, R_F = 510Ω for A = +2; unless otherwise specified.

Non-Inverting Frequency Response

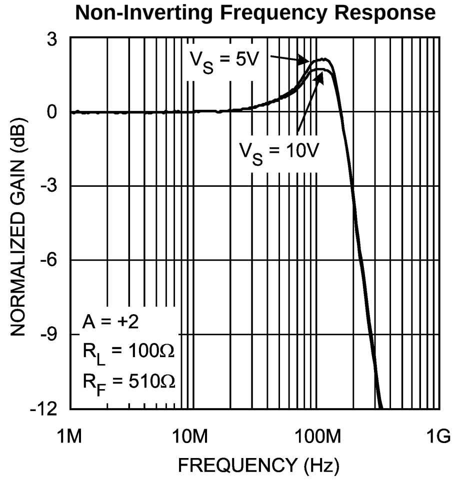


Figure 3.

Inverting Frequency Response

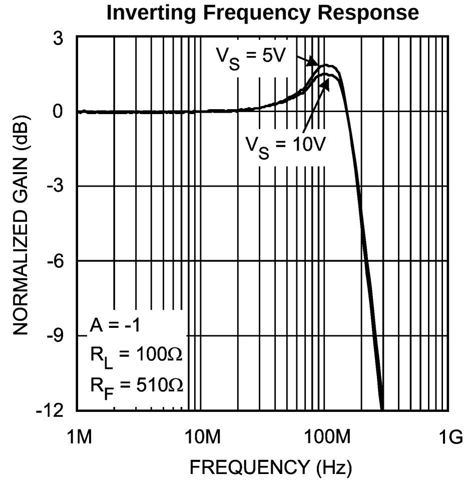


Figure 4.

Non-Inverting Frequency Response for Various Gain

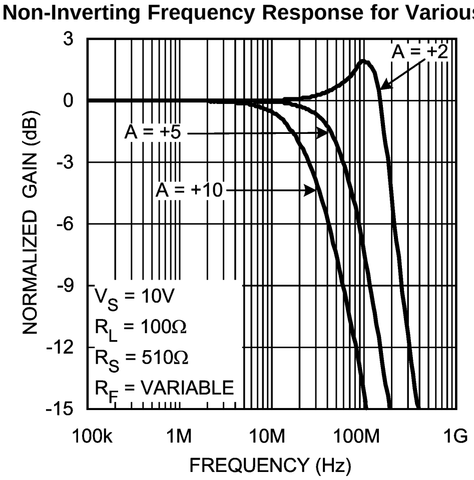


Figure 5.

Inverting Frequency Response for Various Gain

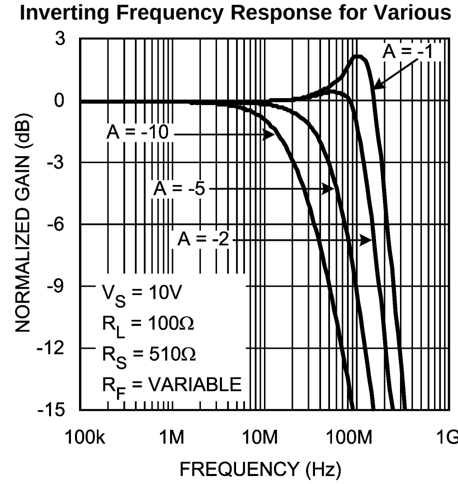


Figure 6.

Non-Inverting Phase vs. Frequency for Various Gain

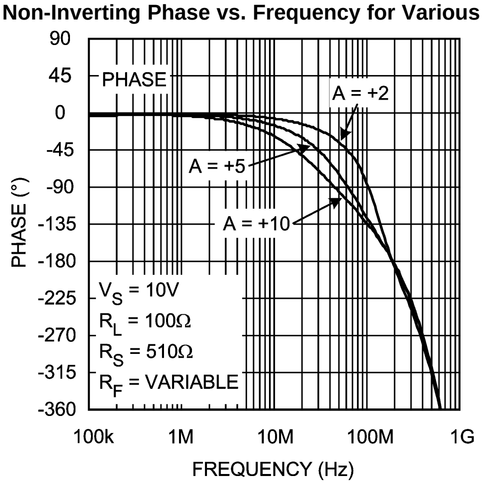


Figure 7.

Inverting Phase vs. Frequency for Various Gain

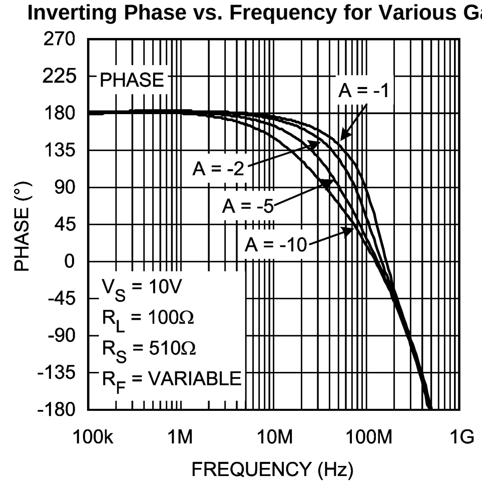


Figure 8.

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Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = +5V, V^- = −5V, R_F = 510Ω for A = +2; unless otherwise specified.

Open Loop Gain & Phase vs. Frequency

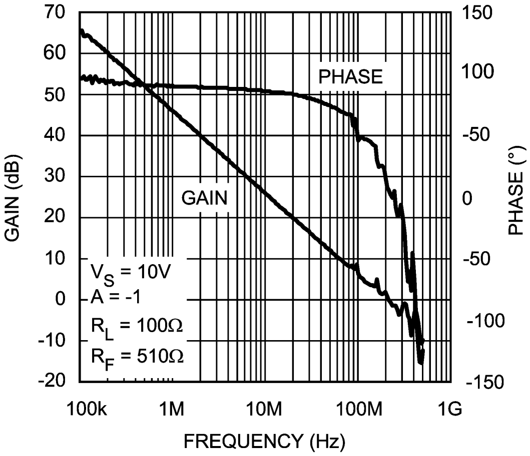

Figure 9.

Open Loop Gain and Phase vs. Frequency Over Temperature

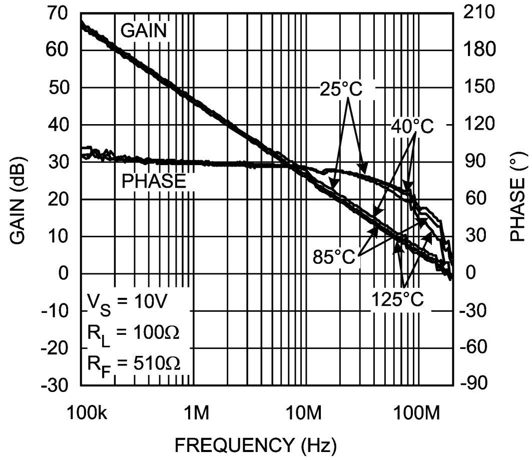

Figure 10.

Non-Inverting Frequency Response Over Temperature

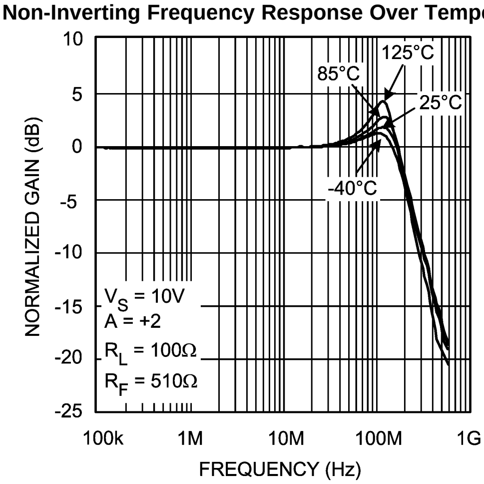

Figure 11.

Inverting Frequency Response Over Temperature

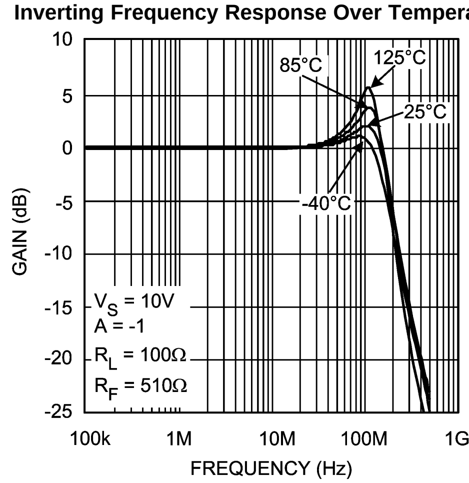

Figure 12.

Gain Flatness 0.1dB

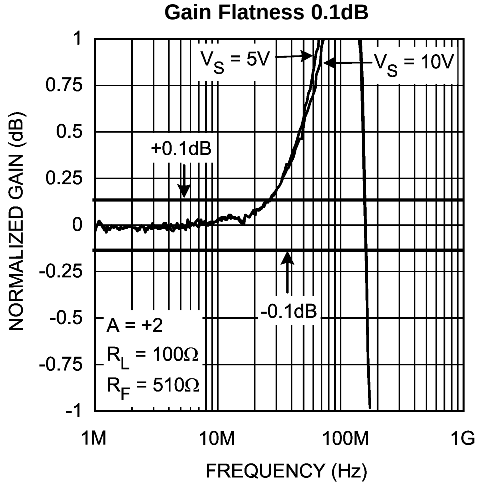

Figure 13.

Differential Gain & Phase for A = +2

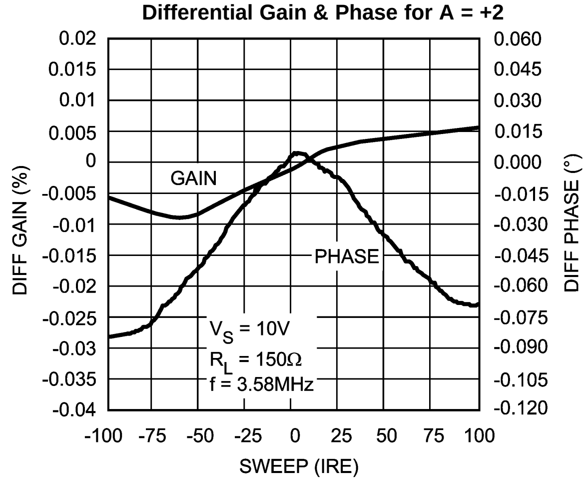

Figure 14.

Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = +5V, V^- = −5V, R_F = 510Ω for A = +2; unless otherwise specified.

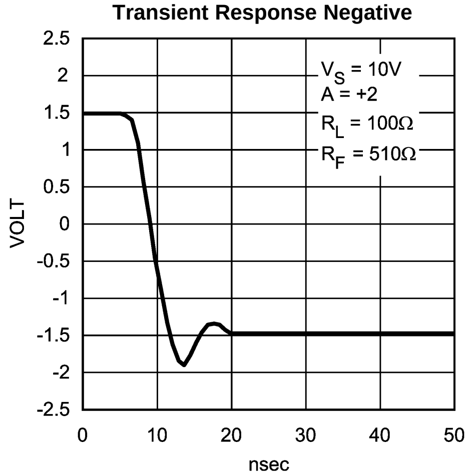

Figure 15.

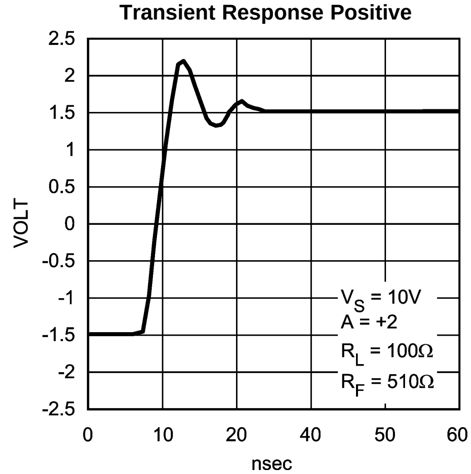

Figure 16.

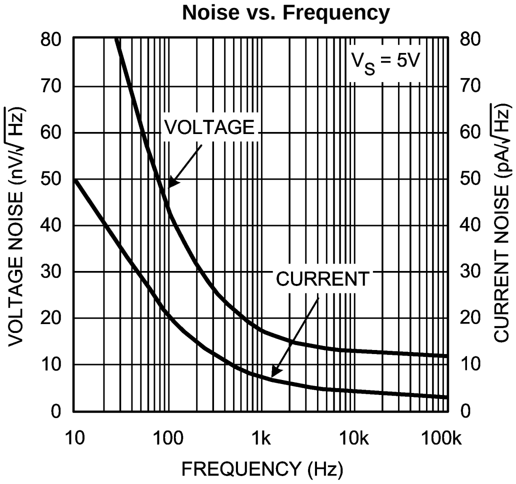

Figure 17.

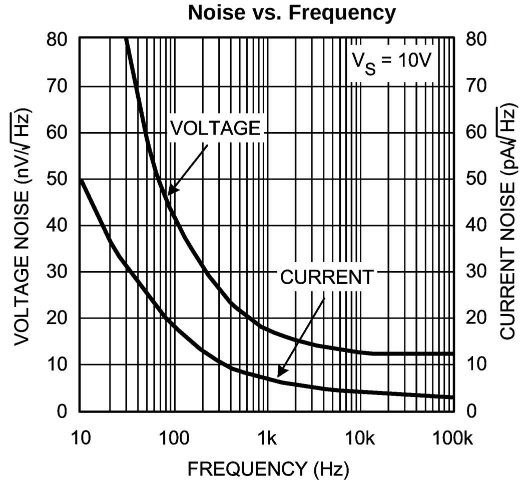

Figure 18.

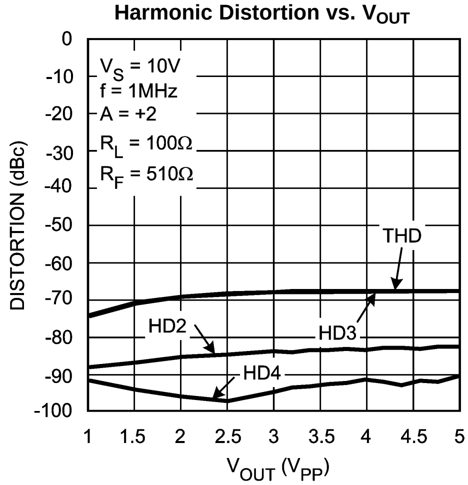

Figure 19.

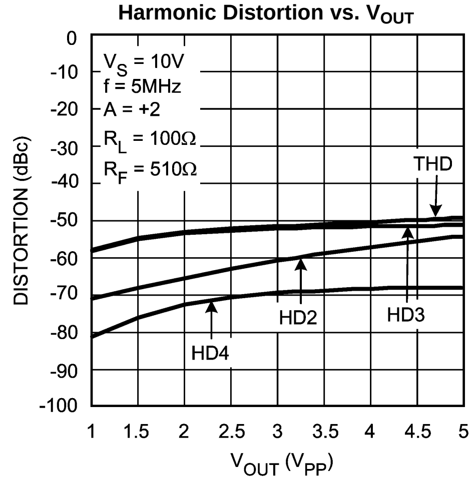

Figure 20.

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Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = +5V, V^- = −5V, R_F = 510Ω for A = +2; unless otherwise specified.

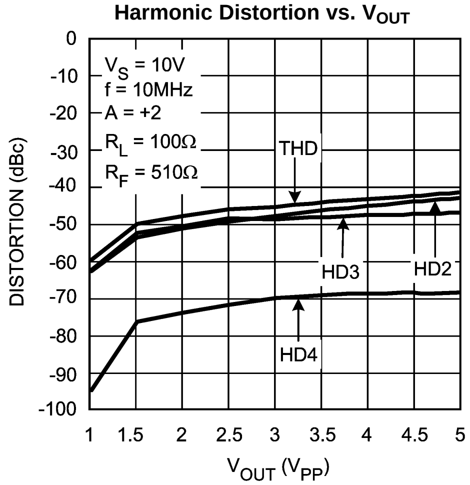
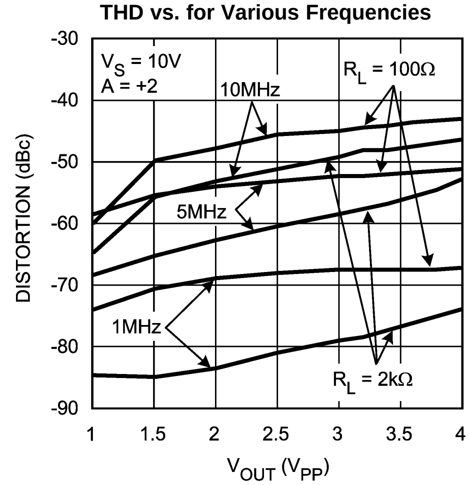


Figure 21.



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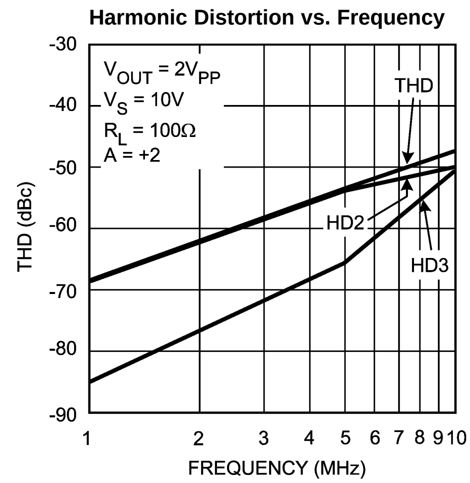

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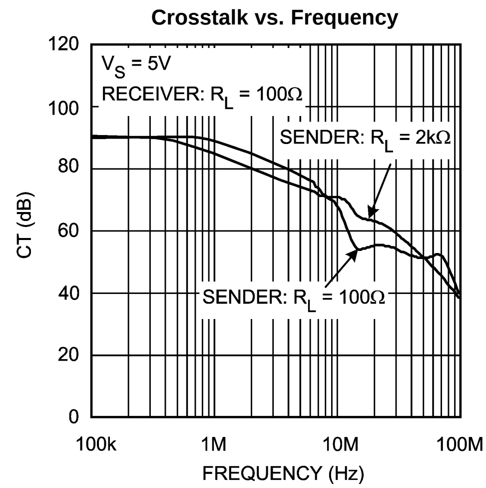

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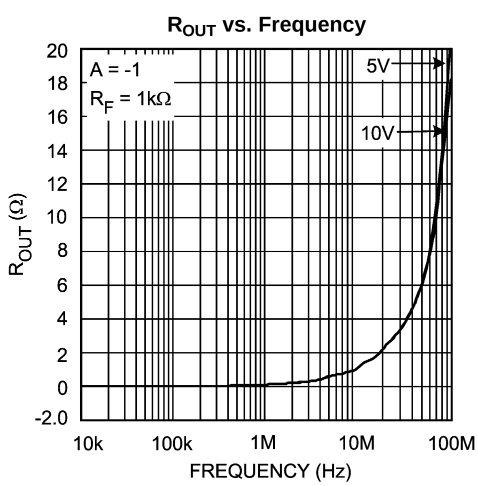

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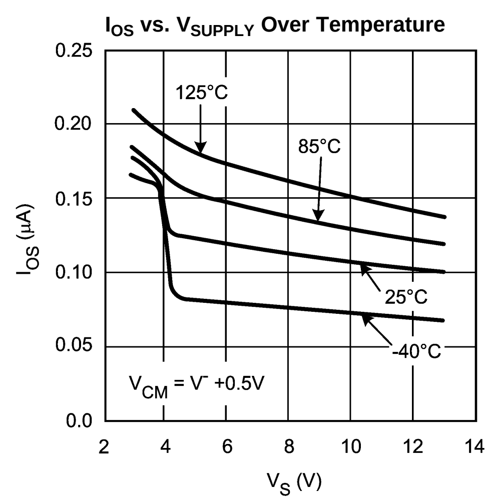


Figure 26.

Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = +5V, V^- = −5V, R_F = 510Ω for A = +2; unless otherwise specified.

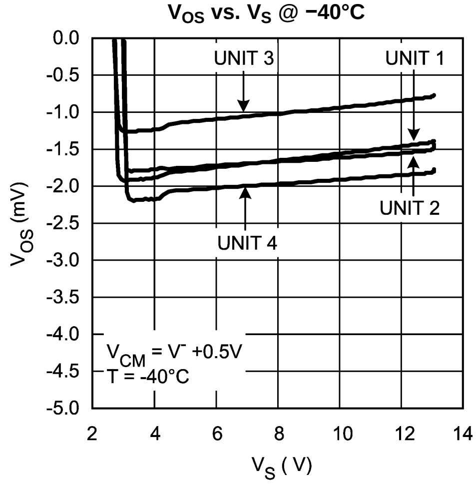
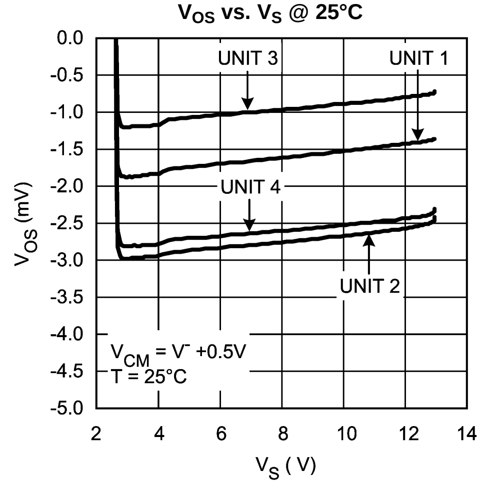


Figure 27.



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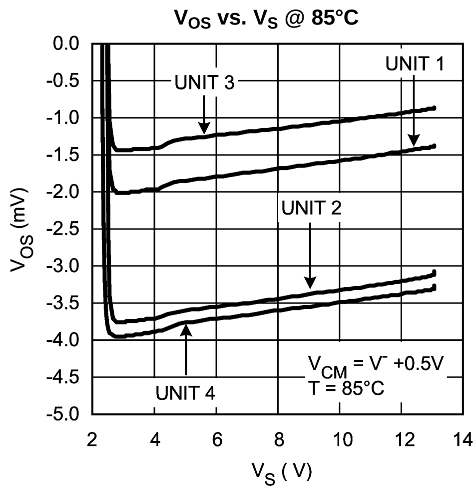
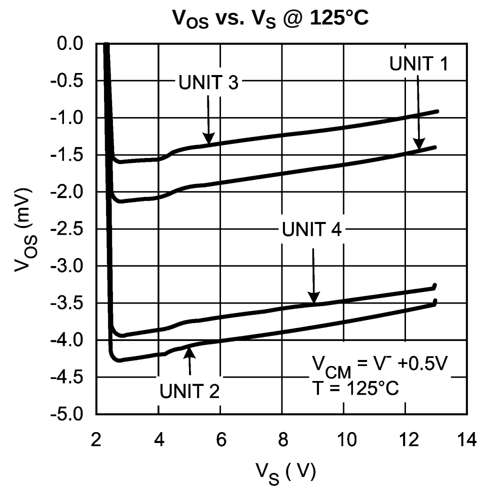


Figure 29.



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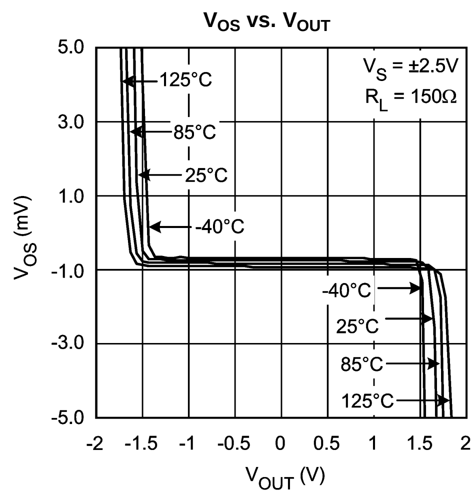

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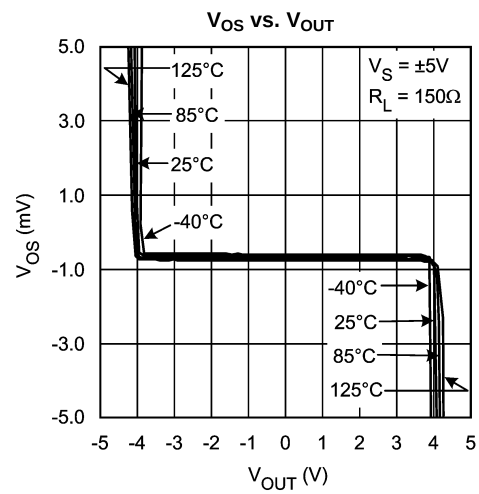

Figure 32.

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Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = +5V, V^- = −5V, R_F = 510Ω for A = +2; unless otherwise specified.

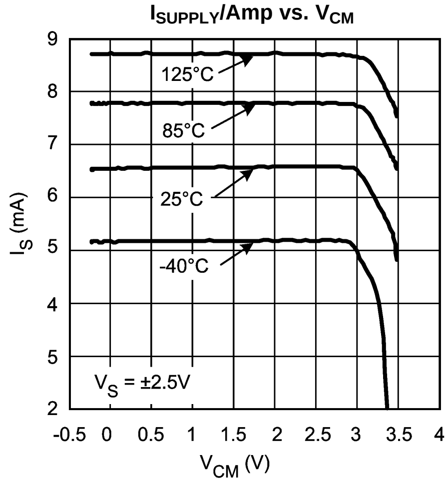
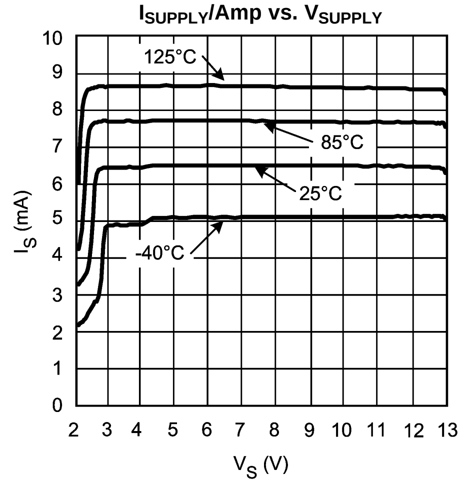


Figure 33.



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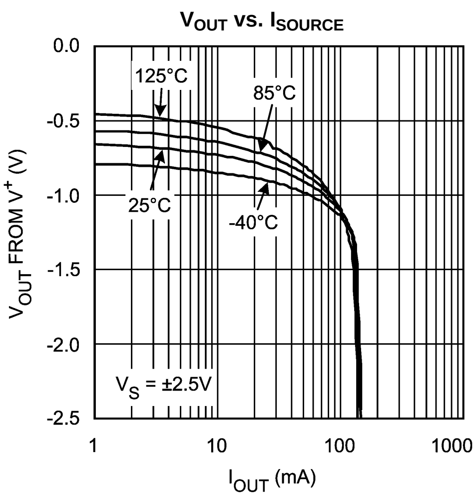

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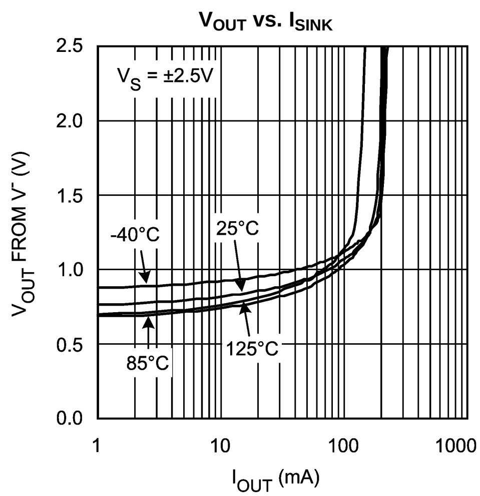

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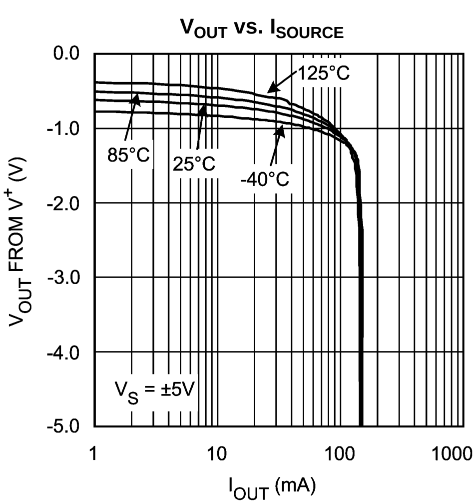

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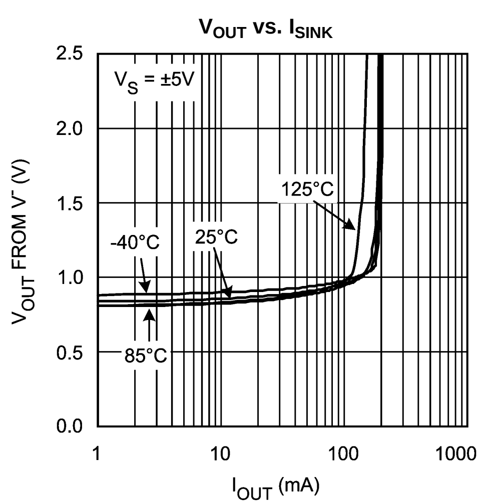


Figure 38.

Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = +5V, V^- = −5V, R_F = 510Ω for A = +2; unless otherwise specified.

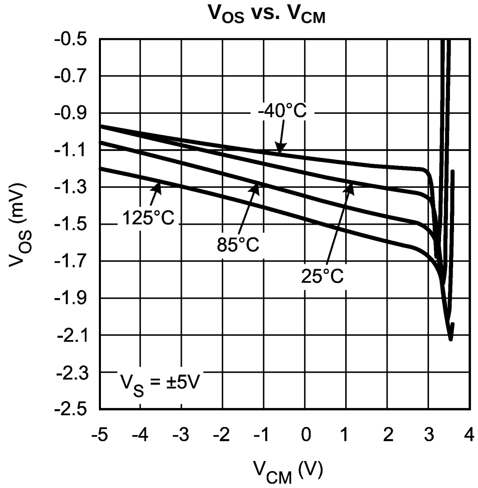


Figure 39.

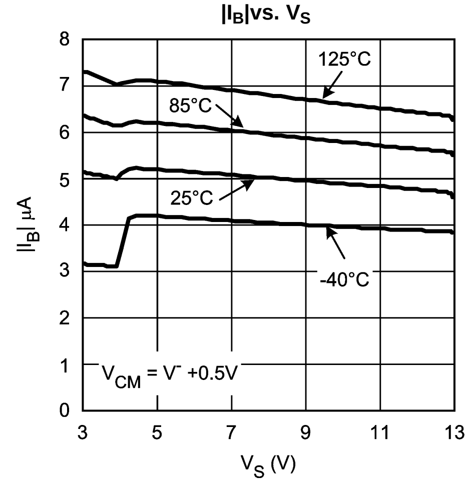


Figure 40.

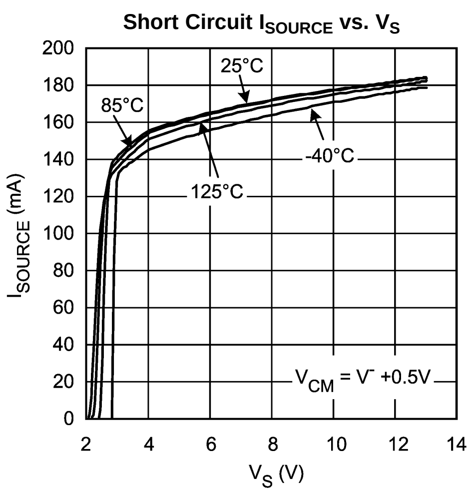
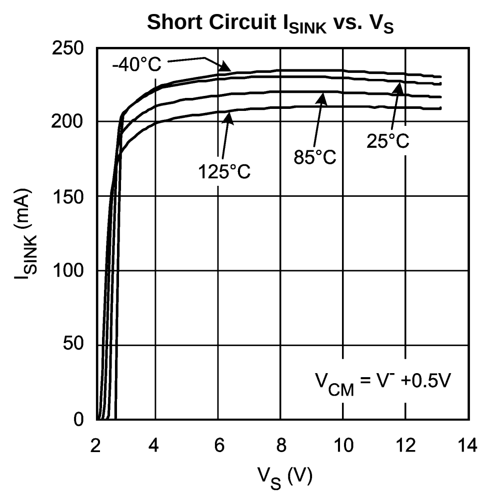


Figure 41.



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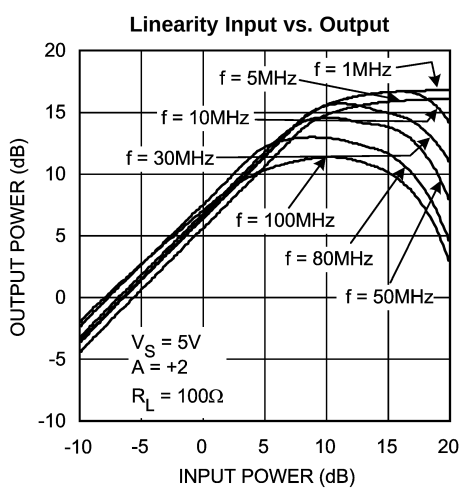

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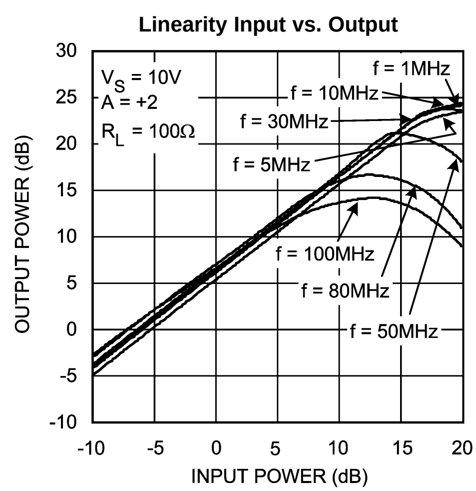

Figure 44.

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Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = +5V, V^- = −5V, R_F = 510Ω for A = +2; unless otherwise specified.

CMRR vs. Frequency

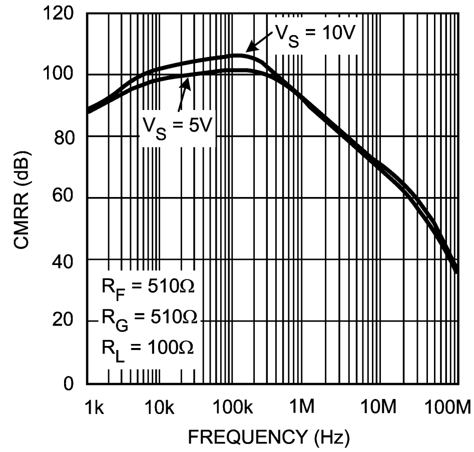

Figure 45.

PSRR vs. Frequency

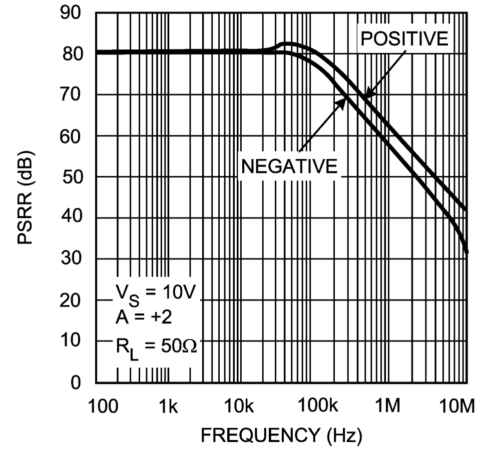

Figure 46.

Small Signal Pulse Response for A = +2

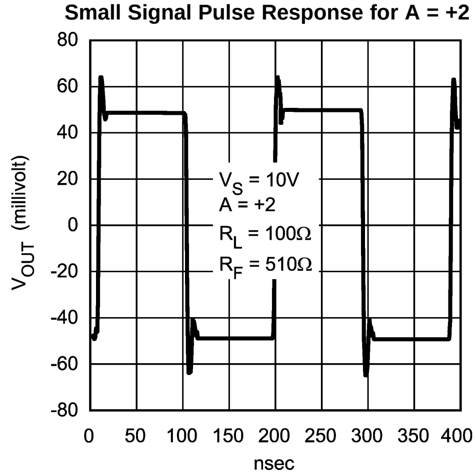

Figure 47.

Small Signal Pulse Response A = −1

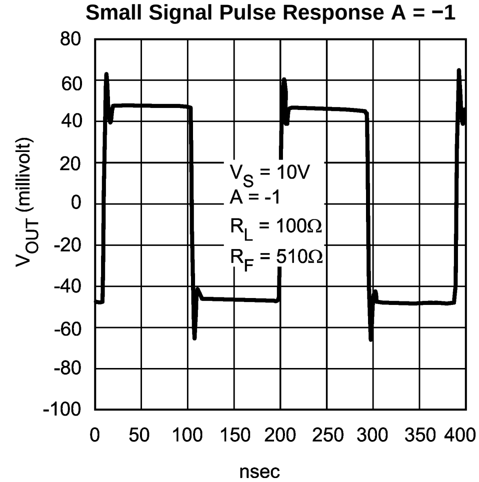

Figure 48.

Large Signal Pulse Response

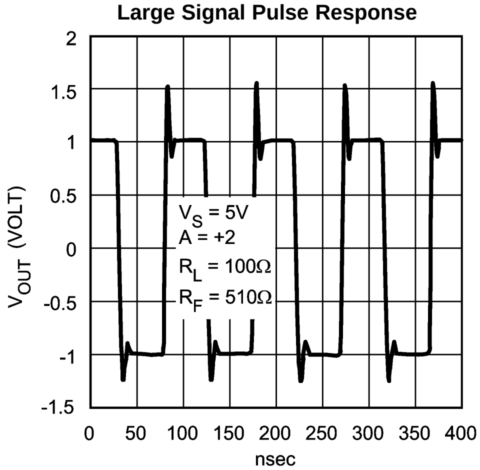

Figure 49.

Large Signal Pulse Response

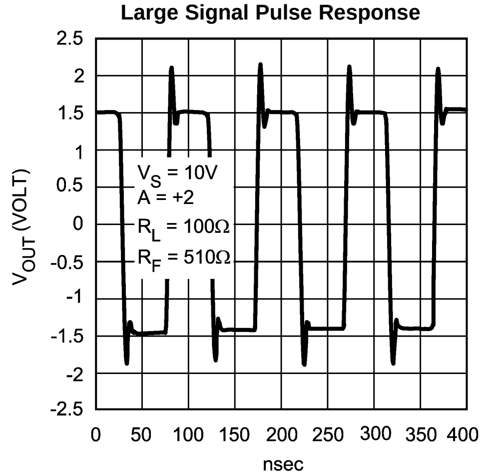

Figure 50.

APPLICATIONS SECTION

LARGE SIGNAL BEHAVIOR

Amplifying high frequency signals with large amplitudes (as in video applications) has some special aspects to look after. The bandwidth of the Op Amp for large amplitudes is less than the small signal bandwidth because of slew rate limitations. While amplifying pulse shaped signals the slew rate properties of the OpAmp become more important at higher amplitude ranges. Due to the internal structure of an Op Amp the output can only change with a limited voltage difference per time unit (dV/dt). This can be explained as follows: To keep it simple, assume that an Op Amp consists of two parts; the input stage and the output stage. In order to stabilize the Op Amp, the output stage has a compensation capacitor in its feedback path. This Miller C integrates the current from the input stage and determines the pulse response of the Op Amp. The input stage must charge/discharge the feedback capacitor, as can be seen in Figure 51.

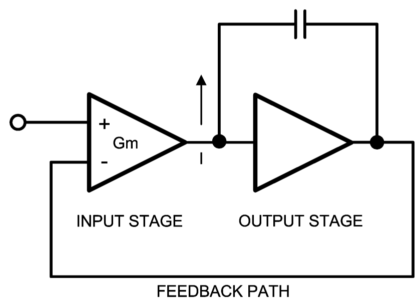

Figure 51.

When a voltage transient is applied to the non inverting input of the Op Amp, the current from the input stage will charge the capacitor and the output voltage will slope up. The overall feedback will subtract the gradually increasing output voltage from the input voltage. The decreasing differential input voltage is converted into a current by the input stage (Gm).

$$I * \Delta t = C * \Delta V \quad (1)$$

$$\Delta V / \Delta t = I / C \quad (2)$$

$$I = \Delta V * Gm \quad (3)$$

where I = current

t = time

C = capacitance

V = voltage

Gm = transconductance

Slew rate ΔV/Δt = volt/second

In most amplifier designs the current I is limited for high differential voltages (Gm becomes zero). The slew rate will than be limited as well:

$$\Delta V / \Delta t = I_{max} / C \quad (4)$$

The LMH6682/83 has a different setup of the input stage. It has the property to deliver more current to the output stage when the input voltage is higher (class AB input). The current into the Miller capacitor exhibits an exponential character, while this current in other Op Amp designs reaches a saturation level at high input levels: (see Figure 52)

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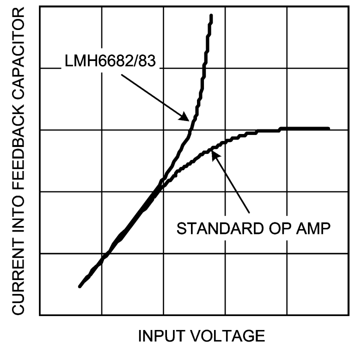

Figure 52.

This property of the LMH6682/83 guaranties a higher slew rate at higher differential input voltages.

$$\Delta V/\Delta t = \Delta V^{*}Gm/C \tag{5}$$

In Figure 53 one can see that a higher transient voltage than will lead to a higher slew rate.

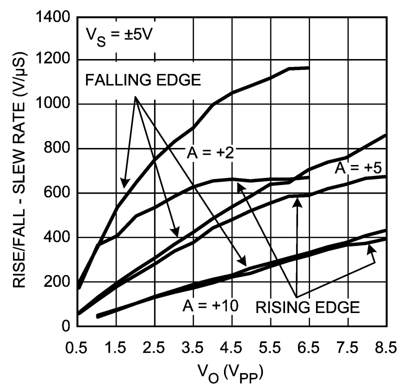

Figure 53.

HANDLING VIDEO SIGNALS

When handling video signals, two aspects are very important especially when cascading amplifiers in a NTSC- or PAL video system. A composite video signal consists of both amplitude and phase information. The amplitude represents saturation while phase determines color (color burst is 3.59MHz for NTSC and 4.58MHz for PAL systems). In this case it is not only important to have an accurate amplification of the amplitude but also it is important not to add a varying phase shift to the video signals. It is a known phenomena that at different dc levels over a certain load the phase of the amplified signal will vary a little bit. In a video chain many amplifiers will be cascaded and all errors will be added together. For this reason, it is necessary to have strict requirements for the variation in gain and phase in conjunction to different dc levels. As can be seen in the tables the number for the differential gain for the LMH6682/83 is only 0.01% and for the differential phase it is only 0.08° at a supply voltage of ±5V. Note that the phase is very dependent of the load resistance, mainly because of the dc current delivered by the parts output stage into the load. For more information about differential gain and phase and how to measure it see Application Note OA-24 SNOA370 which can be found on via TI's home page http://www.ti.com

OUTPUT PHASE REVERSAL

This is a problem with some operational amplifiers. This effect is caused by phase reversal in the input stage due to saturation of one or more of the transistors when the inputs exceed the normal expected range of voltages. Some applications, such as servo control loops among others, are sensitive to this kind of behavior and would need special safeguards to ensure proper functioning. The LMH6682/6683 is immune to output phase reversal with input overload. With inputs exceeded, the LMH6682/6683 output will stay at the clamped voltage from the supply rail. Exceeding the input supply voltages beyond the Absolute Maximum Ratings of the device could however damage or otherwise adversely effect the reliability or life of the device.

DRIVING CAPACITIVE LOADS

The LMH6682/6683 can drive moderate values of capacitance by utilizing a series isolation resistor between the output and the capacitive load. Capacitive load tolerance will improve with higher closed loop gain values. Applications such as ADC buffers, among others, present complex and varying capacitive loads to the Op Amp; best value for this isolation resistance is often found by experimentation and actual trial and error for each application.

DISTORTION

Applications with demanding distortion performance requirements are best served with the device operating in the inverting mode. The reason for this is that in the inverting configuration, the input common mode voltage does not vary with the signal and there is no subsequent ill effects due to this shift in operating point and the possibility of additional non-linearity. Moreover, under low closed loop gain settings (most suited to low distortion), the non-inverting configuration is at a further disadvantage of having to contend with the input common voltage range. There is also a strong relationship between output loading and distortion performance (i.e. 2kΩ vs. 100Ω distortion improves by about 15dB @1MHz) especially at the lower frequency end where the distortion tends to be lower. At higher frequency, this dependence diminishes greatly such that this difference is only about 5dB at 10MHz. But, in general, lighter output load leads to reduced HD3 term and thus improves THD. (See Harmonic Distortion plots, Figures 19 through 23).

PRINTED CIRCUIT BOARD LAYOUT AND COMPONENT VALUES SELECTION

Generally it is a good idea to keep in mind that for a good high frequency design both the active parts and the passive ones are suitable for the purpose you are using them for. Amplifying frequencies of several hundreds of MHz is possible while using standard resistors but it makes life much easier when using surface mount ones. These resistors (and capacitors) are smaller and therefore parasitics have lower values and will have less influence on the properties of the amplifier. Another important issue is the PCB, which is no longer a simple carrier for all the parts and a medium to interconnect them. The board becomes a real part itself, adding its own high frequency properties to the overall performance of the circuit. It's good practice to have at least one ground plane on a PCB giving a low impedance path for all decouplings and other ground connections. Care should be taken especially that on board transmission lines have the same impedance as the cables they are connected to (i.e. 50Ω for most applications and 75Ω in case of video and cable TV applications). These transmission lines usually require much wider traces on a standard double sided PCB than needed for a 'normal' connection. Another important issue is that inputs and outputs must not 'see' each other or are routed together over the PCB at a small distance. Furthermore it is important that components are placed as flat as possible on the surface of the PCB. For higher frequencies a long lead can act as a coil, a capacitor or an antenna. A pair of leads can even form a transformer. Careful design of the PCB avoids oscillations or other unwanted behavior. When working with really high frequencies, the only components which can be used will be the surface mount ones (for more information see OA-15 SNOA367).

As an example of how important the component values are for the behavior of your circuit, look at the following case: On a board with good high frequency layout, an amplifier is placed. For the two (equal) resistors in the feedback path, 5 different values are used to set the gain to +2. The resistors vary from 200Ω to 3kΩ.

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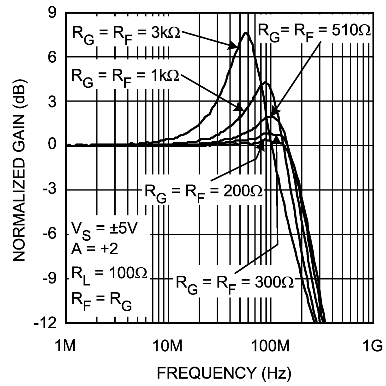

Figure 54.

In Figure 54 it can be seen that there's more peaking with higher resistor values, which can lead to oscillations and bad pulse responses. On the other hand the low resistor values will contribute to higher overall power consumption.

TI suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization.

Device	Package	Evaluation Board PN
LMH6682MA	8-Pin SOIC	CLC730036
LMH6682MM	8-Pin VSSOP	CLC730123
LMH6683MA	14-Pin SOIC	CLC730031
LMH6683MT	14-Pin TSSOP	CLC730131

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	19

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6682MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 82MA	Samples
LMH6682MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 82MA	Samples
LMH6682MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A90A	Samples
LMH6682MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A90A	Samples
LMH6683MA/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMH66 83MA	Samples
LMH6683MAX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMH66 83MA	Samples
LMH6683MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMH66 83MT	Samples
LMH6683MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMH66 83MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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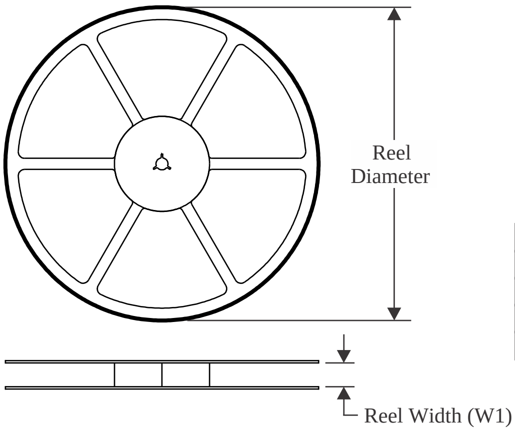
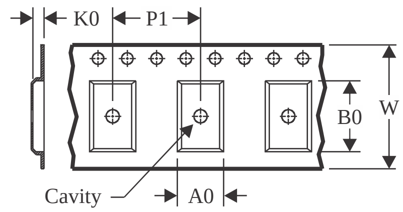
TAPE AND REEL INFORMATION

REEL DIMENSIONS

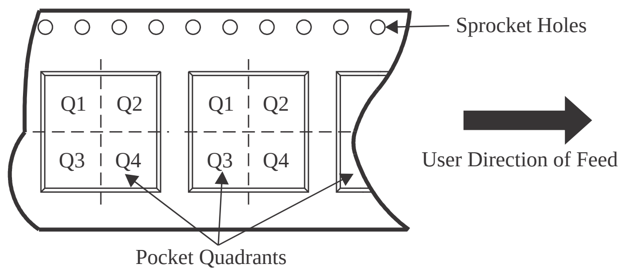


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

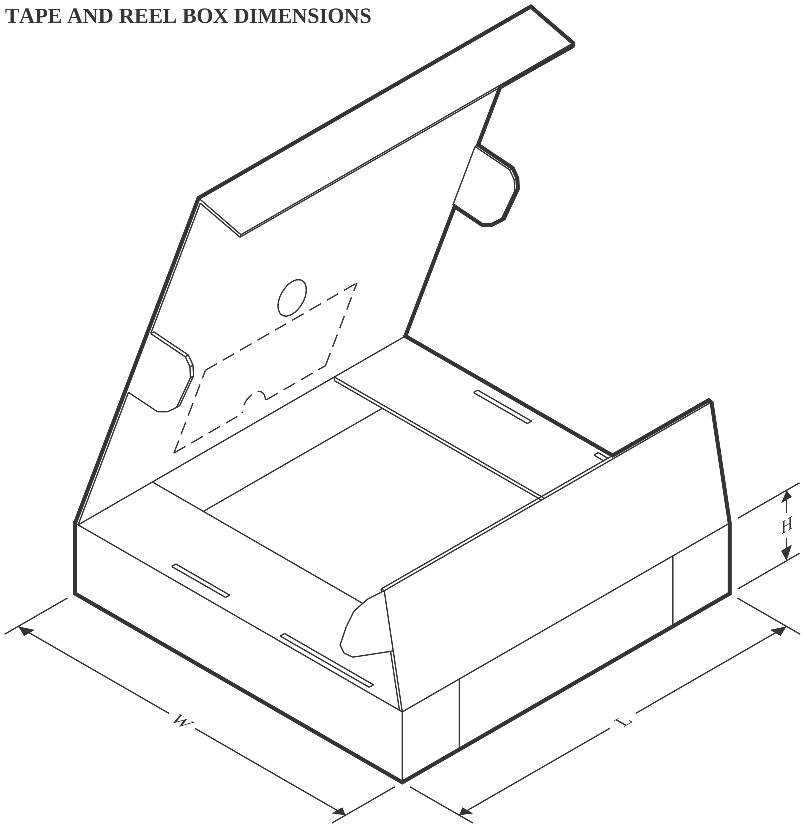
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6682MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6682MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6682MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6683MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMH6683MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMH6683MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

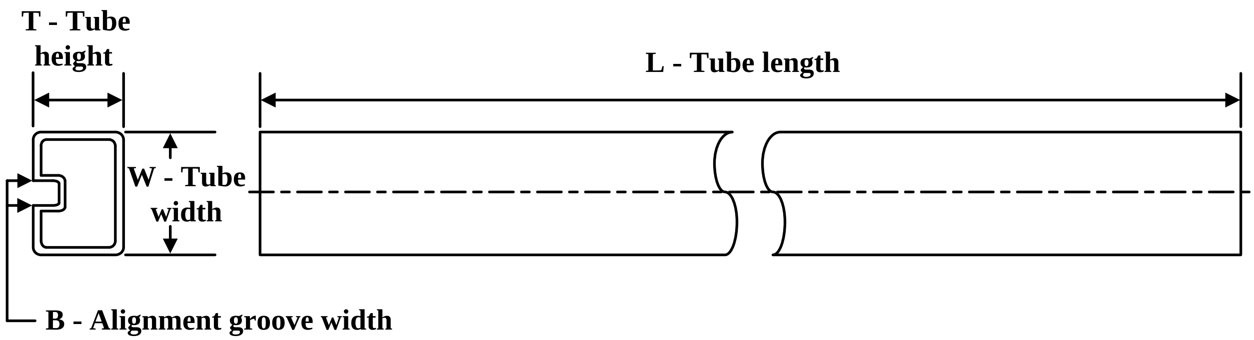
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

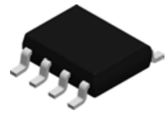
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6682MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6682MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMH6682MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMH6683MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMH6683MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMH6683MTX/NOPB	TSSOP	PW	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6682MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6683MA/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMH6683MT/NOPB	PW	TSSOP	14	94	530	10.2	3600	3.5
LMH6683MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06

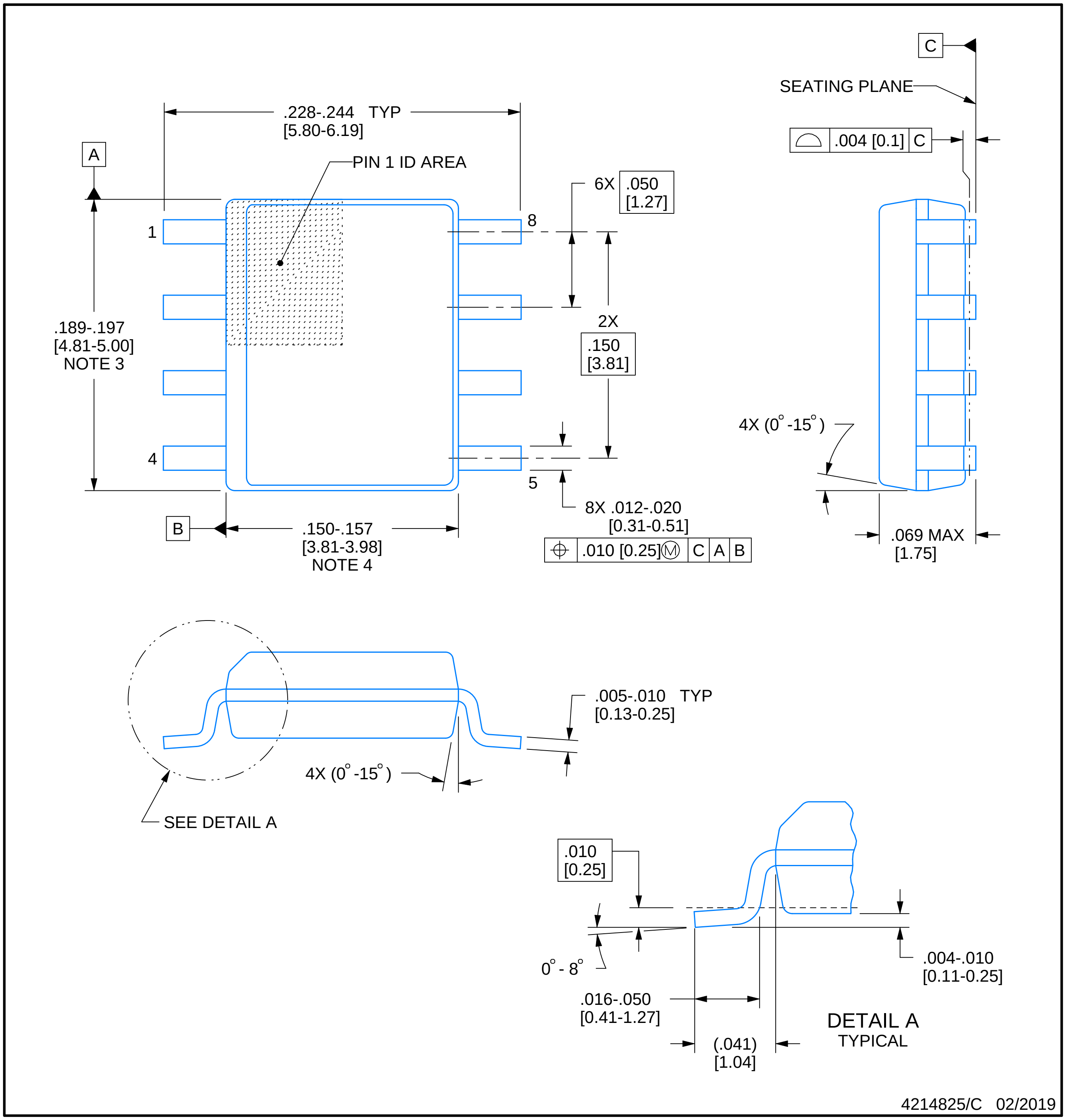


PACKAGE OUTLINE

D0008A

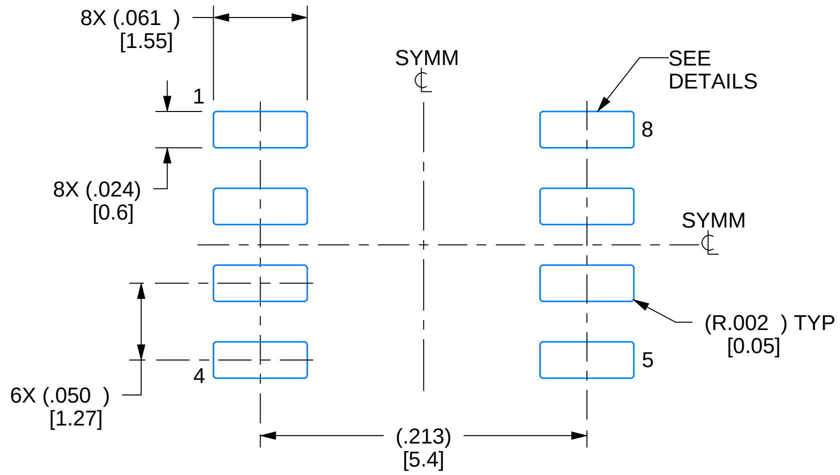
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

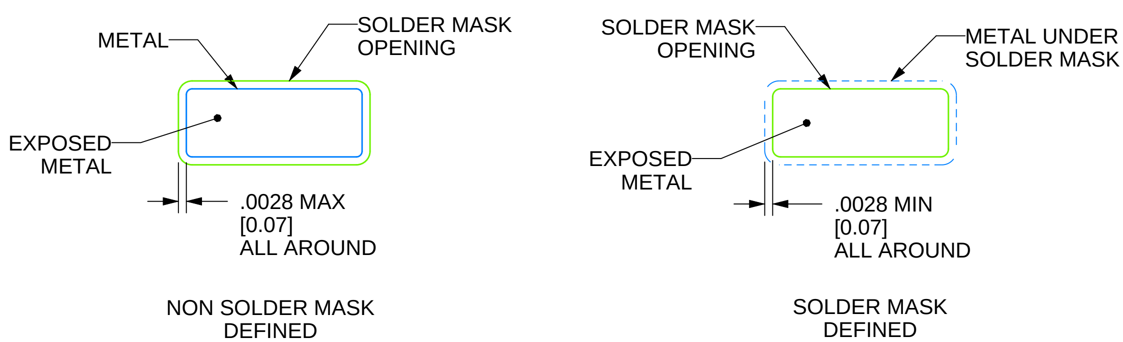


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

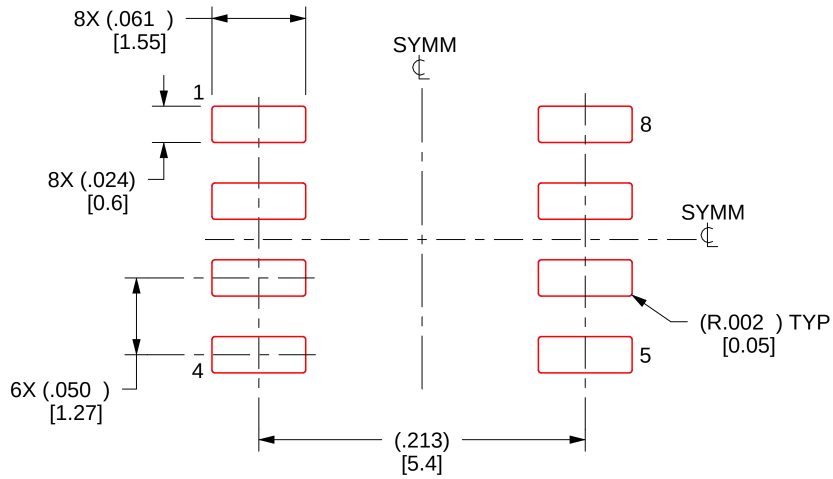


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

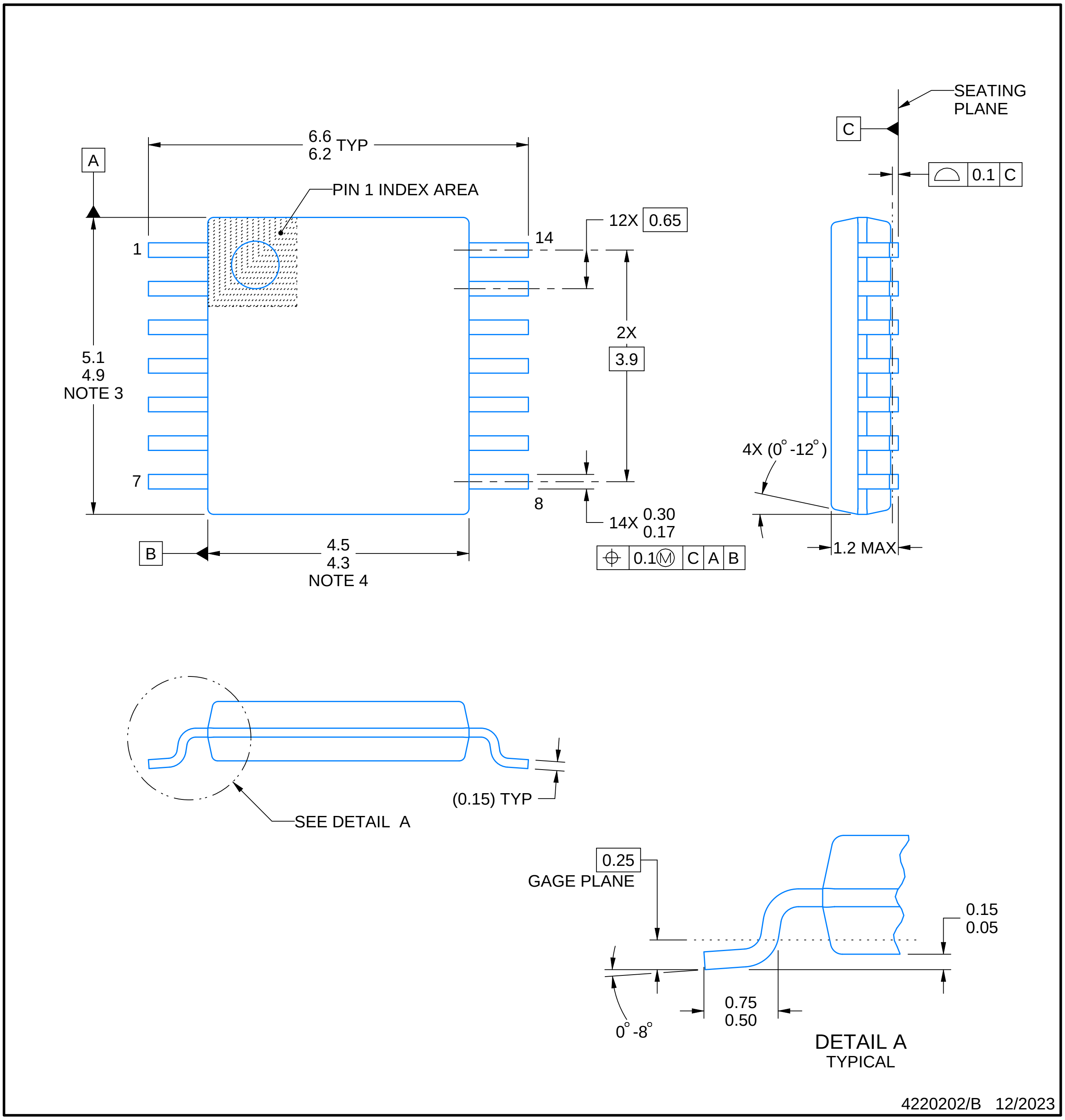


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

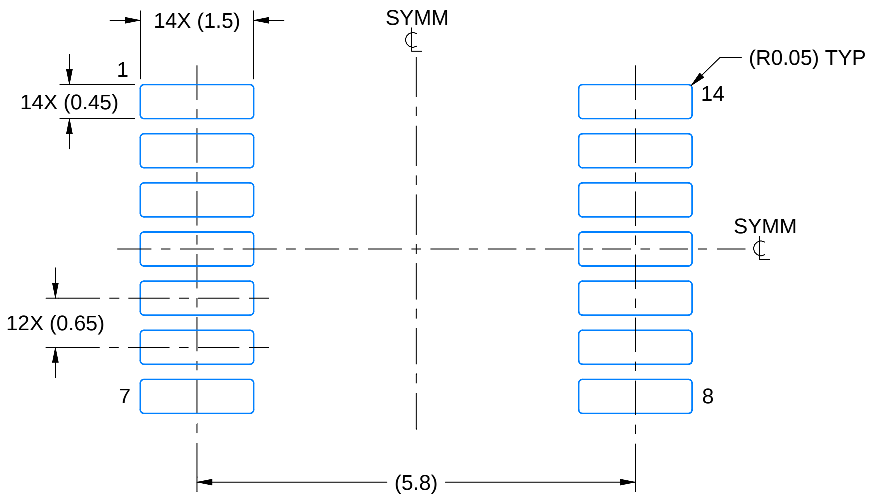
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

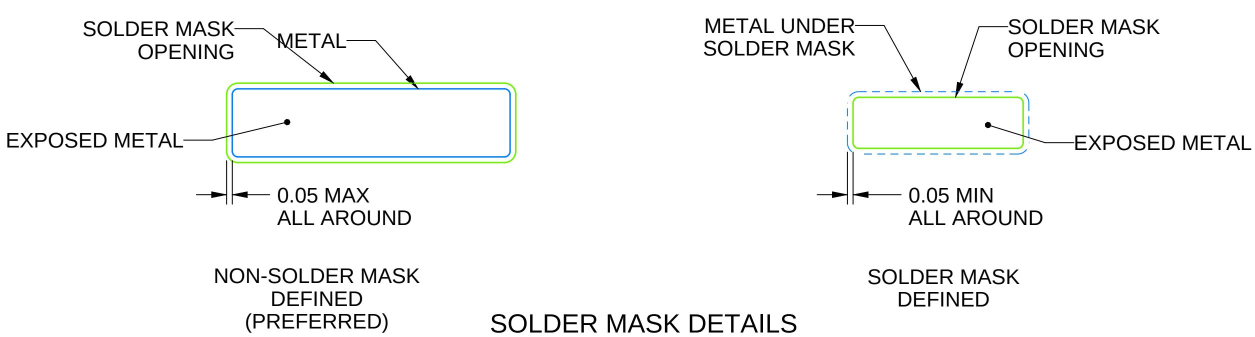


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

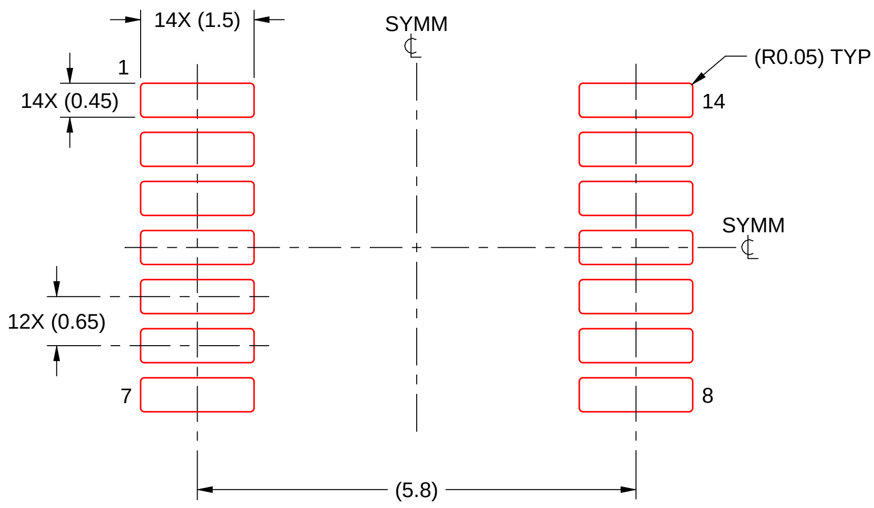


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

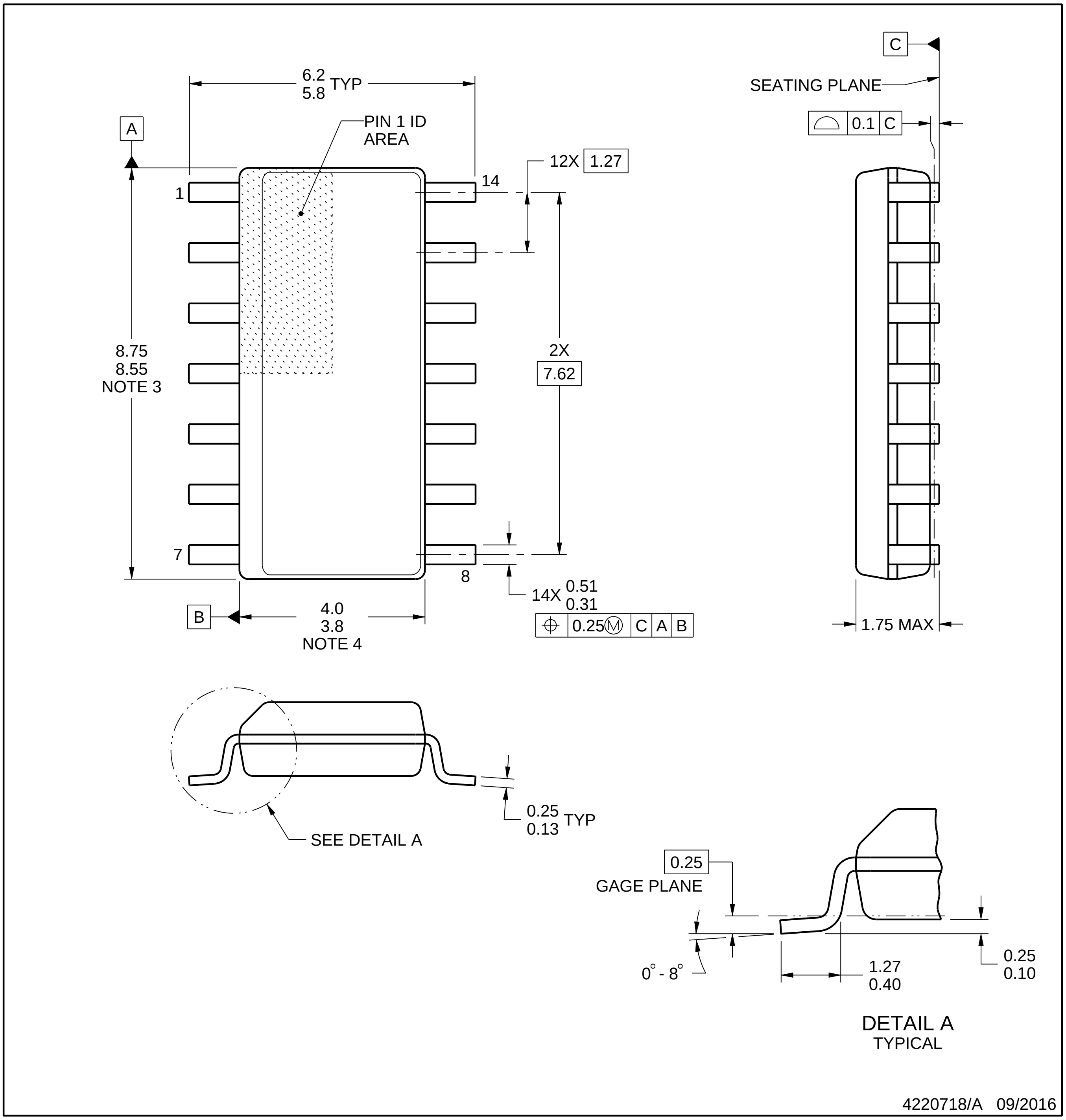


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

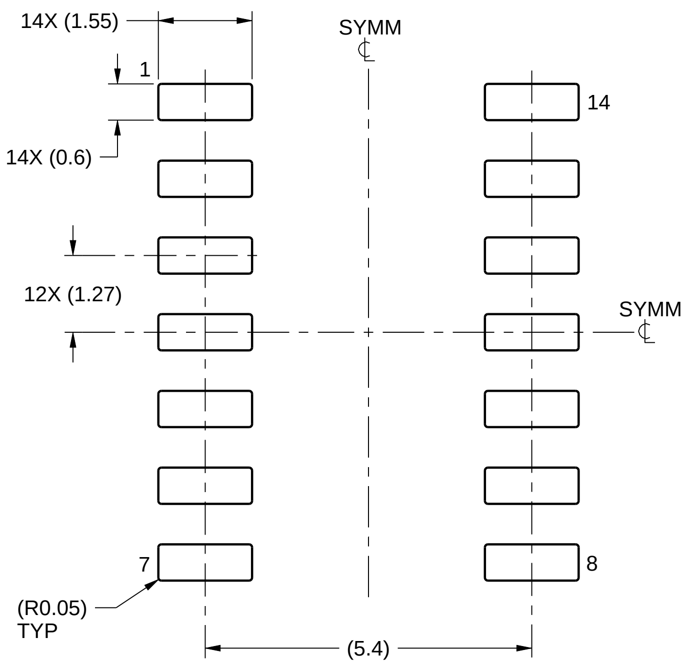
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

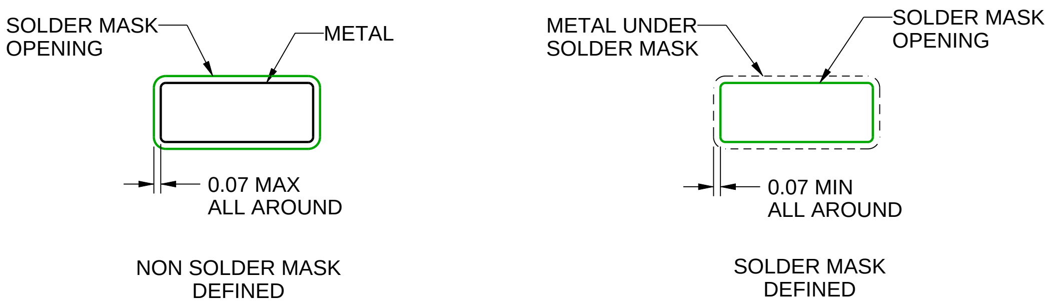


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

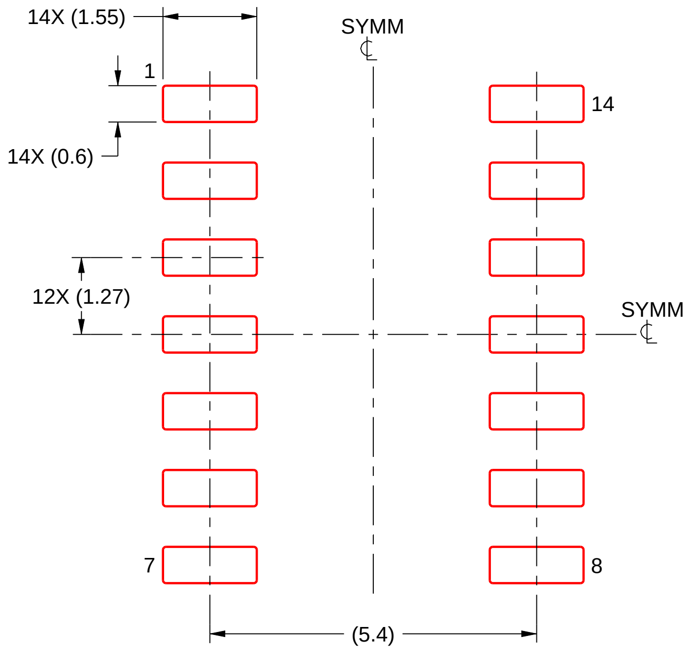


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

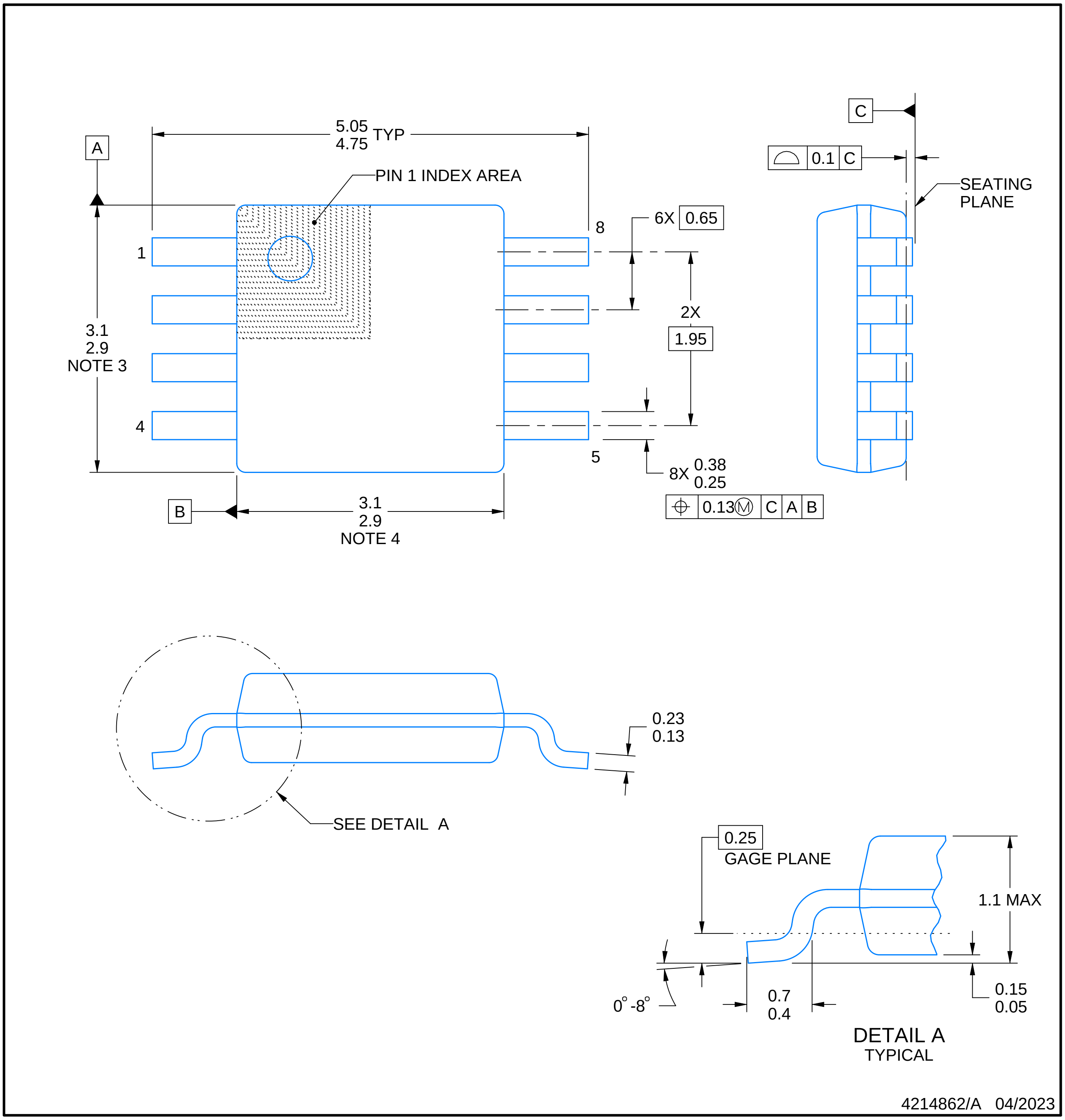


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

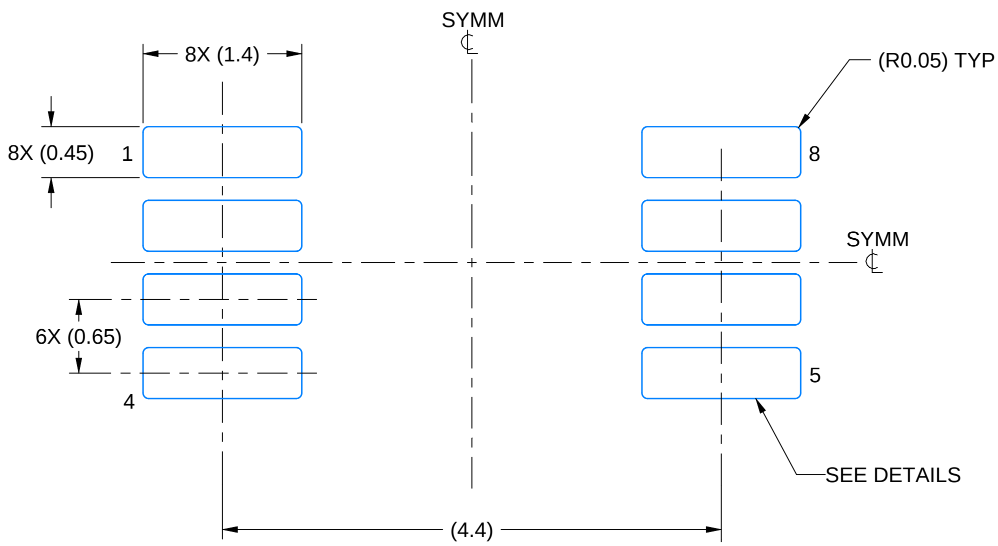


4214862/A 04/2023

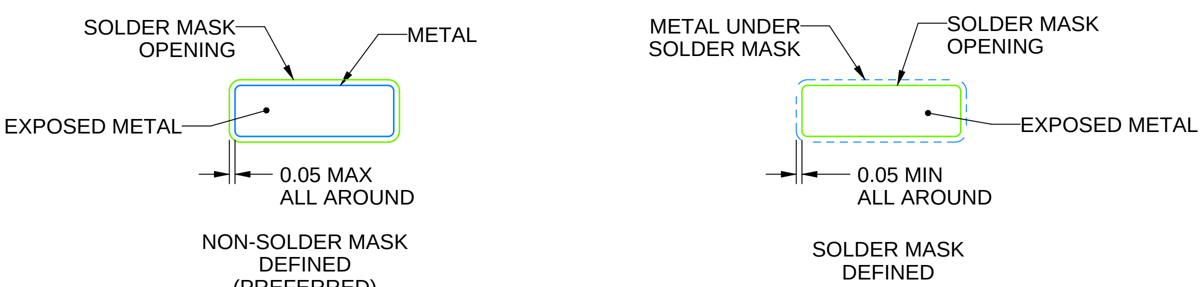
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

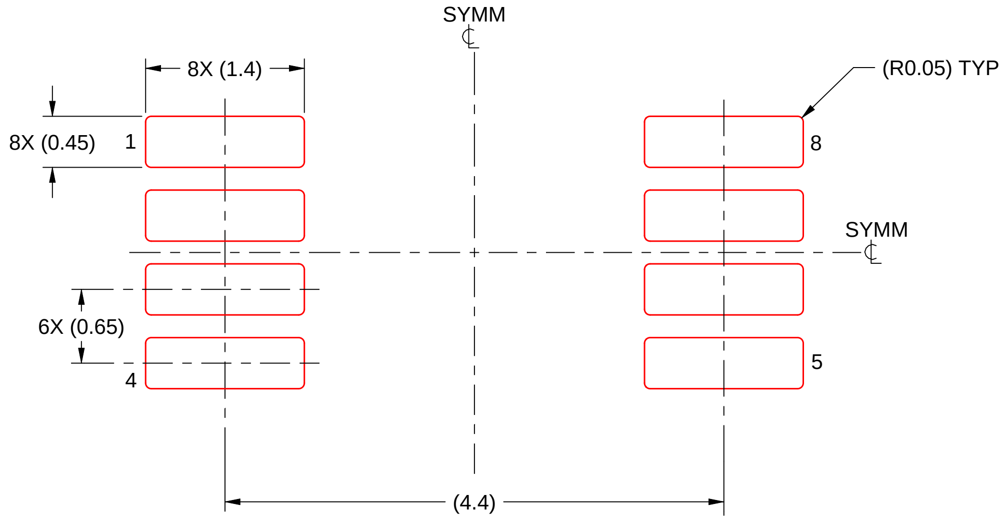


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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