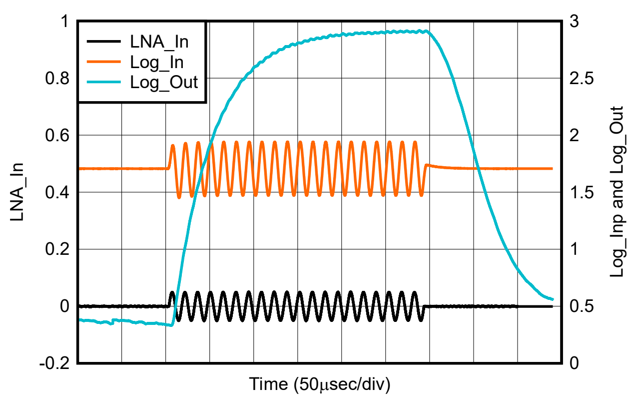
LOG300 40MHz, Logarithmic Detector With Integrated Low-Noise Amplifier

1 Features

- Input range:
  - LNA + log detector: $6\mu V_P$ to $200mV_P$
  - Log detector: $20\mu V_P$ to $1.6V_P$
- Low input-referred noise: < $3\mu V_{RMS}$
- Dynamic range: 98dB with log conformance error (LCE) = ±1.2dB
- Signal detection up to 40MHz; even higher with reduced LCE
- Input frequency detection, zero cross detect
- Supply: 3V to 5.25V

2 Applications

- Ultrasonic distance and material sensing
- Flow cytometry
- ESD and high energy EMI signal detection
- Energy detection
- Bubble, occlusion detection



3 Description

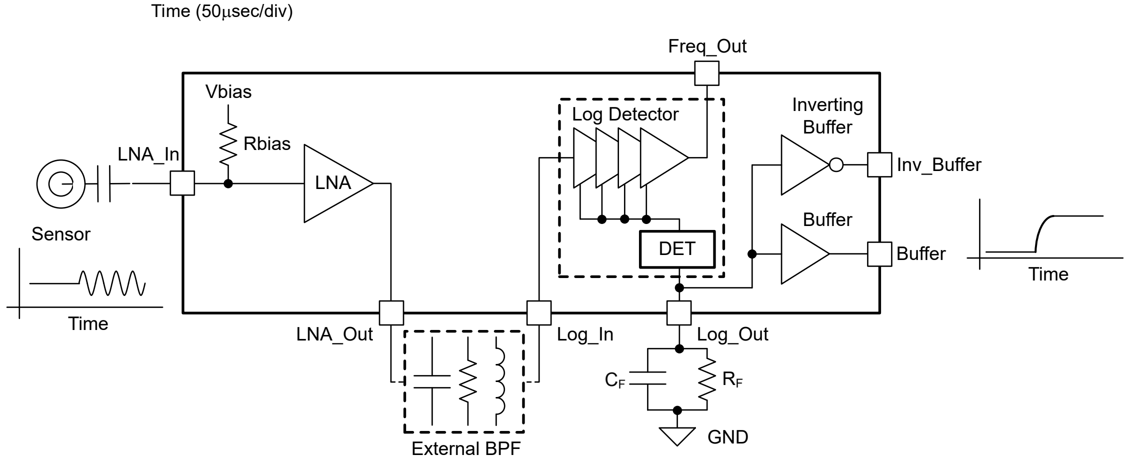
The LOG300 is an integrated Analog Front End (AFE) consisting of low-noise amplifier (LNA) and a Log Detector block. This device supports an input frequency range of up-to 40MHz and a typical dynamic range of 98dB. The LOG300 is intended for use in applications that require a wide dynamic range of voltage and signal measurement. The Log Detector block of LOG300 supports both single-ended and differential inputs. The low input noise of the integrated LNA, allows measurement of signals as low as $6\mu V_P$. The transient output response can be adjusted by tuning the capacitor connected at the Log_Out pin. The integrated frequency detect feature of LOG300 enables users to extract input signal frequency and zero-crossing information.

The LOG300 is available in a 16-pin SOIC and 16-pin VQFN package. The LOG300 is operational from a 3V to 5.25V supply and over the full ambient temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LOG300	D (SOIC, 16)	9.9mm × 6mm
	RGT (VQFN, 16)	3mm × 3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logarithmic Detector / Envelope Detector

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4 Pin Configuration and Functions

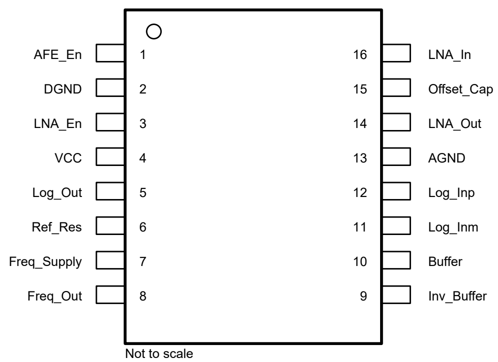


Figure 4-1. D Package, 16-Pin SOIC (top view)

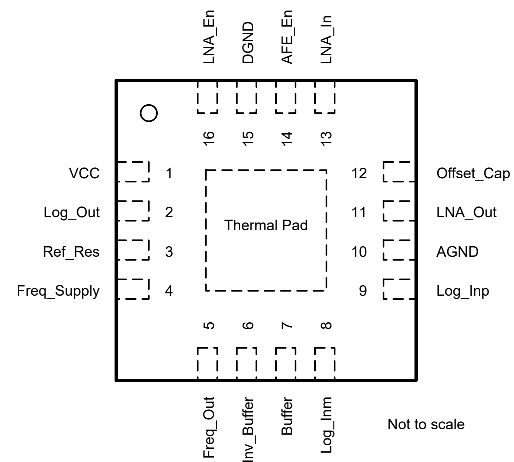


Figure 4-2. RGT Package, 16-Pin VQFN (top view)

Table 4-1. Pin Functions

PIN			TYPE[(1)]	DESCRIPTION
NAME	NO. D (SOIC)	NO. RGT (VQFN)		
AFE_En	1	14	I	LNA and Log Detector block enable and disable pin. AFE_En = High for AFE enable. Floating this pin keeps both blocks enabled as well.
AGND	13	10	P	Analog ground for LNA and Log detector block
Buffer	10	7	O	Noninverting buffered output. $V_{Buffer} = V_{Log\_Out} \times 2$.
DGND	2	15	P	Digital ground for Freq_Out pin
Freq_Out	8	5	O	This pin toggles at the same signal frequency applied at the Log_In.
Freq_Supply	7	4	P	Power supply for Freq_Out function. Float this pin if the frequency-detection feature is not required.
Inv_Buffer	9	6	O	Inverted buffered output. $V_{Inv\_Buffer} = V_{Log\_Out} \times -2$.
LNA_En	3	16	I	Low-noise amplifier enable and disable. LNA_En = High for LNA enable. Floating this pin keeps the LNA enabled as well.
LNA_In	16	13	I	Low-noise amplifier input
LNA_Out	14	11	O	Low-noise amplifier output
Log_Inm	11	8	I	Inverting input of Log Detector block. Connect an appropriate capacitor to ground when used in a single-ended input. Refer to Section 7.3.2.
Log_Inp	12	9	I	Noninverting input of Log Detector block
Log_Out	5	2	O	Unbuffered output of Log Detector block. Connect an appropriate resistor R_F (to set the input to output slope) and capacitor C_F (to set the response time).
Offset_Cap	15	12	I	Connect a recommended capacitor from this pin to ground. This capacitor sets the pole of the internal offset correction loop. Refer to Section 7.3.1 for the recommended capacitor.
Ref_Res	6	3	I	Connect a 1% 56kΩ resistor to this pin. Float this pin if the default relaxed slope accuracy is acceptable.
VCC	4	1	P	Supply
Thermal Pad	—	Thermal Pad	P	Thermal pad. Electrically isolated from the device. Connect to a heat spreading plane, typically ground.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
VCC	Supply voltage and Freq_Supply		5.5	V
	AFE_En and LNA_En	GND	VCC	V
LNA_In	LNA input voltage		±1	V_P
Log_In	Single ended input voltage (Log_Inp and Log_Inm)		(VCC × 0.17) + 0.9	V_P
I_I	Continuous input current for all pins[(2)]		±10	mA
	Continuous power dissipation	See Thermal Information		
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* can cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Current limit the input signals, which can swing more than 0.5V beyond the supply rails to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	3		5.25	V
T_A	Ambient operating temperature	–40	25	125	°C
Ref_Res	Recommended reference resistor to ground		56		kΩ

5.4 Thermal Information

THERMAL METRIC[(1)]		LOG300		UNIT
		D (SOIC)	VQFN (RGT)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.1	48.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.3	56.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	23.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.7	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.1	23.4	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	8.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics Low Noise Amplifier (LNA)

at T_A = 25°C, VCC = 3.3V to 5V, LNA_Out = 1kΩ to AGND, R_{SOURCE} = 50Ω, and input ac coupling capacitor (C_{IN}) = 10nF to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
G_{LNA}	Internal gain			11		V/V
	Internal gain error	T_A = –40°C to +125°C		±0.8	±1	%
AC PERFORMANCE						
SSBW	Small-signal bandwidth	LNA_Out = 20mV_{PP}		39		MHz
LSBW	Large-signal bandwidth			36		MHz
SR	Slew rate	2V step at LNA_Out		200		V/µs
	Total input referred noise	f > 100kHz, includes gain and bias resistors		2.6		nV/√Hz
	Overdrive recovery time	2 × output overdrive		1		µs
	Capacitive drive[(1)]	< 3dB of peaking		∞		nF
INPUT						
V_{LNA_In}	Linear input voltage	VCC = 5V			200	mV_P
		VCC = 3.3V			140	
	Internal bias voltage	At LNA_In, T_A = –40°C to +125°C		VCC × 0.044		mV
	Input impedance of LNA			1.7 || 1.8		kΩ || pF
OUTPUT						
	Output bias point of LNA	LNA_In = open		V_{BIAS} × 11		V
	Output impedance of LNA		0.850	1	1.150	kΩ
POWER SUPPLY						
	Quiescent operating current			2	2.7	mA
		T_A = –40°C to +125°C			3	
POWER DOWN						
	LNA enable voltage threshold	Floating = enable	VCC – 1.2			V
	LNA disable voltage threshold				GND + 0.6	V
	Turn-on time	Time from disable to enable		36	60	µs
	Turn off time	Time from enable to disable		130	200	ns

(1) Infinite capacitive drive possible due to presence of 1kΩ of isolation resistor

5.6 Electrical Characteristics Log Detector

at T_A = 25°C, VCC = 3.3V to 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB) for VCC = 5V and R_F = 30kΩ for VCC = 3.3V, Ref_resistor = 1% 56kΩ, 10nF capacitor to AGND on Log_inp and Log_inm (unless otherwise noted)[4]

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
LCE	Log conformance error[3]	f = 1MHz			±0.6	±1	dB
			T_A = –40°C to +125°C			±1.1	
		f = 40MHz			±2	±2.5	
			T_A = –40°C to +125°C			±2.9	
DR	Dynamic range[3]	LCE = ±1dB, f = 1MHz		96	98		dB
	Log Detector slope[1]				R_F value in kΩ[2]		mV/dB
	Log Detector slope variation[3]	Ref_Res = 56kΩ of 1% accuracy, f = 1MHz			±1	±6	%
			T_A = –40°C to +125°C			±6.8	
		Ref_Res = open, f = 1MHz			±4.5		
			T_A = –40°C to +125°C		±5.6		
INPUT							
V_{Log_In}	Typical input voltage	VCC = 3.3V, LCE = ±2dB, f = 20MHz		20μ		1.2	V_P
			T_A = –40°C to +85°C	24μ		1	
			T_A = –40°C to +125°C	26μ		0.8	
		VCC = 5V, LCE = ±2dB, f = 20MHz		20μ		1.6	
			T_A = –40°C to +85°C	22μ		1.6	
			T_A = –40°C to +125°C	32μ		1.6	
	Differential input voltage	(Log_Inp) – (Log_Inm), T_A = –40°C to +125°C				±1.6	V
	Internal bias voltage	Log_Inp and Log_Inm			1.7		V
	Input impedance	for Log_Inp and Log_Inm			1.7 || 10		kΩ || pF
LOG_OUT							
	Log_Out rise time	C_F = 220pF			20		μs
		C_F = 1nF			95		
	Log_Out fall time	C_F = 220pF			27		μs
		C_F = 1nF			100		
	Output overdrive recovery	C_F = 220pF			250		μs
	Minimum output voltage[5] [3]	Log_Inp = 10nF to AGND		83	155	205	mV
			T_A = –40°C to +125°C			340	
	Maximum output voltage	T_A = –40°C to +125°C		VCC– 0.3			V

5.6 Electrical Characteristics Log Detector (continued)

at T_A = 25°C, VCC = 3.3V to 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB) for VCC = 5V and R_F = 30kΩ for VCC = 3.3V, Ref_resistor = 1% 56kΩ, 10nF capacitor to AGND on Log_inp and Log_inm (unless otherwise noted)(4)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BUFFER OUTPUT							
	Gain	V_{Buffer}/V_{Log_Out}			+2		V/V
	Output voltage equation				2 × Log_Out		V
	Output-referred offset					30	mV
	Output voltage	T_A = –40°C to +125°C		GND + 0.1		VCC– 0.1	V
	Rise-and-fall response time(2)	C_{Load} || R_{Load} = 100pF || 10kΩ			1.5		µs
	Short-circuit current	Source-and-sink current		20			mA
Z_{OUT}	Output impedance				5.3		Ω
INV_BUFFER OUTPUT							
	Gain	$V_{Inv\_Buffer}/V_{Log\_Out}$			–2		V/V
	Output voltage equation				VCC – (2 × Log_Out)		V
	Output voltage	T_A = –40°C to +125°C		GND + 0.1		VCC – 0.1	V
	Rise-and-fall response time(2)	C_{Load} || R_{Load} = 100pF || 10kΩ			1.5		µs
	Output-referred offset					32	mV
	Short-circuit current	Source-and-sink current		20			mA
	Output impedance				6.3		Ω
FREQUENCY DETECT OUTPUT							
	Frequency detect block typical input sensitivity	Log_Inp signal of f < 2MHz		250µ		1.6	V_P
		Log_Inp signal of f < 20MHz		1.7m		1.6	
	Freq_Out swing			DGND		Freq_Supply	V
POWER SUPPLY							
	Quiescent current	Freq_Supply = Open			4.1	4.6	mA
			T_A = –40°C to +125°C			5.9	
		Freq_Supply = VCC				0.37	

(1) Log Detector slope reduces with increased input signal frequency, refer to *Typical Characteristics*
(2) Refer to *Parameter Measurement Information* for definition of R_F
(3) Charecterized through 32 units
(4) The symbol f stands for a short burst of sinewave of a frequency, f, applied at the Log_Inp pin. This definition holds through across the data sheet.
(5) Minimum output voltage is the lowest voltage Log_Out settles to, when inputs are shorted to AGND pin via a high value capacitor with no signal being applied.

5.7 Electrical Characteristics LNA + Log Detector (AFE)

at T_A = 25°C, VCC = 5V, C_F = 1nF and R_F = 43kΩ (slope = 43mV/dB for f = 1MHz), Ref_resistor = 1% 56kΩ, with 2nd-order external band-pass filter (BPF) of gain = –7dB, and R_{SOURCE} = 50Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AFE AC PERFORMANCE							
LCE	Log conformance error	f = 1MHz			±0.6	±1.2	dB
			T_A = –40°C to +125°C			±1.3	
DR	Dynamic range	For LCE = ±1.2dB, f = 1MHz			91		dB
	Log Detector slope variation	Ref_Res = open			±4.5		%
		Ref_Res = 56kΩ of 1% accuracy			±1	±7	
		Ref_Res = 56kΩ of 1%	T_A = –40°C to +125°C			±7	
AFE INPUT							
AFE input	Typical input voltage	LCE = ±1dB, f = 1MHz		6µ		200m	V_P
			T_A = –40°C to +125°C	8µ		200m	
		LCE = ±1dB, f = 20MHz		9µ		200m	
			T_A = –40°C to +125°C	10µ		200m	
	Output rise time	BPF = 180kHz, C_F = 350pF			35		µs
		BPF = 1MHz, C_F = 500pF			50		
	Output fall time	BPF = 180kHz, C_F = 350pF			65		µs
		BPF = 1MHz, C_F = 500pF			45		
LOG_OUT							
	Minimum output voltage	LNA_In = 10nF to AGND			290	335	mV
			T_A = –40°C to +125°C			436	
POWER SUPPLY							
	Quiescent current	Total AFE, LNA_Out = open, Freq_Supply = open			6	7.2	mA
			T_A = –40°C to +125°C			8.3	
POWER DOWN							
	Disabled current	Total AFE	T_A = –40°C to +125°C			130	µA
AFE_En	AFE enable voltage threshold	Floating = enable		VCC– 1.2			V
	AFE disable voltage threshold					AGND + 0.6	V

5.8 Typical Characteristics: VCC = 5V

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB) and Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm, (unless otherwise noted). For AFE, 2nd-order BPF centered around frequency "f" with gain = -7dB used between LNA and Log Detector block.

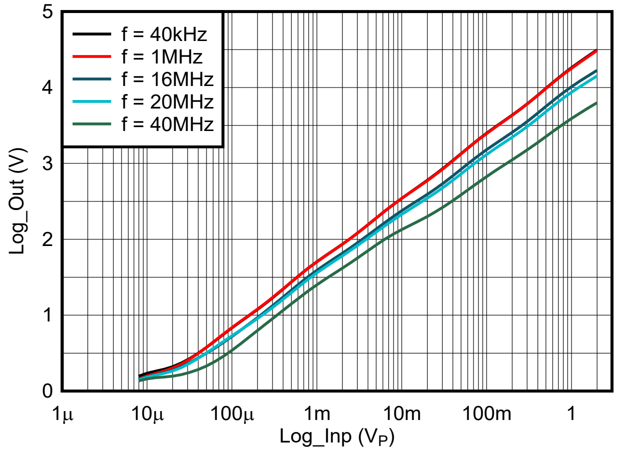


Figure 5-1. Log Detector Slope at Various Frequencies

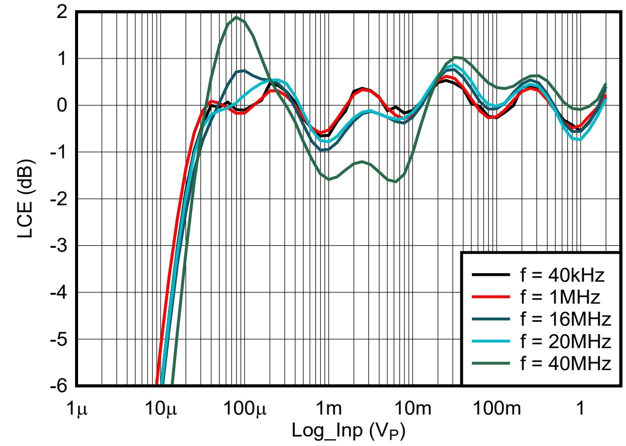


Figure 5-2. Log Conformance Error for Different Frequencies

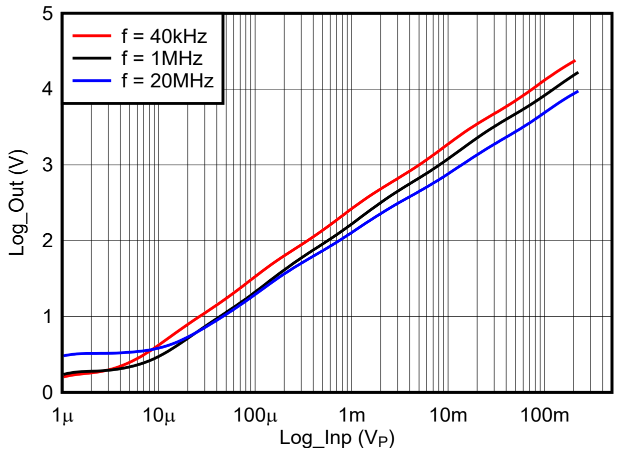


Figure 5-3. AFE Slope at Various Frequencies

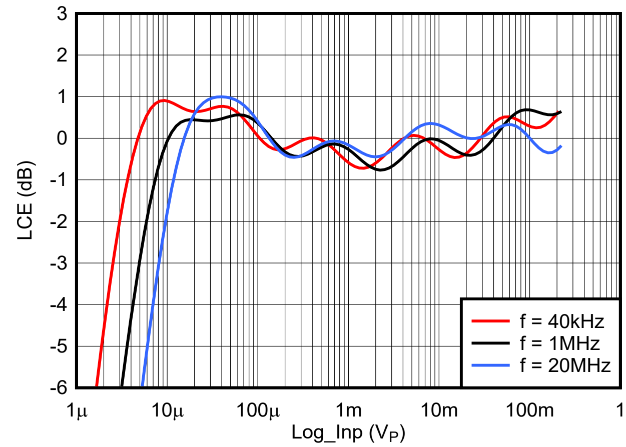


Figure 5-4. AFE Log Conformance Error for Different Frequencies

5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB) and Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm, (unless otherwise noted). For AFE, 2nd-order BPF centered around frequency "f" with gain = -7dB used between LNA and Log Detector block.

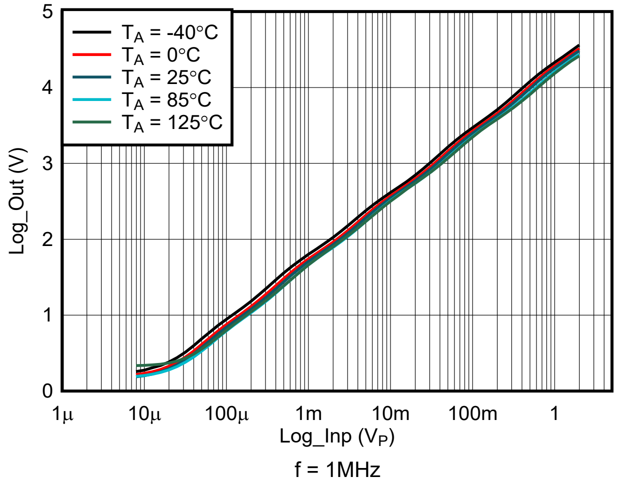


Figure 5-5. Log Detector Slope at Different Temperature Points

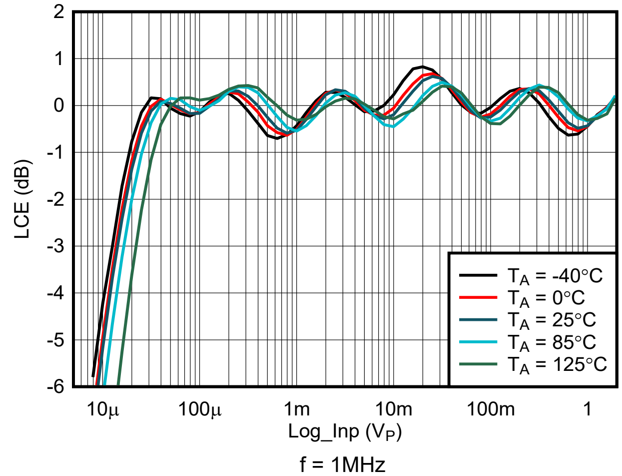


Figure 5-6. Log Conformance Error for Different Temperature Points

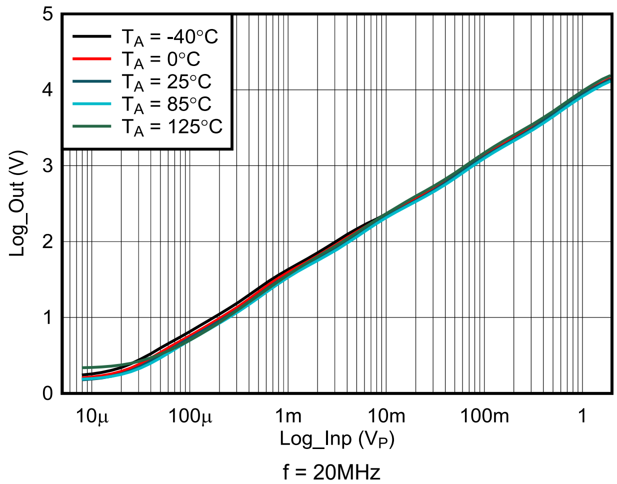


Figure 5-7. Log Detector Slope at Different Temperature Points

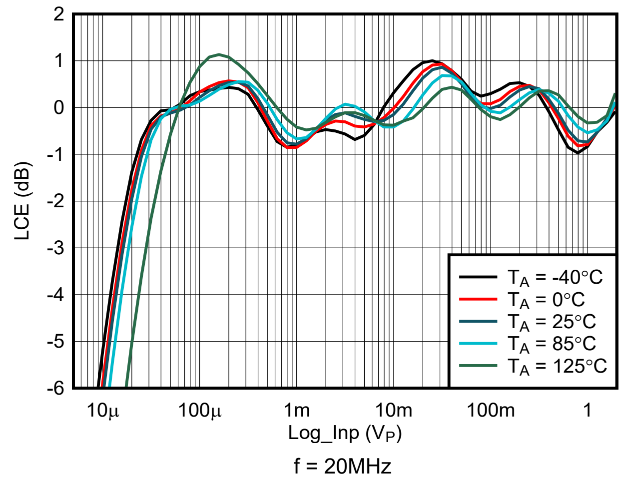


Figure 5-8. Log Conformance Error for Different Temperature Points

5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB) and Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm, (unless otherwise noted). For AFE, 2nd-order BPF centered around frequency "f" with gain = -7dB used between LNA and Log Detector block.

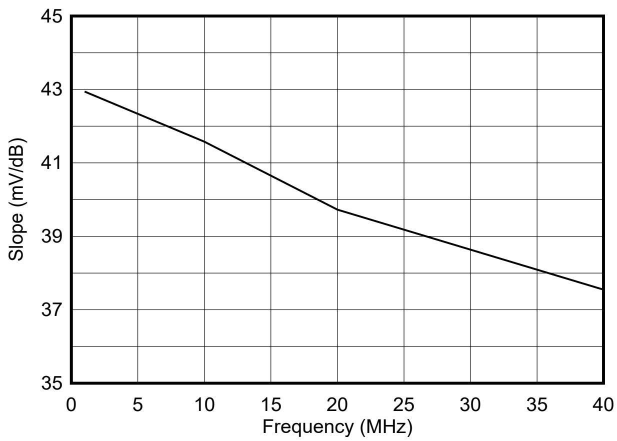
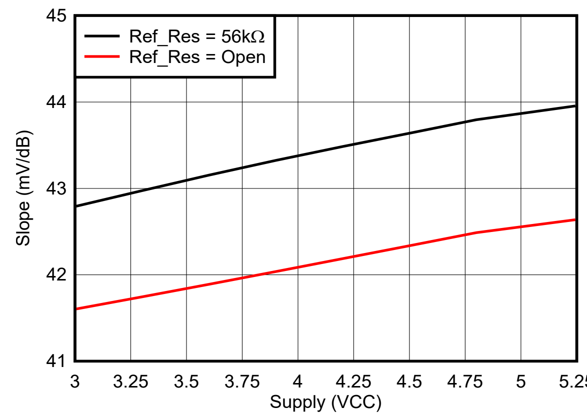
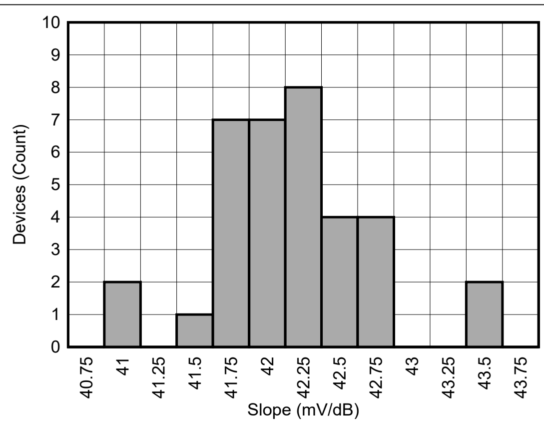


Figure 5-9. Log Detector Slope Variation with Input Signal Frequency



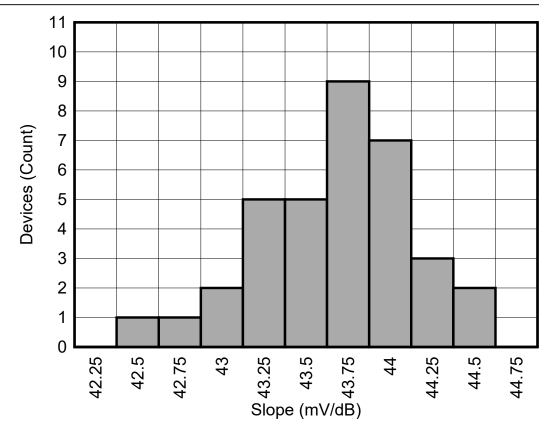
f = 1MHz

Figure 5-10. Log Detector Slope Variation vs Supply



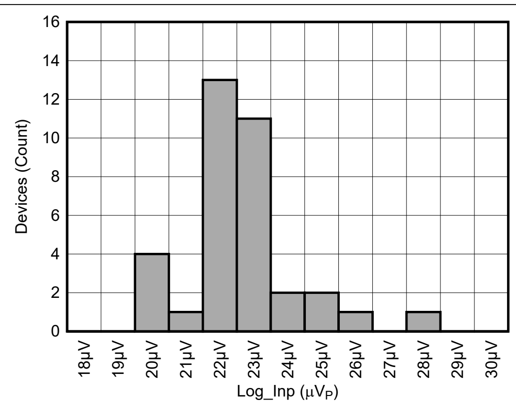
Ref_Res = 56kΩ μ = 43.55mV/dB σ = 0.44mV/dB

Figure 5-11. Log Detector Slope Histogram with Ref_Res



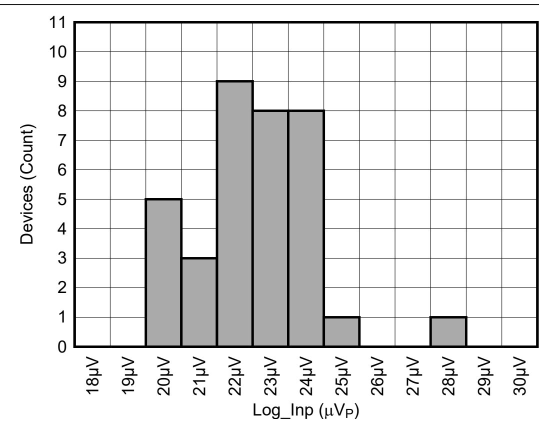
Ref_Res = Open μ = 42.03mV/dB σ = 0.53mV/dB

Figure 5-12. Log Detector Slope Histogram without Ref_Res



LCE = ±1dB, μ = 22.15μV_P σ = 1.59μV_P
f = 1MHz

Figure 5-13. Minimum Input Sensitivity of Log_Detector

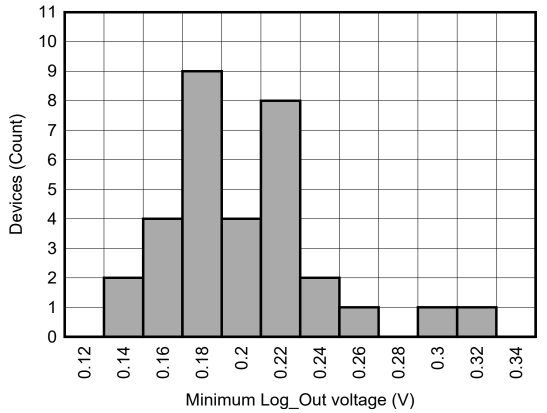


LCE = ±2dB, μ = 22.14μV_P σ = 1.67μV_P
f = 20MHz

Figure 5-14. Minimum Input Sensitivity of Log_Detector

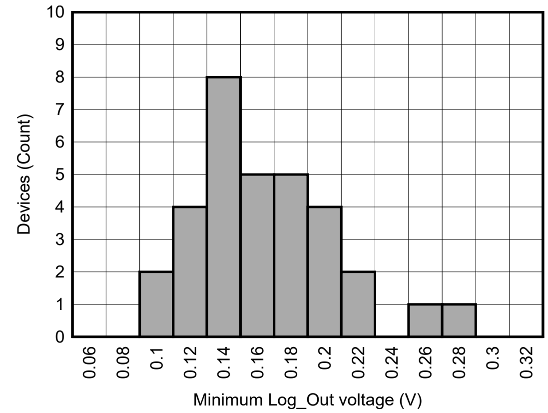
5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB) and Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm, (unless otherwise noted). For AFE, 2nd-order BPF centered around frequency "f" with gain = -7dB used between LNA and Log Detector block.



50Ω + 10nF at Log_Inp to AGND   μ = 0.19V   σ = 0.04V

Figure 5-15. Minimum Output Voltage at Log_Out



10nF at Log_Inp to AGND   μ = 0.15V   σ = 0.04V

Figure 5-16. Minimum Output Voltage at Log_Out

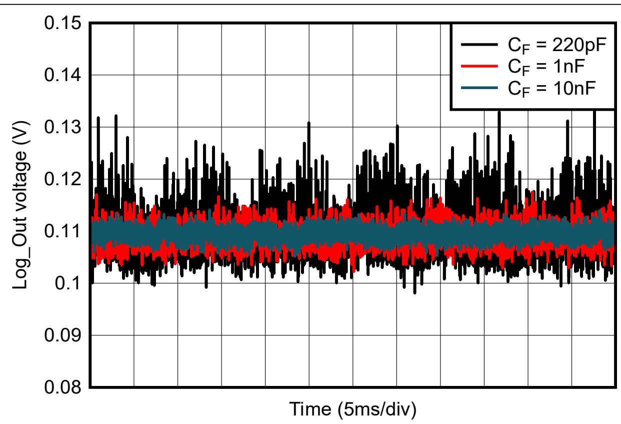


Figure 5-17. Minimum Log_Out Voltage vs Time

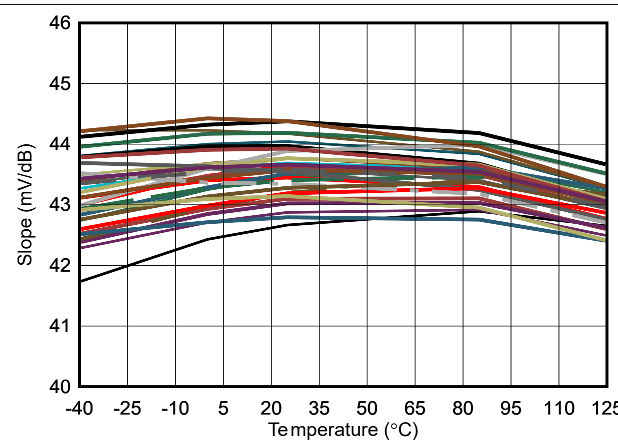
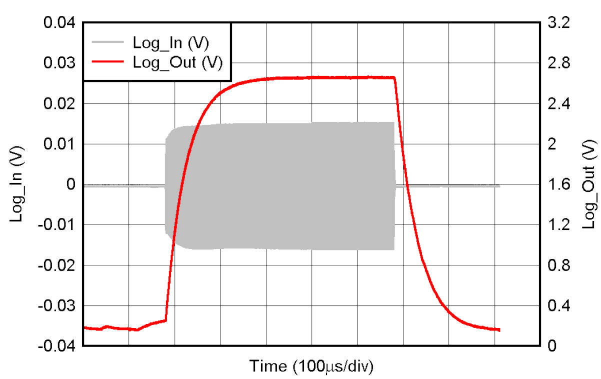
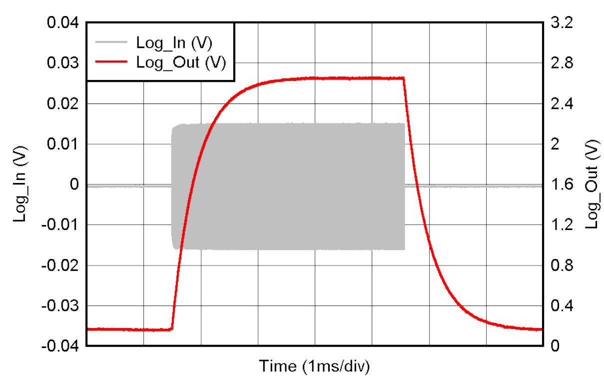


Figure 5-18. Slope Variation vs Temperature



f = 1MHz C_F = 1nF

Figure 5-19. Log Detector Rise and Fall Time

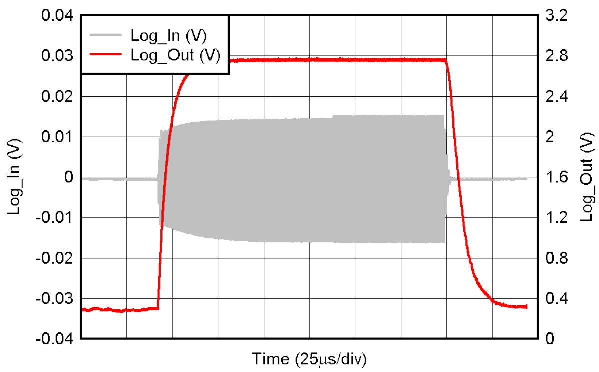


f = 1MHz C_F = 10nF

Figure 5-20. Log Detector Rise and Fall Time

5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB) and Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm, (unless otherwise noted). For AFE, 2nd-order BPF centered around frequency "f" with gain = -7dB used between LNA and Log Detector block.



f = 1MHz C_F = 100pF

Figure 5-21. Log Detector Rise and Fall Time

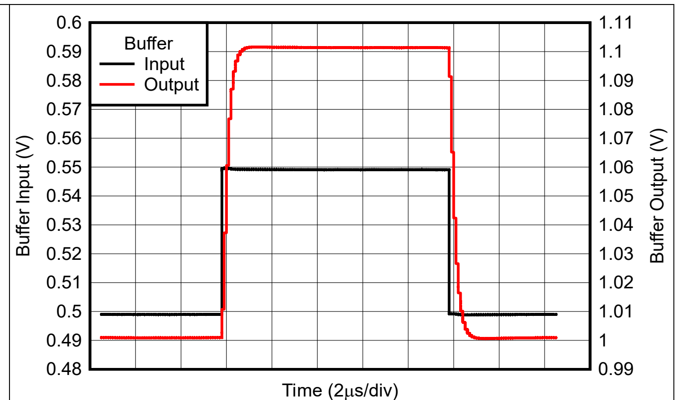


Figure 5-22. Small-Signal Step Response: Buffer

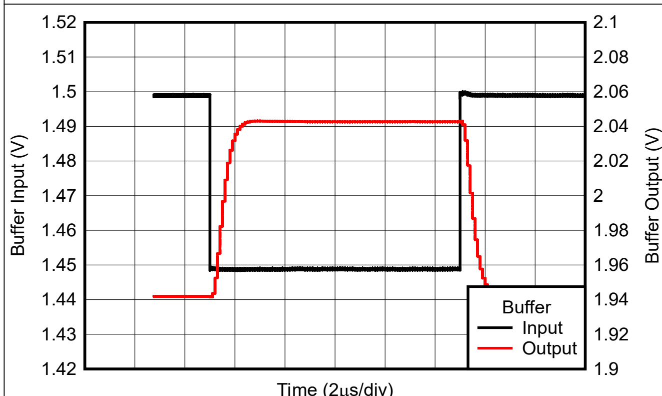


Figure 5-23. Small-Signal Step Response: Inverting Buffer

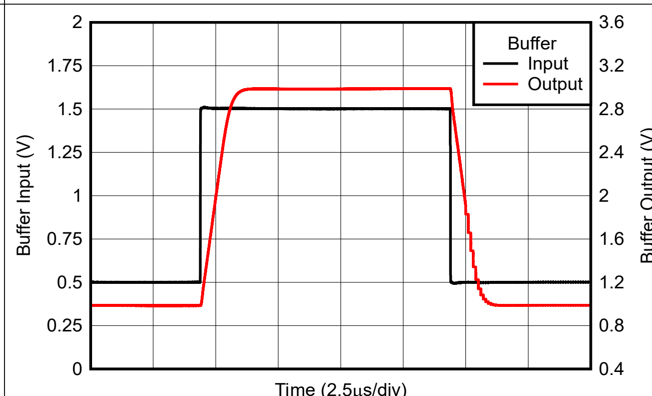


Figure 5-24. Large-Signal Step Response: Buffer

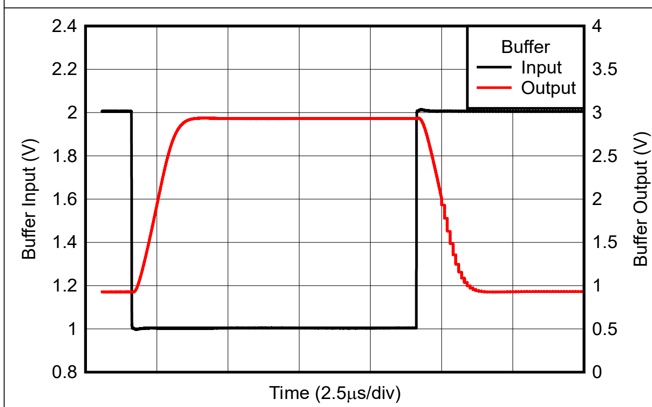
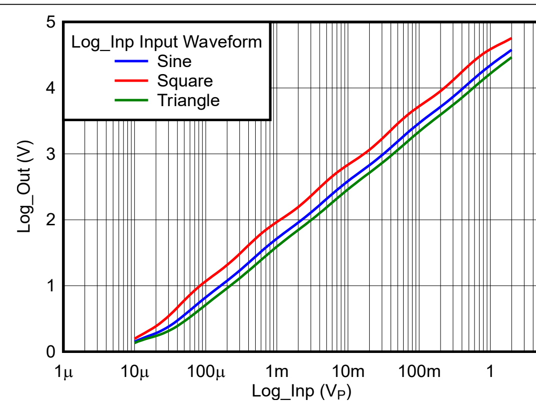


Figure 5-25. Large-Signal Step Response: Inverting Buffer



f = 1MHz

Figure 5-26. Log Detector Slope for Various Input Waveforms

5.8 Typical Characteristics: VCC = 5V (continued)

at T_A = 25°C, VCC = 5V, C_F = 1nF, R_F = 43kΩ (slope = 43mV/dB) and Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm, (unless otherwise noted). For AFE, 2nd-order BPF centered around frequency "f" with gain = -7dB used between LNA and Log Detector block.

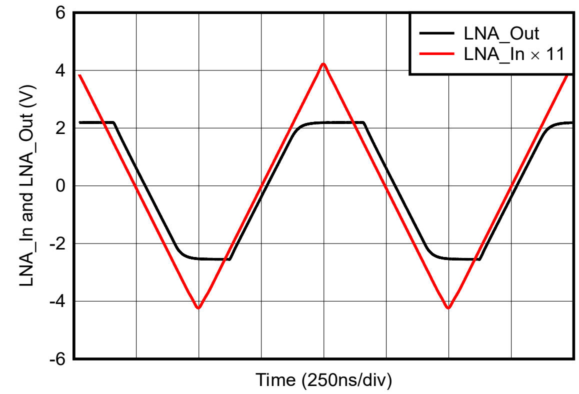
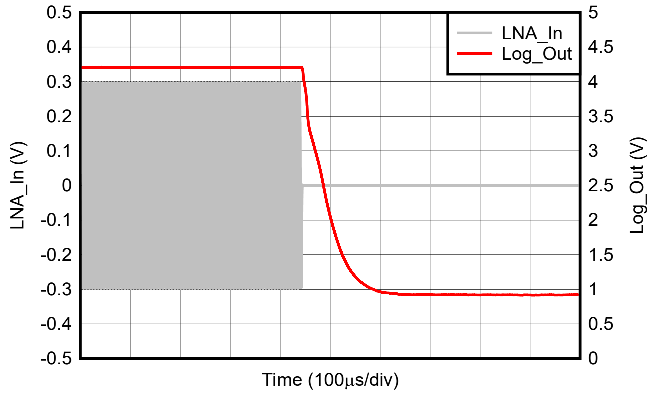


Figure 5-27. LNA Overdrive Recovery



BPF = 180kHz, C_F = 220pF

Figure 5-28. AFE Overdrive Recovery

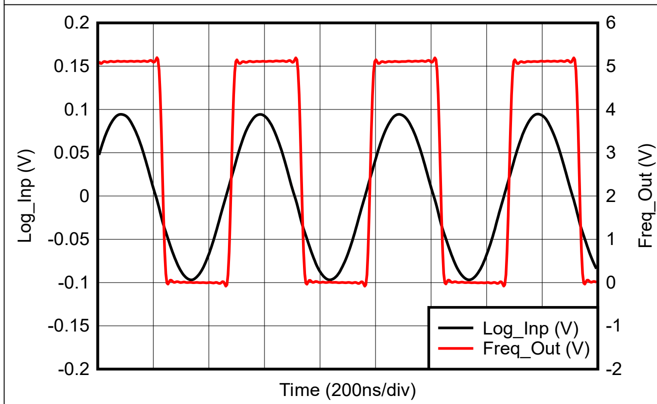
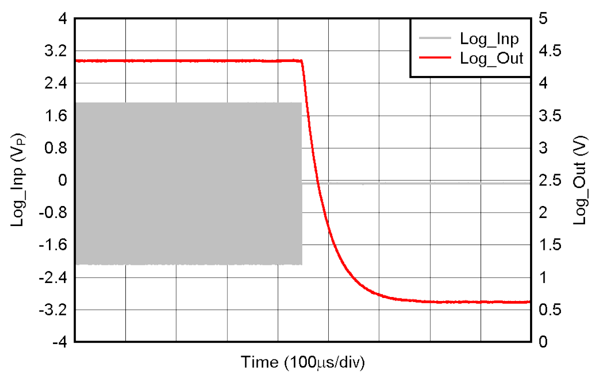
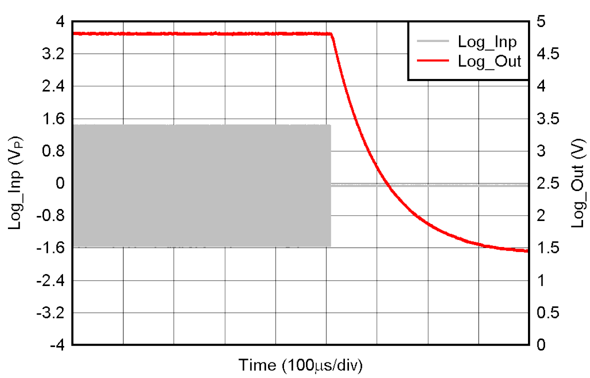


Figure 5-29. Frequency Detector Output Waveform



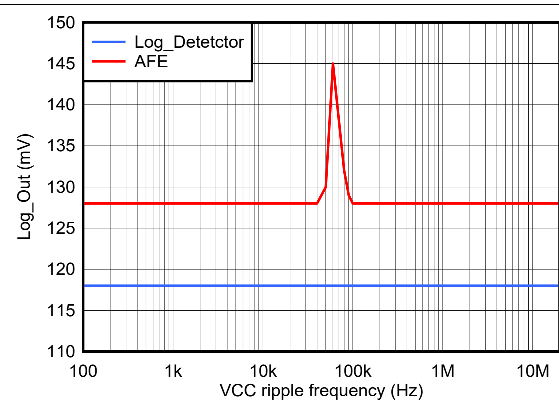
C_F = 200pF , Log_Inp = $4V_P$

Figure 5-30. Log Detector Input Stage Overdrive



C_F = 200pF, R_F = 100kΩ

Figure 5-31. Log Detector Output Stage Overdrive



AFE; BPF = 80kHz, RC filter on VCC of R = 50Ω, C = 12µF

Figure 5-32. Output vs 100mVpp Ripple Injected on VCC

5.9 Typical Characteristics: VCC = 3.3V

at T_A = 25°C, VCC = 3.3V, C_F = 1nF, R_F = 30kΩ (slope = 30mV/dB) and Ref_Res = 1% 56kΩ, and 10nF capacitor to AGND on Log_Inp and Log_Inm, (unless otherwise noted). For AFE, 2nd-order BPF centered around frequency "f" with gain = -7dB used between LNA and Log Detector block.

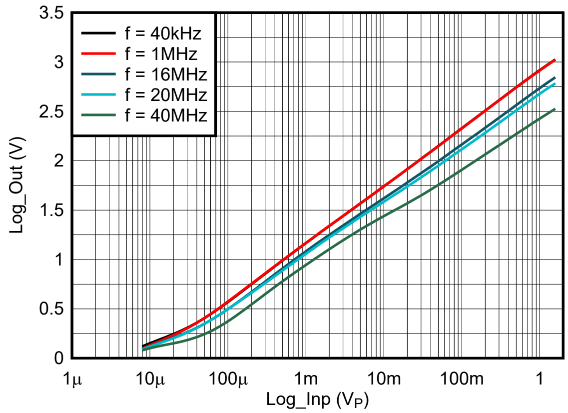


Figure 5-33. Log Detector Slope at Various Frequencies

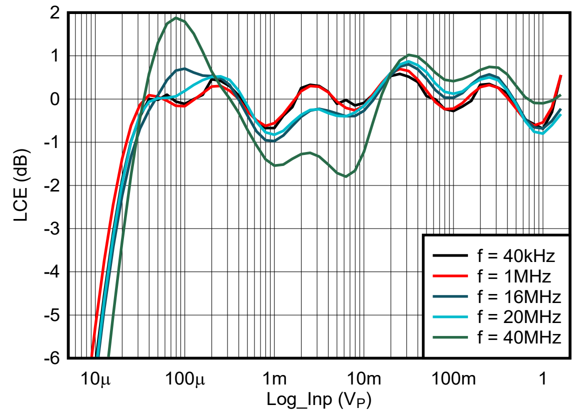


Figure 5-34. Log Conformance Error for Different Frequencies

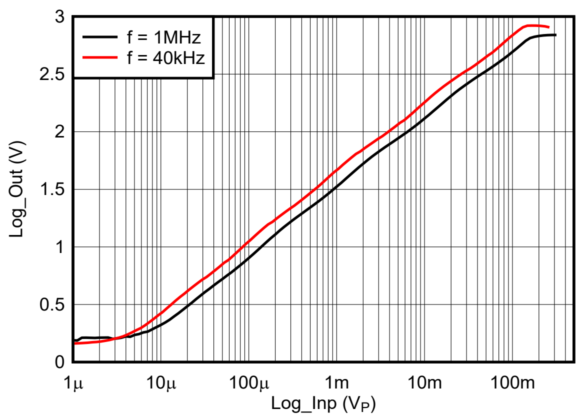


Figure 5-35. AFE Slope at Various Frequencies

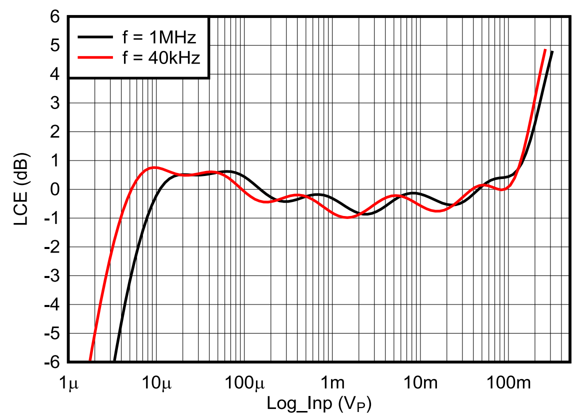


Figure 5-36. AFE Log Conformance Error for Different Frequencies

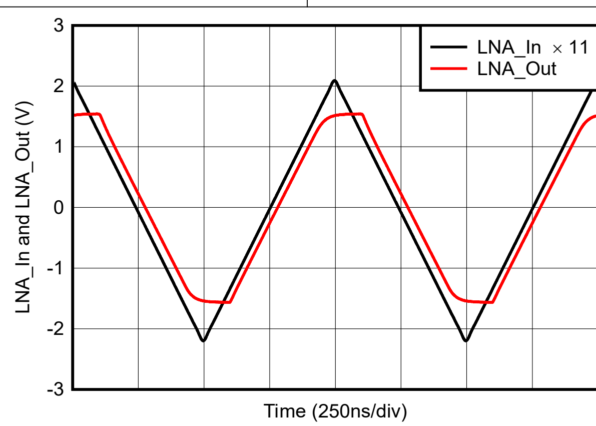


Figure 5-37. LNA Overdrive Recovery

6 Parameter Measurement Information

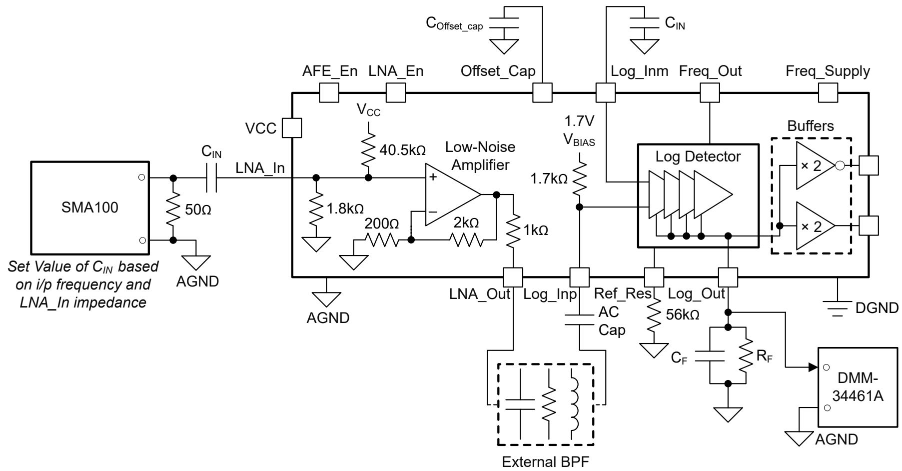


Figure 6-1. LOG300 Slope Characterization

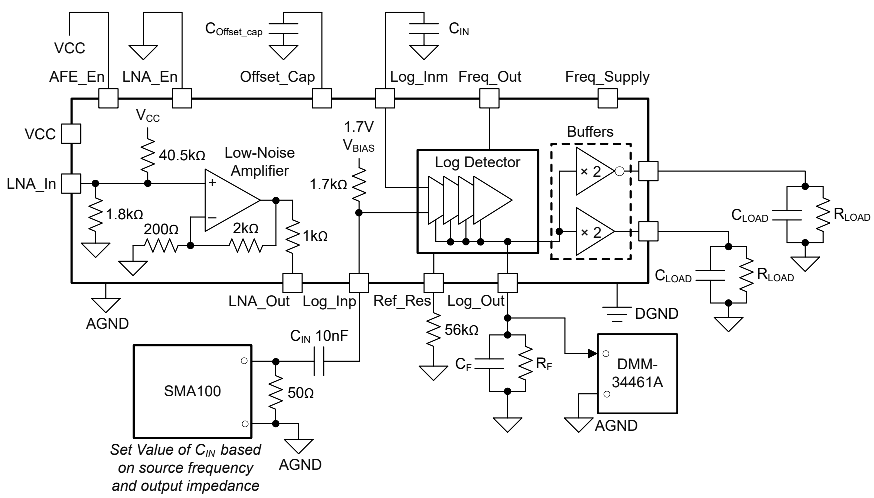


Figure 6-2. Log Detector Slope Characterization

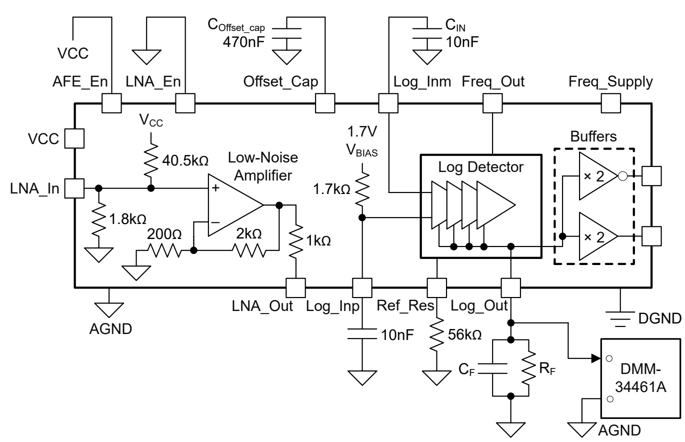


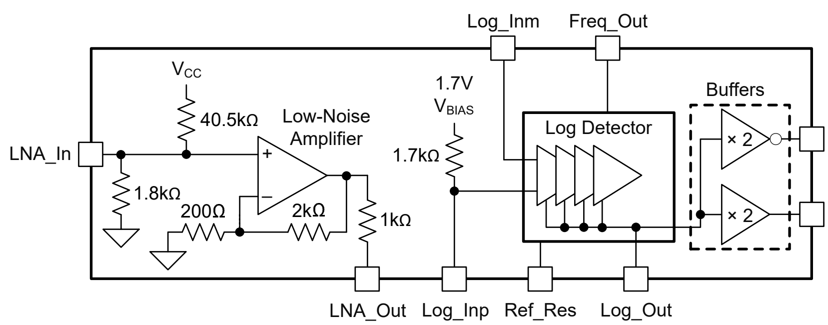
Figure 6-3. Log Detector Minimum Output Voltage Measurement

7 Detailed Description

7.1 Overview

The LOG300 is a highly sensitive analog front-end system for power measurements of up to 40MHz signals with a typical dynamic range of 98dB. The LOG300 is intended for use in a wide variety of applications like ultrasonic Rx signal chains, amplitude demodulation, signal power measurement, grid monitoring and so on. The LOG300 provides an analog envelope of an amplitude proportional to the log of the input signal. This behavior provides the application circuit precise input signal amplitude measurement without the need of high-speed signal acquisition components. The integrated frequency-detect feature enables zero-crossing and frequency measuring capability of the incoming signal.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Offset Correction Loop (OCL)

The LOG300 comes with an internal offset correction loop (OCL) designed to correct for any small offset voltage errors due to external factors or due to the input gain blocks mismatch. The LOG300 internal gain blocks offer very high gain; therefore, any small error at the input is sufficient to saturate the log output.

The Offset_Cap (see Section 6) sets the time constant of the offset correction loop. Set the value of the OCL pole to less than the incoming signal frequency so that the OCL does not respond to the incoming signal. Use the following formula to calculate the value of Offset_Cap based on the frequency of the incoming signal.

$$C_{Offset\_Cap}\left(nF\right) \geq \frac{6000}{Frequency\ of\ input\ signal\ (kHz)} \quad (1)$$

Where

- Offset capacitor must never be less than 1nF. If the formula yields a value of C_{Offset_Cap} less than 1nF, use 1nF.
- Using a value of C_{Offset_Cap} greater than the calculated value using above equation is acceptable since the OCL loop is set to a lower frequency.

7.3.2 Single and Differential Input

The Log Detector block of the LOG300 supports both single-ended and differential input signals. Irrespective of the type of input signal, the impedances of the Log_Inp and Log_Inm pins to AGND have to be matched.

The requirement for impedance matching arises from the fact that any supply noise or externally coupled noise passes through these impedances and the generated voltage. If the impedances are mismatched at the two inputs a differential voltage is seen by the Log Detector block thereby increasing the minimum output voltage at the Log_Out pin.

Achieving impedance matching for differential inputs can be straightforward. However for single-ended inputs, impedance matching can be quite complex. If board space is not limited TI recommends to copy the input structure at the Log_Inp pin as is on to the Log_Inm input. Please take note of the default internal output impedance of the LNA of 1kΩ when copying the structure to the Log_Inm pin.

If the above recommendation is not possible, match the impedances between the two pins at the frequency with the highest probability of noise coupling. For example if the VCC power is being derived by a DC/DC converter switching at a maximum frequency of 500kHz, using option 1 gives the best impedance matching between Log_Inp and Log_Inm. If the VCC ripple is at 100kHz then both option 1 and option 2 result in the same rejection response.

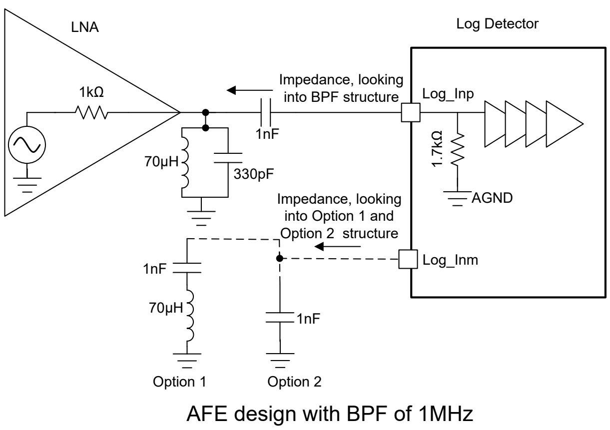


Figure 7-1. Impedance Structure at Log_Inp and Log_Inm

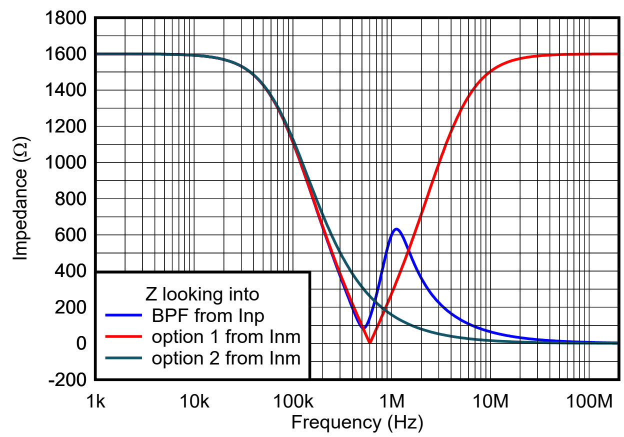


Figure 7-2. Impedance vs Frequency at Log_Inp and Log_Inm

7.3.3 Input Frequency Detect

The Log_Out pin creates an envelope proportional to the incoming signal; therefore, the frequency and phase information of the input signal is lost. The frequency detect feature enables the LOG300 to recover this frequency information. The frequency detect pin toggles at the same frequency as the input, and can therefore be used to calculate the input signal frequency or the input signal zero crossing points.

The internal circuit consists of a comparator with one of the inputs connected to the pin Log_In bias voltage and the other input of the comparator connected to the last stage of the Log Detector gain block (see Figure 7-3). Log_In is ac coupled; therefore, the incoming signal is biased to the internal bias voltage.

The comparator compares the gained Log_In (both single-ended and differential) signal biased at the internal bias voltage with the DC internal bias voltage, thereby toggling at every instance of a zero crossing. If the incoming signal is not a symmetric waveform or consists of multiple frequency content, the frequency detect feature compares the zero crossings of the incoming signal.

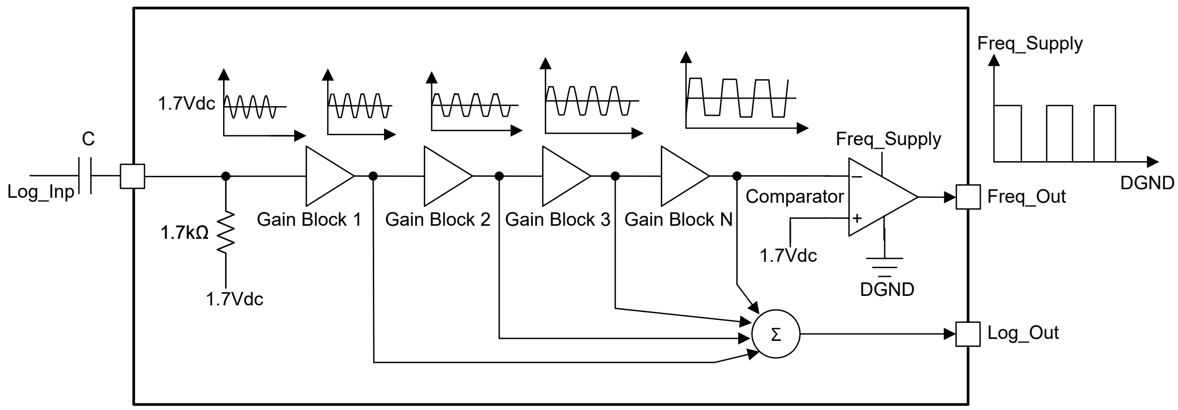


Figure 7-3. Internal Block Diagram for Frequency Detect

7.4 Device Functional Modes

The LOG300 offers three functional modes:

- AFE Disabled
  - In this mode, the complete AFE (LOG300) is disabled and consumes only about 100µA.
- LNA Disabled
  - In this mode, the LNA is disabled, while the Log Detector block is still operational. See Section 5.6 for detailed parameters in this mode.
  - Typically, this mode is used when the input sensitivity required is relaxed and the application prioritizes a lower quiescent current. Disabling the LNA helps save 2mA of quiescent current originally consumed by the LNA.
- Normal operating mode
  - In this mode, all blocks of the LOG300 are operational. See Section 5.7 for detailed parameters such as power consumption, acceptable supply, and input output range.
  - This mode can be entered by floating the LNA_En and AFE_En pins or by tying them to VCC.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LOG300 is a good fit for multiple applications involving ultrasound receive signal measurement, power, and energy measurements. The wide dynamic range and high input sensitivity makes the LOG300 an excellent option for applications such as the example in Section 8.2.1 involving measurement of low amplitude signals without the need of expensive, high-bandwidth, low-noise components.

8.2 Typical Application

8.2.1 Ultrasonic Distance Measurement

This design example demonstrates the circuit calculations and discrete component selection around the LOG300 to achieve a highly sensitive receive signal chain for a typical ultrasonic distance based measurement sensor.

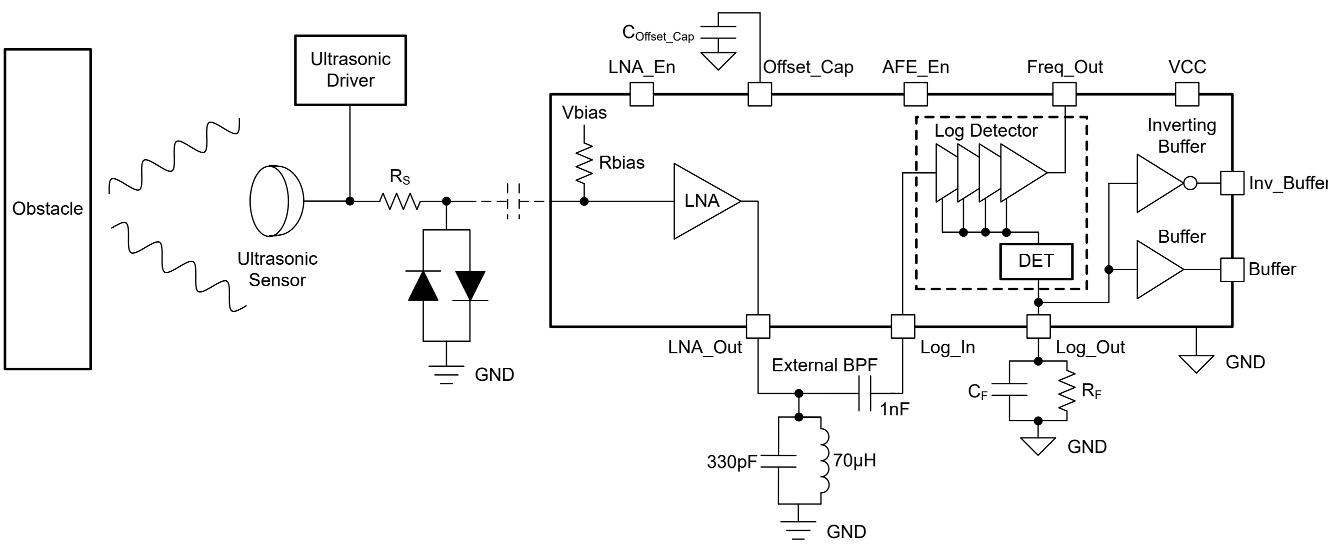


Figure 8-1. Ultrasonic Distance Sensor

8.2.1.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply (VCC)	5V
Minimum input signal measuring capability	$6\mu V_P$
Maximum input signal measuring capability: Linear	$200mV_P$
Maximum input signal handling capability (V_{max})	$100V_P$
Frequency of Tx and Rx signal	1MHz
Log_Out; Output range	0.5V to 4.5V

8.2.1.2 Detailed Design Procedure

The LOG300 supports a 5V VCC. Add a 10Ω and 10µF || 10nF close to the VCC pin to provide sufficient decoupling and immunity from external noise. This supply filter has a pole of 1.59kHz that is sufficiently less than the frequency of interest, which is 1MHz.

The absolute maximum voltage rating of pin LNA_In is ±1V. Add a back-to-back diode along with a series resistor (R_S) at the input of the LNA (see also Figure 8-1). The back-to-back diode protects the LNA_In pin from being exposed to any high voltages, especially during the transmit operation. Choose the series resistance value in accordance to the maximum power rating (P_{MAX}) of the back-to-back diode. The added series resistor contributes to the input noise and deteriorates the minimum input sensitivity.

$$R_S = \frac{(0.7V \times (V_{max} - 0.7V))}{P_{max}} \tag{2}$$

The maximum expected output voltage of the LNA with a back-to-back diode placed at the input is:

$$11V/V \times 0.7V_P = 7.7V_P \tag{3}$$

Since the LNA is only powered from a 5V supply; the maximum output is only $2.5V_P$.

The maximum input for the Log_Inp pin is $1.7V_P$ for 5VCC (see also Section 5.1); therefore, add a band-pass filter (BPF) of appropriate attenuation in the pass-band region so that the detector block absolute maximum voltage rating is not violated. In this particular case, ensure that the BPF has an attenuation of at least −3.3dB. A BPF of −4.3dB is shown in Figure 8-1.

Choose an Offset_Cap value based on Section 7.3.1.

Choose the value of C_F based on the required rise time of the Log_Out pin voltage (V_{Log_Out}). A lower-value C_F improves the rise time at the cost of higher ripple on the output envelope. For reference plots see also Section 5.8. Connect an oscilloscope at the Log_Out pin, triggered during the receive burst operation, to find the correct balance between the required rise time and the acceptable ripple.

The R_F resistor decides the input-to-output slope. The value of R_F in kΩ equals the input-to-output slope in mV/dB. In this example, calculate R_F using the below set of equations:

$$Slope\ mV/dB = R_F\ k\Omega = \frac{(Saturated\ output\ voltage - Minimum\ output\ voltage)}{(20\ x\ log\ (Maximum\ LNA\_In - Minimum\ LNA\_In))} \tag{4}$$

$$\text{Slope mV/dB} = \frac{(4.5V - 0.5V)}{(20 \times \log(200mV - 6\mu V))} \tag{5}$$

$$Slope\ (mV/dB) = 44mV/dB\ hence\ use\ R_F\ k\Omega = 44k\Omega \tag{6}$$

Note

The maximum and minimum Log_Out values have been relaxed to design for the output to operate well within the linear range.

The voltage measured at Log_Out can be traced back to calculate the input amplitude using the below equation:

$$Log\_Out_A = Slope\ x \left(\frac{Log\_In_A}{Log\_In_B}\right) + Log\_Out_B \tag{7}$$

$$Log\_In_A = \left(\frac{Log\_Out_A - Log\_Out_B}{Slope\ x\ Log\_In_B}\right) \tag{8}$$

Where : A stands for values of Log_Out and Log_In at the required measurement point and B stands for Log_Out and Log_In values at a known input value measured during factory calibration or production.

8.2.1.3 Application Curves

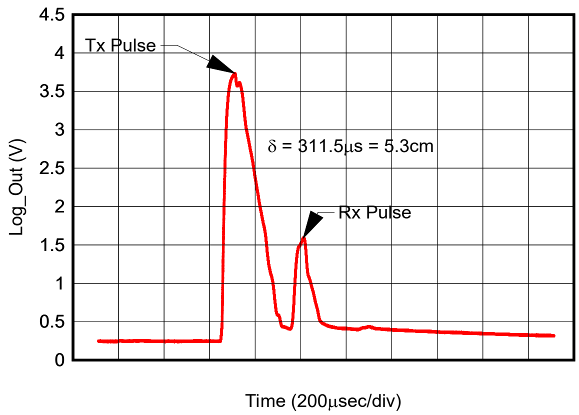


Figure 8-2. Log_Out Response for Ultrasonic Distance Measurement

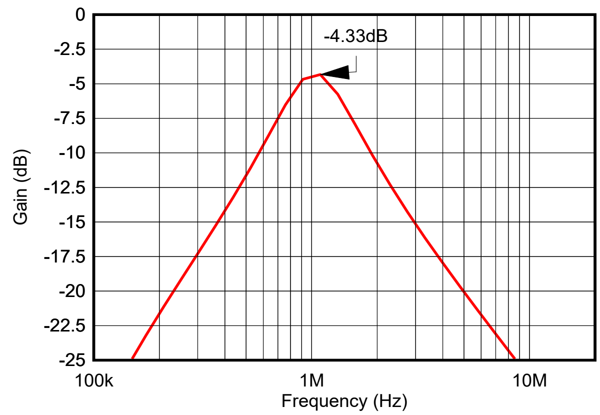


Figure 8-3. Band-Pass Filter Frequency Response

8.3 Power Supply Recommendations

The LOG300 contains two supply pins. The analog power supply pin (VCC) and the frequency detect block supply pin (Freq_Supply). Both pins can be biased at any voltage between 3V to 5.25V with respect to the AGND. While both these pins are connected to different circuitry internally, TI recommends to connect both of these pins to the same potential. Provide separate decoupling capacitors, resistors, and ferrite beads to these supply pins (see Section 8.4.2) to maintain sufficient immunity against cross coupling.

The LOG300 is sensitive to the noise coupling through the supply pins. Use a low-pass filter on the supply line with a cutoff frequency less than the incoming frequency signal.

For example if the incoming signal is 100kHz, and the band-pass filter has been tuned to achieve a center frequency of 100kHz, design a RC filter on the supply with a cut off frequency of at least 10kHz. For a higher signal frequency the RC values start diminishing to smaller values and hence the cut off frequency can be parked to any appropriate value.

An external band-pass filter if used between the LNA and the LOG detector block, along with a low-pass filter on the supply pins provides enough power-supply rejection to keep Log_Out unaffected.

8.4 Layout

8.4.1 Layout Guidelines

Follow these instructions to improve the performance and noise immunity of the LOG300:

- Provide a star connection style supply for Freq_supply and VCC. This connection enables better noise immunity and decoupling.
- Design Log_Inp, Log_Inm and LNA_In traces with guard traces to improve immunity against noise pickup. Use shielding when possible to improve radiated noise immunity.
- Place small capacitors on the AFE and LNA enable pins to allow high-frequency noise to be grounded before entering into the device.
- As per Section 7.3.2 the impedance seen from Log_Inp and Log_Inm to the external circuit must be the same. The trace length to Log_Inp and Log_Inm must be kept similar to keep impedance matched.
- Keep minimal capacitance at the Freq_Out pin either by placing the load circuit close to the pin or by removing the analog ground plane under the output trace or both.
- Dedicate one layer of the PCB for a solid analog ground pour to terminate all the capacitors used across the pins using sufficient vias.

8.4.2 Layout Example

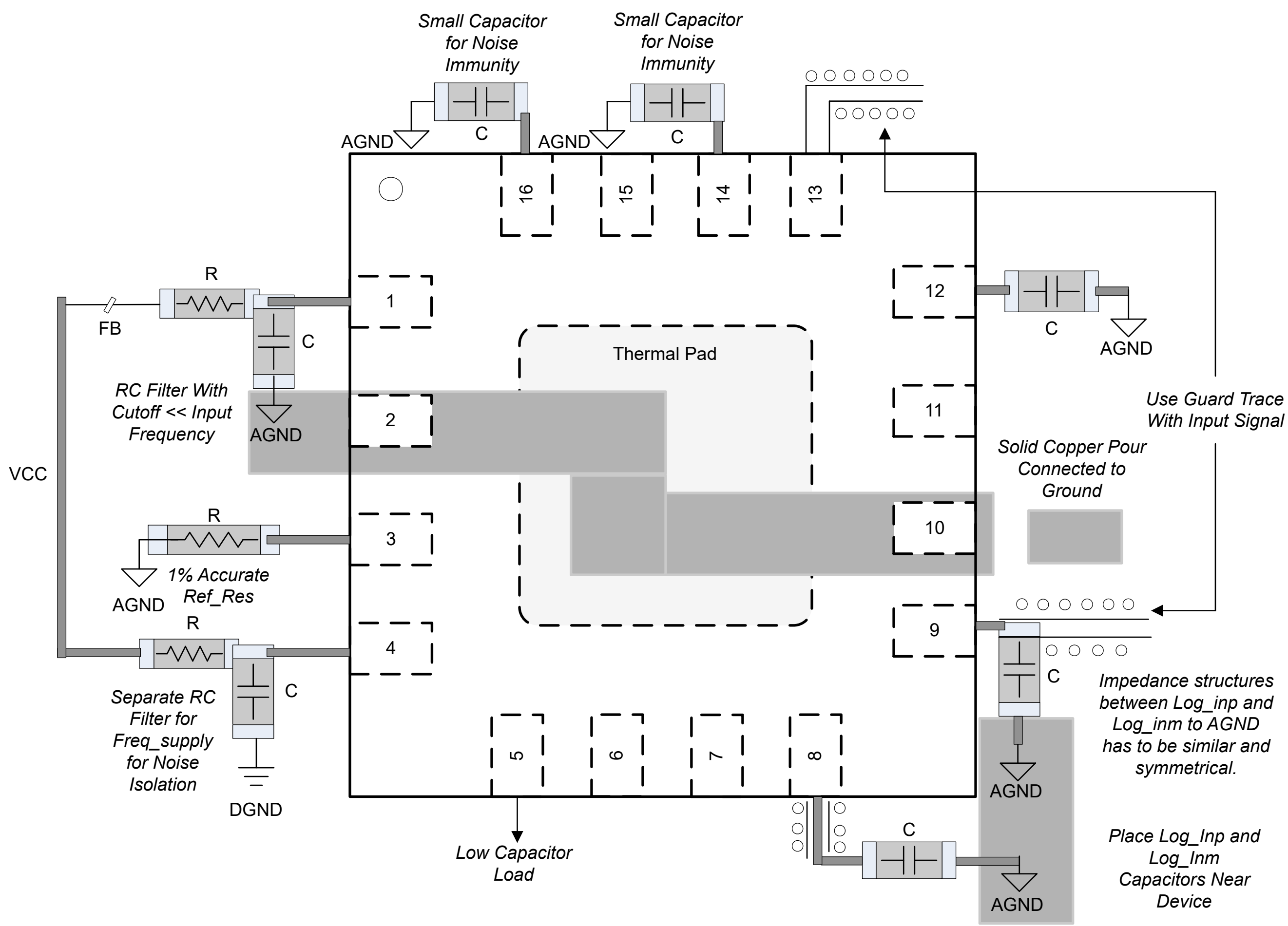


Figure 8-4. Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2024) to Revision A (October 2024)	Page
• Changed document status from advanced information (preview) to production data (active)	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XLOG300RGTR	ACTIVE	VQFN	RGT	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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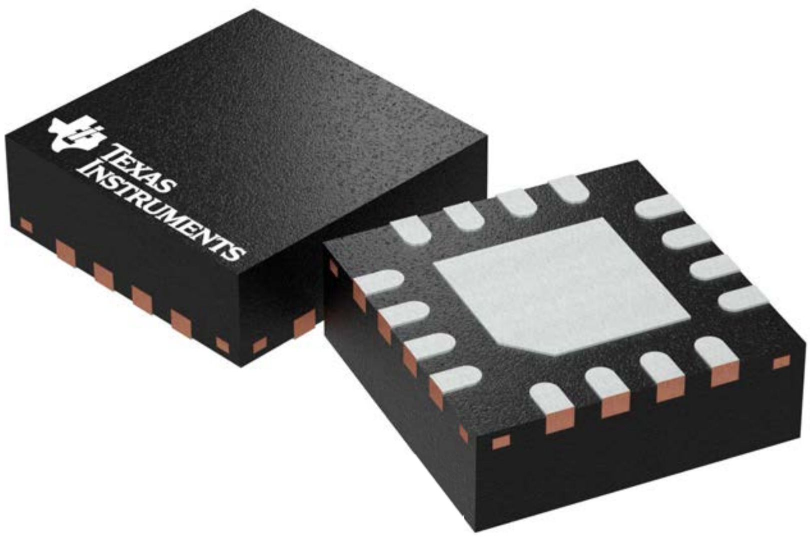
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

RGT 16 VQFN - 1 mm max height

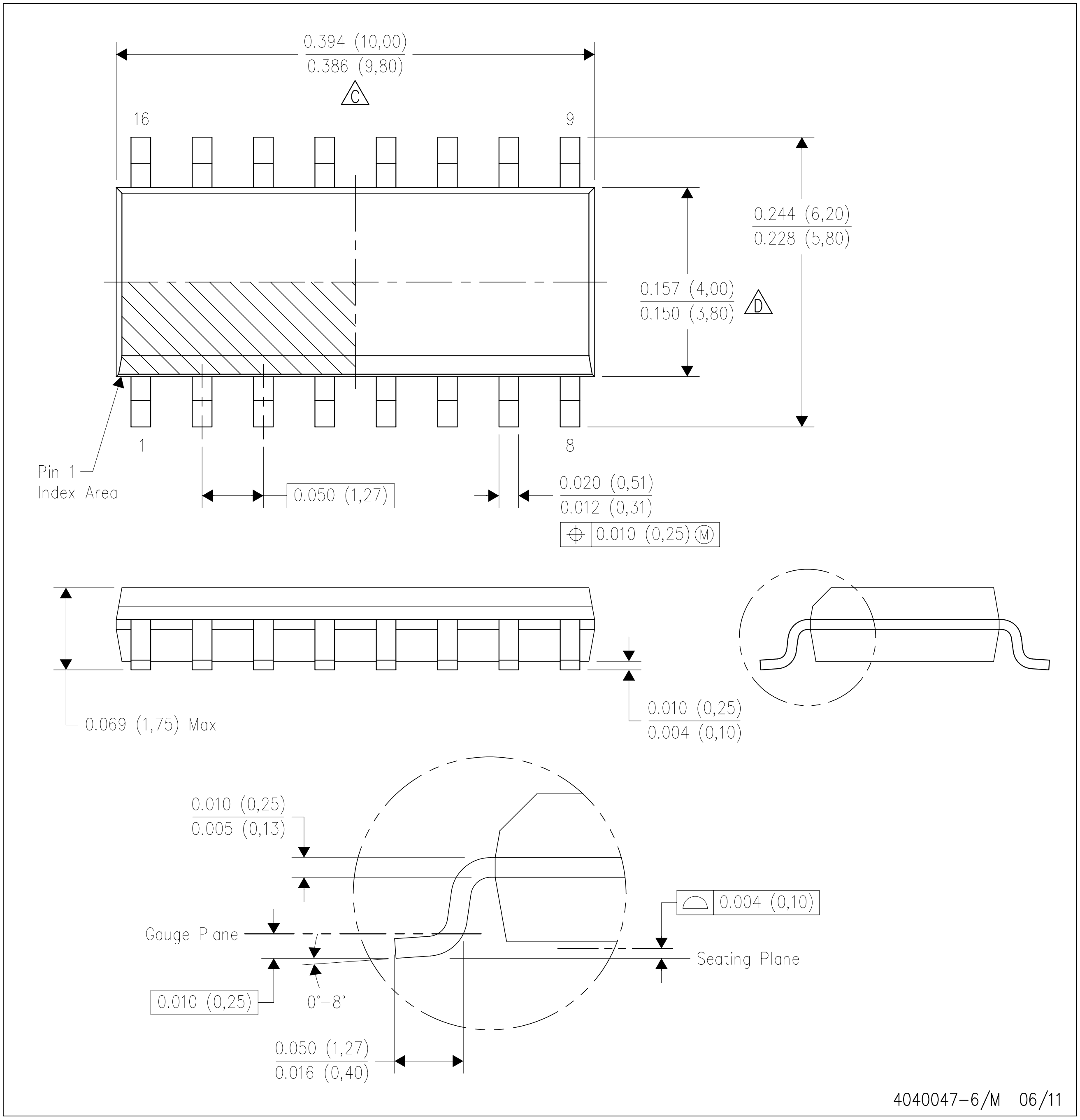
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/I

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE AND DISCLAIMER

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