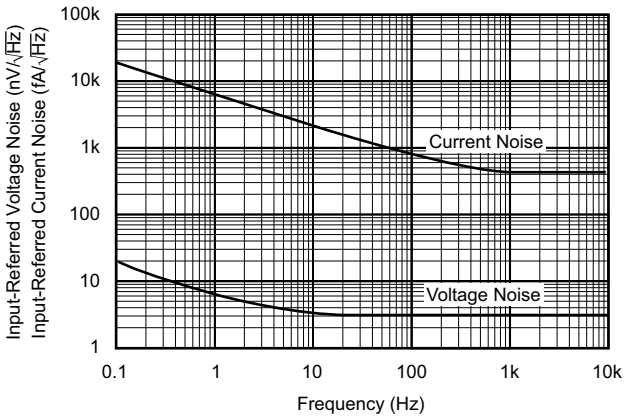
OPAx227, OPAx228 High-Precision, Low-Noise Operational Amplifiers

1 Features

- Low noise: 3 nV/√Hz
- Wide bandwidth:
  - OPA227: 8 MHz, 2.3 V/µs
  - OPA228: 33 MHz, 10 V/µs
- Settling time: 5 µs
- High CMRR: 138 dB
- High open-loop gain: 160 dB
- Low input bias current: 10 nA maximum
- Low offset voltage: 75 µV maximum
- Wide supply range: ±2.5 V to ±18 V
- Single, dual, and quad versions

2 Applications

- Data acquisition (DAQ)
- Condition monitoring sensor
- Spectrum analyzer
- Professional audio amplifier (rack mount)
- Industrial AC-DC



Input Voltage and Current Noise Spectral Density vs Frequency

3 Description

The OPAx227 and OPAx228 series operational amplifiers combine low noise and wide bandwidth with high precision to make them an excellent choice for applications requiring both ac and precision dc performance.

The OPAx227 are unity-gain stable and features high slew rate (2.3 V/µs) and wide bandwidth (8 MHz). The OPAx228 are optimized for closed-loop gains of 5 or greater, and offers higher speed with a slew rate of 10 V/µs and a bandwidth of 33 MHz.

The OPAx227 and OPAx228 series operational amplifiers are an excellent choice for professional audio equipment. In addition, low quiescent current and low cost make these op amps an excellent choice for portable applications requiring high precision.

The OPAx227 and OPAx228 series operational amplifiers are pin-for-pin replacements for the industry-standard OP27 and OP37 with substantial improvements across the board. The dual and quad versions are available for space savings and per-channel cost reduction.

The OPAx227 and OPAx228, are available in DIP-8 and SO-8 packages. The OPA4227 and OPA4228 are available in DIP-14 and SO-14 packages with standard pin configurations. Operation is specified from –40°C to +85°C.

Device Information

PART NUMBER	CHANNELS	PACKAGE(1)
OPA227, OPA228	Single	P (PDIP, 8)
		D (SOIC, 8)
OPA2227, OPA2228	Dual	P (PDIP, 8)
		D (SOIC, 8)
OPA4227, OPA4228	Quad	N (PDIP, 14)
		D (SOIC, 14)

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

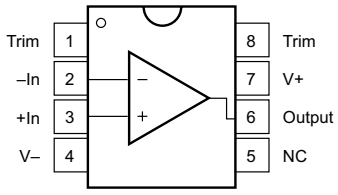
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2015) to Revision C (November 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added dual supply voltage in *Absolute Maximum Ratings*	5
• Added symbol for output short circuit in *Absolute Maximum Ratings*	5
• Added symbol for operating temperature in *Absolute Maximum Ratings*	5
• Added symbol for junction temperature in *Absolute Maximum Ratings*	5
• Changed HBM value in *ESD Ratings*	5
• Added CDM in *ESD Ratings*	5
• Changed to single supply voltage and dual supply voltage in *Recommended Operating Conditions*	5
• Changed format of thermal information tables for better clarity	6
• Changed package to P (PDIP) for OPA222xP and OPA222xPA devices in *Thermal Information*	6
• Deleted redundant power supply voltage from *Electrical Characteristics of OPAx227* because same information already listed in *Recommended Operating Conditions*	7
• Deleted redundant temperature from *Electrical Characteristics of OPAx227* because same information already listed in *Recommended Operating Conditions*	7
• Deleted redundant power supply voltage from *Electrical Characteristics of OPAx228* because same information already listed in *Recommended Operating Conditions*	9
• Deleted redundant temperature from *Electrical Characterisitcs of OPAx228* because same information already listed in *Recommended Operating Conditions*	9

Changes from Revision A (January 2005) to Revision B (April 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions



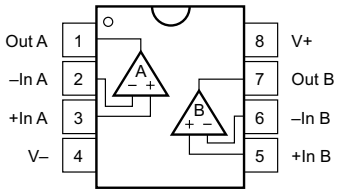
DIP-8, SO-8

NC = Not Connected

Figure 5-1. OPA227, OPA228: D (8-Pin SOIC) or P (8-Pin PDIP) Package (Top View)

Table 5-1. Pin Functions: OPA227 and OPA228

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	Offset Trim	Input	Input offset voltage trim (leave floating if not used)
2	-In	Input	Inverting input
3	+In	Input	Noninverting input
4	V-	—	Negative (lowest) power supply
5	NC	—	No internal connection (can be left floating)
6	Output	Output	Output
7	V+	—	Positive (highest) power supply
8	Trim	—	Input offset voltage trim (leave floating if not used)

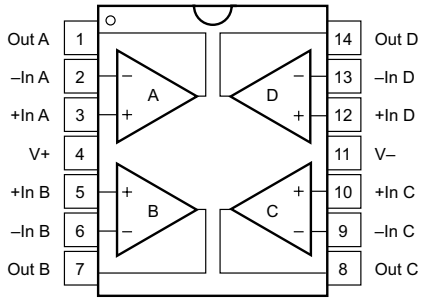


DIP-8, SO-8

Figure 5-2. OPA2227, OPA2228: D (8-Pin SOIC) or P (8-Pin PDIP) Package (Top View)

Table 5-2. Pin Functions: OPA2227 and OPA2228

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	Out A	Output	Output channel A
2	–In A	Input	Inverting input channel A
3	+In A	Input	Noninverting input channel A
4	V-	—	Negative (lowest) power supply
5	+In B	Input	Noninverting input channel B
6	–In B	Input	Inverting input channel B
7	Out B	Output	Output channel B
8	V+	—	Positive (highest) power supply



DIP-14, SO-14

Figure 5-3. OPA4227, OPA4228: D (14-Pin SOIC) or N (14-Pin PDIP) Package (Top View)

Table 5-3. Pin Functions: OPA4227 and OPA4228

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	Out A	Output	Output channel A
2	-In A	Input	Inverting input channel A
3	+In A	Input	Noninverting input channel A
4	V+	—	Positive (highest) power supply
5	+In B	Input	Noninverting input channel B
6	-In B	Input	Inverting input channel B
7	Out B	Output	Output channel B
8	Out C	Output	Output channel C
9	-In C	Input	Inverting input channel C
10	+In C	Input	Noninverting input channel C
11	V-	—	Negative (lowest) power supply
12	+In D	Input	Noninverting input channel D
13	-In D	Input	Inverting input channel D
14	Out D	Output	Output channel D

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Single supply voltage, V_S = (V+) – (V–)			36	V
	Dual supply voltage, V_S = (V+) – (V–)			±18	
	Signal input pins	Voltage	(V–) – 0.7	(V+) + 0.7	V
		Current		20	mA
I_{SC}	Output short circuit(2)		Continuous		
T_A	Operating temperature		–55	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Single supply voltage, V_S = (V+) – (V–)	4.5	30	36	V
	Dual supply voltage, V_S = (V+) – (V–)	±2.25	±15	±18	
	Specified temperature	–40		85	°C

6.4 Thermal Information: OPA227, OPA228

THERMAL METRIC[1]		OPA227P, OPA227PA, OPA228P, OPA228PA	OPA227U, OPA227UA, OPA228U, OPA228UA	UNIT
		P (PDIP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.9	110.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	37.7	52.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.1	52.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.1	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26	51.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information: OPA2227, OPA2228

THERMAL METRIC[1]		OPA2227P, OPA2227PA, OPA2228P, OPA2228PA	OPA2227U, OPA2227UA, OPA2228U, OPA2228UA	UNIT
		P (PDIP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	101.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	52.2	46.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.3	45.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	6.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.5	42.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Thermal Information: OPA4227, OPA4228

THERMAL METRIC[1]		OPA4227P, OPA4227PA, OPA4228P, OPA4228PA	OPA4227U, OPA4227UA, OPA4228U, OPA4228UA	UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.5	65	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	20	23.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.9	20.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.3	19.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics: OPAx227

at T_A = +25°C, V_S = ±5 V to ±15 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	U, P grades			±5	±75	μV
			T_A = –40°C to +85°C			±100	
		UA, PA grades			±10	±200	
			T_A = –40°C to +85°C			±200	
dV_{OS}/dT	Input offset voltage drift	U, P grades	T_A = –40°C to +85°C		±0.1	±0.6	μV/°C
		UA, PA grades	T_A = –40°C to +85°C		±0.3	±2	
PSRR	Power-supply rejection ratio	V_S = ±2.5 V to ±18 V			±0.5	±2	μV/V
			T_A = –40°C to +85°C			±2	
	Long-term drift				0.2		μV/mo
	Channel separation (dual, quad)	DC			0.2		μV/V
		f = 1 kHz, R_L = 5 kΩ			110		dB
INPUT BIAS CURRENT							
I_B	Input bias current				±2.5	±10	nA
		T_A = –40°C to +85°C				±10	
I_{OS}	Input offset current				±2.5	±10	nA
		T_A = –40°C to +85°C				±10	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			90		nV_{PP}
					15		nV_{RMS}
e_n	Input voltage noise density	f = 10 Hz			3.5		nV/√Hz
		f = 100 Hz			3		
		f = 1 kHz			3		
i_n	Input current noise density	f = 1 kHz			0.4		pA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) + 2 V < V_{CM} < (V+) – 2 V		120	138		dB
			T_A = –40°C to +85°C	120			
INPUT IMPEDANCE							
	Differential				10 || 12		MΩ || pF
	Common-mode	V_{CM} = (V–) + 2 V to (V+) – 2 V			1 || 3		GΩ || pF

6.7 Electrical Characteristics: OPAx227 (continued)

at T_A = +25°C, V_S = ±5 V to ±15 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 2 V < V_O < (V+) – 2 V		132	160		dB
			T_A = –40°C to +85°C	132			
		(V–) + 3.5 V < V_O < (V+) – 3.5 V, R_L = 600 Ω		132	160		
			T_A = –40°C to +85°C	132			
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				8		MHz
SR	Slew rate				2.3		V/µs
	Settling time	G = 1, 10-V step, C_L = 100 pF	To 0.1%		5		µs
			To 0.01%		5.6		
	Overload recovery time	V_{IN} × G = V_S			1.3		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00005		%
OUTPUT							
	Voltage output	T_A = –40°C to +85°C		(V–) + 2		(V+) + 2	V
			R_L = 600 Ω	(V–) + 3.5		(V+) + 3.5	V
I_{SC}	Short-circuit current				±45		mA
C_{LOAD}	Capacitive load drive				See Typical Characteristics		
Z_O	Open-loop output impedance	f = 1 MHz			27		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			±3.7	±3.8	mA
			T_A = –40°C to +85°C			±4.2	

6.8 Electrical Characteristics: OPAx228

at T_A = +25°C, V_S = ±5 V to ±15 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	U, P grades			±5	±75	μV
			T_A = –40°C to +85°C			±100	
		UA, PA grades			±10	±200	
			T_A = –40°C to +85°C			±200	
dV_{OS}/dT	Input offset voltage drift	U, P grades	T_A = –40°C to +85°C		±0.1	±0.6	μV/°C
		UA, PA grades	T_A = –40°C to +85°C		±0.3	±2	
PSRR	Power-supply rejection ratio	V_S = ±2.5 V to ±18 V			±0.5	±2	μV/V
			T_A = –40°C to +85°C			±2	
	Long-term drift				0.2		μV/mo
	Channel separation (dual, quad)	DC			0.2		μV/V
		f = 1 kHz, R_L = 5 kΩ			110		dB
INPUT BIAS CURRENT							
I_B	Input bias current				±2.5	±10	nA
		T_A = –40°C to +85°C				±10	
I_{OS}	Input offset current				±2.5	±10	nA
		T_A = –40°C to +85°C				±10	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			90		nV_{PP}
					15		nV_{RMS}
e_n	Input voltage noise density	f = 10 Hz			3.5		nV/√Hz
		f = 100 Hz			3		
		f = 1 kHz			3		
i_n	Input current noise density	f = 1 kHz			0.4		pA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) + 2 V < V_{CM} < (V+) – 2 V		120	138		dB
			T_A = –40°C to +85°C	120			
INPUT IMPEDANCE							
	Differential				10 || 12		MΩ || pF
	Common-mode	V_{CM} = (V–) + 2 V to (V+) – 2 V			1 || 3		GΩ || pF

6.8 Electrical Characteristics: OPAx228 (continued)

at T_A = +25°C, V_S = ±5 V to ±15 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 2 V < V_O < (V+) – 2 V		132	160		dB
			T_A = –40°C to +85°C	132			
		(V–) + 3.5 V < V_O < (V+) – 3.5 V, R_L = 600 Ω		132	160		
			T_A = –40°C to +85°C	132			
FREQUENCY RESPONSE							
	Minimum closed-loop gain				5		V/V
GBW	Unity gain bandwidth				33		MHz
SR	Slew rate				11		V/µs
	Settling time	G = 1, 10-V step, C_L = 100 pF	To 0.1%		1.5		µs
			To 0.01%		2		
	Overload recovery time	V_{IN} × G = V_S			0.6		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00005		%
OUTPUT							
	Voltage output	T_A = –40°C to +85°C		(V–) + 2		(V+) + 2	V
			R_L = 600 Ω	(V–) + 3.5		(V+) + 3.5	
I_{SC}	Short-circuit current				±45		mA
C_{LOAD}	Capacitive load drive				See Typical Characteristics		
Z_O	Open-loop output impedance	f = 1 MHz			27		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			±3.7	±3.8	mA
			T_A = –40°C to +85°C			±4.2	

6.9 Typical Characteristics

At T_A = 25°C, R_L = 10 kΩ, and V_S = ±15 V, unless otherwise noted.

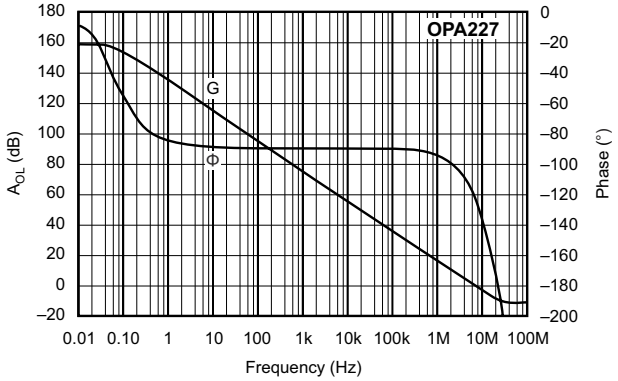


Figure 6-1. Open-Loop Gain and Phase vs Frequency

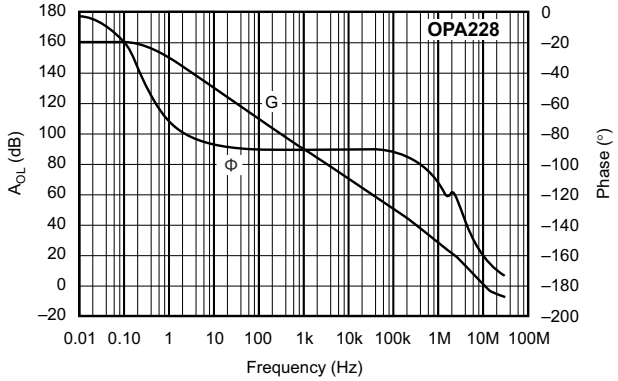


Figure 6-2. Open-Loop Gain and Phase vs Frequency

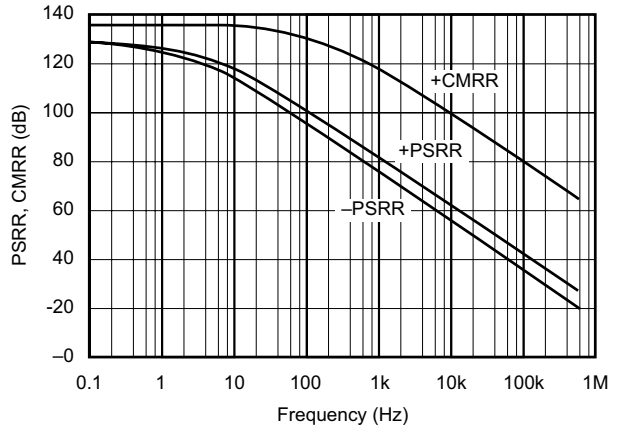


Figure 6-3. Power Supply and Common-Mode Rejection Ratio vs Frequency

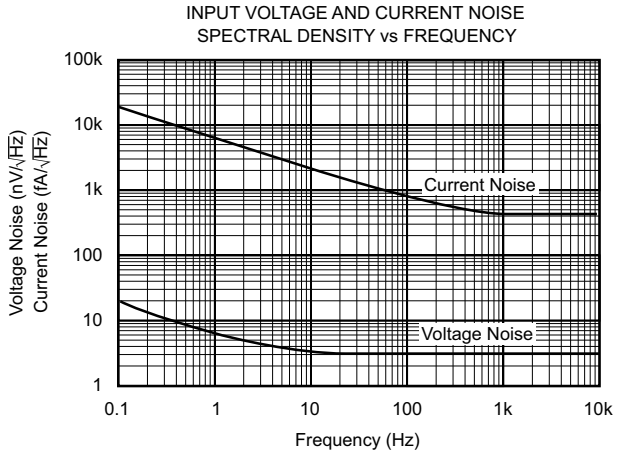


Figure 6-4. Input Voltage and Current Noise Spectral Density vs Frequency

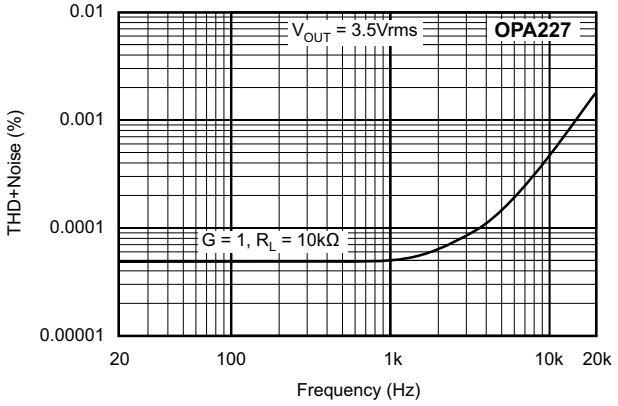


Figure 6-5. Total Harmonic Distortion + Noise vs Frequency

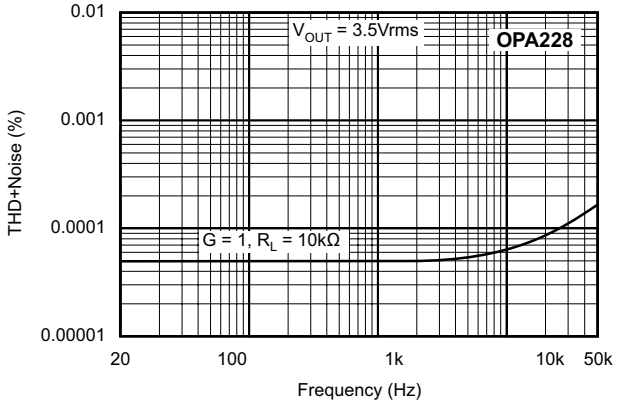


Figure 6-6. Total Harmonic Distortion + Noise vs Frequency

6.9 Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, and V_S = ±15 V, unless otherwise noted.

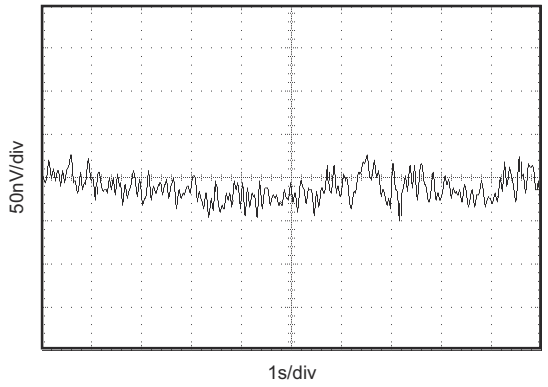


Figure 6-7. Input Noise Voltage vs Time

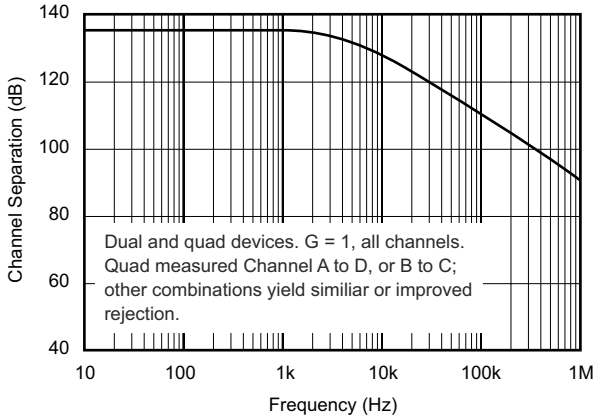


Figure 6-8. Channel Separation vs Frequency

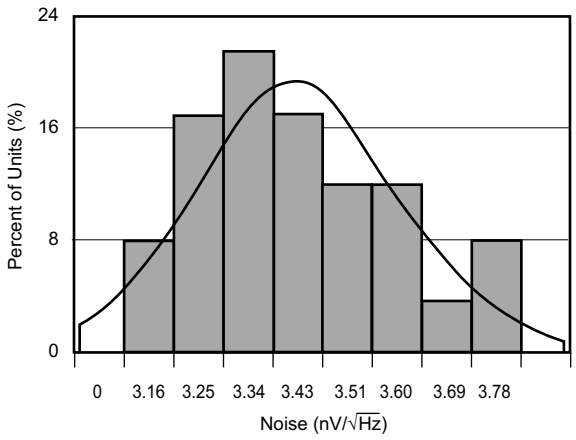


Figure 6-9. Voltage Noise Distribution (10 Hz)

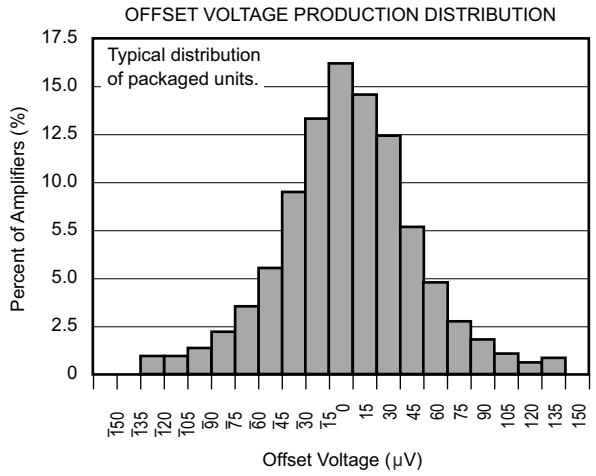


Figure 6-10. Offset Voltage Production Distribution

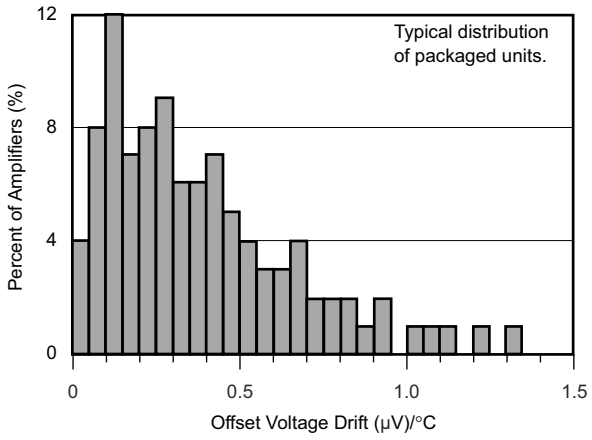


Figure 6-11. Offset Voltage Drift Production Distribution

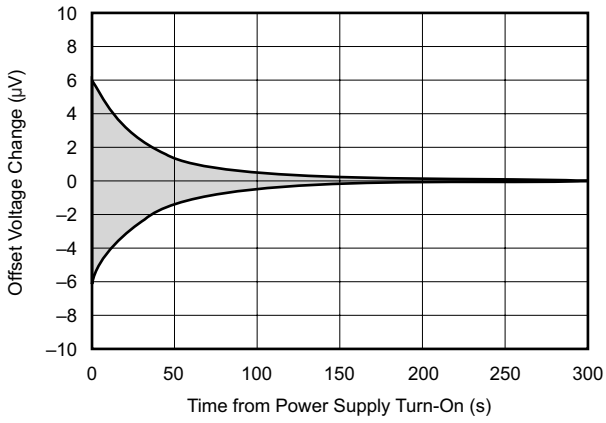


Figure 6-12. Warm-Up Offset Voltage Drift

6.9 Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, and V_S = ±15 V, unless otherwise noted.

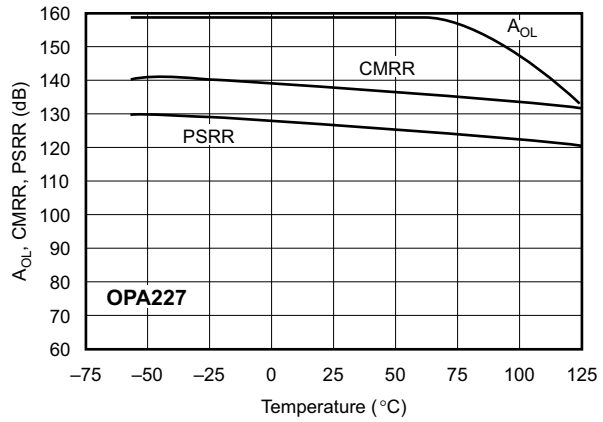


Figure 6-13. A_{OL}, CMRR, PSRR vs Temperature

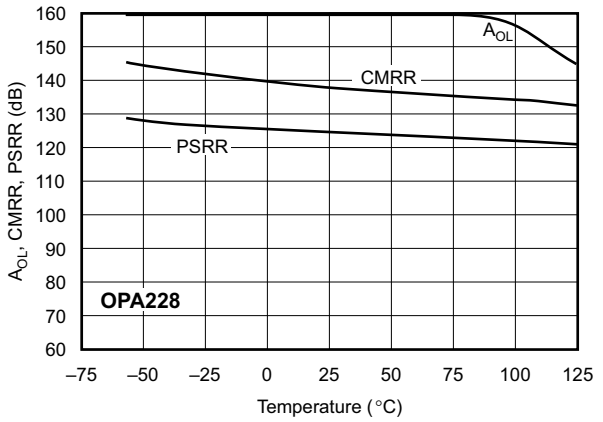


Figure 6-14. A_{OL}, CMRR, PSRR vs Temperature

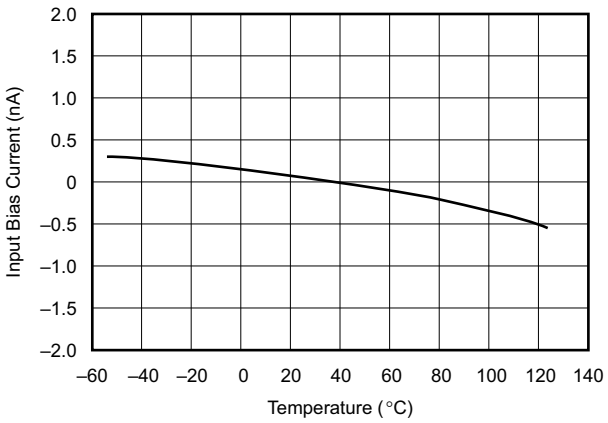


Figure 6-15. Input Bias Current vs Temperature

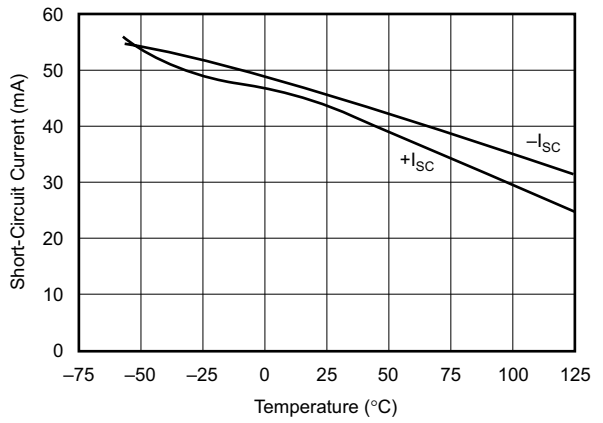


Figure 6-16. Short-Circuit Current vs Temperature

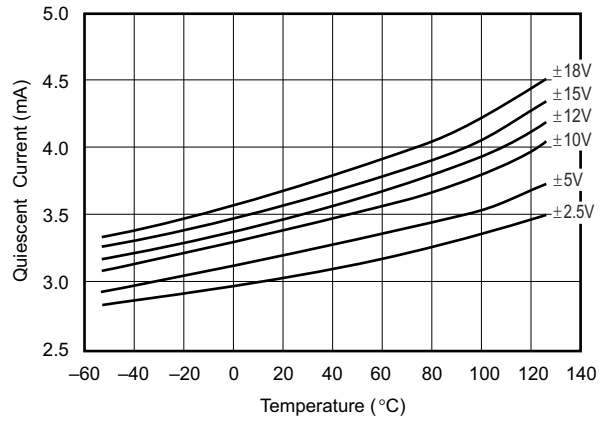


Figure 6-17. Quiescent Current vs Temperature

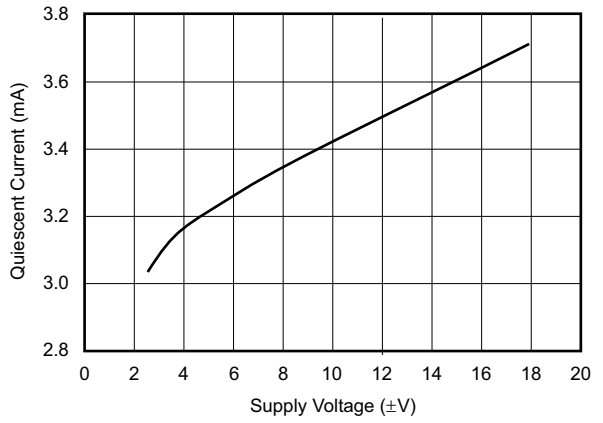


Figure 6-18. Quiescent Current vs Supply Voltage

6.9 Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, and V_S = ±15 V, unless otherwise noted.

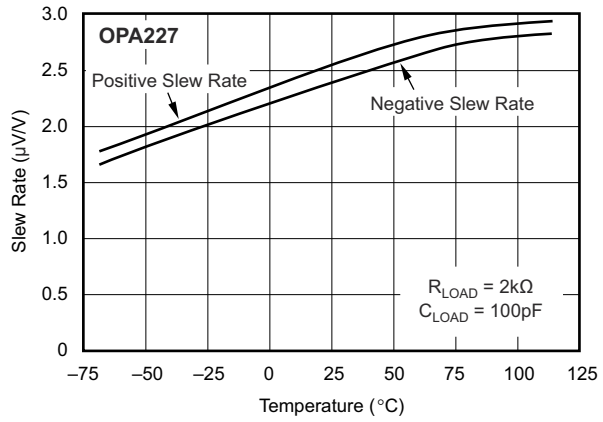


Figure 6-19. Slew Rate vs Temperature

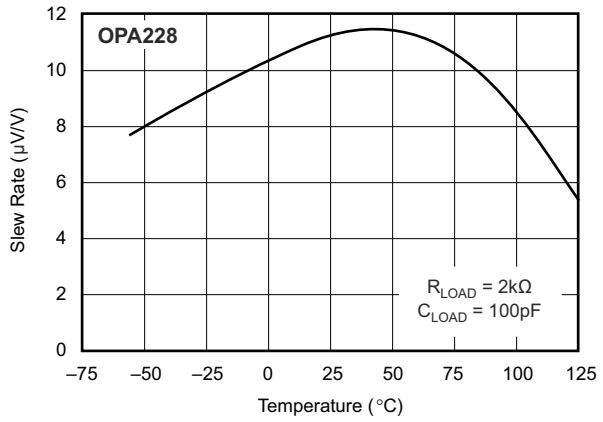


Figure 6-20. Slew Rate vs Temperature

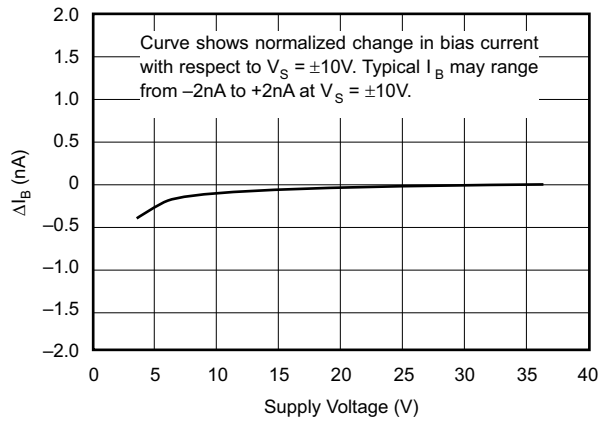


Figure 6-21. Change in Input Bias Current vs Power Supply Voltage

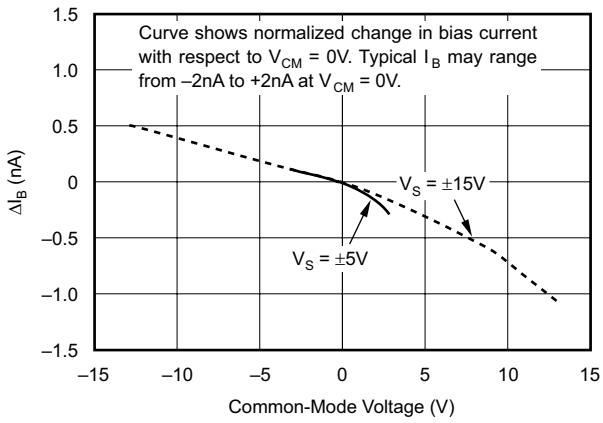


Figure 6-22. Change in Input Bias Current vs Common-Mode Voltage

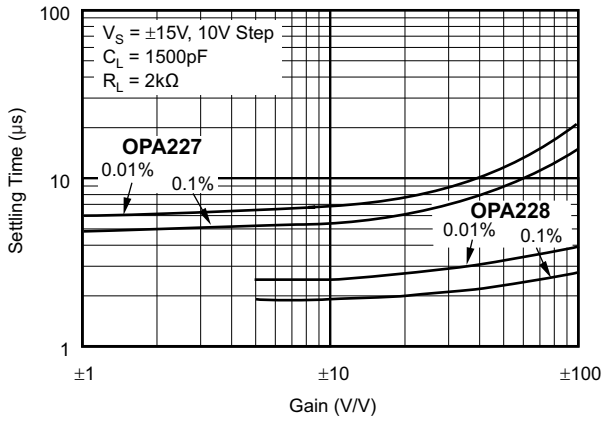


Figure 6-23. Settling Time vs Closed-Loop Gain

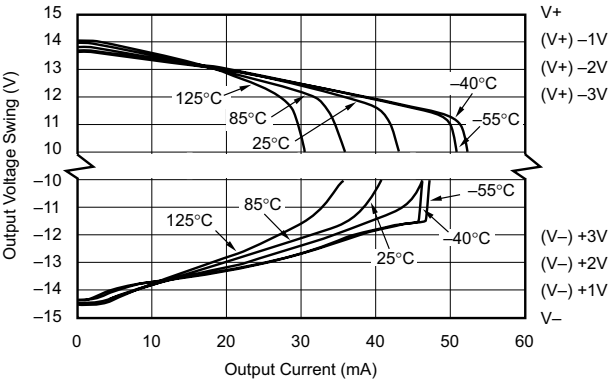


Figure 6-24. Output Voltage Swing vs Output Current

6.9 Typical Characteristics (continued)

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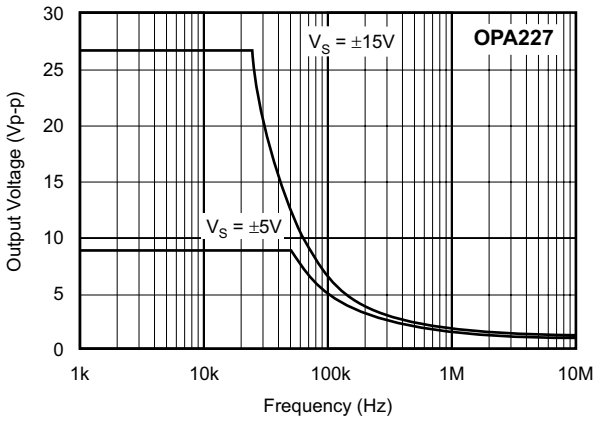


Figure 6-25. Maximum Output Voltage vs Frequency

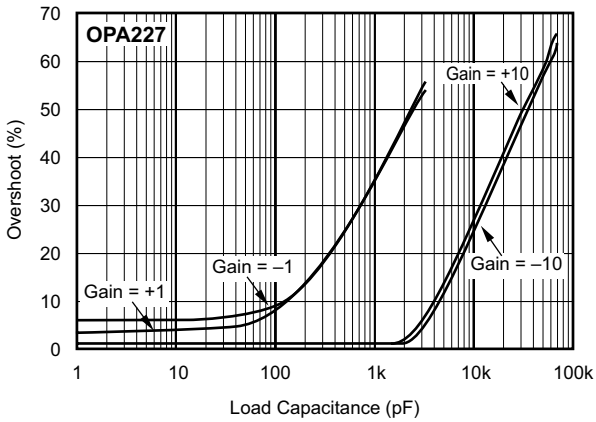
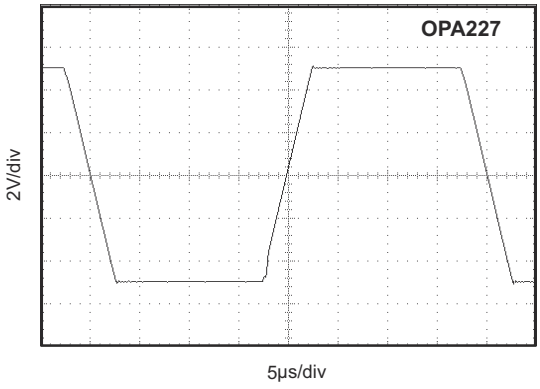
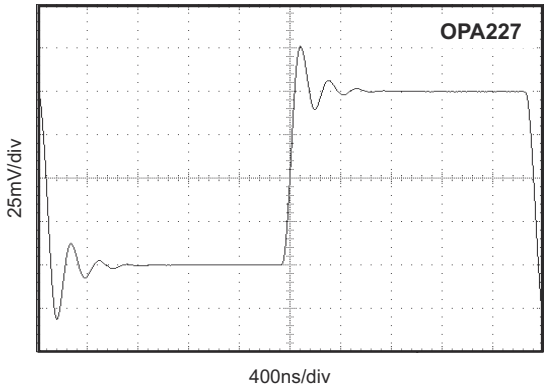


Figure 6-26. Small-Signal Overshoot vs Load Capacitance



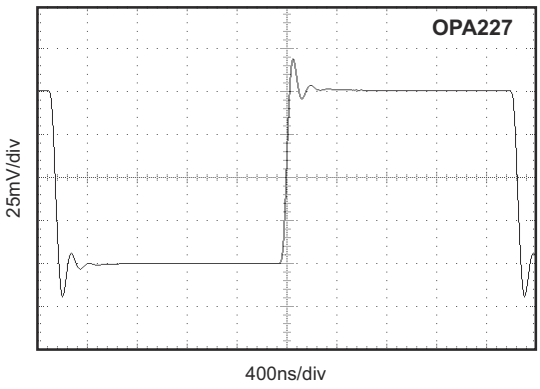
G = –1, C_L = 1500 pF

Figure 6-27. Large-Signal Step Response



G = 1, C = 1000 pF

Figure 6-28. Small-Signal Step Response



G = 1, C_L = 5 pF

Figure 6-29. Small-Signal Step Response

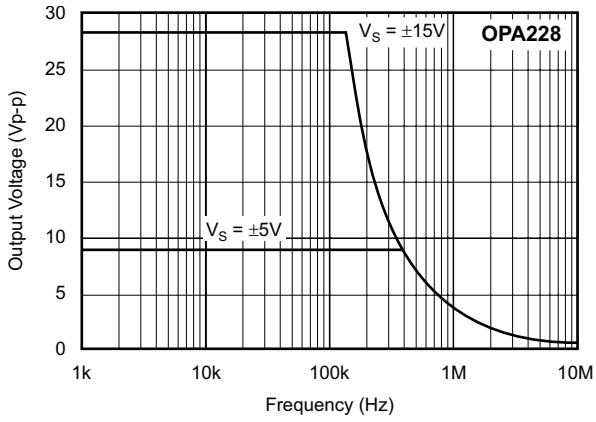


Figure 6-30. Maximum Output Voltage vs Frequency

6.9 Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, and V_S = ±15 V, unless otherwise noted.

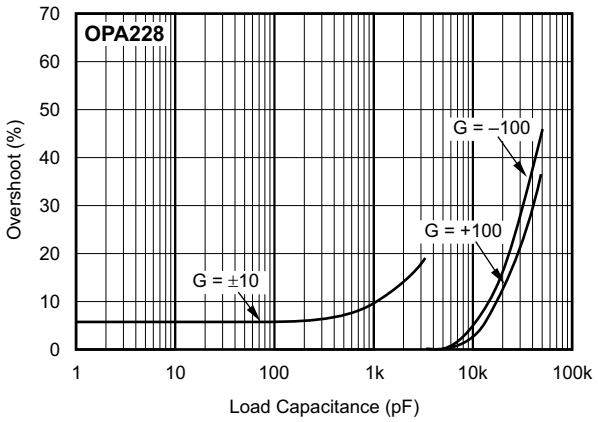
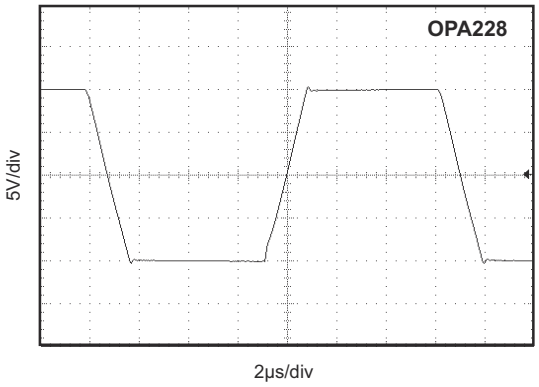
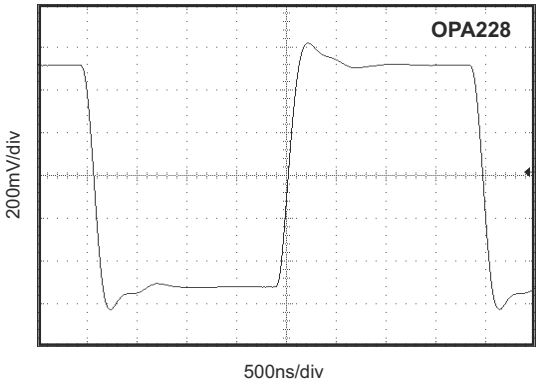


Figure 6-31. Small-Signal Overshoot vs Load Capacitance



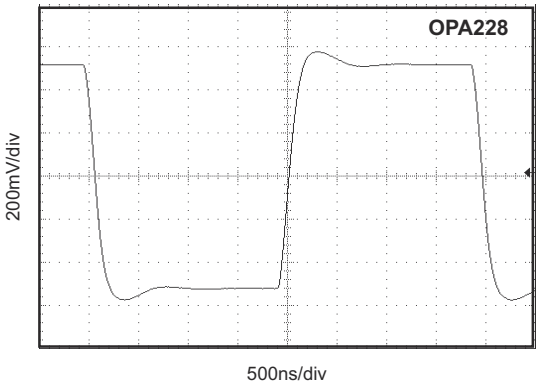
G = –10, C_L = 100 pF

Figure 6-32. Large-Signal Step Response



G = 10, C_L = 1000 pF R_L = 1.8 kΩ

Figure 6-33. Small-Signal Step Response



G = 10, C_L = 1000 pF R_L = 1.8 kΩ

Figure 6-34. Small-Signal Step Response

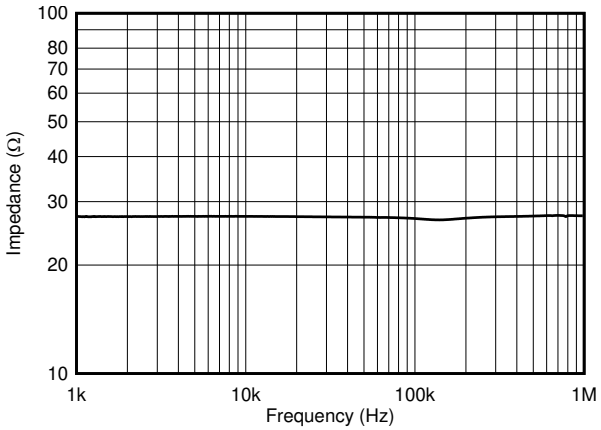


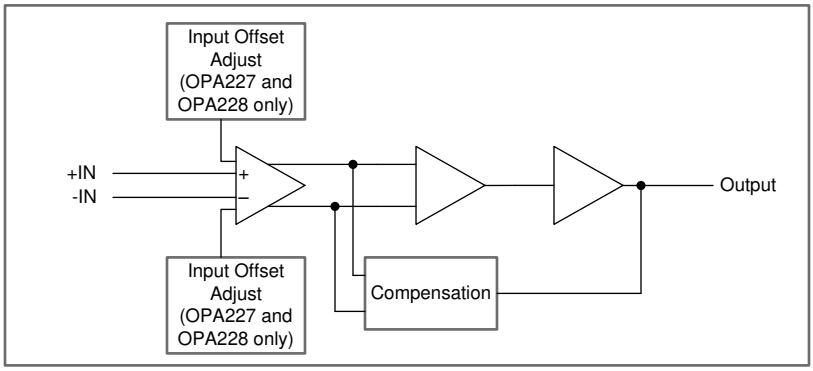
Figure 6-35. Open-loop Output Impedance

7 Detailed Description

7.1 Overview

The OPAx22x series operational amplifiers combine low noise and wide bandwidth with high precision to make them an excellent choice for applications requiring both ac and precision dc performance. The OPAx227 are unity-gain stable and features high slew rate (2.3 V/µs) and wide bandwidth (8 MHz). The OPAx228 are optimized for closed-loop gains of 5 or greater, and offer higher speed with a slew rate of 10 V/µs and a bandwidth of 33 MHz.

7.2 Functional Block Diagram



7.3 Feature Description

The OPAx22x series are unity-gain stable and free from unexpected output phase reversal, making these devices easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies can require decoupling capacitors close to the device pins. In most cases 0.1-µF capacitors are adequate.

7.3.1 Offset Voltage and Drift

The OPAx22x series have very low offset voltage and drift. To achieve highest dc precision, optimize the circuit layout and mechanical conditions. Connections of dissimilar metals can generate thermal potentials at the operational amplifier inputs, which can degrade the offset voltage and drift. These thermocouple effects can exceed the inherent drift of the amplifier and ultimately degrade performance. The thermal potentials can be made to cancel by making sure that the potentials are equal at both input terminals. In addition:

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as those created by cooling fans.

7.3.2 Operating Voltage

The OPAx22x series of operational amplifiers operate from ±2.5-V to ±18-V dual supplies with excellent performance. Unlike most operational amplifiers that are specified at only one supply voltage, the OPA227 series is specified for real-world applications; a single set of specifications applies over the ±5-V to ±15-V supply range. The OPAx22x devices are specified for use with ±5-V to ±15-V power supplies. Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPAx22x series can operate with as little as 5 V between the supplies and with up to 36 V between the supplies. For example, the positive supply can be set to 25 V and the negative supply set to –5 V, or vice versa. Key parameters are specified over the temperature range of –40°C to +85°C. Parameters that vary significantly with operating voltage or temperature are shown in *Section 6.9*.

7.3.3 Offset Voltage Adjustment

The OPAx22x series are laser-trimmed for very low offset and drift so most applications do not require external adjustment. However, the OPA227 and OPA228 (single versions) provide offset voltage trim connections on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 7-1. Use this adjustment only to null the offset of the operational amplifier. DO not use this adjustment to compensate for offsets created elsewhere in the system because additional temperature drift can be introduced.

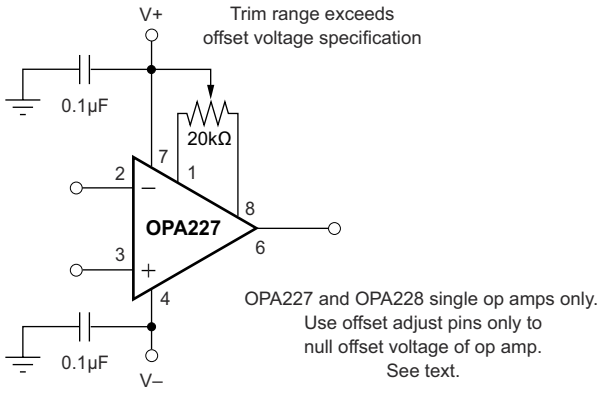


Figure 7-1. OPA227 Offset Voltage Trim Circuit

7.3.4 Input Protection

Back-to-back diodes (see Figure 7-2) are used for input protection on the OPAx22x. Exceeding the turn-on threshold of these diodes, as in a pulse condition, can cause current to flow through the input protection diodes as a result of the amplifier finite slew rate. Without external current limiting resistors, the input devices can be destroyed. Sources of high-input current can cause subtle damage to the amplifier. Although the unit can still be functional, important parameters such as input offset voltage, drift, and noise can shift.

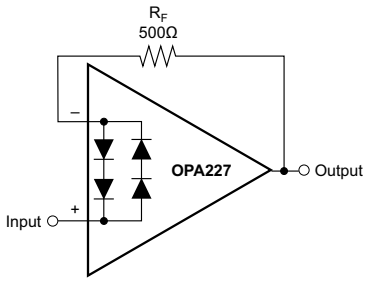


Figure 7-2. Pulsed Operation

When using the OPA227 as a unity-gain buffer (follower), limit the input current to 20 mA. This limiting is accomplished by inserting a feedback resistor or a resistor in series with the source. Equation 1 calculates the sufficient resistor size.

$$R_X = V_S/20mA - R_{SOURCE} \quad (1)$$

where

- R_X is either in series with the source or inserted in the feedback path.

For example, a 10-V pulse (V_S = 10 V) requires a total loop resistance of 500 Ω. If the source impedance is large enough to sufficiently limit the current, no additional resistors are needed. Carefully choose the size of any external resistors because of increased noise. For further information on noise calculation, see *Section 7.3.6*. Figure 7-2 shows an example implementing a current limiting feedback resistor.

7.3.5 Input Bias Current Cancellation

The input bias current of the OPAx22x series is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between with input bias current and the cancellation current. The residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately equal. A resistor added to cancel the effect of the input bias current (as shown in Figure 7-3) can actually increase offset and noise and is therefore not recommended.

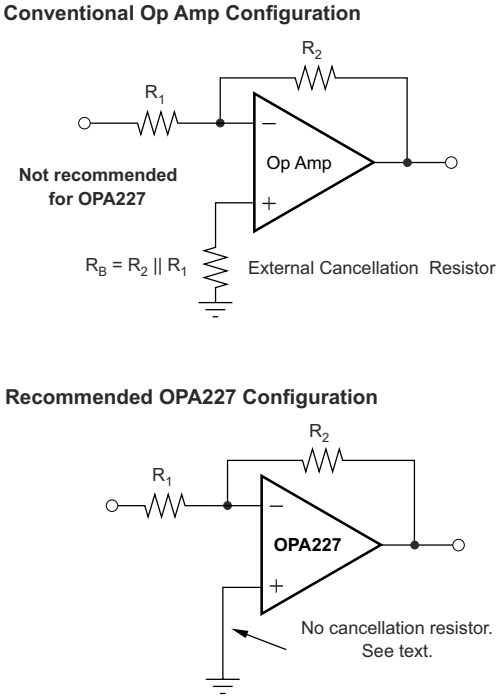


Figure 7-3. Input Bias Current Cancellation

7.3.6 Noise Performance

Figure 7-4 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network; therefore, no additional noise contributions). Two different operational amplifiers are shown with total circuit noise calculated. The OPA227 has very low voltage noise, making this device an excellent choice for low source impedances (less than 20 kΩ). A similar precision operational amplifier, the OPA277, has somewhat higher voltage noise but lower current noise. The OPA277 provides excellent noise performance at moderate source impedance (10 kΩ to 100 kΩ). Above 100 kΩ, a FET-input operational amplifier such as the OPA132 (very low current noise) can provide improved performance. Use the equation in Figure 7-4 to calculate the total circuit noise, where e_n = voltage noise, i_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38 × 10^{-23} J/K, and T is temperature in K. For more details on calculating noise, see Section 7.3.7.

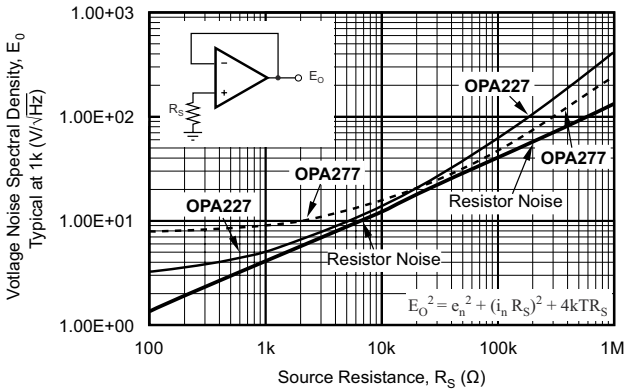


Figure 7-4. Noise Performance of the OPA227 in Unity-Gain Buffer Configuration

7.3.7 Basic Noise Calculations

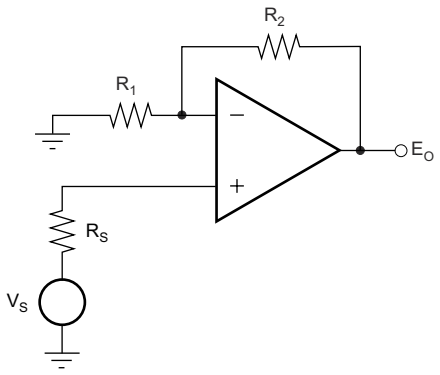
Design of low noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is shown plotted in Figure 7-4. Because the source impedance is usually fixed, select the operational amplifier and the feedback resistors to minimize any contribution to the total noise.

Figure 7-4 shows the total noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network and therefore no additional noise contributions). The operational amplifier contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Consequently, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise can dominate.

Figure 7-5 shows both inverting and noninverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown in the following images for both configurations.

Noise in Noninverting Gain Configuration



Noise at the output:

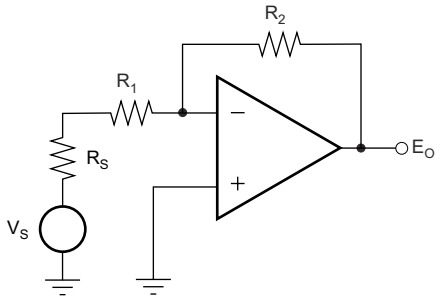
$$E_O^2 = \left(1+\frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2\left(1+\frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \bullet \left(1+\frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \bullet \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1+\frac{R_2}{R_1+R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \bullet \left(\frac{R_2}{R_1+R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \bullet \left(\frac{R_2}{R_1+R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA227 and OPA228 series op amps at 1kHz, e_n = 3nV/$\sqrt{Hz}$ and i_n = 0.4pA/$\sqrt{Hz}$.

Figure 7-5. Noise Calculation in Gain Configurations

Figure 7-6 shows the 0.1 Hz 10 Hz bandpass filter used to test the noise of the OPA227 and OPA228. The filter circuit was designed using Texas Instruments' FilterPro software (available at www.ti.com). Figure 7-7 shows the configuration of the OPA227 and OPA228 for noise testing.

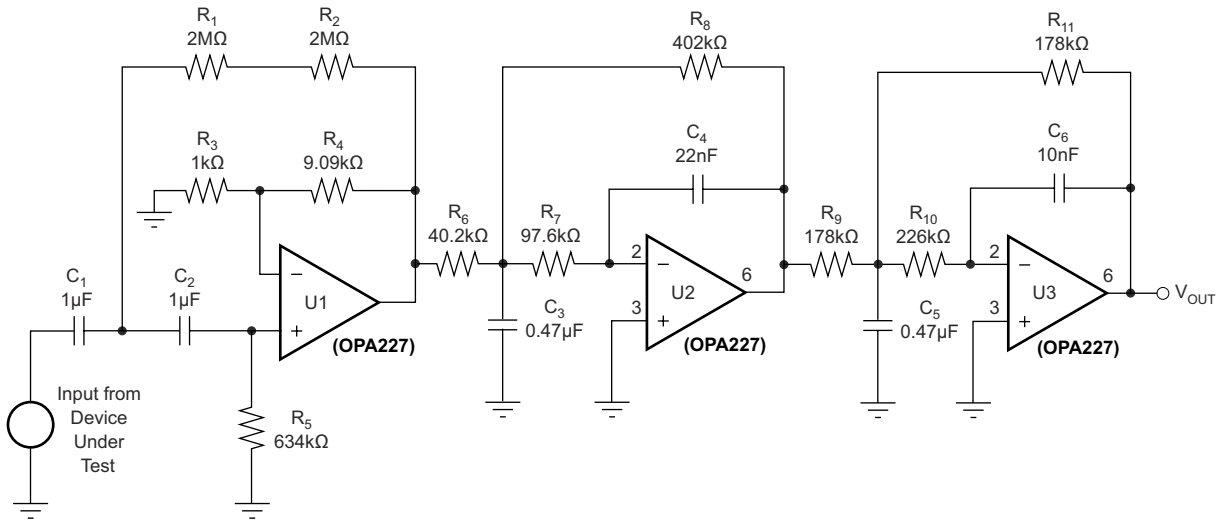


Figure 7-6. 0.1 Hz to 10 Hz Bandpass Filter Used to Test Wideband Noise of the OPAx22x Series

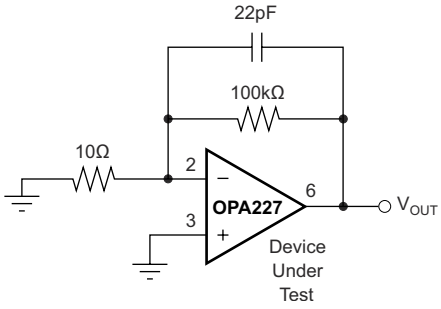


Figure 7-7. Noise Test Circuit

7.3.8 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

1. Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
2. The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
3. EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in application report SBOA128, EMI Rejection Ratio of Operational Amplifiers, available for download at www.ti.com. The EMIRR IN+ of the OPA227 is plotted versus frequency as shown in Figure 7-8.

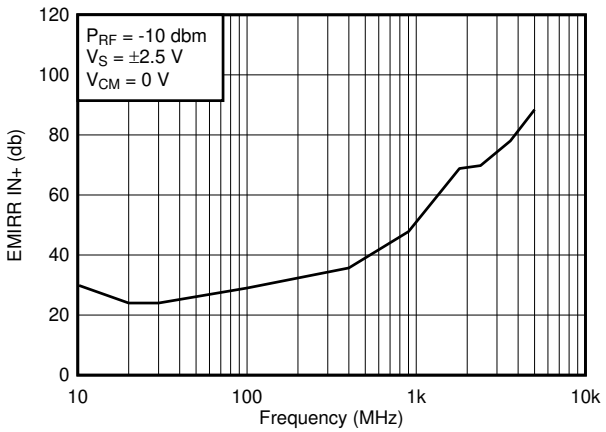


Figure 7-8. OPA227 EMIRR IN+ vs Frequency

If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The OPAx227 unity-gain bandwidth is 8 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

Table 7-1 shows the EMIRR IN+ values for the OPA227 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 7-1 can be centered on or operated near the particular frequency shown. This information can be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 7-1. OPAx227 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite and space operation, weather, radar, UHF	35.7 dB
900 MHz	GSM, radio communication and navigation, GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	47.8 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	68.8 dB
2.4 GHz	802.11b/g/n, Bluetooth® mobile personal communication, ISM, amateur radio and satellite, S-band	69.8 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78 dB
5 GHz	802.11a/n, aero communication and navigation, mobile communication, space and satellite operation, C-band	88.4 dB

7.3.8.1 EMIRR IN+ Test Configuration

Figure 7-9 shows the circuit configuration to test the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input terminal using a transmission line. The operational amplifier is configured in a unity gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy. For more details, see *EMI Rejection Ratio of Operational Amplifiers* application note.

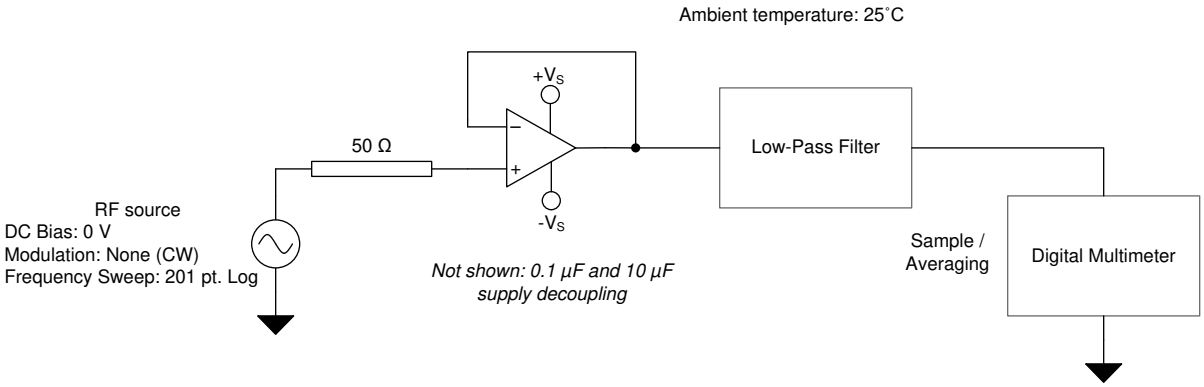


Figure 7-9. EMIRR IN+ Test Configuration Schematic

7.4 Device Functional Modes

The OPAx22x has a single functional mode and are operational when the power-supply voltage is greater than 5 V (±2.5 V). The maximum power supply voltage for the OPAx22x is 36 V (±18 V).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx22x series are precision operational amplifiers with very low noise. The OPAx227 series is unity-gain stable with a slew rate of 2.3 V/µs and 8 MHz bandwidth. The OPAx228 series is optimized for higher-speed applications with gains of 5 or greater, featuring a slew rate of 10 V/µs and 33-MHz bandwidth. Applications with noisy or high impedance power supplies can require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Typical Application

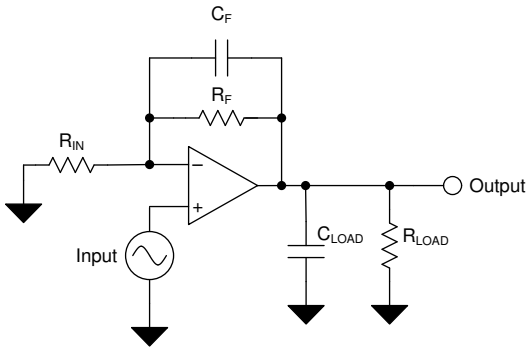


Figure 8-1. Typical Application Schematic

8.2.1 Using the OPAx228 in Low Gains

The OPAx228 family is intended for applications with signal gains of 5 or greater, but can also take advantage of the high-speed in lower gains. Without external compensation, the OPA228 has sufficient phase margin to maintain stability in unity gain with purely resistive loads. However, the addition of load capacitance can reduce the phase margin and destabilize the operational amplifier.

8.2.1.1 Design Requirements

1. Operate OPAx228 gain is less than 5 V/V
2. Stable operation with capacitive load

8.2.1.2 Detailed Design Procedure

A variety of compensation techniques have been evaluated specifically for use with the OPA228. The recommended configuration consists of an additional capacitor (C_F) in parallel with the feedback resistance, as shown in Figure 8-2 and Figure 8-3. This feedback capacitor serves two purposes in compensating the circuit. The operational amplifier's input capacitance and the feedback resistors interact to cause phase shift that can result in instability. C_F compensates the input capacitance, minimizing peaking. Additionally, at high frequencies, the closed-loop gain of the amplifier is strongly influenced by the ratio of the input capacitance and the feedback capacitor. Thus, C_F can be selected to yield good stability while maintaining high-speed.

Without external compensation, the noise specification of the OPA228 is the same as that for the OPA227 in gains of 5 or greater. With the additional external compensation, the output noise of the OPA228 is higher. The amount of noise increase is directly related to the increase in high-frequency closed-loop gain established by the C_{IN}/C_F ratio.

Figure 8-2 and Figure 8-3 show the recommended circuit for gains of 2 and –2, respectively. The figures suggest approximate values for C_F. Because compensation highly depends on circuit design, board layout, and load conditions, optimize C_F experimentally for best results. Figure 8-4 and Figure 8-6 show the large- and small-signal step responses for the G = 2 configuration with 100-pF load capacitance.Figure 8-5 and Figure 8-7 show the large- and small-signal step responses for the G = –2 configuration with 100-pF load capacitance.

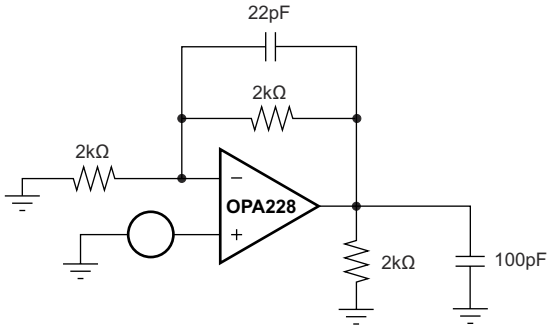


Figure 8-2. Compensation of the OPA228 for G = 2

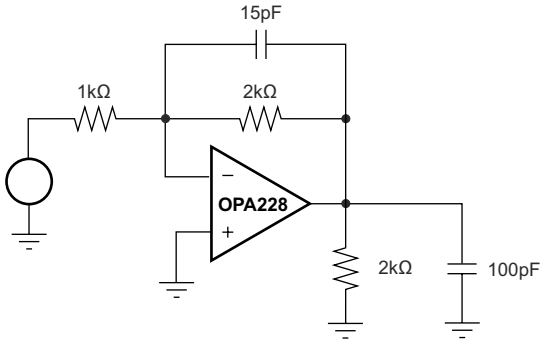


Figure 8-3. Compensation for OPA228 for G = –2

8.2.1.3 Application Curves

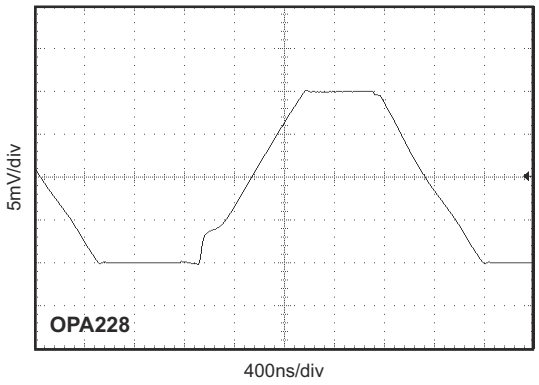


Figure 8-4. Large-Signal Step Response, G = 2, C_{LOAD} = 100 pF, Input Signal = 5 Vp-p

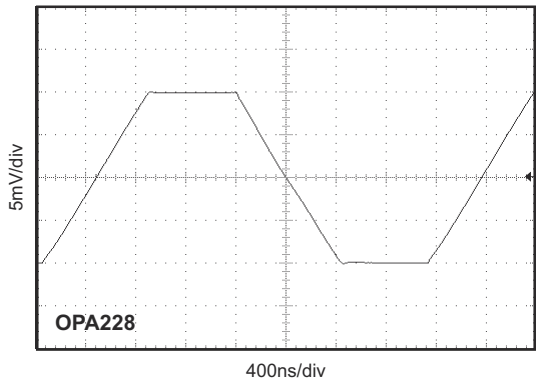


Figure 8-5. Large-Signal Step Response, G = –2, CLOAD = 100 pF, Input Signal = 5 Vp-p

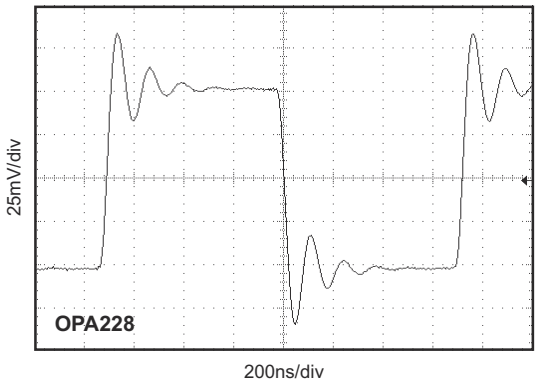


Figure 8-6. Small-Signal Step Response, G = 2, C_{LOAD} = 100 pF, Input Signal = 50 mVp-p.

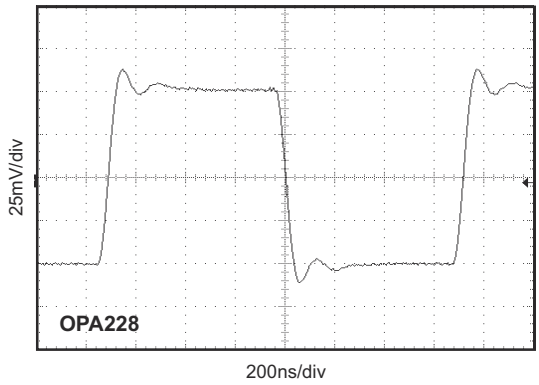


Figure 8-7. Small-Signal Step Response, G = –2, C_{LOAD} = 100 pF, Input Signal = 50 mVp-p.

8.2.2 Three-Pole, 20 kHz Low Pass, 0.5-dB Chebyshev Filter

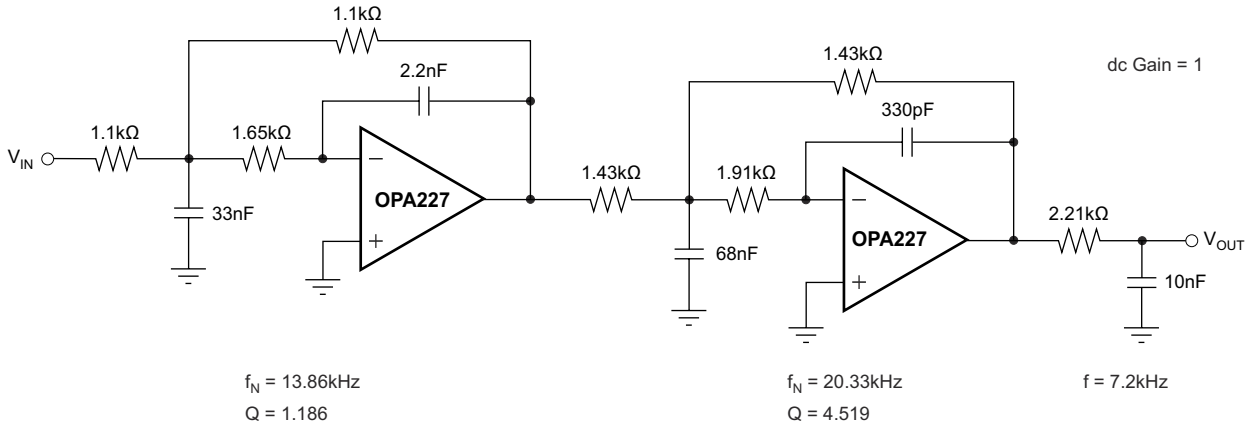


Figure 8-8. Three-Pole, 20 kHz Low Pass, 0.5-dB Chebyshev Filter

8.2.3 Long-Wavelength Infrared Detector Amplifier

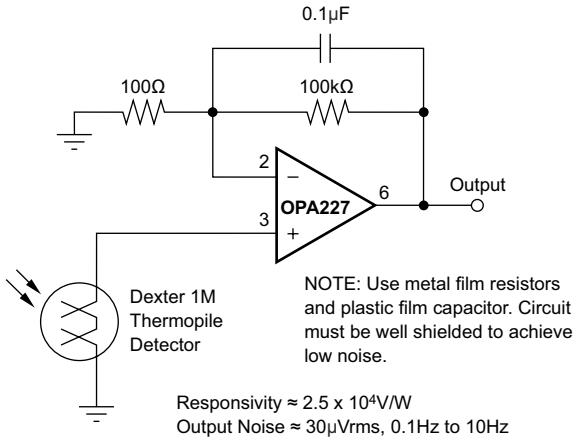


Figure 8-9. Long-Wavelength Infrared Detector Amplifier

8.2.4 High Performance Synchronous Demodulator

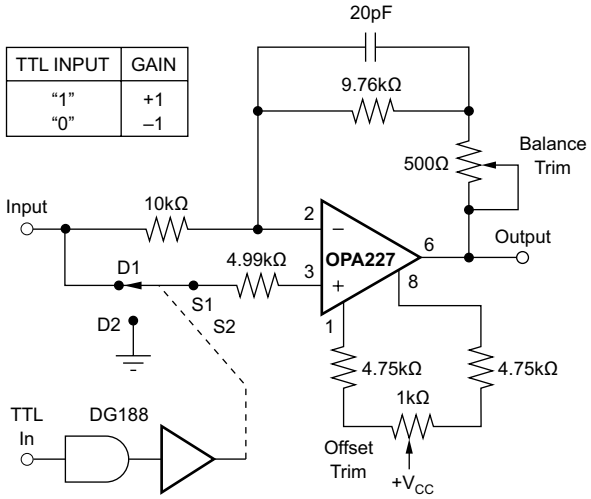


Figure 8-10. High Performance Synchronous Demodulator

8.2.5 Headphone Amplifier

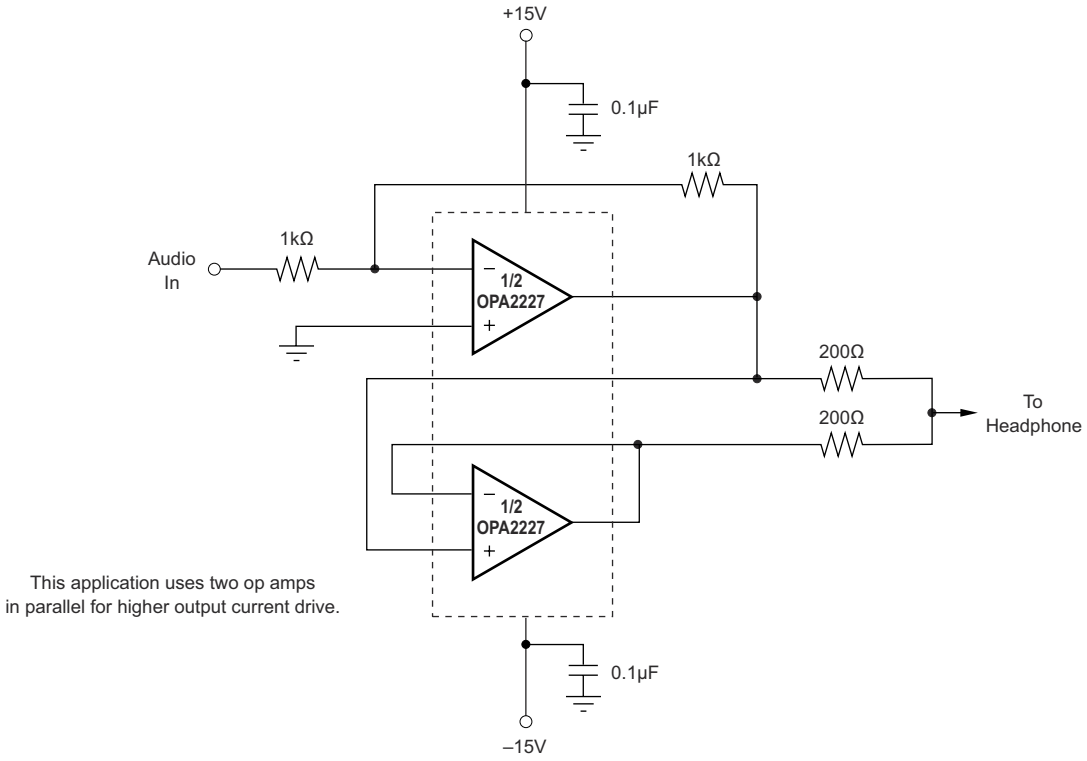


Figure 8-11. Headphone Amplifier

8.2.6 Three-Band Active Tone Control (Bass, Midrange, and Treble)

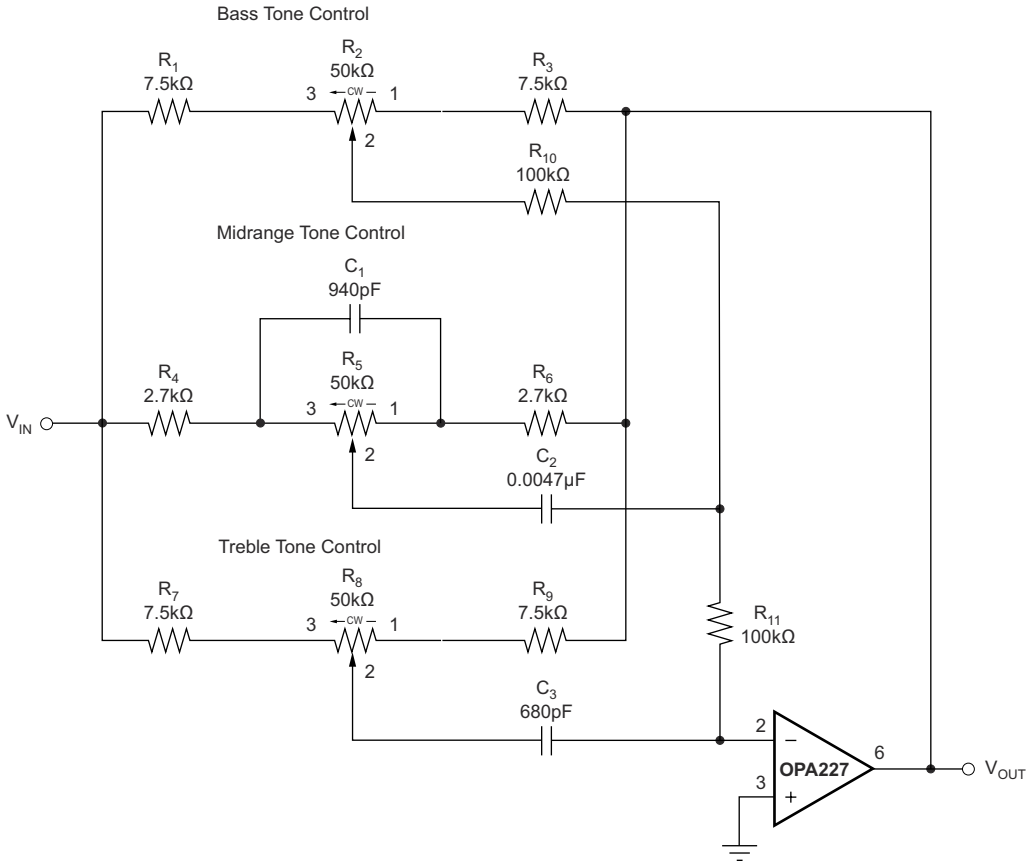


Figure 8-12. Three-Band Active Tone Control (Bass, Midrange, and Treble)

8.3 Power Supply Recommendations

The OPAx22x series are specified for operation from 5 V to 36 V (±2.5 V to ±18 V); many specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in Section 6.

CAUTION

Supply voltages larger than 36 V can permanently damage the device; see Section 6.1.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 8.4.1*.

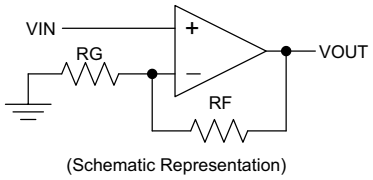
8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *Section 8.4.2*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

8.4.2 Layout Example



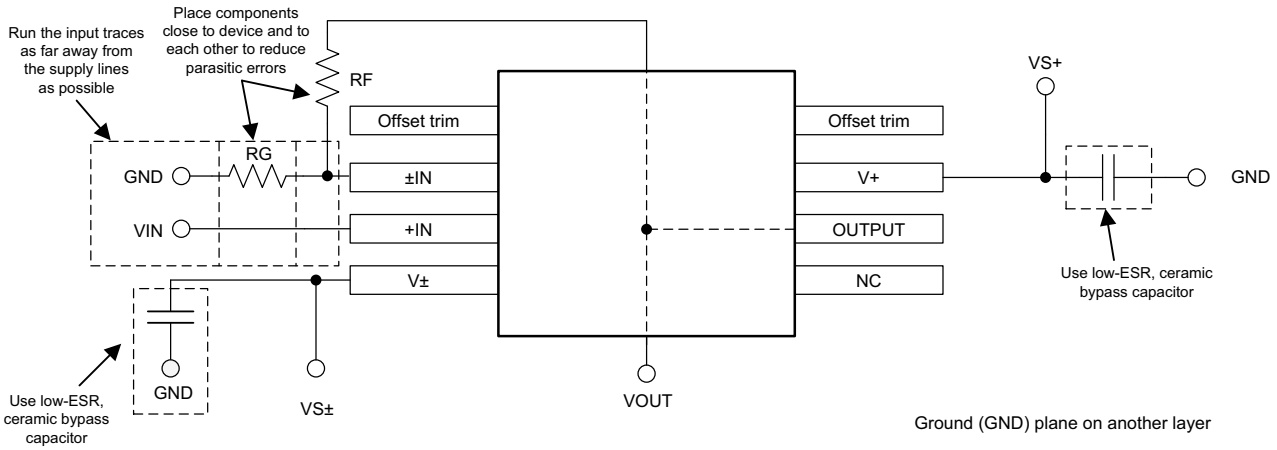


Figure 8-13. OPAx227 Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

9.1.1.2 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

9.2 Documentation Support

9.2.1 Related Documentation

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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TINA™ is a trademark of DesignSoft, Inc.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2227P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	OPA2227P	Samples
OPA2227PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	OPA2227P A	Samples
OPA2227U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U	Samples
OPA2227U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U	Samples
OPA2227UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U A	Samples
OPA2227UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U A	Samples
OPA2228P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	OPA2228P	Samples
OPA2228PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	OPA2228P A	Samples
OPA2228PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	OPA2228P A	Samples
OPA2228PG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	OPA2228P	Samples
OPA2228U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2228U	Samples
OPA2228U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2228U	Samples
OPA2228UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2228U A	Samples
OPA2228UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2228U A	Samples
OPA227P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	OPA227P	Samples
OPA227PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	OPA227P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										A	
OPA227PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	OPA227P A	Samples
OPA227PG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	OPA227P	Samples
OPA227U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 227U	Samples
OPA227U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 227U	Samples
OPA227UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 227U A	Samples
OPA227UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 227U A	Samples
OPA228P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	OPA228P	Samples
OPA228PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	OPA228P A	Samples
OPA228PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	OPA228P A	Samples
OPA228U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-55 to 125	OPA 228U	Samples
OPA228UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-55 to 125	OPA 228U A	Samples
OPA228UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-55 to 125	OPA 228U A	Samples
OPA4227PA	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA4227PA	Samples
OPA4227PAG4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA4227PA	Samples
OPA4227UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU | NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4227UA	Samples
OPA4227UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4227UA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4228PA	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	OPA4228PA	Samples
OPA4228UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-55 to 125	OPA4228UA	Samples
OPA4228UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-55 to 125	OPA4228UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2227 :

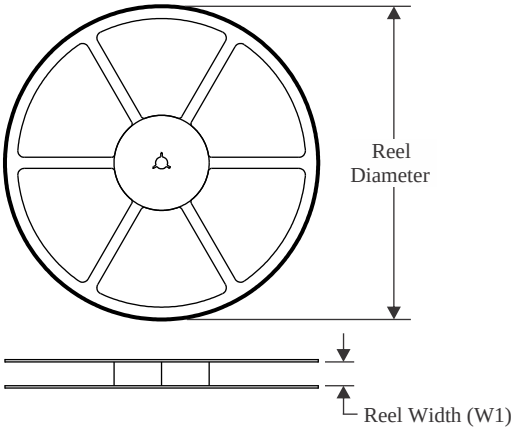
- Enhanced Product : OPA2227-EP

NOTE: Qualified Version Definitions:

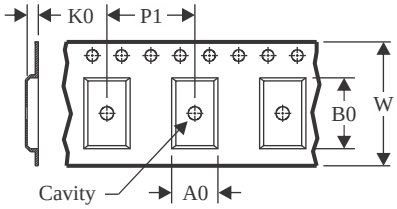
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

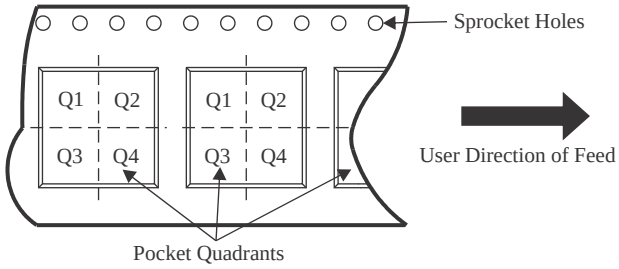


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

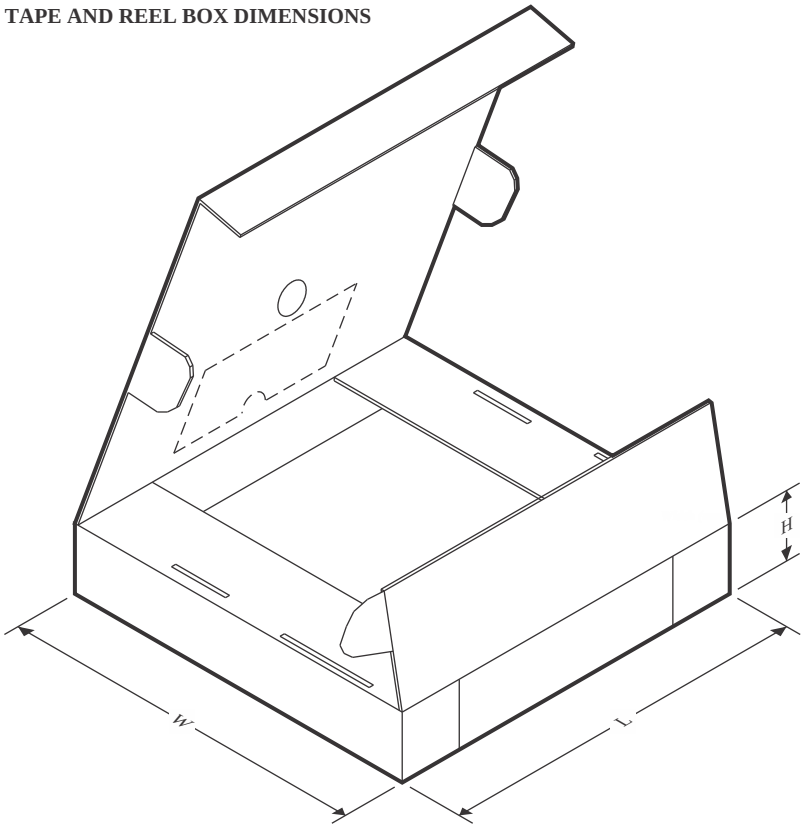


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2227U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2227U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2227UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2227UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2228U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2228U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2228UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2228UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA227U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA227U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA227UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA227UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA228UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA228UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4227UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4227UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4228UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

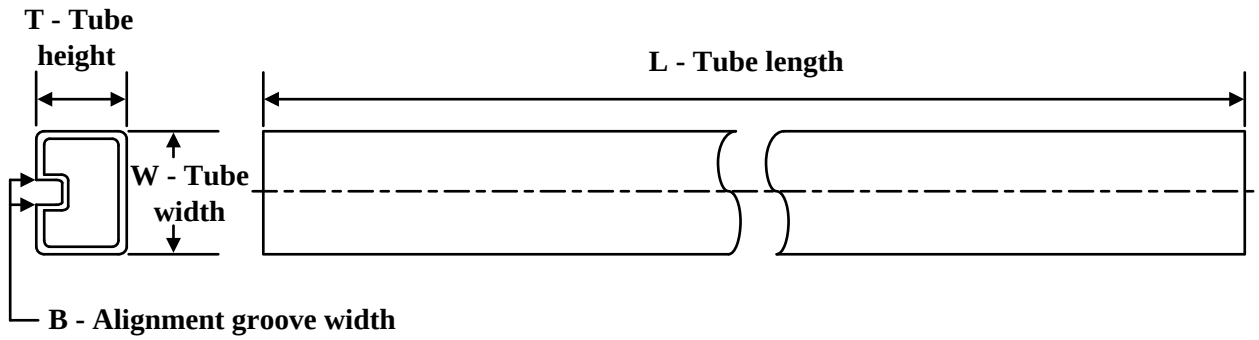
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

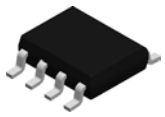
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2227U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2227U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2227UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2227UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2228U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2228U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2228UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2228UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA227U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA227U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA227UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA227UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA228UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA228UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4227UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0
OPA4227UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0
OPA4228UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2227P	P	PDIP	8	50	506	13.97	11230	4.32
OPA2227PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2227U	D	SOIC	8	75	506.6	8	3940	4.32
OPA2227UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2228P	P	PDIP	8	50	506	13.97	11230	4.32
OPA2228PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2228PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2228PG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2228U	D	SOIC	8	75	506.6	8	3940	4.32
OPA2228UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA227P	P	PDIP	8	50	506	13.97	11230	4.32
OPA227PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA227PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA227PG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA227U	D	SOIC	8	75	506.6	8	3940	4.32
OPA227UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA228P	P	PDIP	8	50	506	13.97	11230	4.32
OPA228PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA228PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA228U	D	SOIC	8	75	506.6	8	3940	4.32
OPA228UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA4227PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4227PAG4	N	PDIP	14	25	506	13.97	11230	4.32
OPA4227UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4228PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4228UA	D	SOIC	14	50	506.6	8	3940	4.32

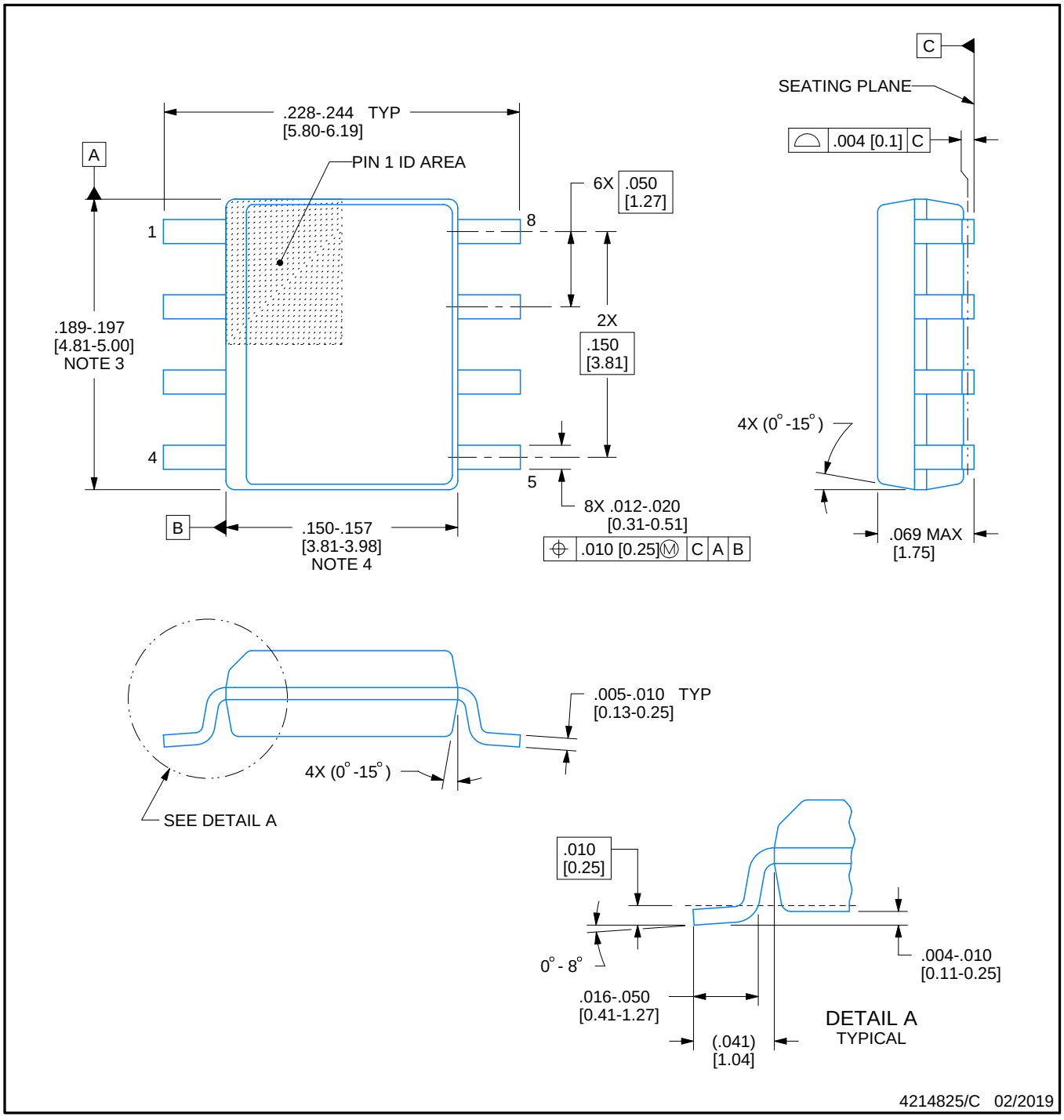


PACKAGE OUTLINE

D0008A

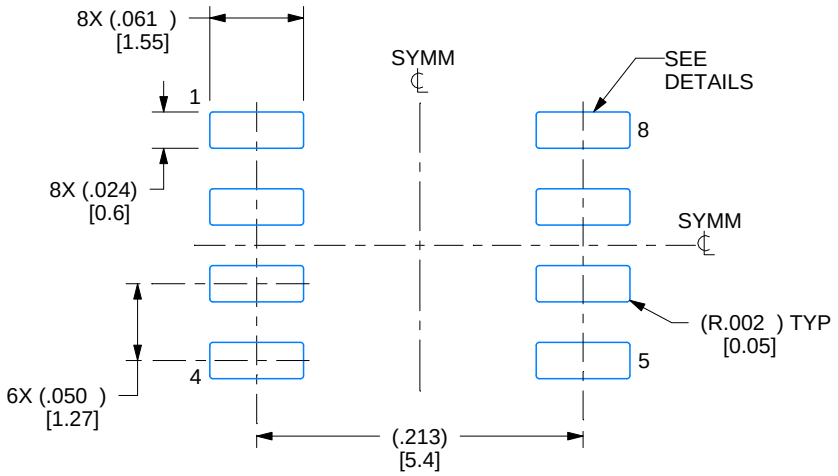
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

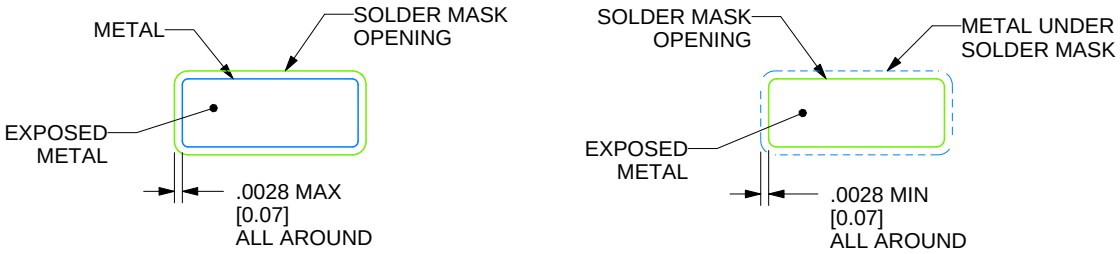


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

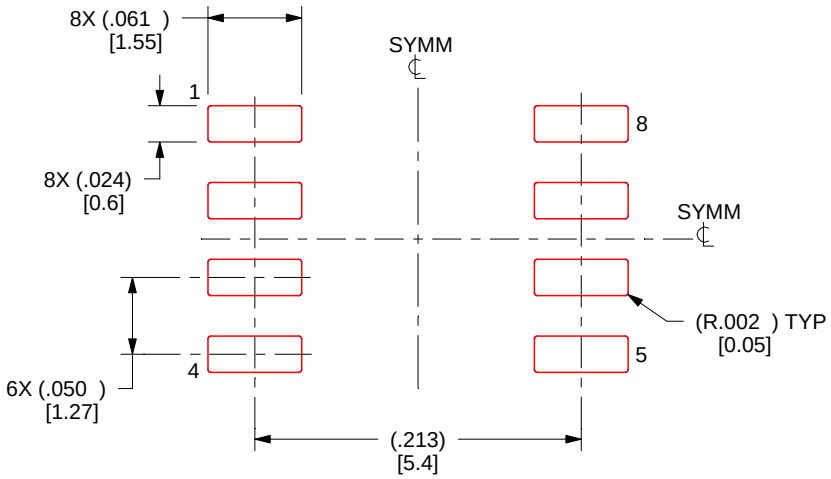
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



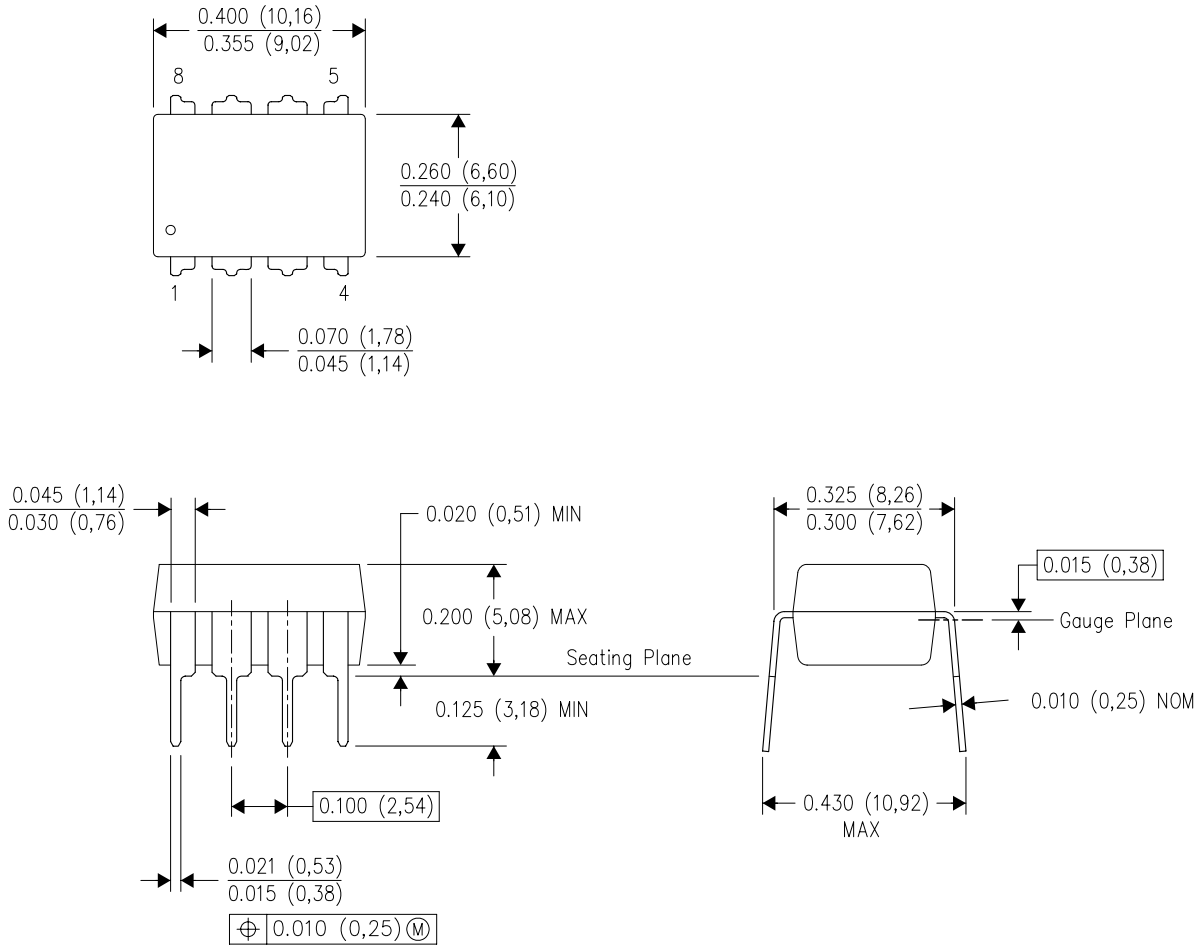
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

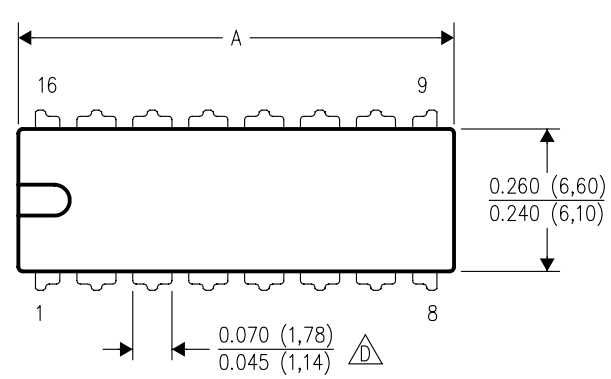


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

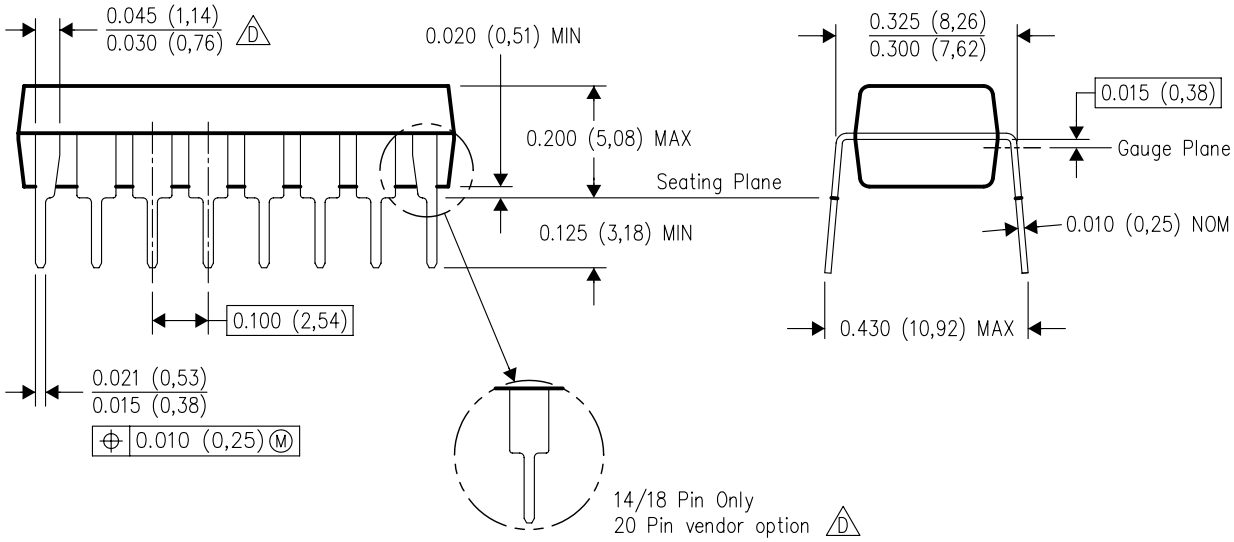
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

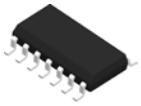


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

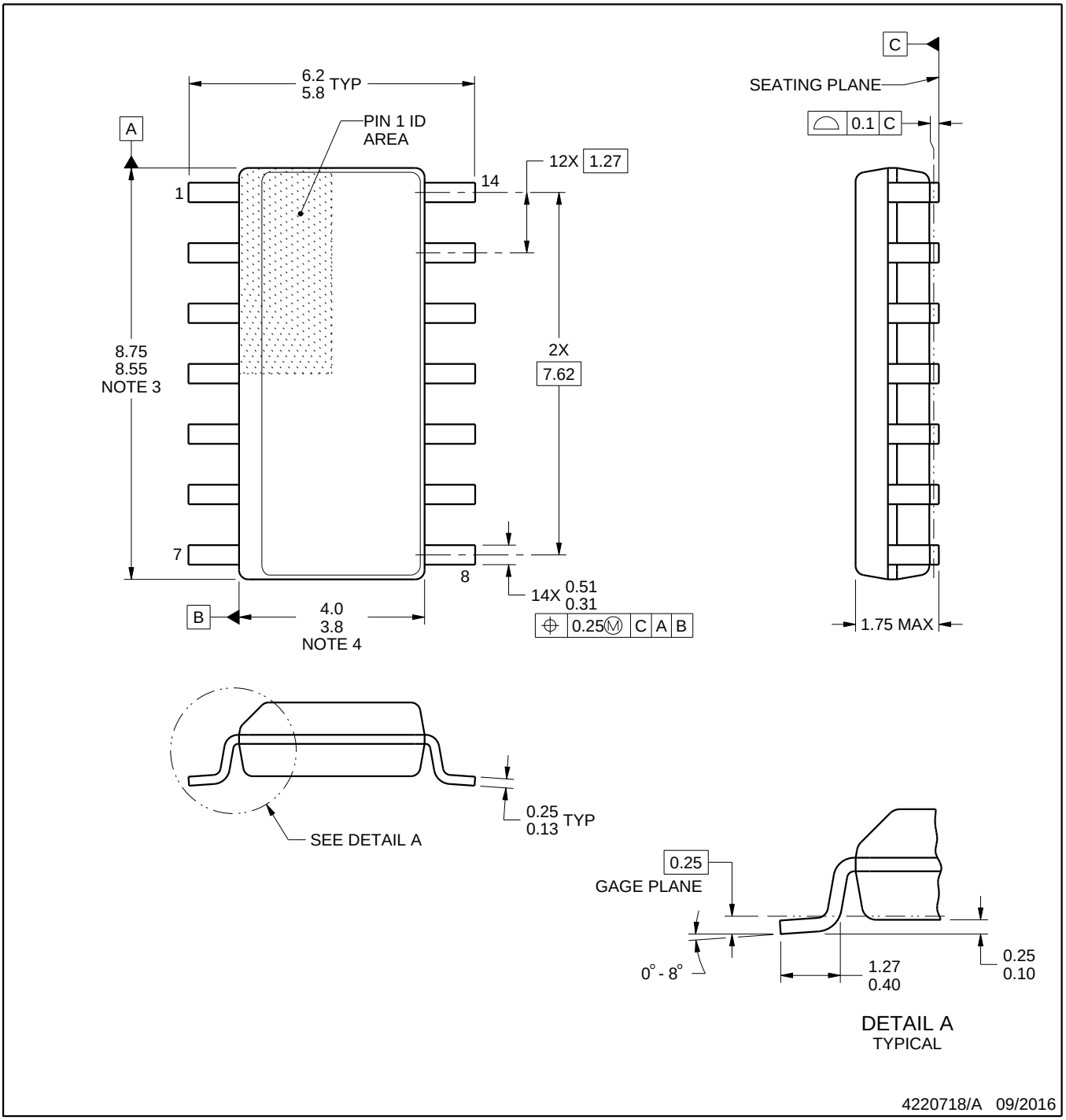


PACKAGE OUTLINE

D0014A

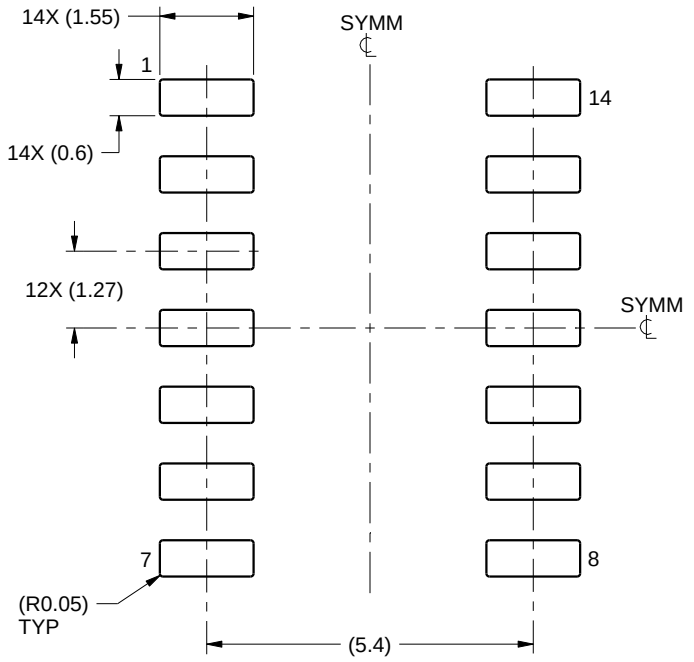
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

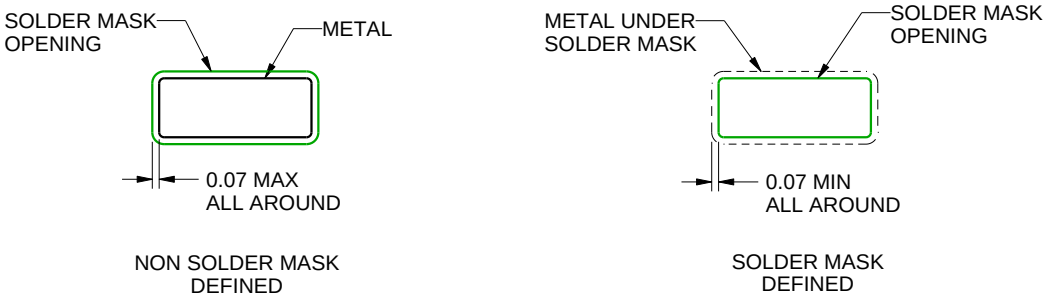


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

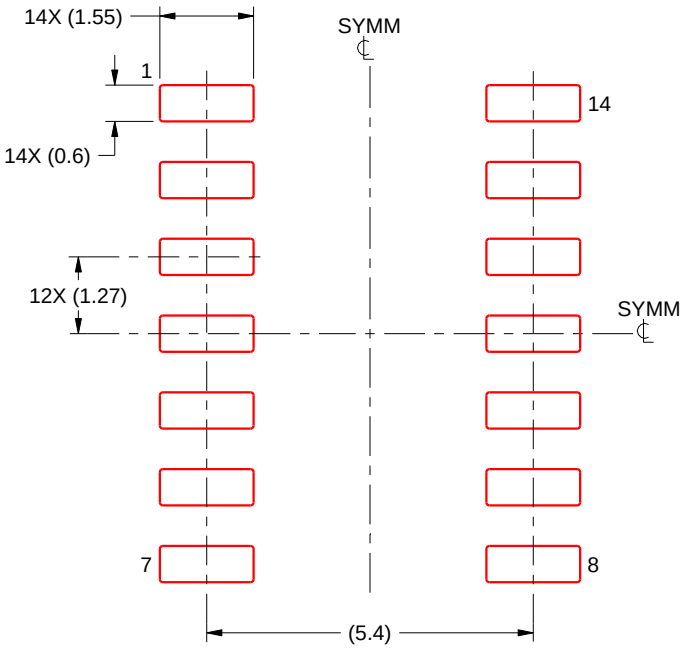
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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